

# 1, 2, 6 and 8 Channel, 10-Bit Serial I/O Data Acquisition Systems

## FEATURES

- Programmable Features
  - Unipolar/Bipolar Conversions
  - Differential/Single Ended Multiplexer Configurations
- Sample and Holds
- Single Supply 5V, 10V or  $\pm 5V$  Operation
- Direct 3 or 4 Wire Interface to Most MPU Serial Ports and All MPU Parallel I/O Ports
- Analog Inputs Common-Mode to Supply Rails
- Resolution 10 Bits
- Total Unadjusted Error (A Grade)  $\pm 1/2\text{LSB}$  Over Temp
- Fast Conversion Time  $20\mu\text{s}$
- Low Supply Current LTC1091 3.5mA Max, 1.5mA Typ  
 LTC1092/3/4 2.5mA Max, 1mA Typ

## DESCRIPTION

The LTC1091/2/3/4 10-bit data acquisition systems are designed to provide complete function, excellent accuracy and ease of use when digitizing analog data from a wide variety of signal sources and transducers. Built around a 10-bit, switched capacitor, successive approximation A/D core, these devices include software configurable analog multiplexers and bipolar and unipolar conversion modes

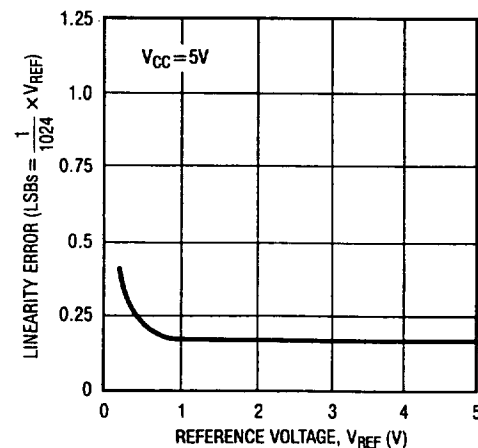
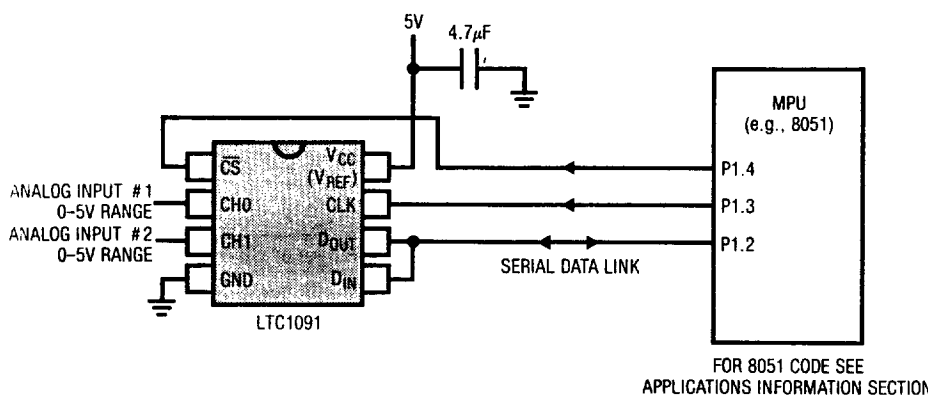
as well as on chip sample and holds. On-chip serial ports allow efficient data transfer to a wide range of microprocessors and microcontrollers. These circuits can provide a complete data acquisition system in ratiometric applications or can be used with an external reference in others.

The high impedance analog inputs and the ability to operate with reduced spans (below 1V full scale) allow direct connection to sensors and transducers in many applications, eliminating the need for gain stages.

An efficient serial port communicates without external hardware to most MPU serial ports and all MPU parallel I/O ports allowing eight channels of data to be transmitted over as few as 3 wires. This, coupled with low power consumption, makes remote location possible and facilitates transmitting data through isolation barriers.

Temperature drift of offset, linearity, and full scale error are all extremely low (1ppm/ $^{\circ}\text{C}$  typically) allowing all grades to be specified with offset and linearity errors of  $\pm 0.5\text{LSB}$  maximum over temperature. In addition, the A grade devices are specified with full scale error and total unadjusted error (including the effects of offset, linearity, and full scale errors) of  $\pm 0.5\text{LSB}$  maximum over temperature. The lower grade has a full scale specification of  $\pm 2\text{LSB}$  for applications where full scale is adjustable or less critical.

## TYPICAL APPLICATION



# LTC1091/LTC1092 LTC1093/LTC1094

## ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltage ( $V_{CC}$ ) to GND or  $V^-$  ..... 12V  
 Negative Supply Voltage ( $V^-$ ) ..... -6V to GND  
 Voltage

Analog Reference and LTC1091/2  $\overline{CS}$

Inputs ..... ( $V^-$ ) - 0.3V to  $V_{CC} + 0.3V$

Digital Inputs (except LTC1091/2  $\overline{CS}$ ) ..... -0.3V to 12V

Digital Outputs ..... -0.3V to  $V_{CC} + 0.3V$

Power Dissipation ..... 500mW

Operating Temperature Range

LTC1091-4AC, LTC1091-4C ..... -40°C to 85°C

LTC1091-4AM, LTC1091-4M ..... -55°C to 125°C

Storage Temperature Range ..... -65°C to 150°C

Lead Temperature (Soldering, 10 sec.) ..... 300°C

## PACKAGE/ORDER INFORMATION

<p>TOP VIEW</p> <p>J PACKAGE 8 LEAD CERAMIC DIP</p> <p>N PACKAGE 8 LEAD PLASTIC DIP</p>	<p>ORDER PART NUMBER</p> <p>LTC1091AMJ8 LTC1091MJ8 LTC1091ACJ8 LTC1091CJ8 LTC1091ACN8 LTC1091CN8</p>	<p>TOP VIEW</p> <p>J PACKAGE 8 LEAD CERAMIC DIP</p> <p>N PACKAGE 8 LEAD PLASTIC DIP</p>	<p>ORDER PART NUMBER</p> <p>LTC1092AMJ8 LTC1092MJ8 LTC1092ACJ8 LTC1092CJ8 LTC1092ACN8 LTC1092CN8</p>
<p>TOP VIEW</p> <p>J PACKAGE 16 LEAD CERAMIC DIP</p> <p>N PACKAGE 16 LEAD PLASTIC DIP</p>	<p>LTC1093AMJ LTC1093MJ LTC1093ACJ LTC1093CJ LTC1093ACN LTC1093CN</p>	<p>TOP VIEW</p> <p>J PACKAGE 20 LEAD CERAMIC DIP</p> <p>N PACKAGE 20 LEAD PLASTIC DIP</p>	<p>LTC1094AMJ LTC1094MJ LTC1094ACJ LTC1094CJ LTC1094ACN LTC1094CN</p>

## PRODUCT GUIDE

PART NUMBER	# CHANNELS	CONVERSION MODES		REDUCED SPAN CAPABILITY (SEPARATE $V_{REF}$ )	$\pm 5V$ CAPABILITY	
		UNIPOLAR	BIPOLAR			
LTC1091	2	•				Pin for pin 10-bit upgrade of ADC0832
LTC1092	1	•		•		Pin for pin 10-bit upgrade of ADC0831
LTC1093	6	•	•	•	•	
LTC1094	8	•	•	•	•	

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LTC1091-4/LTC1091-4A		UNITS
			MIN	MAX	
$V_{CC}$	Supply Voltage		4.5	10	V
$V^-$	Negative Supply Voltage	$V_{CC} = 5V$ LTC1093/4	-5.5	0	V
$f_{CLK}$	Clock Frequency	$V_{CC} = 5V$	0.01	0.5	MHz
$t_{CYC}$	Total Cycle Time	LTC1091 LTC1092 LTC1093/4	15 CLK Cycles + 2 $\mu$ s 12 CLK Cycles + 2 $\mu$ s 18 CLK Cycles + 2 $\mu$ s		
$t_{hDI}$	Hold Time, $D_{IN}$ After SCLK $\uparrow$	$V_{CC} = 5V$	150		ns
$t_{su\overline{CS}}$	Setup Time $\overline{CS}$ Before CLK $\uparrow$	$V_{CC} = 5V$	1		$\mu$ s
$t_{suDI}$	Setup Time, $D_{IN}$ Stable Before CLK $\uparrow$	$V_{CC} = 5V$	400		ns
$t_{WHCLK}$	CLK High Time	$V_{CC} = 5V$	0.8		$\mu$ s
$t_{WLCLK}$	CLK Low Time	$V_{CC} = 5V$	1		$\mu$ s
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time Between Data Transfer Cycles	$V_{CC} = 5V$	2		$\mu$ s
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	LTC1091 LTC1092 LTC1093/4	15 12 18		CLK Cycles CLK Cycles CLK Cycles

## CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS	LTC1091-4A			LTC1091-4			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Offset Error	(Note 4)			$\pm 0.5$			$\pm 0.5$	LSB
Linearity Error	(Notes 4 and 5)			$\pm 0.5$			$\pm 0.5$	LSB
Full Scale Error	(Note 4)			$\pm 0.5$			$\pm 2.0$	LSB
Total Unadjusted Error	$V_{REF} = 5.000V$ (Notes 4 and 6)			$\pm 0.5$				LSB
Reference Input Resistance	$V_{REF} = 5V$ , LTC1092/3/4	5	10		5	10		k $\Omega$
Analog and REF Input Range	(Note 7)	$(V^-) - 0.05V$ to $V_{CC} + 0.05V$						V
On Channel Leakage Current (Note 8)	On Channel = 5V Off Channel = 0V			1			1	$\mu$ A
	On Channel = 0V Off Channel = 5V			-1			-1	$\mu$ A
Off Channel Leakage Current (Note 8)	On Channel = 5V Off Channel = 0V			-1			-1	$\mu$ A
	On Channel = 0V Off Channel = 5V			1			1	$\mu$ A

## AC CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LTC1091-4/LTC1091-4A			UNITS
			MIN	TYP	MAX	
$t_{SMPL}$	Analog Input Sample Time	See Operating Sequence		1.5		CLK Cycles
$t_{CONV}$	Conversion Time	See Operating Sequence		10		CLK Cycles
$t_{dDO}$	Delay Time, CLK $\downarrow$ to D $_{OUT}$ Data Valid	See Test Circuits	●	400	850	ns
$t_{dis}$	Delay Time, $\overline{CS}$ $\downarrow$ to D $_{OUT}$ Hi-Z	See Test Circuits	●	180	450	ns
$t_{en}$	Delay Time, CLK $\downarrow$ to D $_{OUT}$ Enabled	See Test Circuits	●	160	450	ns
$t_{hDO}$	Time Output Data Remains Valid After SCLK $\downarrow$			150		ns
$t_f$	D $_{OUT}$ Fall Time	See Test Circuits	●	90	300	ns
$t_r$	D $_{OUT}$ Rise Time	See Test Circuits	●	60	300	ns
$C_{IN}$	Input Capacitance	Analog Inputs On Channel		65		pF
		Off Channel		5		pF
		Digital Inputs		5		pF

## DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LTC1091-4/LTC1091-4A			UNITS
			MIN	TYP	MAX	
$V_{IH}$	High Level Input Voltage	$V_{CC} = 5.25V$	●	2.0		V
$V_{IL}$	Low Level Input Voltage	$V_{CC} = 4.75V$	●		0.8	V
$I_{IH}$	High Level Input Current	$V_{IN} = V_{CC}$	●		2.5	$\mu A$
$I_{IL}$	Low Level Input Current	$V_{IN} = 0V$	●		-2.5	$\mu A$
$V_{OH}$	High Level Output Voltage	$V_{CC} = 4.75V, I_O = 10\mu A$ $I_O = 360\mu A$	●	2.4	4.7	V
			●		4.0	V
$V_{OL}$	Low Level Output Voltage	$V_{CC} = 4.75V, I_O = 1.6mA$	●		0.4	V
$I_{OZ}$	Hi-Z Output Leakage	$V_{OUT} = V_{CC}, \overline{CS}$ High $V_{OUT} = 0V, \overline{CS}$ High	●		3	$\mu A$
			●		-3	$\mu A$
$I_{SOURCE}$	Output Source Current	$V_{OUT} = 0V$			-10	mA
$I_{SINK}$	Output Sink Current	$V_{OUT} = V_{CC}$			10	mA
$I_{CC}$	Positive Supply Current	$\overline{CS}$ High, LTC1091	●	1.5	3.5	mA
		$\overline{CS}$ High, REF $^+$ Open, LTC1092/3/4	●	1.0	2.5	mA
$I_{REF}$	Reference Current	$V_{REF} = 5V, LTC1092/3/4$	●	0.5	1.0	mA
$I^-$	Negative Supply Current	$\overline{CS}$ High, $V^- = -5V, LTC1093/4$	●	1	50	$\mu A$

**Note 1:** Absolute maximum ratings are those values beyond which the life of a device may be impaired.

**Note 2:** All voltage values are with respect to ground with DGND, AGND, GND and REF $^-$  wired together (unless otherwise noted). REF $^-$  is internally connected to the AGND pin on the LTC1093. DGND, AGND, REF $^-$  and V $^-$  are internally connected to the GND pin on the LTC1091/2.

**Note 3:**  $V_{CC} = 5V, V_{REF+} = 5V, V_{REF-} = 0V, V^- = 0V$  for unipolar mode and  $-5V$  for bipolar mode, CLK = 0.5MHz unless otherwise specified. The ● indicates specs which apply over the full operating temperature range; all other limits and typicals  $T_A = 25^\circ C$ .

**Note 4:** These specs apply for both unipolar (LTC1091-4) and bipolar (LTC1093/4 only) modes. In bipolar mode, one LSB is equal to the bipolar input span ( $2V_{REF}$ ) divided by 1024. For example, when  $V_{REF} = 5V$ , 1LSB bipolar) =  $2(5V)/1024 = 9.77mV$ .

**Note 5:** Linearity error is specified between the actual end points of the A/D transfer curve.

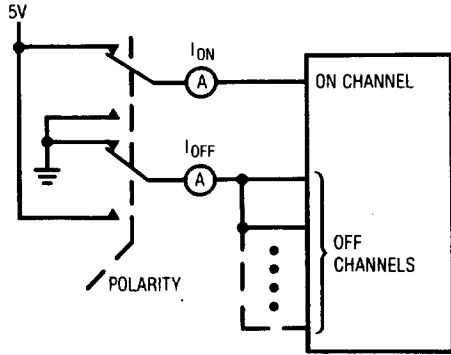
**Note 6:** Total unadjusted error includes offset, full scale, linearity, multiplexer and hold step errors.

**Note 7:** Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages one diode drop below V $^-$  or one diode drop above V $_{CC}$ . Be careful during testing at low V $_{CC}$  levels (4.5V), as high level reference or analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for inputs near full-scale. This spec allows 50mV forward bias of either diode. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over initial tolerance, temperature variations and loading.

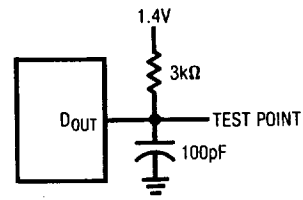
**Note 8:** Channel leakage current is measured after the channel selection.

## TEST CIRCUITS

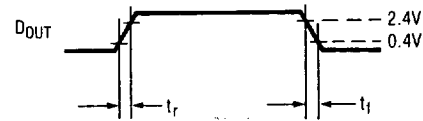
On and Off Channel Leakage Current



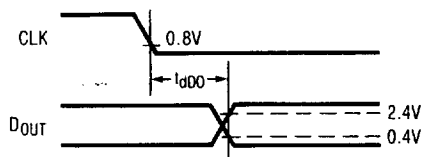
Load Circuit for  $t_{dDO}$ ,  $t_r$ , and  $t_f$



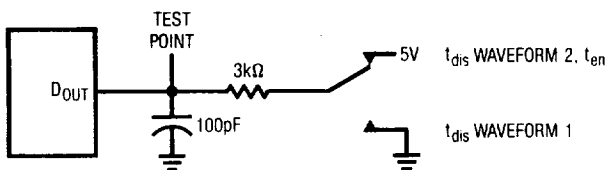
Voltage Waveforms for  $D_{OUT}$  Rise and Fall Times,  $t_r$ ,  $t_f$



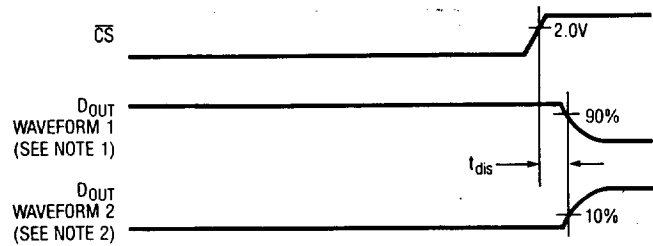
Voltage Waveforms for  $D_{OUT}$  Delay Time,  $t_{dDO}$



Load Circuit for  $t_{dis}$  and  $t_{en}$



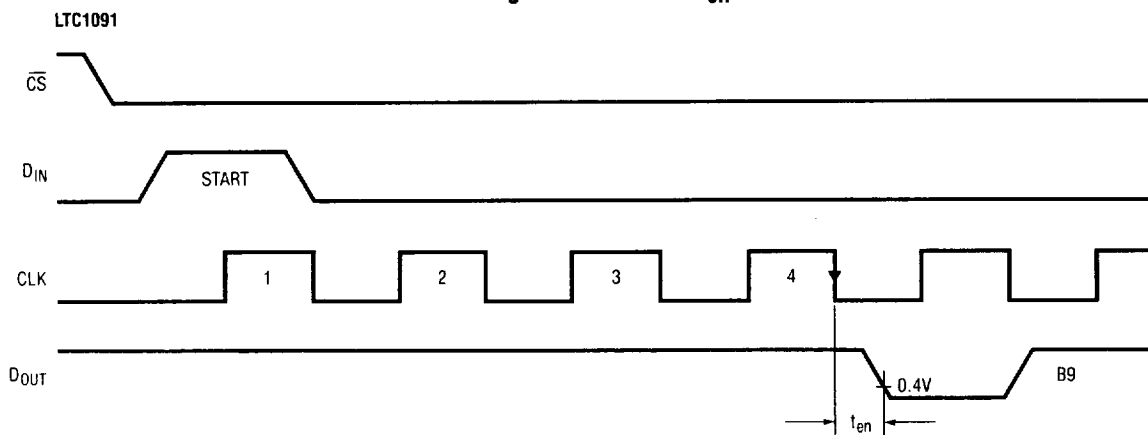
Voltage Waveforms for  $t_{dis}$



NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.

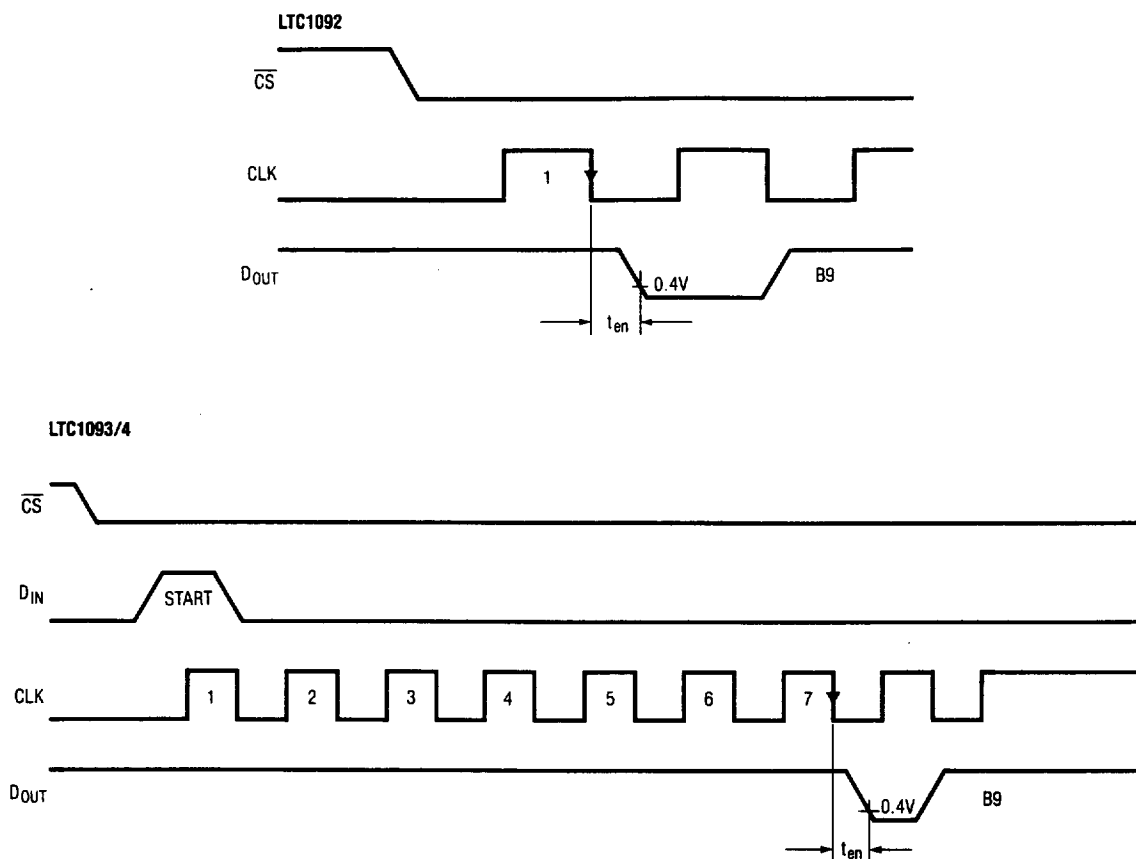
NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

Voltage Waveforms for  $t_{en}$



## TEST CIRCUITS

Voltage Waveforms for  $t_{en}$



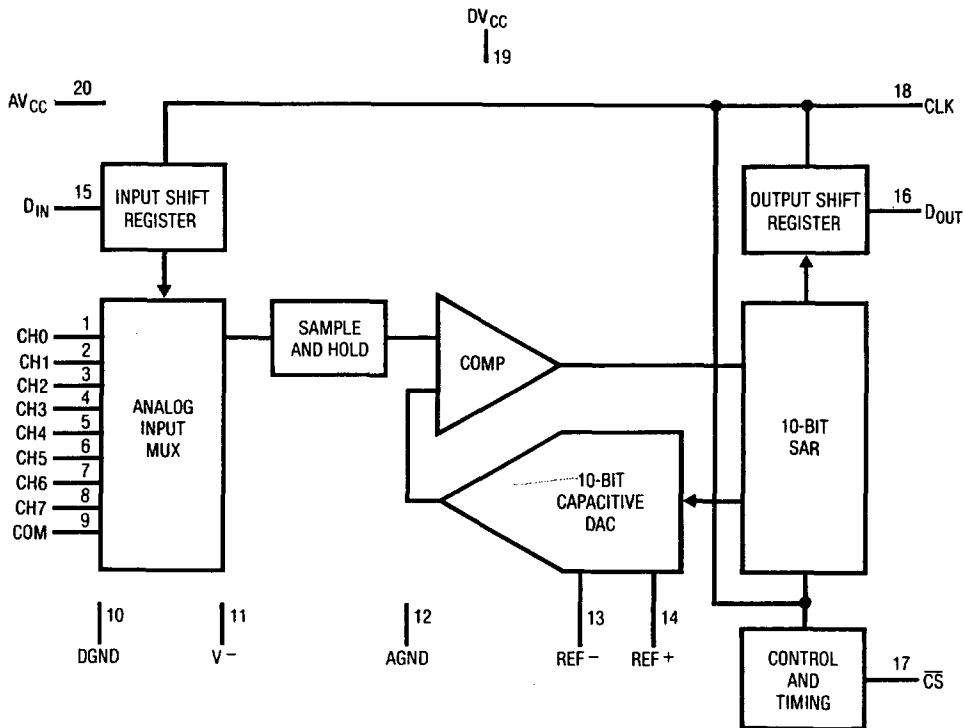
## PIN FUNCTIONS LTC1091/2

LTC1091 #	LTC1092 #	PIN	FUNCTION	DESCRIPTION
1	1	$\overline{CS}$	Chip Select Input	A logic low on this input enables the LTC1091/2.
2, 3	2, 3	CH0, CH1	Analog Inputs	These inputs must be free of noise with respect to GND.
4	4	IN +, IN -	Analog Inputs	These inputs must be free of noise with respect to GND.
5	4	GND	Analog Ground	GND should be tied directly to an analog ground plane.
5	5	$D_{IN}$	Digital Data Input	The multiplexer address is shifted into this input.
5	5	$V_{REF}$	Reference Input	The reference input defines the span of the A/D converter and must be kept free of noise with respect to AGND.
6	6	$D_{OUT}$	Digital Data Output	The A/D conversion result is shifted out of this output.
7	7	CLK	Shift Clock	This clock synchronizes the serial data transfer.
8	7	$V_{CC}(V_{REF})$	Positive Supply and Reference Voltage	This pin provides power and defines the span of the A/D converter. It must be kept free of noise and ripple by bypassing directly to the analog ground plane.
8	8	$V_{CC}$	Positive Supply Voltage	This pin provides power to the A/D converter. It must be kept free of noise and ripple by bypassing directly to the analog ground plane.

**PIN FUNCTIONS** LTC1093/4

LTC1093 #	LTC1094 #	PIN	FUNCTION	DESCRIPTION
1-6	1-8	CH0-CH5	Analog Inputs	The analog inputs must be free of noise with respect to AGND.
7	9	CH0-CH7	Analog Inputs	The analog inputs must be free of noise with respect to AGND.
		COM	Common	The common pin defines the zero reference point for all single ended inputs. It must be free of noise and is usually tied to the analog ground plane.
8	10	DGND	Digital Ground	This is the ground for the internal logic. Tie to the ground plane.
9	11	V <sup>-</sup>	Negative Supply	Tie V <sup>-</sup> to most negative potential in the circuit. (Ground in single supply applications.)
10	12	AGND	Analog Ground	AGND should be tied directly to the analog ground plane.
11		V <sub>REF</sub>	Reference Input	The reference input must be kept free of noise with respect to AGND.
	13, 14	REF +, REF -	Reference Input	The reference input must be kept free of noise with respect to AGND.
12	15	D <sub>IN</sub>	Data Input	The A/D configuration word is shifted into this input.
13	16	D <sub>OUT</sub>	Digital Data Output	The A/D conversion result is shifted out of this output.
14	17	CS	Chip Select Input	A logic low on this input enables the LTC1093/4.
15	18	CLK	Shift Clock	This clock synchronizes the serial data transfer.
16		V <sub>CC</sub>	Positive Supply	This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.
	19, 20	AV <sub>CC</sub> , DV <sub>CC</sub>	Positive Supply	This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane. AV <sub>CC</sub> and DV <sub>CC</sub> should be tied together on the LTC1094.

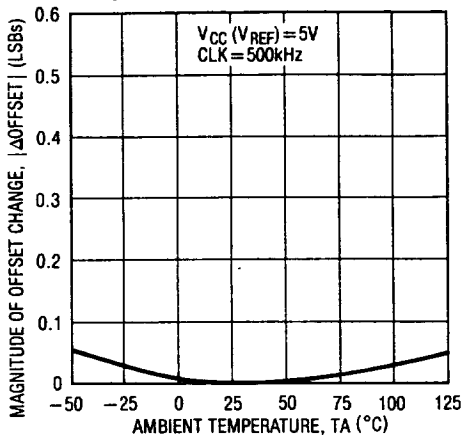
**BLOCK DIAGRAM** (Pin numbers refer to LTC1094)



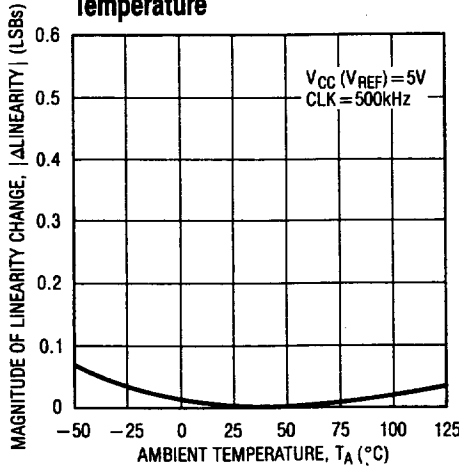
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# TYPICAL PERFORMANCE CHARACTERISTICS LTC1091-4

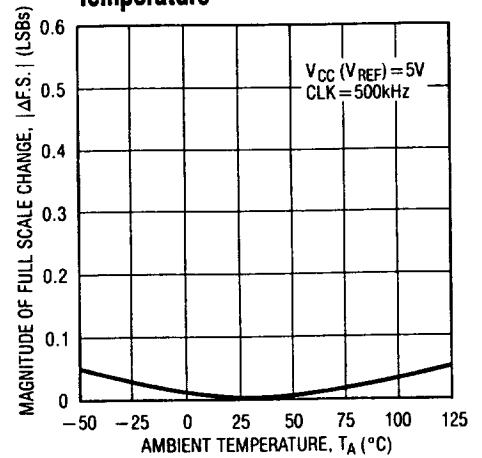
**Change in Offset Error vs Temperature**



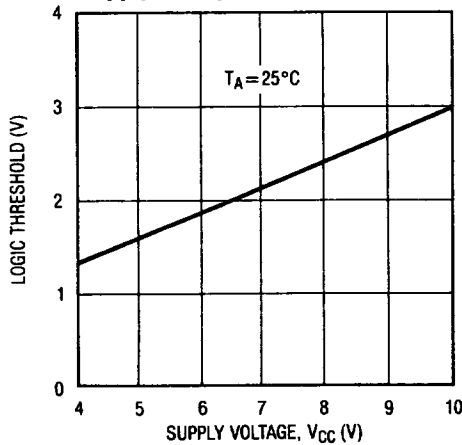
**Change in Linearity Error vs Temperature**



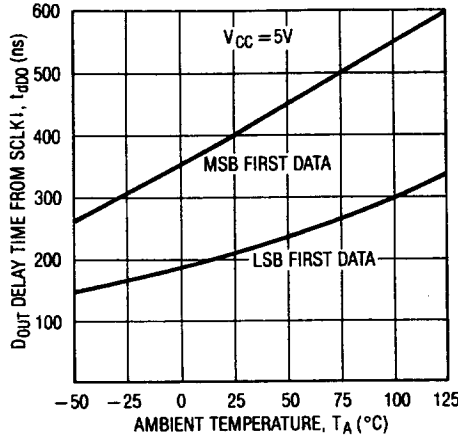
**Change in Full Scale Error vs Temperature**



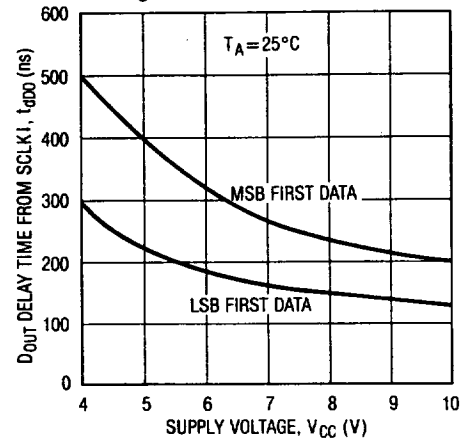
**Digital Input Logic Threshold vs Supply Voltage**



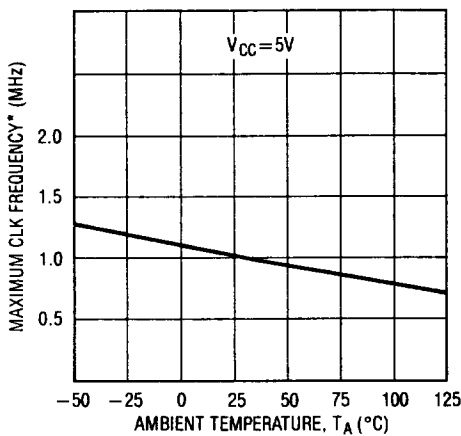
**DOUT Delay Time vs Temperature**



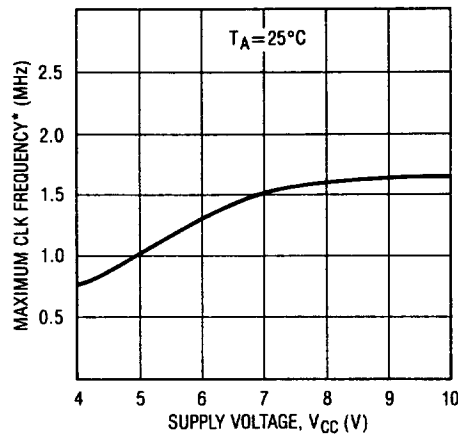
**DOUT Delay Time vs Supply Voltage**



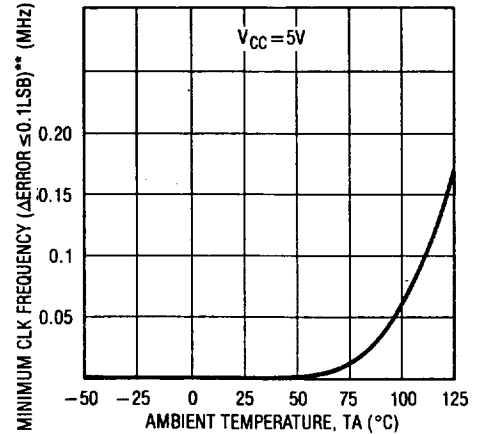
**Maximum Clock Rate vs Temperature**



**Maximum Clock Rate vs Supply Voltage**



**Minimum Clock Rate vs Temperature**



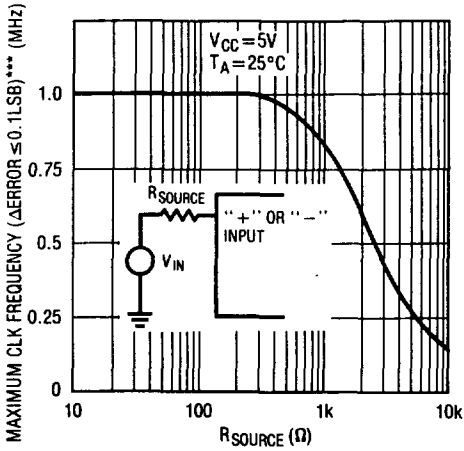
\*MAXIMUM CLK FREQUENCY REPRESENTS THE HIGHEST FREQUENCY AT WHICH CLK CAN BE OPERATED (WITH 50% DUTY CYCLE) WHILE STILL PROVIDING 100ns SETUP TIME FOR THE DEVICE RECEIVING THE DOUT DATA.

\*\*AS THE CLK FREQUENCY IS DECREASED FROM 500kHz, MINIMUM CLK FREQUENCY (ΔERROR ≤ 0.1LSB) REPRESENTS THE FREQUENCY AT WHICH A 0.1LSB SHIFT IN ANY CODE TRANSITION FROM ITS 500kHz VALUE IS FIRST DETECTED.

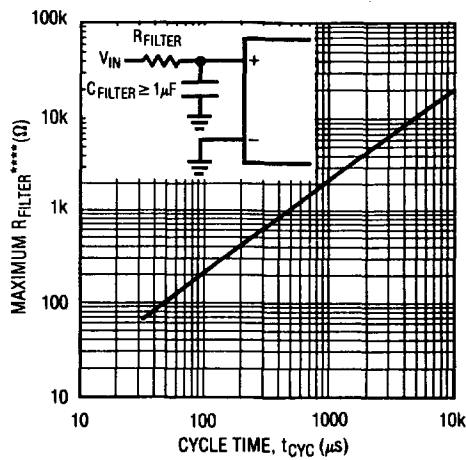


# TYPICAL PERFORMANCE CHARACTERISTICS

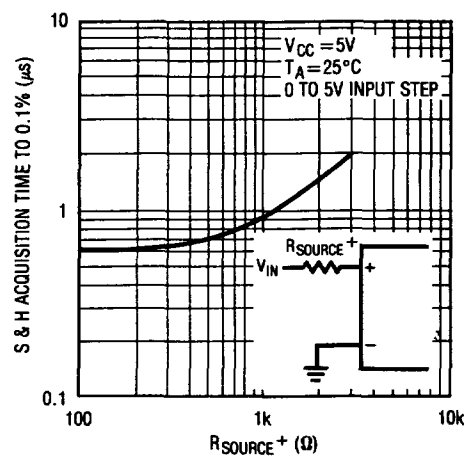
**Maximum Clock Rate vs Source Resistance LTC1091-4**



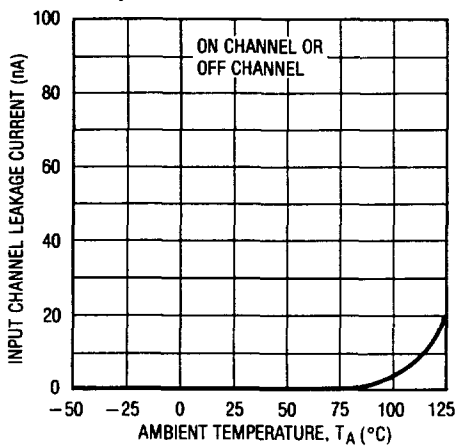
**Maximum Filter Resistor vs Cycle Time LTC1091-4**



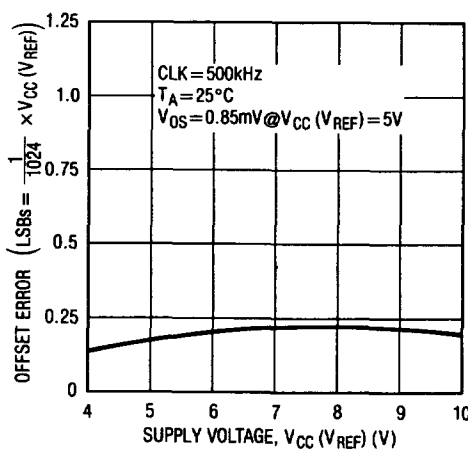
**Sample and Hold Acquisition Time vs Source Resistance LTC1091-4**



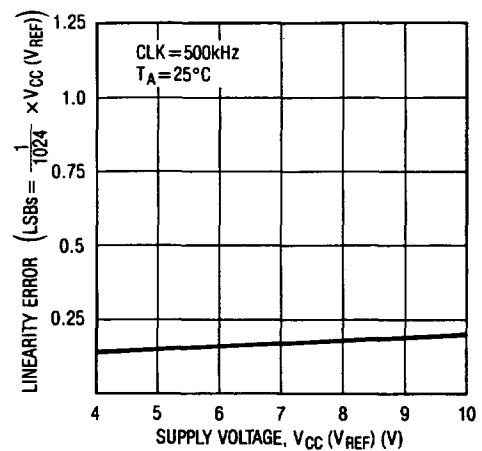
**Input Channel Leakage Current vs Temperature LTC1091/2**



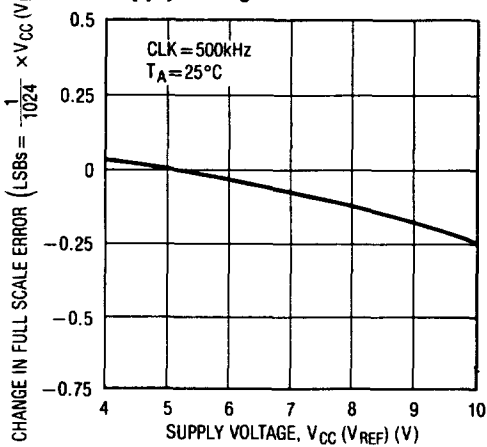
**Offset Error vs Supply Voltage LTC1091**



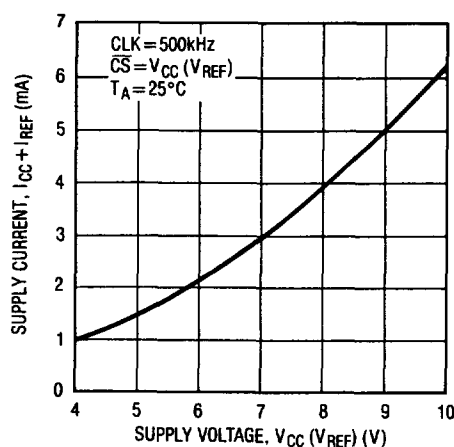
**Linearity Error vs Supply Voltage LTC1091**



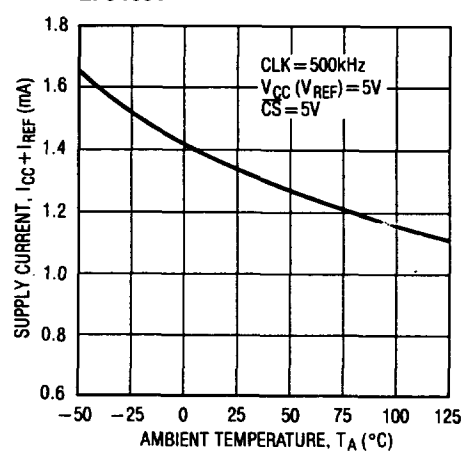
**Change in Full Scale Error vs Supply Voltage LTC1091**



**Supply Current vs Supply Voltage LTC1091**



**Supply Current vs Temperature LTC1091**

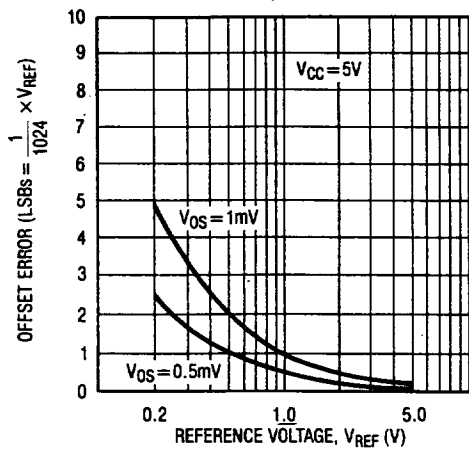


\*\*\*AS THE CLK FREQUENCY AND SOURCE RESISTANCE ARE INCREASED, MAXIMUM CLK FREQUENCY ( $\Delta$ ERROR  $\leq$  0.1LSB) REPRESENTS THE FREQUENCY AT WHICH A 0.1LSB SHIFT IN ANY CODE TRANSITION FROM ITS 500kHz, 0Ω VALUE IS FIRST DETECTED.

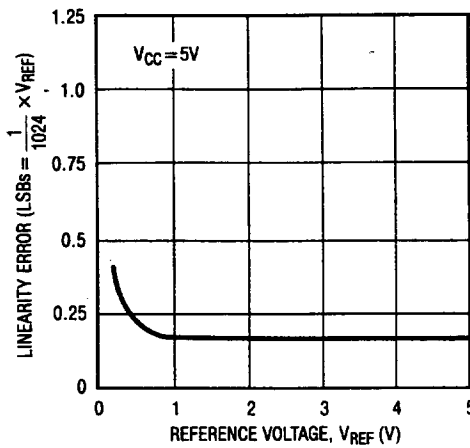
\*\*\*\*MAXIMUM  $R_{FILTER}$  REPRESENTS THE FILTER RESISTOR VALUE AT WHICH A 0.1LSB CHANGE IN FULL-SCALE ERROR FROM ITS VALUE AT  $R_{FILTER}=0$  IS FIRST DETECTED.

# TYPICAL PERFORMANCE CHARACTERISTICS

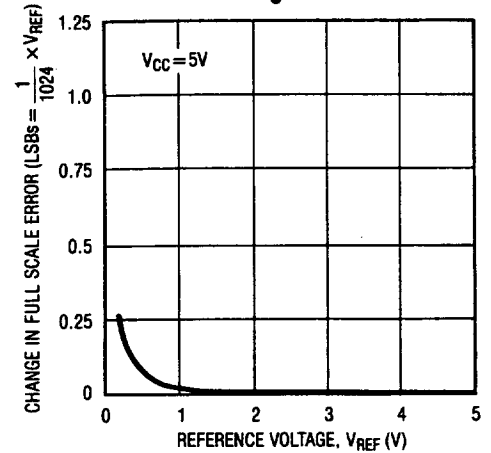
**Unadjusted Offset Error vs Reference Voltage LTC1092/3/4**



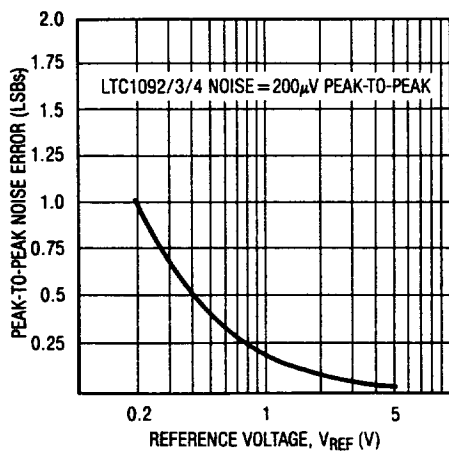
**Linearity Error vs Reference Voltage LTC1092/3/4**



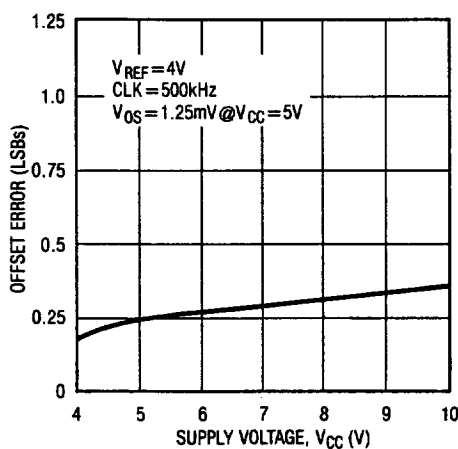
**Change in Full Scale Error vs Reference Voltage LTC1092/3/4**



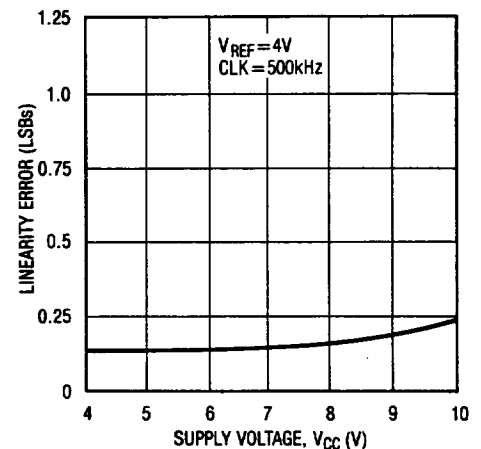
**Noise Error vs Reference Voltage LTC1092/3/4**



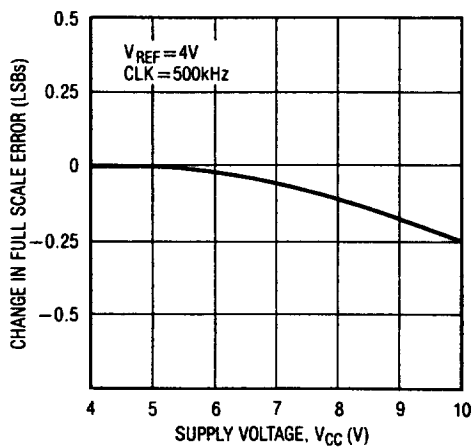
**Offset Error vs Supply Voltage LTC1092/3/4**



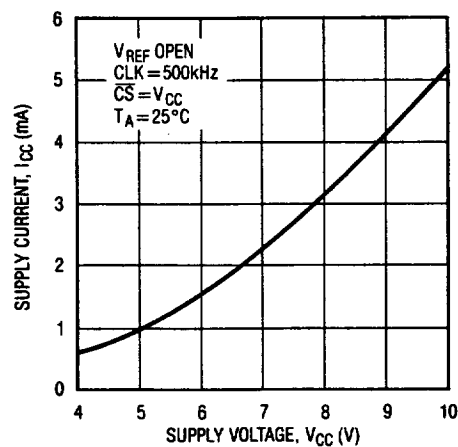
**Linearity Error vs Supply Voltage LTC1092/3/4**



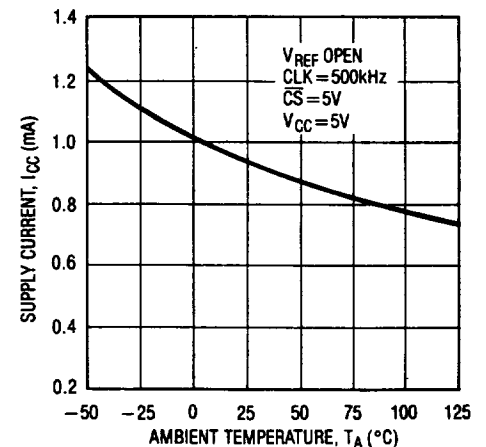
**Change in Full Scale Error vs Supply Voltage LTC1092/3/4**



**Supply Current vs Supply Voltage LTC1092/3/4**

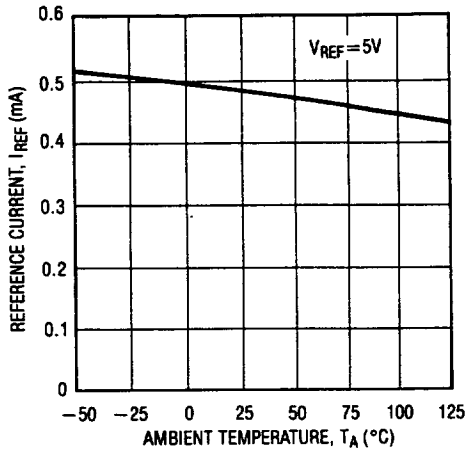


**Supply Current vs Temperature LTC1092/3/4**

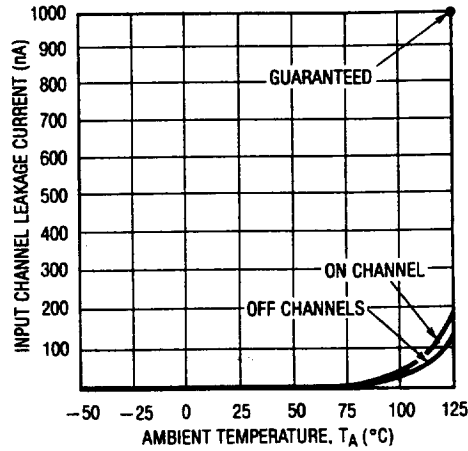


## TYPICAL PERFORMANCE CHARACTERISTICS

Reference Current vs Temperature  
LTC1092/3/4



Input Channel Leakage Current vs Temperature LTC1093/4



## APPLICATIONS INFORMATION

The LTC1091-4 are data acquisition components which contain the following functional blocks:

1. 10-bit successive approximation A/D converter
2. Analog multiplexer (MUX)
3. Sample and hold (S/H)
4. Synchronous, half duplex serial interface
5. Control and timing logic

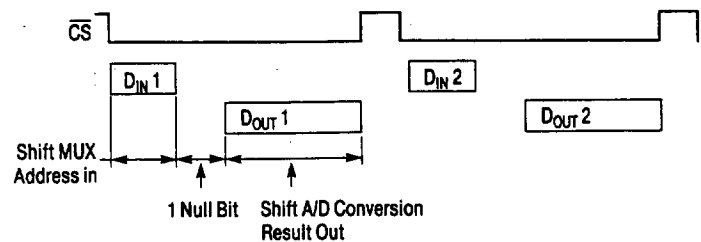
### DIGITAL CONSIDERATIONS

#### 1. Serial Interface

The LTC1091/3/4 communicates with microprocessors and other external circuitry via a synchronous, half duplex, four wire serial interface while the LTC1092 uses a three wire interface (see Operating Sequence). The clock (CLK) synchronizes the data transfer with each bit being transmitted on the falling CLK edge and captured on the rising CLK edge in both transmitting and receiving systems. The LTC1091/3/4 first receives input data and then transmits back the A/D conversion result (half duplex). Because of

the half duplex operation,  $D_{IN}$  and  $D_{OUT}$  may be tied together allowing transmission over just 3 wires:  $\overline{CS}$ , CLK and DATA ( $D_{IN}/D_{OUT}$ ).

Data transfer is initiated by a falling chip select ( $\overline{CS}$ ) signal. After  $\overline{CS}$  falls the LTC1091/3/4 looks for a start bit. After the start bit is received, a 3-bit input word (6-bits for the LTC1093/4) is shifted into the  $D_{IN}$  input which configures the LTC1091/3/4 and starts the conversion. After one null bit, the result of the conversion is output on the  $D_{OUT}$  line. At the end of the data exchange  $\overline{CS}$  should be brought high. This resets the LTC1091/3/4 in preparation for the next data exchange.



## APPLICATIONS INFORMATION

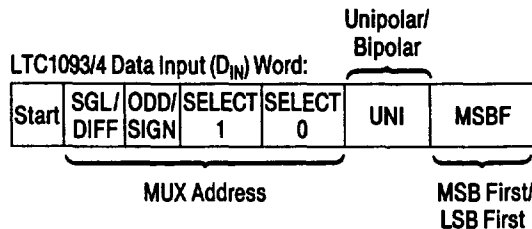
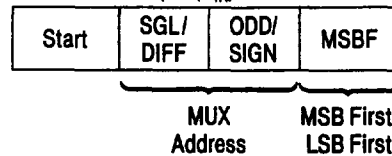
The LTC1092 does not require a configuration input word and has no  $D_{IN}$  pin. A falling  $\overline{CS}$  initiates data transfer as shown in the LTC1092 operating sequence. After  $\overline{CS}$  falls, the first CLK pulse enables  $D_{OUT}$ . After one null bit, the A/D conversion result is output on the  $D_{OUT}$  line. Bringing  $\overline{CS}$  high resets the LTC1092 for the next data exchange.

### 2. Input Data Word

The LTC1092 requires no  $D_{IN}$  word. It is permanently configured to have a single differential input and to operate in unipolar mode. The conversion result is output on the  $D_{OUT}$  line in MSB first sequence, followed by LSB sequence providing easy interface to MSB or LSB first serial ports. The following discussion applies to the configuration of the LTC1091/3/4.

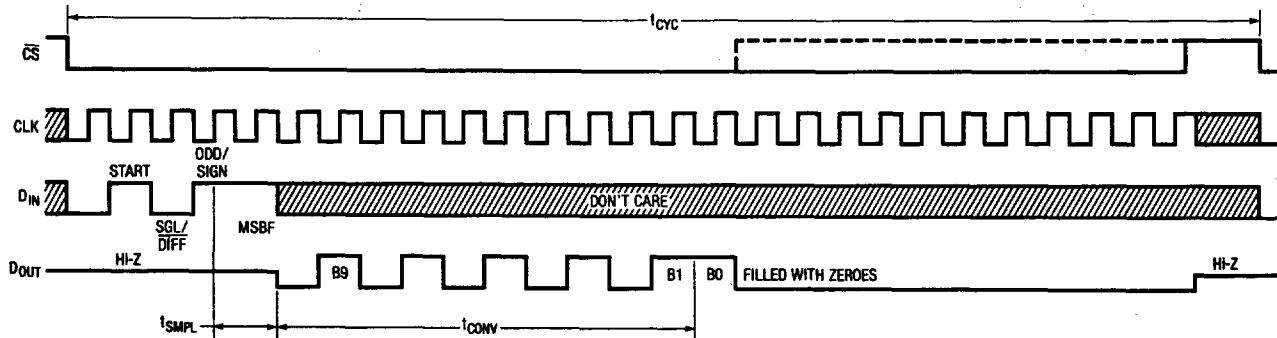
The LTC1091/3/4 clocks data into the  $D_{IN}$  input on the rising edge of the clock. The input data words are defined as follows:

LTC1091 Data Input ( $D_{IN}$ ) Word:

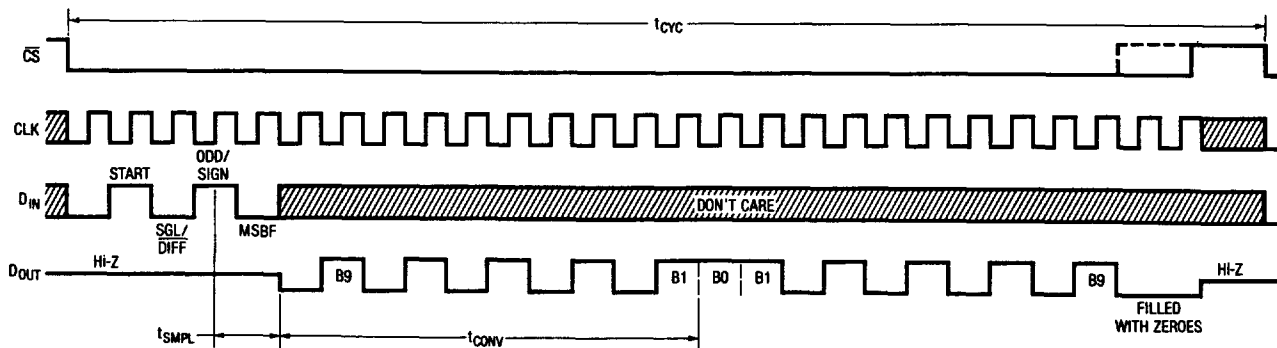


### LTC1091 Operating Sequence Example: Differential Inputs (CH1 +, CH0 -)

#### MSB First Data (MSBF = 1)

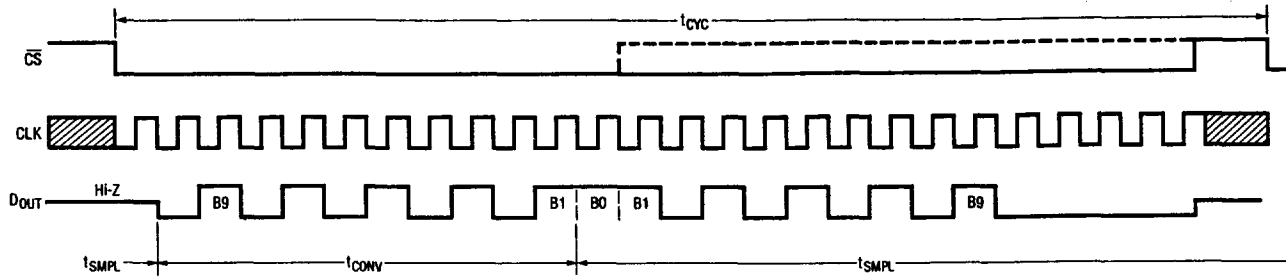


#### LSB First Data (MSBF = 0)



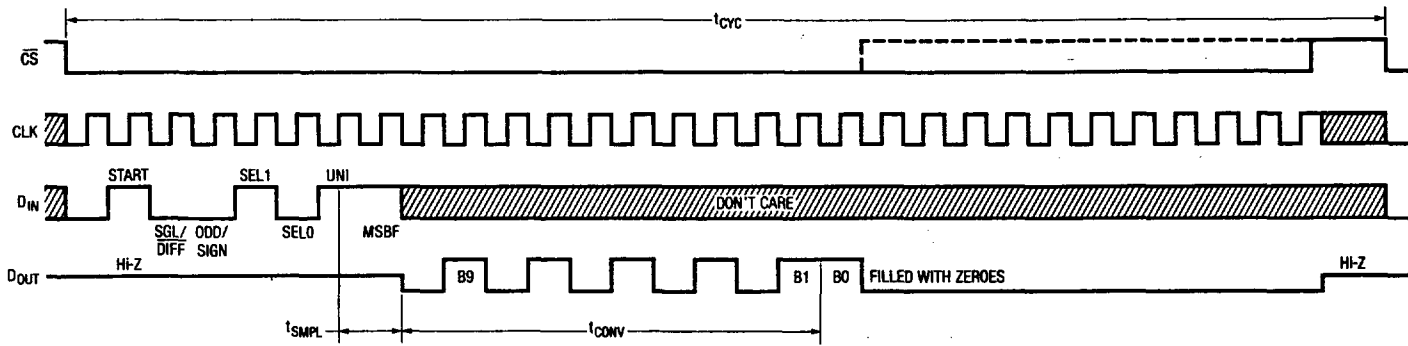
## APPLICATIONS INFORMATION

### LTC1092 Operating Sequence

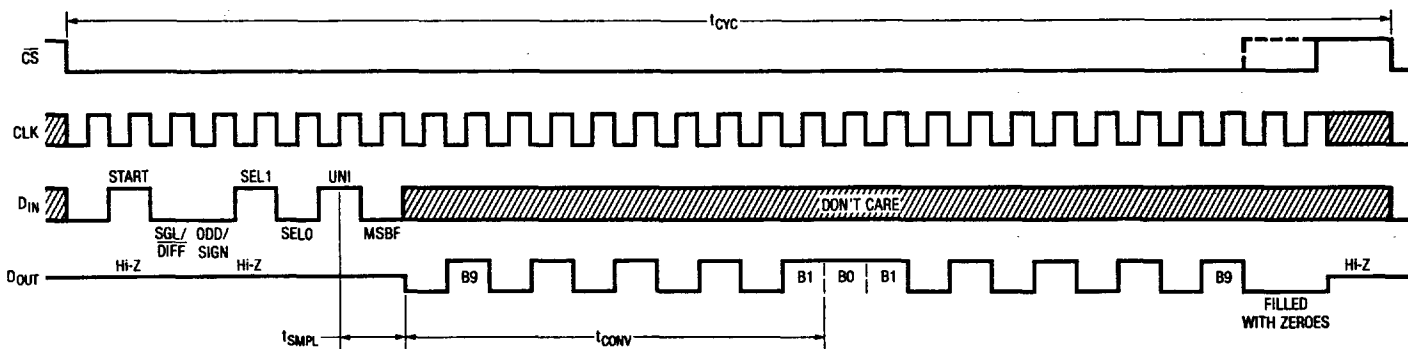


### LTC1093/4 Operating Sequence Example: Differential Inputs (CH4 +, CH5 -), Unipolar Mode

#### MSB First Data (MSBF = 1)



#### LSB First Data (MSBF = 0)



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## APPLICATIONS INFORMATION

### Start Bit

The first "logical one" clocked into the  $D_{IN}$  input after  $\overline{CS}$  goes low is the start bit. The start bit initiates the data transfer. The LTC1091/3/4 will ignore all leading zeros which precede this logical one. After the start bit is received, the remaining bits of the input word will be clocked in. Further inputs on the  $D_{IN}$  pin are then ignored until the next  $\overline{CS}$  cycle.

### Multiplexer (MUX) Address

The bits of the input word following the START bit assign the MUX configuration for the requested conversion. For a

given channel selection, the converter will measure the voltage between the two channels indicated by the + and - signs in the selected row of the following tables. In single ended mode, all input channels are measured with respect to GND on the LTC1091 and COM on the LTC1093/4.

### LTC1093 Channel Selection

MUX ADDRESS			DIFFERENTIAL CHANNEL SELECTION						
SGL/DIFF	ODD/SIGN	SELECT	0	1	2	3	4	5	
0	0	0 0	+	-					
0	0	0 1			+	-			
0	0	1 0					+	-	
0	0	1 1	NOT USED						
0	1	0 0	-	+					
0	1	0 1			-	+			
0	1	1 0					-	+	
0	1	1 1	NOT USED						

MUX ADDRESS			SINGLE ENDED CHANNEL SELECTION						
SGL/DIFF	ODD/SIGN	SELECT	0	1	2	3	4	5	COM
1	0	0 0	+						-
1	0	0 1			+				-
1	0	1 0					+		-
1	0	1 1	NOT USED						
1	1	0 0		+					-
1	1	0 1				+			-
1	1	1 0						+	-
1	1	1 1	NOT USED						

### LTC1091 Channel Selection

MUX ADDRESS		CHANNEL #		GND
SGL/DIFF	ODD/SIGN	0	1	
Single-ended MUX mode	1	0	+	-
	1	1		+
Differential MUX mode	0	0	+	-
	0	1	-	+

### LTC1094 Channel Selection

MUX ADDRESS			DIFFERENTIAL CHANNEL SELECTION							
SGL/DIFF	ODD/SIGN	SELECT	0	1	2	3	4	5	6	7
0	0	0 0	+	-						
0	0	0 1			+	-				
0	0	1 0					+	-		
0	0	1 1							+	-
0	1	0 0	-	+						
0	1	0 1			-	+				
0	1	1 0					-	+		
0	1	1 1							-	+

MUX ADDRESS			SINGLE ENDED CHANNEL SELECTION								
SGL/DIFF	ODD/SIGN	SELECT	0	1	2	3	4	5	6	7	COM
1	0	0 0	+								-
1	0	0 1			+						-
1	0	1 0					+				-
1	0	1 1							+		-
1	1	0 0		+							-
1	1	0 1				+					-
1	1	1 0						+			-
1	1	1 1								+	-

## APPLICATIONS INFORMATION

### MSB First/LSB First (MSBF)

The output data of the LTC1091/3/4 is programmed for MSB first or LSB first sequence using the MSBF bit. When the MSBF bit is a logical one, data will appear on the  $D_{OUT}$  line in MSB first format. Logical zeros will be filled in indefinitely following the last data bit to accommodate longer word lengths required by some microprocessors. When the MSBF bit is a logical zero, LSB first data will follow the normal MSB first data on the  $D_{OUT}$  line. (See operating sequence).

### Unipolar/Bipolar (UNI)

The UNI bit of the LTC1093/4 determines whether the conversion will be unipolar or bipolar. When UNI is a logical one, a unipolar conversion will be performed on the selected input voltage. When UNI is a logical zero, a bipolar conversion will result. The input span and code assignment for each conversion type are shown in the figures below.

The LTC1091/2 are permanently configured for unipolar mode.

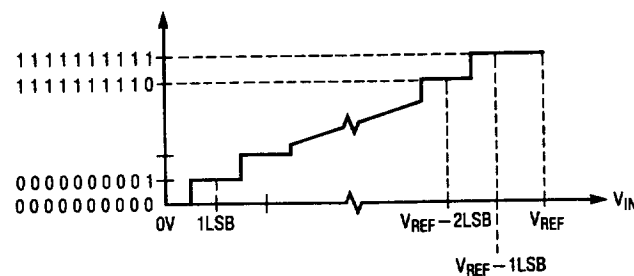
### Unipolar Output Code (UNI = 1)

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE ( $V_{REF} = 5V$ )
1111111111	$V_{REF} - 1LSB$	4.9951V
1111111110	$V_{REF} - 2LSB$	4.9902V
⋮	⋮	⋮
⋮	⋮	⋮
0000000001	1LSB	0.0049V
0000000000	0V	0V

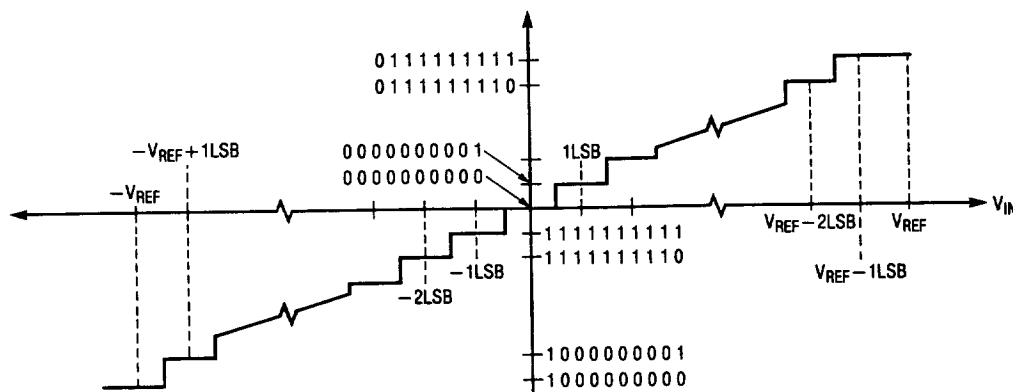
### Bipolar Output Code (UNI = 0) LTC1093/4 Only

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE ( $V_{REF} = 5V$ )
0111111111	$V_{REF} - 1LSB$	4.9902V
0111111110	$V_{REF} - 2LSB$	4.9805V
⋮	⋮	⋮
⋮	⋮	⋮
0000000001	1LSB	0.0098V
0000000000	0V	0V
1111111111	-1LSB	-0.0098V
1111111110	-2LSB	-0.0195V
⋮	⋮	⋮
⋮	⋮	⋮
1000000001	$-(V_{REF}) + 1LSB$	-4.9902V
1000000000	$-(V_{REF})$	-5.000V

### Unipolar Transfer Curve (UNI = 1)



### Bipolar Transfer Curve (UNI = 0) LTC1093/4 Only



## APPLICATIONS INFORMATION

### 3. Accommodating Microprocessors with Different Word Lengths

The LTC1091/3/4 will fill zeroes indefinitely after the transmitted data until CS is brought high. At that time the D<sub>OUT</sub> line is disabled. This makes interfacing easy to MPU serial ports with different transfer increments including 4 bits (e.g., COP400) and 8 bits (e.g., SPI and MICROWIRE/PLUS). Any word length can be accommodated by the correct positioning of the start bit in the LTC1091 input word.

Figure 1 shows examples of LTC1091 input and output words for 4-bit and 8-bit processors. A complete data exchange can be implemented with two 4-bit MPU outputs and three inputs in 4-bit systems and one 8-bit output and two inputs in 8-bit systems. The resulting data winds up left justified in the MPU with zeroes automatically filled in the unused low order bits by the LTC1091. In section 5 another example is given using the MC68HC05C4 which eliminates one 8-bit transfer and positions data right justified inside the MPU.

### 4. Operation with D<sub>IN</sub> and D<sub>OUT</sub> Tied Together

The LTC1091/3/4 can be operated with D<sub>IN</sub> and D<sub>OUT</sub> tied together. This eliminates one of the lines required to communicate to the MPU. Data is transmitted in both directions on a single wire. The processor pin connected to this data line should be configurable as either an input or an output. The LTC1091, for example, will take control of the data line and drive it low on the 4th falling CLK edge after the start bit is received (see Figure 2). Therefore the processor port line must be switched to an input before this happens, to avoid a conflict.

In the next section, an example is made of interfacing the LTC1091 with D<sub>IN</sub> and D<sub>OUT</sub> tied together to the Intel 8051 MPU.

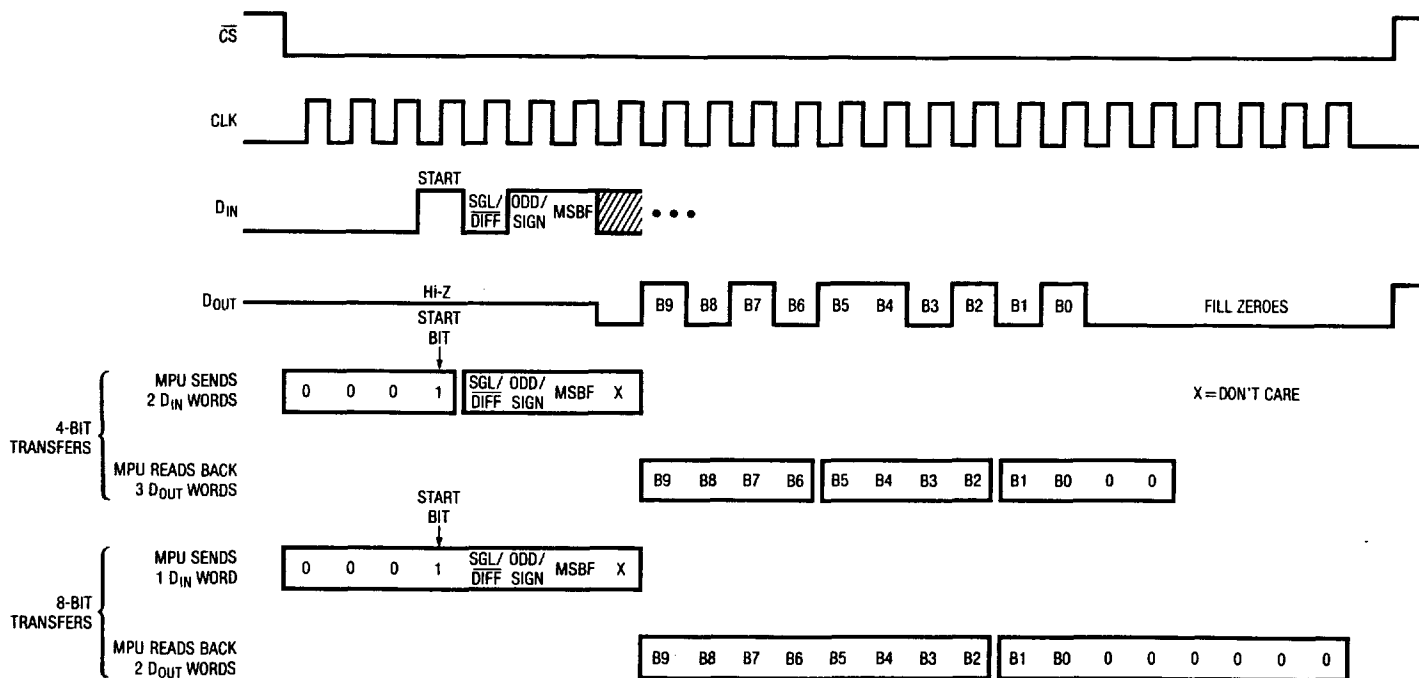


Figure 1. LTC1091 Input and Output Word Arrangements for 4-Bit and 8-Bit Serial Port Microprocessors



## APPLICATIONS INFORMATION

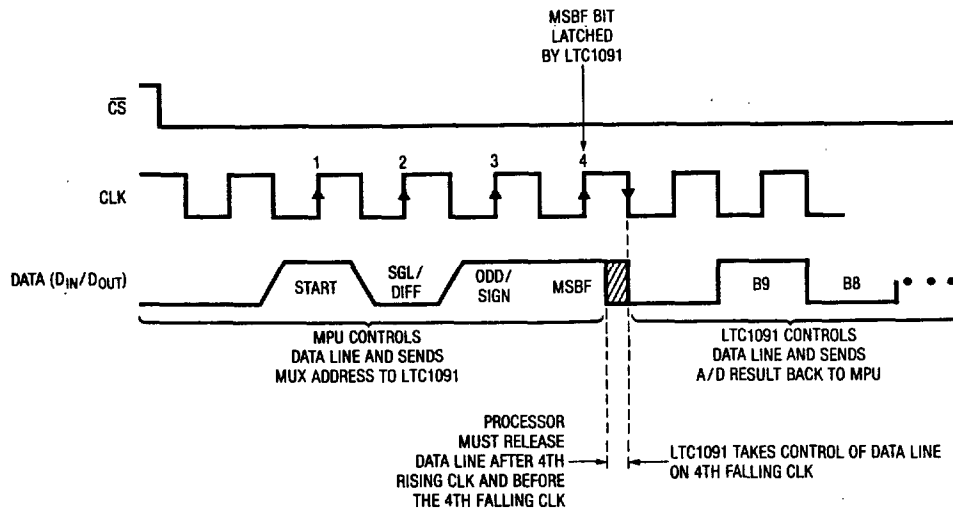


Figure 2. LTC1091 Operation with  $D_{IN}$  and  $D_{OUT}$  Tied Together

### 5. Microprocessor Interfaces

The LTC1091-4 can interface directly (without external hardware) to most popular microprocessor (MPU) synchronous serial formats (see Table 1). If an MPU without a dedicated serial port is used, then 3 or 4 of the MPU's parallel port lines can be programmed to form the serial link to the LTC1091-4. Included here are one serial interface example and one example showing a parallel port programmed to form the serial interface.

Table 1. Microprocessors with Hardware Serial Interfaces Compatible with the LTC1091-4

PART NUMBER	TYPE OF INTERFACE
<b>Motorola</b>	
MC6805S2, S3	SPI
MC68HC11	SPI
MC68HC05	SPI
<b>RCA</b>	
CDP68HC05	SPI
<b>Hitachi</b>	
HD6305	SCI Synchronous
HD63705	SCI Synchronous
HD6301	SCI Synchronous
HD63701	SCI Synchronous
HD6303	SCI Synchronous
HD64180	CSI/O
<b>National Semiconductor</b>	
COP400 Family	MICROWIRE†
COP800 Family	MICROWIRE/PLUS†
NS8050U	MICROWIRE/PLUS
HPC16000 Family	MICROWIRE/PLUS
<b>Texas Instruments</b>	
TMS7002	Serial Port
TMS7042	Serial Port
TMS70C02	Serial Port
TMS70C42	Serial Port
TMS32011*	Serial Port
TMS32020	Serial Port

\*Requires external hardware

†MICROWIRE and MICROWIRE/PLUS are trademarks of National Semiconductor Corp.

## APPLICATIONS INFORMATION

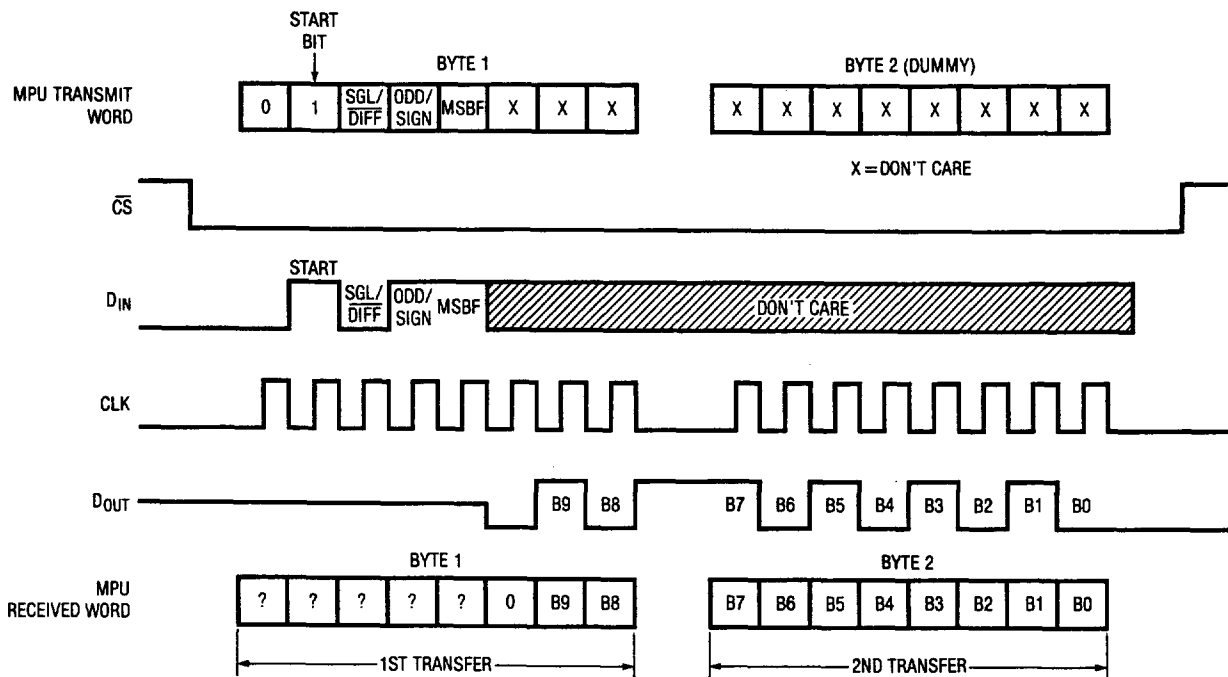
### Motorola SPI (MC68HC05C4, MC68HC11)

The MC68HC05C4 has been chosen as an example of an MPU with a dedicated serial port. This MPU transfers data MSB first and in 8-bit increments. With two 8-bit transfers, the A/D result is read into the MPU. The first 8-bit transfer sends the  $D_{IN}$  word to the LTC1091 and clocks B9 and B8 of the A/D conversion result into the processor. The sec-

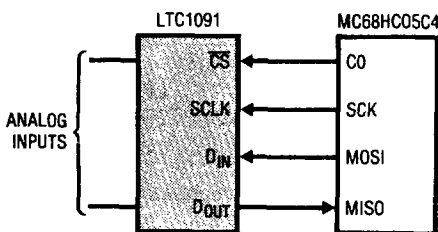
ond 8-bit transfer clocks the remaining bits, B7 through B0, into the MPU.

ANDING the first MPU received byte with 03 Hex clears the 6 most significant bits. Notice how the position of the start bit in the first MPU transmit word is used to position the A/D result right justified in two memory locations.

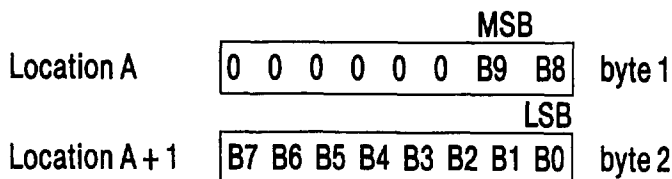
#### Data Exchange Between LTC1091 and MC68HC05C4



#### Hardware and Software Interface to Motorola MC68HC05C4 Microcontroller



$D_{OUT}$  from LTC1091 stored in MC68HC05C4 RAM



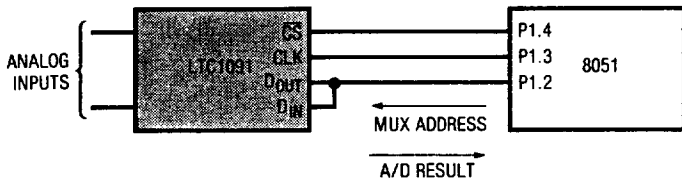
LABEL	MNEMONIC	COMMENTS
START	BCLRn	Bit 0 Port C goes low ( $\overline{CS}$ goes low)
	LDA	Load LTC1090 $D_{IN}$ word into Acc.
	STA	Load LTC1090 $D_{IN}$ word into SPI from Acc. Transfer begins.
	TST	Test status of SPIF
	BPL	Loop to previous instruction if not done with transfer
	LDA	Load contents of SPI data register into Acc. ( $D_{OUT}$ MSBs)
	STA	Start next SPI cycle
	AND	Clear 6 MSBs of first $D_{OUT}$ word
	STA	Store in memory location A (MSBs)
	TST	Test status of SPIF
	BPL	Loop to previous instruction if not done with transfer
	BSETn	Set B0 of Port C ( $\overline{CS}$ goes high)
	LDA	Load contents of SPI data register into Acc. ( $D_{OUT}$ LSBs)
	STA	Store in memory location A + 1 (LSBs)

## APPLICATIONS INFORMATION

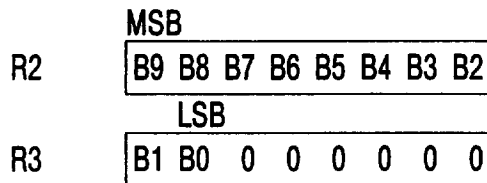
### Interfacing to the Parallel Port of the Intel 8051 Family

The Intel 8051 has been chosen to demonstrate the interface between the LTC1091 and parallel port microprocessors. Normally the  $\overline{CS}$ , SCLK and  $D_{IN}$  signals would be generated on 3 port lines and the  $D_{OUT}$  signal read on a 4th port line. This works very well. However, we will demonstrate here an interface with the  $D_{IN}$  and  $D_{OUT}$  of the LTC1091 tied together as described in section 4. This saves one wire.

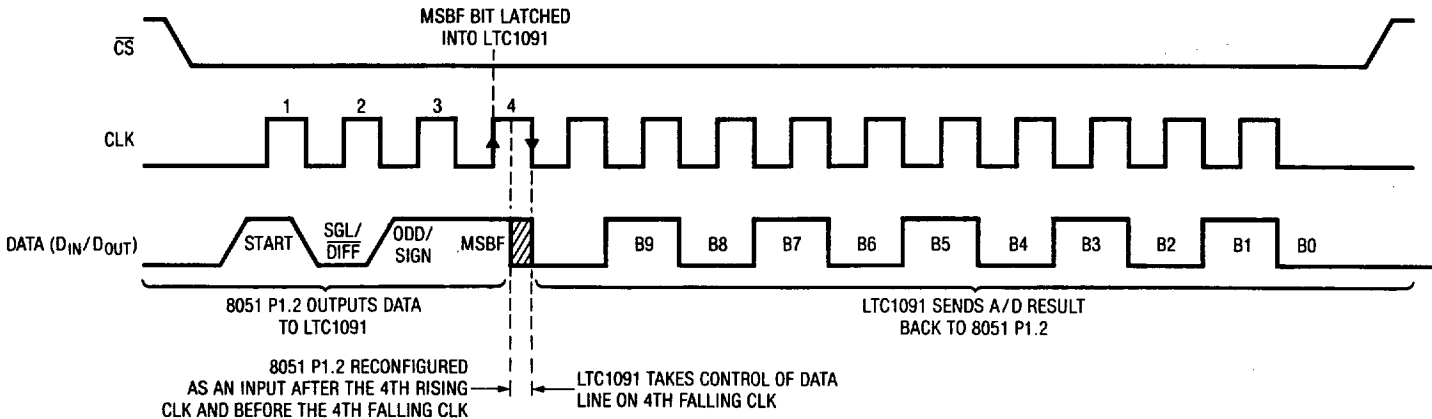
The 8051 first sends the start bit and MUX address to the LTC1091 over the data line connected to P1.2. Then P1.2 is reconfigured as an input (by writing to it a one) and the 8051 reads back the 10-bit A/D result over the same data line.



### $D_{OUT}$ from LTC1091 stored in 8051 RAM



LABEL	MNEMONIC	OPERAND	COMMENTS
LOOP 1	MOV	A, #FFH	$D_{IN}$ word for LTC1091
	SETB	P1.4	Make sure $\overline{CS}$ is high
	CLR	P1.4	$\overline{CS}$ goes low
	MOV	R4, #04	Load counter
	RLC	A	Rotate $D_{IN}$ bit into Carry
	CLR	P1.3	SCLK goes low
LOOP	MOV	P1.2, C	Output $D_{IN}$ bit to LTC1091
	SETB	P1.3	SCLK goes high
	DJNZ	R4, LOOP 1	Next bit
	MOV	P1, #04	Bit 2 becomes an input
	CLR	P1.3	SCLK goes low
	MOV	R4, #09	Load counter
	MOV	C, P1.2	Read data bit into Carry
	RLC	A	Rotate data bit into Acc.
	SETB	P1.3	SCLK goes high
	CLR	P1.3	SCLK goes low
	DJNZ	R4, LOOP	Next bit
	MOV	R2, A	Store MSBs in R2
	MOV	C, P1.2	Read data bit into Carry
	SETB	P1.3	SCLK goes high
	CLR	P1.3	SCLK goes low
	CLR	A	Clear Acc.
	RLC	A	Rotate data bit from Carry to Acc.
	MOV	C, P1.2	Read data bit into Carry
RRC	A	Rotate right into Acc.	
RRC	A	Rotate right into Acc.	
MOV	R3, A	Store LSBs in R3	
SETB	P1.4	$\overline{CS}$ goes high	



## APPLICATIONS INFORMATION

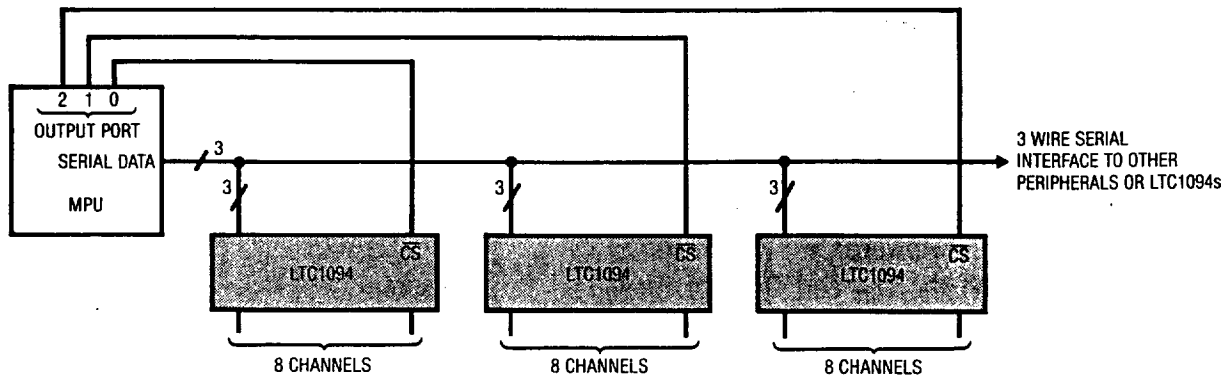


Figure 3. Several LTC1094s Sharing One 3 Wire Serial Interface

### Sharing the Serial Interface

The LTC1094 can share the same 2 or 3 wire serial interface with other peripheral components or other LTC1094s (see Figure 3). In this case, the  $\overline{CS}$  signals decide which LTC1094 is being addressed by the MPU.

## ANALOG CONSIDERATIONS

### 1. Grounding

The LTC1091–4 should be used with an analog ground plane and single point grounding techniques.

The AGND pin (GND on the LTC1091/2) should be tied directly to this ground plane.

The DGND pin of the LTC1093/4 can also be tied directly to this ground plane because minimal digital noise is generated within the chip itself.

The  $V_{CC}$  pin should be bypassed to the ground plane with a  $4.7\mu\text{F}$  tantalum with leads as short as possible.  $AV_{CC}$  and  $DV_{CC}$  should be tied together on the LTC1094. The  $V^-$  pin (LTC1093/4) should be bypassed with a  $0.1\mu\text{F}$  ceramic disk. For single supply applications,  $V^-$  can be tied to the ground plane.

It is also recommended that the  $REF^-$  pin and the COM pin be tied directly to the ground plane. All analog inputs should be referenced directly to the single point ground. Digital inputs and outputs should be shielded from and/or routed away from the reference and analog circuitry.

Figure 4 shows an example of an ideal LTC1091 ground plane design for a two sided board. Of course this much ground plane will not always be possible, but users should strive to get as close to this ideal as possible.

### 2. Bypassing

For good performance,  $V_{CC}$  must be free of noise and ripple. Any changes in the  $V_{CC}$  voltage with respect to analog ground during a conversion cycle can induce errors or noise in the output code. Because the  $V_{CC}$  ( $V_{REF}$ ) pin of the LTC1091 defines the voltage span of the A/D converter, its bypassing is especially important.  $V_{CC}$  noise and ripple can be kept below  $1\text{mV}$  by bypassing the  $V_{CC}$  pin directly to the analog ground plane with a  $4.7\mu\text{F}$  tantalum with leads as short as possible.  $AV_{CC}$  and  $DV_{CC}$  should be tied together on the LTC1094. Figures 5 and 6 show the effects of good and poor  $V_{CC}$  bypassing.

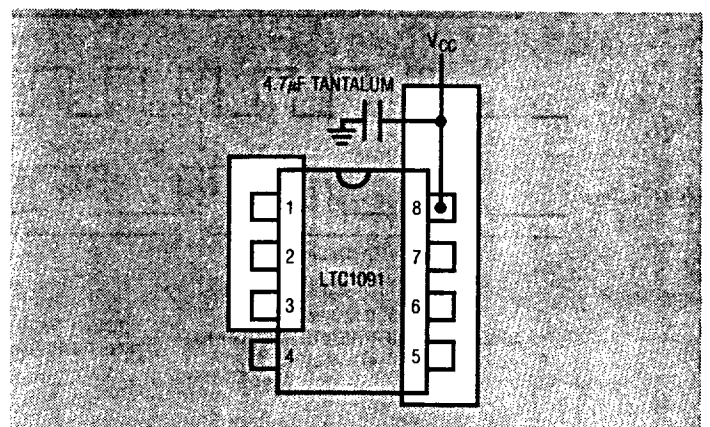


Figure 4. Example Ground Plane for the LTC1091

## APPLICATIONS INFORMATION

### 3. Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1091-4 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. However, if large source resistances are used or if slow settling op amps drive the inputs, care must be taken to insure that the transients caused by the current spikes settle completely before the conversion begins.

#### Source Resistance

The analog inputs of the LTC1091-4 look like a 60pF capacitor ( $C_{IN}$ ) in series with a 500Ω resistor ( $R_{ON}$ ) as shown in Figure 7.  $C_{IN}$  gets switched between the selected “+” and “-” inputs once during each conversion cycle. Large external source resistors and capacitances will slow the settling of the inputs. It is important that the overall RC time constants be short enough to allow the analog inputs to completely settle within the allowed time.

#### “+” Input Settling

This input capacitor is switched onto the “+” input during the sample phase ( $t_{SMPL}$ , see Figure 8). The sample phase is the 1/2 CLK cycles before the conversion starts. The voltage on the “+” input must settle completely within this sample time. Minimizing  $R_{SOURCE}^+$  and  $C1$  will improve the input settling time. If large “+” input source resistance must be used, the sample time can be increased by using a slower CLK frequency. With the minimum possible sample time of 3μs,  $R_{SOURCE}^+ < 2k$  and  $C1 < 20pF$  will provide adequate settling.

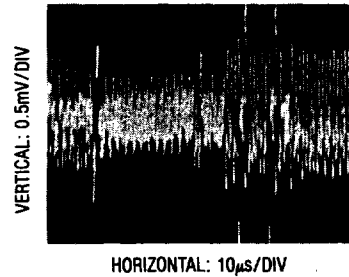


Figure 5. Poor  $V_{CC}$  Bypassing. Noise and Ripple Can Cause A/D Errors

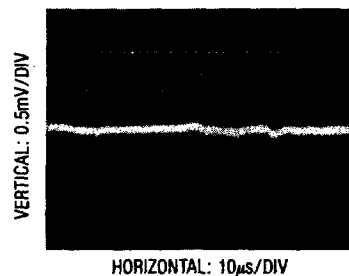


Figure 6. Good  $V_{CC}$  Bypassing Keeps Noise and Ripple On  $V_{CC}$  Below 1mV

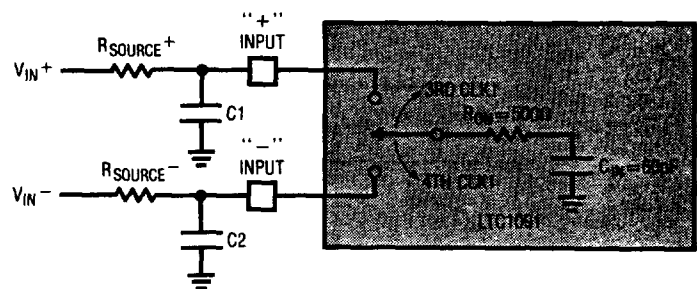


Figure 7. Analog Input Equivalent Circuit

## APPLICATIONS INFORMATION

### “-” Input Settling

At the end of the sample phase the input capacitor switches to the “-” input and the conversion starts (see Figure 8). During the conversion, the “+” input voltage is effectively “held” by the sample and hold and will not affect the conversion result. However, it is critical that the “-” input voltage settle completely during the first CLK cycle of the conversion time and be free of noise. Minimizing  $R_{SOURCE^-}$  and  $C_2$  will improve settling time. If large “-” input source resistance must be used, the time allowed for settling can be extended by using a slower CLK frequency. At the maximum CLK rate of 500kHz,  $R_{SOURCE^-} < 1k\Omega$  and  $C_2 < 20pF$  will provide adequate settling.

### Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settle within the allowed time (see Figure 8). Again, the “+” and “-” input sampling times can be extended as described above to accommodate slower op amps. Most op amps including the LT1006 and LT1013 single supply op amps, can be made to settle well even with the minimum settling windows of  $3\mu s$  (“+” input) and  $2\mu s$  (“-” input) which occur at the maximum clock rate of 500kHz. Figures 9 and 10 show examples of adequate and poor op amp settling.

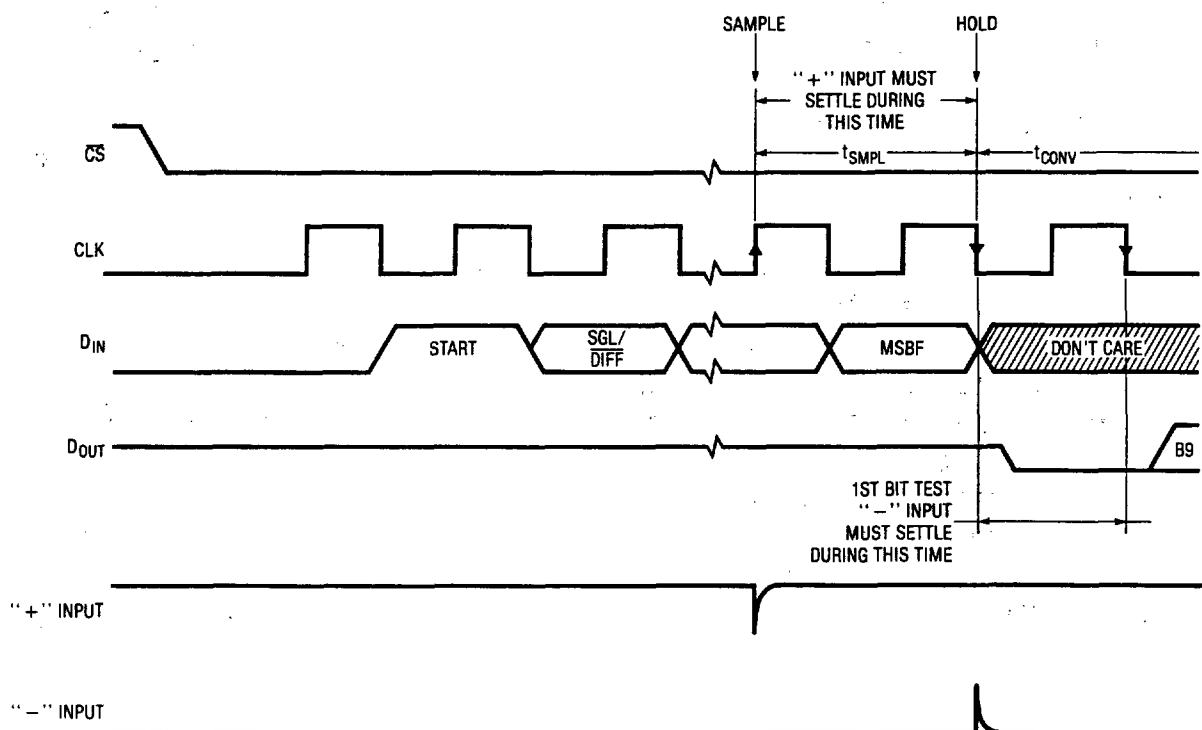


Figure 8. “+” and “-” Input Settling Windows

## APPLICATIONS INFORMATION

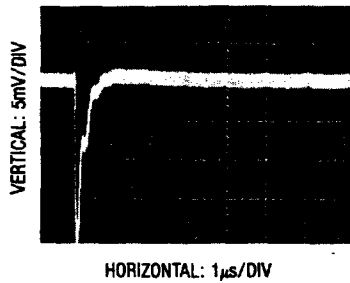


Figure 9. Adequate Settling of Op Amp Driving Analog Input

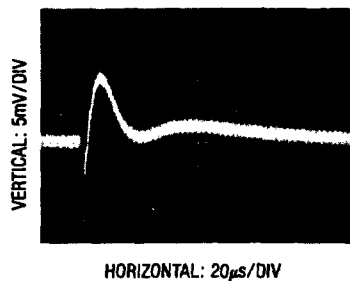


Figure 10. Poor Op Amp Settling Can Cause A/D Errors

### RC Input Filtering

It is possible to filter the inputs with an RC network as shown in Figure 11. For large values of  $C_F$  (e.g.,  $1\mu\text{F}$ ), the capacitive input switching currents are averaged into a net DC current. Therefore, a filter should be chosen with a small resistor and large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately  $I_{DC} = 60\text{pF} \times V_{IN}/t_{CYC}$  and is roughly proportional to  $V_{IN}$ . When running at the minimum cycle time of  $32\mu\text{s}$ , the input current equals  $9\mu\text{A}$  at  $V_{IN} = 5\text{V}$ . In this case, a filter resistor of  $50\Omega$  will cause 0.1LSB of full-scale error. If a larger filter resistor must be used, errors can be eliminated by increasing the cycle time as shown in the typical curve of Maximum Filter Resistor vs Cycle Time.

### Input Leakage Current

Input leakage currents can also create errors if the source resistance gets too large. For instance, the maximum input leakage specification of  $1\mu\text{A}$  (at  $125^\circ\text{C}$ ) flowing through a source resistance of  $1\text{k}\Omega$  will cause a voltage drop of  $1\text{mV}$  or 0.2LSB. This error will be much reduced at lower temperatures because leakage drops rapidly (see typical curve of Input Channel Leakage Current vs Temperature).

## 4. Sample and Hold

### Single Ended Inputs

The LTC1091, LTC1093 and LTC1094 provide a built-in sample and hold (S&H) function for signals acquired in the single ended mode. This sample and hold allows conversion of rapidly varying signals (see typical curve of S&H Acquisition Time vs Source Resistance). The input voltage is sampled during the  $t_{SAMPL}$  time as shown in Figure 8. The sampling interval begins as the bit preceding the MSBF bit is shifted in and continues until the falling CLK edge after the MSBF bit is received. On this falling edge, the S&H goes into hold mode and the conversion begins.

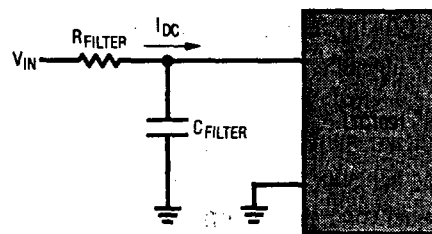


Figure 11. RC Input Filtering

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## APPLICATIONS INFORMATION

### Differential Inputs

With differential inputs, the A/D no longer converts just a single voltage but rather the difference between two voltages. In this case, the voltage on the selected “+” input is still sampled and held and therefore may be rapidly time varying just as in single ended mode. However, the voltage on the selected “-” input must remain constant and be free of noise and ripple throughout the conversion time. Otherwise, the differencing operation may not be performed accurately. The conversion time is 10 CLK cycles. Therefore, a change in the “-” input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the “-” input this error would be:

$$V_{\text{ERROR(MAX)}} = V_{\text{PEAK}} \times 2 \times \pi \times f(\text{“-”}) \times 10/f_{\text{CLK}}$$

Where  $f(\text{“-”})$  is the frequency of the “-” input voltage,  $V_{\text{PEAK}}$  is its peak amplitude and  $f_{\text{CLK}}$  is the frequency of the CLK. In most cases  $V_{\text{ERROR}}$  will not be significant. For a 60Hz signal on the “-” input to generate a 1/4LSB error (1.25mV) with the converter running at CLK = 500kHz, its peak value would have to be 150mV.

### 5. Reference Inputs

The voltage on the reference inputs of the LTC1091-4 defines the voltage span of the A/D converter. The reference inputs look primarily like a 10kΩ resistor but will have transient capacitive switching currents due to the switched capacitor conversion technique (see Figure 12). During each bit test of the conversion (every CLK cycle), a capacitive current spike will be generated on the reference pins by the A/D. These current spikes settle quickly and do not cause a problem. However, if slow settling circuitry is used to drive the reference inputs, care must be taken to ensure that transients caused by these current spikes settle completely during each bit test of the conversion.

When driving the reference inputs, three things should be kept in mind:

1. The source resistance ( $R_{\text{OUT}}$ ) driving the reference inputs should be low (less than 1Ω) to prevent DC drops caused by the 1mA maximum reference current ( $I_{\text{REF}}$ ).
2. Transients on the reference inputs caused by the capacitive switching currents must settle completely during each bit test (each CLK cycle). Figures 13 and 14 show examples of both adequate and poor settling. Using a slower CLK will allow more time for the reference to settle. However, even at the maximum CLK rate of 500kHz most references and op amps can be made to settle within the 2μs bit time.
3. It is recommended that the REF- input of the LTC1094 be tied directly to the analog ground plane. If REF- is biased at a voltage other than ground, the voltage must not change during a conversion cycle. This voltage must also be free of noise and ripple with respect to analog ground.

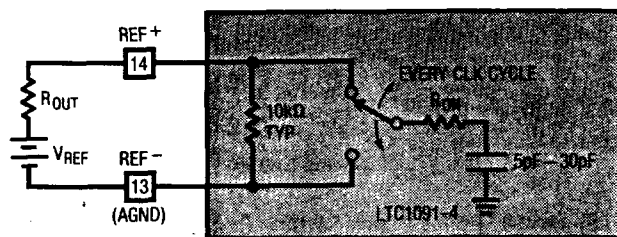


Figure 12. Reference Input Equivalent Circuit

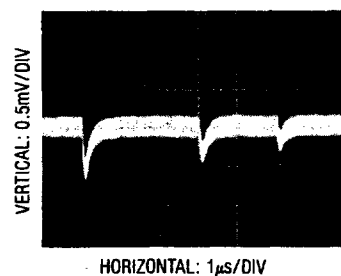


Figure 13. Adequate Reference Settling

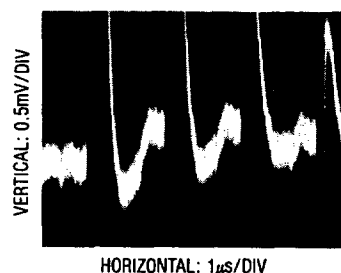


Figure 14. Poor Reference Settling Can Cause A/D Errors



## APPLICATIONS INFORMATION

### 6. Reduced Reference Operation

The minimum reference voltage of the LTC1091 is limited to 4.5V because the  $V_{CC}$  supply and reference are internally tied together. However, the LTC1092/3/4 can operate with reference voltages below 1V.

The effective resolution of the LTC1092/3/4 can be increased by reducing the input span of the converter. The LTC1092/3/4 exhibits good linearity and gain over a wide range of reference voltages (see typical curves of Linearity and Full Scale Error vs Reference Voltage). However, care must be taken when operating at low values of  $V_{REF}$  because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converter. The following factors must be considered when operating at low  $V_{REF}$  values.

1. Offset
2. Noise
3. Conversion speed (CLK frequency)

#### Offset with Reduced $V_{REF}$

The offset of the LTC1092/3/4 has a larger effect on the output code when the A/D is operated with reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Unadjusted Offset Error vs Reference Voltage shows how offset in LSBs is related to reference voltage for a typical value of  $V_{OS}$ . For example, a  $V_{OS}$  of 0.5mV which is 0.1LSB with a 5V reference becomes 0.5LSB with a 1V reference and 2.5LSBs with a 0.2V reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the “-” input to the LTC1092/3/4.

#### Noise with Reduced $V_{REF}$

The total input referred noise of the LTC1092/3/4 can be reduced to approximately 200 $\mu$ V peak-to-peak using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference inputs. This noise is insignificant with a 5V reference but will become a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Noise Error vs Reference Voltage shows the LSB contribution of this 200 $\mu$ V of noise.

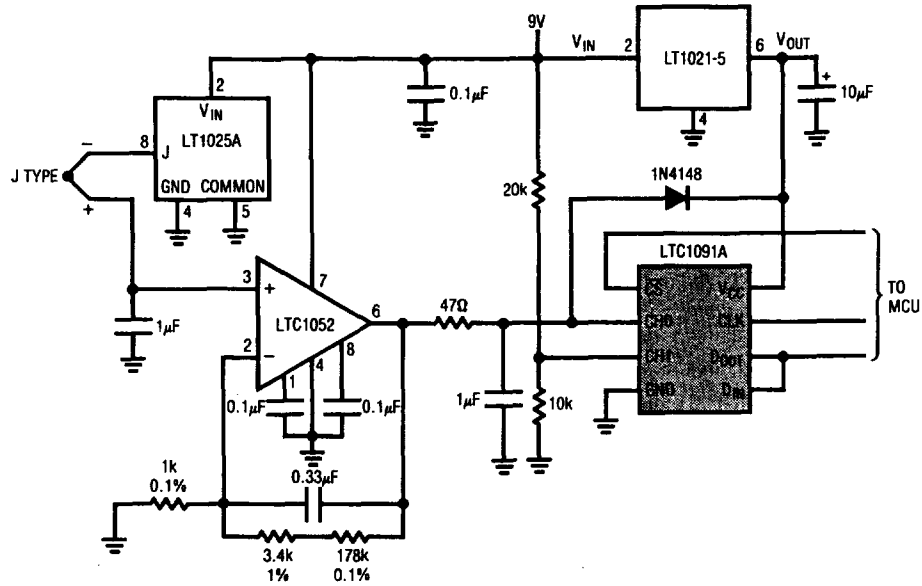
For operation with a 5V reference, the 200 $\mu$ V noise is only 0.04LSB peak-to-peak. In this case, the LTC1092/3/4 noise will contribute virtually no uncertainty to the output code. However, for reduced references, the noise may become a significant fraction of an LSB and cause undesirable jitter in the output code. For example, with a 1V reference, this same 200 $\mu$ V noise is 0.2LSB peak-to-peak. This will reduce the range of input voltages over which a stable output code can be achieved by 0.2LSB. If the reference is further reduced to 200mV, the 200 $\mu$ V noise becomes equal to one LSB and a stable code may be difficult to achieve. In this case averaging readings may be necessary.

This noise data was taken in a very clean setup. Any setup induced noise (noise or ripple on  $V_{CC}$ ,  $V_{REF}$ ,  $V_{IN}$  or  $V^-$ ) will add to the internal noise. The lower the reference voltage to be used, the more critical it becomes to have a clean, noise-free setup.

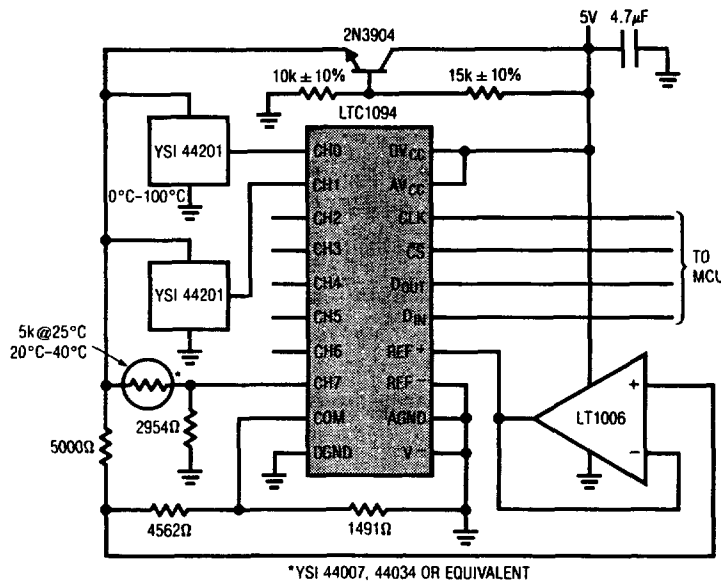
#### Conversion Speed with Reduced $V_{REF}$

With reduced reference voltages, the LSB step size is reduced and the LTC1092/3/4 internal comparator overdrive is reduced. Therefore, it may be necessary to reduce the maximum CLK frequency when low values of  $V_{REF}$  are used.

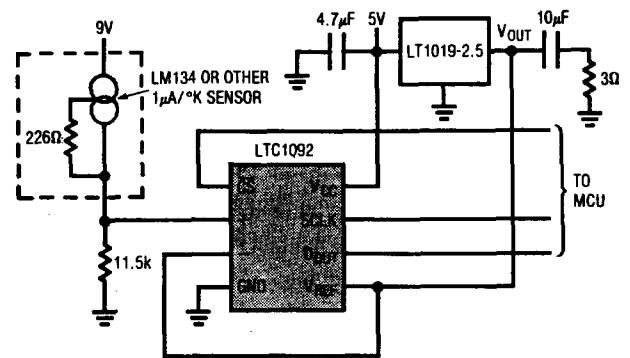
## TYPICAL APPLICATIONS



0°C-500°C Furnace Exhaust Gas Temperature Monitor with Low Supply Detection



0°C-100°C 0.25°C Accurate Thermistor Based Temperature Measurement System



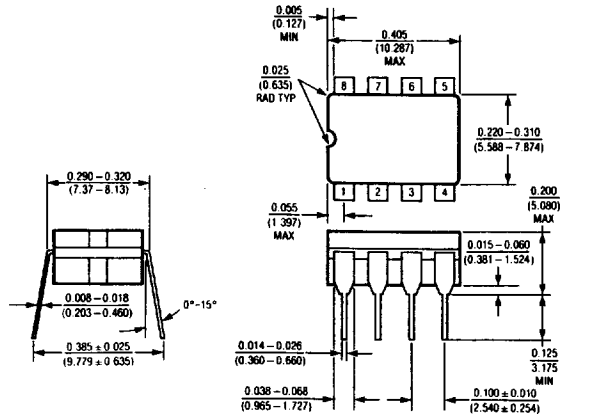
-55°C to +125°C Thermometer Using Current Output Silicon Sensors



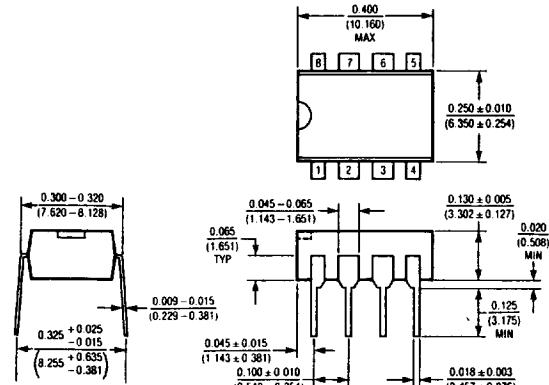
**PACKAGE DESCRIPTION** Dimensions in inches (millimeters) unless otherwise noted.

J Package	$T_{jmax}$ 150°C	$\theta_{JA}$ 100°C/W
N Package	$T_{jmax}$ 110°C	$\theta_{JA}$ 150°C/W

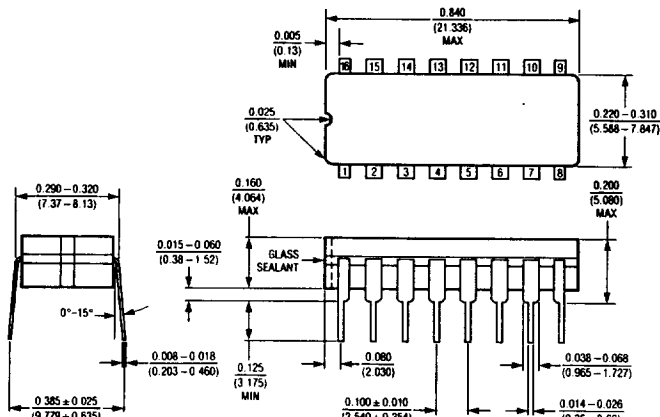
**J Package**  
8 Lead Ceramic DIP



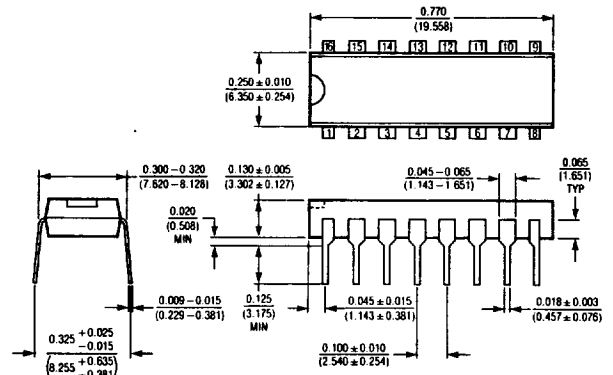
**N Package**  
8 Lead Plastic DIP



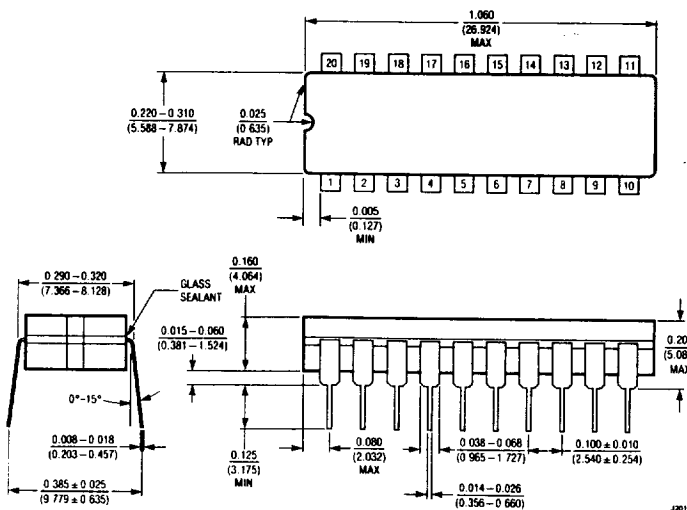
**J Package**  
16 Lead Ceramic DIP



**N Package**  
16 Lead Plastic DIP



**J Package**  
20 Lead Ceramic DIP



**N Package**  
20 Lead Plastic DIP

