## Document Title

**256Kx16 bit Low Power and Low Voltage CMOS Static RAM**

## Revision History

| Revision No | History | Draft Date | Remark |
|---|---|---|---|
| 0.0 | Initial draft | June 26, 1998 | Preliminary |
| 0.01 | Errata correction | August 17, 1998 | |

## *256Kx16 bit Low Power and Low Voltage CMOS Static RAM*

### FEATURES

- Process Technology: TFT
- Organization: 256K x16
- Power Supply Voltage
  KM616S4110C Family: 2.3~2.7V
- Low Data Retention Voltage: 2.0V(Min)
- Three state output and TTL Compatible
- Dual $\overline{CS}$ and standby control by $\overline{UB}$, $\overline{LB}$
- Package Type: 48-CSP

### GENERAL DESCRIPTION

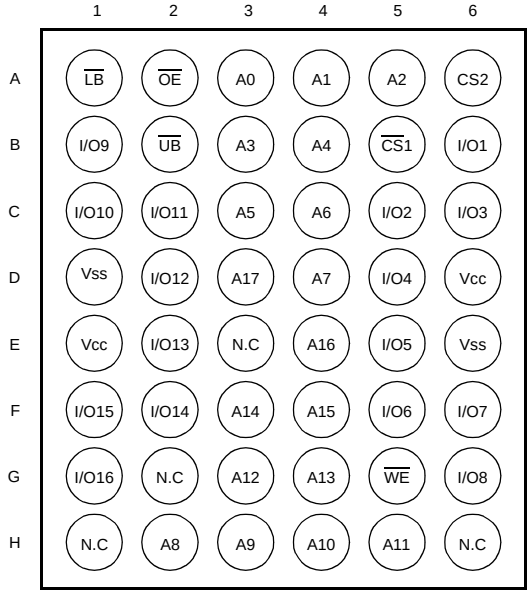
The KM616S4110C families are fabricated by SAMSUNG′s advanced CMOS process technology. The families support industrial operating temperature ranges and have chip scale package for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

### PRODUCT FAMILY

| Product Family | Operating Temperature | Vcc Range | Speed(ns) | Power Dissipation | | PKG Type |
|---|---|---|---|---|---|---|
| | | | | Standby ($I_{SB1}$, Max) | Operating ($I_{CC2}$, Max) | |
| KM616S4110CLI-L | Industrial(-40~85°C) | 2.3~2.7V | 100[1]/120 | 15µA | 25mA | 48-CSP |

1. The parameter is measured with 30pF test load.

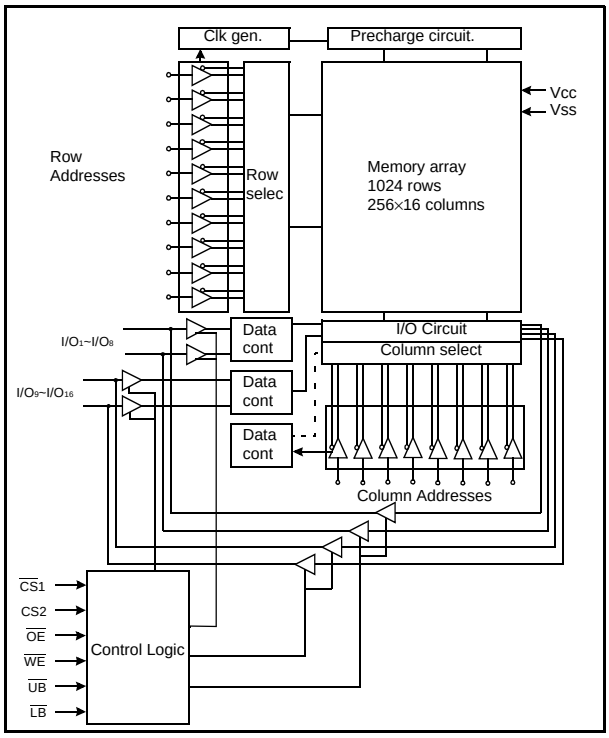
### PIN DESCRIPTION




**48-ball CSP - Top View (Ball Down)**

| Name | Function | Name | Function |
|---|---|---|---|
| $\overline{CS}_1$,$CS_2$ | Chip Select Inputs | Vcc | Power |
| $\overline{OE}$ | Output Enable Input | Vss | Ground |
| $\overline{WE}$ | Write Enable Input | $\overline{UB}$ | Upper Byte($I/O_{9\sim16}$) |
| $A_0$~$A_{17}$ | Address Inputs | $\overline{LB}$ | Lower Byte($I/O_{1\sim8}$) |
| $I/O_1$~$I/O_{16}$ | Data Inputs/Outputs | NC | No Connection |

### FUNCTIONAL BLOCK DIAGRAM



## PRODUCT LIST

| Industrial Temp Products(-40~85°C) | |
|---|---|
| **Part Name** | **Function** |
| KM616S4110CLZI-10L<br>KM616S4110CLZI-12L | 48-CSP, 100ns, 2.5V, LL<br>48-CSP, 120ns, 2.5V, LL |

## FUNCTIONAL DESCRIPTION

| $\overline{CS_1}$ | $CS_2$ | $\overline{OE}$ | $\overline{WE}$ | $\overline{LB}$ | $\overline{UB}$ | $I/O_{1\sim8}$ | $I/O_{9\sim16}$ | Mode | Power |
|---|---|---|---|---|---|---|---|---|---|
| H | X[1] | X[1] | X[1] | X[1] | X[1] | High-Z | High-Z | Deselected | Standby |
| X[1] | L | X[1] | X[1] | X[1] | X[1] | High-Z | High-Z | Deselected | Standby |
| X[1] | X[1] | X[1] | X[1] | H | H | High-Z | High-Z | Deselected | Standby |
| L | H | H | H | L | X[1] | High-Z | High-Z | Output Disabled | Active |
| L | H | H | H | X[1] | L | High-Z | High-Z | Output Disabled | Active |
| L | H | L | H | L | H | Dout | High-Z | Lower Byte Read | Active |
| L | H | L | H | H | L | High-Z | Dout | Upper Byte Read | Active |
| L | H | L | H | L | L | Dout | Dout | Word Read | Active |
| L | H | X[1] | L | L | H | Din | High-Z | Lower Byte Write | Active |
| L | H | X[1] | L | H | L | High-Z | Din | Upper Byte Write | Active |
| L | H | X[1] | L | L | L | Din | Din | Word Write | Active |

1. X means don't care. (Must be low or high state)

## ABSOLUTE MAXIMUM RATINGS[1]

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Voltage on any pin relative to Vss | $V_{IN}$,$V_{OUT}$ | -0.5 to $V_{CC}$+0.5 | V |
| Voltage on Vcc supply relative to Vss | $V_{CC}$ | -0.3 to 4.6 | V |
| Power Dissipation | $P_D$ | 1.0 | W |
| Storage temperature | $T_{STG}$ | -65 to 150 | °C |
| Operating Temperature | $T_A$ | -40 to 85 | °C |

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS[1)]

| Item | Symbol | Product | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | Vcc | KM616S4110C Family | 2.3 | 2.5 | 2.7 | V |
| Ground | Vss | All Family | 0 | 0 | 0 | V |
| Input high voltage | $V_{IH}$ | KM616S4110C Family | 2.0 | - | Vcc+0.3[2)] | V |
| Input low voltage | $V_{IL}$ | KM616S4110C Family | -0.3[3)] | - | 0.6 | V |

Note:
1. $T_A$=-40 to 85°C, otherwise specified
2. Overshoot: $V_{CC}$+1.0V in case of pulse width ≤ 10ns
3. Undershoot: -1.0V in case of pulse width ≤ 10ns
4. Overshoot and undershoot are sampled, not 100% tested.

## CAPACITANCE[1)] (f=1MHz, $T_A$=25°C)

| Item | Symbol | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | $V_{IN}$=0V | - | 8 | pF |
| Input/Output capacitance | $C_{IO}$ | $V_{IO}$=0V | - | 10 | pF |

1. Capacitance is sampled, not 100% tested

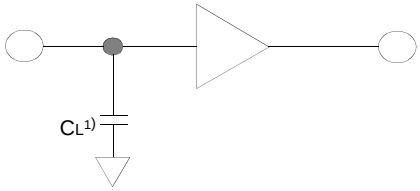
## DC AND OPERATING CHARACTERISTICS

| Item | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input leakage current | $I_{LI}$ | $V_{IN}$=Vss to Vcc | -1 | - | 1 | µA |
| Output leakage current | $I_{LO}$ | $\overline{CS_1}$=$V_{IH}$, $CS_2$=$V_{IL}$ or $\overline{OE}$=$V_{IH}$ or $\overline{WE}$=$V_{IL}$, $V_{IO}$=Vss to Vcc | -1 | - | 1 | µA |
| Operating power supply current | $I_{CC}$ | $I_{IO}$=0mA, $\overline{CS_1}$=$V_{IL}$, $CS_2$=$V_{IH}$, $V_{IN}$=$V_{IH}$ or $V_{IL}$ | - | - | 1 | mA |
| Average operating current | $I_{CC1}$ | Cycle time=1µs, 100%duty, $I_{IO}$=0mA, $\overline{CS_1}$≤0.2V, $CS_2$≥Vcc-0.2V, $V_{IN}$≤0.2V or $V_{IN}$≥VCC-0.2V | - | - | 4 | mA |
| | $I_{CC2}$ | Cycle time=Min, $I_{IO}$=0mA, 100% duty, $\overline{CS_1}$=$V_{IL}$, $CS_2$=$V_{IH}$, VIN=$V_{IL}$ or $V_{IH}$ | - | - | 25 | mA |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 0.5mA | | | 0.4 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = -0.5mA | 2.0 | | | V |
| Standby Current(TTL) | $I_{SB}$ | $\overline{CS_1}$=$V_{IH}$, $CS_2$=$V_{IL}$, Other inputs=$V_{IH}$ or $V_{IL}$ | - | - | 0.3 | mA |
| Standby Current(CMOS) | $I_{SB1}$ | $\overline{CS_1}$≥Vcc-0.2V, $CS_2$≥Vcc-0.2V($\overline{CS_1}$ controlled) or $CS_2$≤0.2V($CS_2$ controlled), Other inputs=0~Vcc | - | - | 15 | µA |

## AC OPERATING CONDITIONS

**TEST CONDITIONS**(Test Load and Input/Output Reference)

Input pulse level: 0.4 to 2.2V
Input rising and falling time: 5ns
Input and output reference voltage:1.1V
Output load(see right): $C_L$=100pF+1TTL
$C_L$=30pF+1TTL




1.Including scope and jig capacitance

## AC CHARACTERISTICS ($V_{CC}$=2.3~2.7V, $T_A$=-40 to 85°C)

| Parameter List | | Symbol | Speed Bins | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 100ns | | 120ns | | |
| | | | Min | Max | Min | Max | |
| Read | Read cycle time | $t_{RC}$ | 100 | - | 120 | - | ns |
| | Address access time | $t_{AA}$ | - | 100 | - | 120 | ns |
| | Chip select to output | $t_{CO}$ | - | 100 | - | 120 | ns |
| | Output enable to valid output | $t_{OE}$ | - | 50 | - | 50 | ns |
| | $\overline{LB}$, $\overline{UB}$ valid to data output | $t_{BA}$ | - | 100 | - | 120 | ns |
| | Chip select to low-Z output | $t_{LZ}$ | 10 | - | 10 | - | ns |
| | Output enable to low-Z output | $t_{OLZ}$ | 5 | - | 5 | - | ns |
| | $\overline{LB}$, $\overline{UB}$ enable to low-Z output | $t_{BLZ}$ | 10 | - | 10 | - | ns |
| | Output hold from address change | $t_{OH}$ | 15 | - | 15 | - | ns |
| | Chip disable to high-Z output | $t_{HZ}$ | 0 | 30 | 0 | 35 | ns |
| | $\overline{OE}$ disable to high-Z output | $t_{OHZ}$ | 0 | 30 | 0 | 35 | ns |
| | $\overline{UB}$, $\overline{LB}$ disable to high-Z output | $t_{BHZ}$ | 0 | 30 | 0 | 35 | ns |
| Write | Write cycle time | $t_{WC}$ | 100 | - | 120 | - | ns |
| | Chip select to end of write | $t_{CW}$ | 80 | - | 100 | - | ns |
| | Address set-up time | $t_{AS}$ | 0 | - | 0 | - | ns |
| | Address valid to end of write | $t_{AW}$ | 80 | - | 100 | - | ns |
| | Write pulse width | $t_{WP}$ | 70 | - | 80 | - | ns |
| | Write recovery time | $t_{WR}$ | 0 | - | 0 | - | ns |
| | Write to output high-Z | $t_{WHZ}$ | 0 | 30 | 0 | 35 | ns |
| | Data to write time overlap | $t_{DW}$ | 40 | - | 50 | - | ns |
| | Data hold from write time | $t_{DH}$ | 0 | - | 0 | - | ns |
| | End write to output low-Z | $t_{OW}$ | 5 | - | 5 | - | ns |
| | $\overline{LB}$, $\overline{UB}$ valid to end of write | $t_{BW}$ | 80 | - | 100 | - | ns |

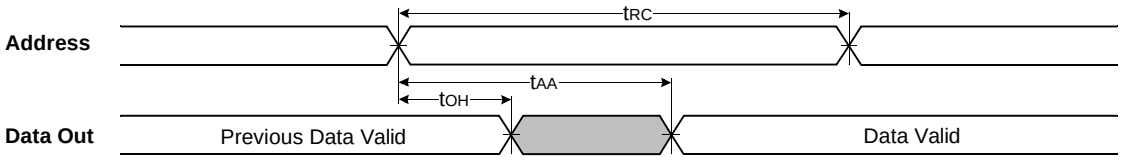
## DATA RETENTION CHARACTERISTICS

| Item | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Vcc for data retention | $V_{DR}$ | $\overline{CS_1}$≥Vcc-0.2V[1)] | 2.0 | - | 2.7 | V |
| Data retention current | $I_{DR}$ | Vcc=2.5V, $\overline{CS_1}$≥Vcc-0.2V[1)] | - | 0.5 | 15 | µA |
| Data retention set-up time | $t_{SDR}$ | See data retention waveform | 0 | - | - | ms |
| Recovery time | $t_{RDR}$ | | 5 | - | - | |

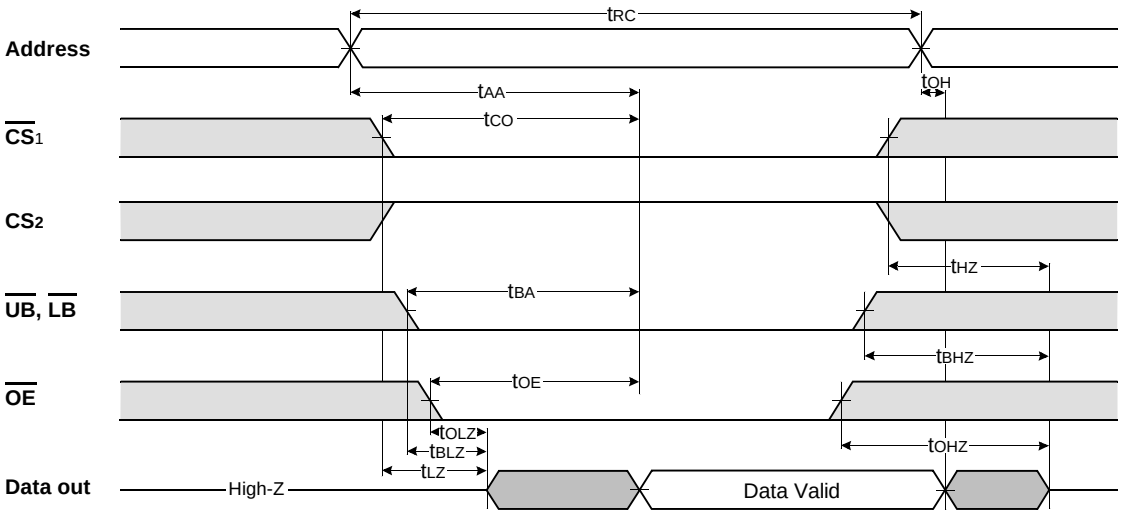
1. $\overline{CS_1}$≥Vcc-0.2V,$CS_2$≥Vcc-0.2V($\overline{CS_1}$ controlled) or $CS_2$≥Vcc-0.2V($CS_2$ controlled)

## TIMMING DIAGRAMS

### TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS_1}$=$\overline{OE}$=$V_{IL}$, $CS_2$=$\overline{WE}$=$V_{IH}$, $\overline{UB}$ or/and $\overline{LB}$=$V_{IL}$)



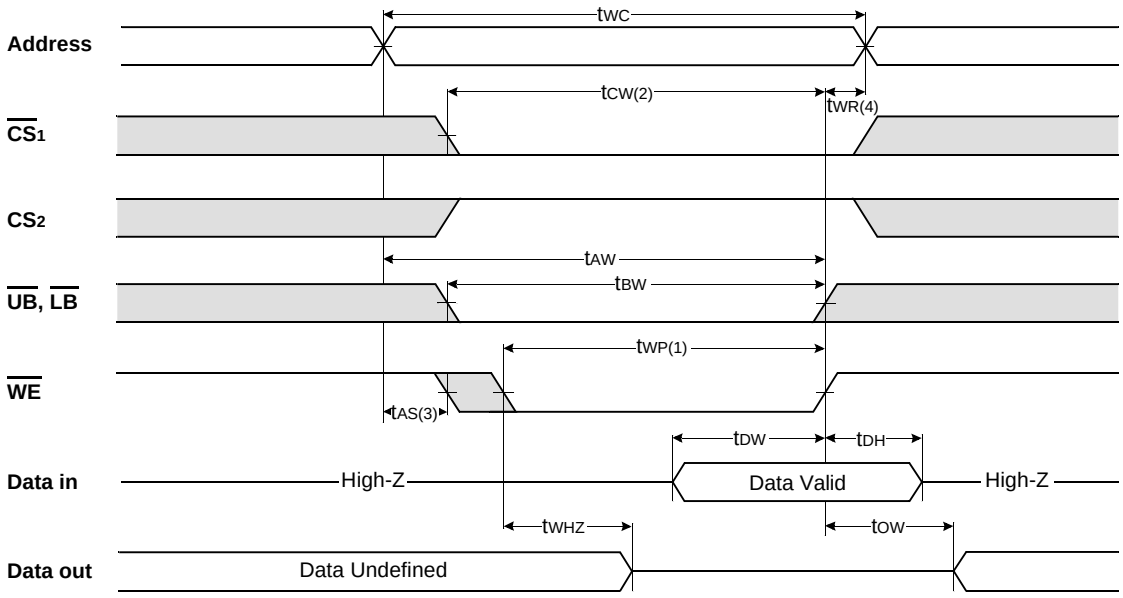

### TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=$V_{IH}$)



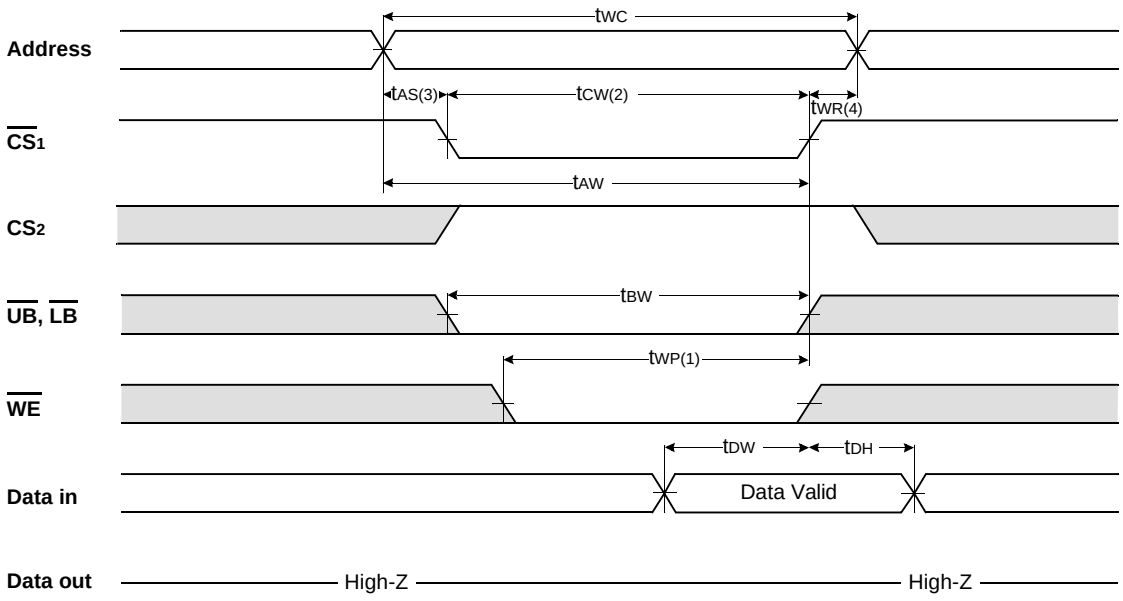

**NOTES (**READ CYCLE)

1. $t_{HZ}$ and $t_{OHZ}$ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}$(Max.) is less than $t_{LZ}$(Min.) both for a given device and from device to device interconnection.

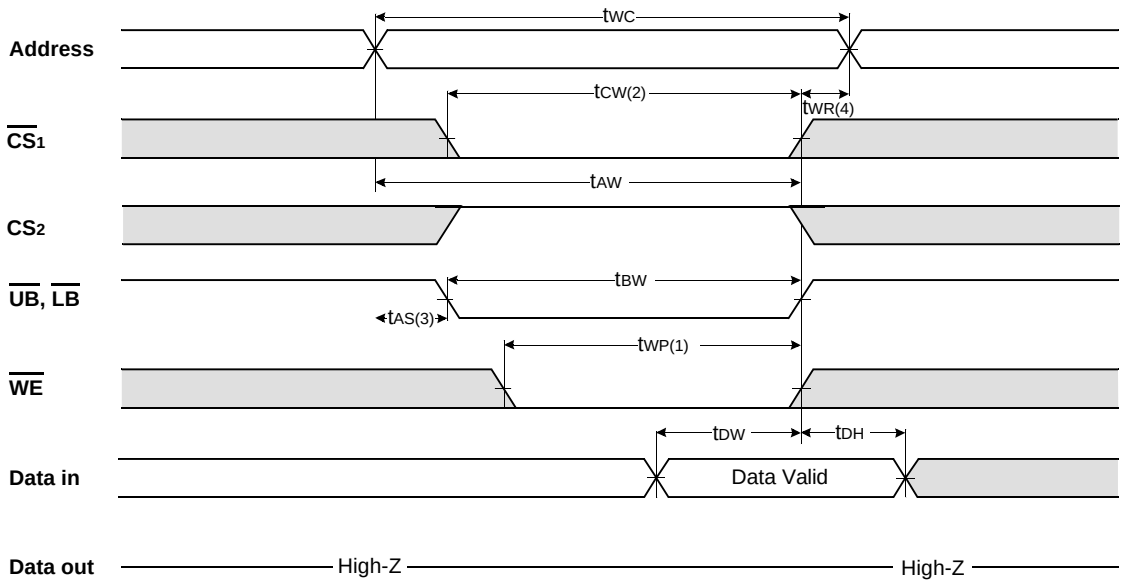
**TIMING WAVEFORM OF WRITE CYCLE(1)** ($\overline{WE}$ Controlled)




**TIMING WAVEFORM OF WRITE CYCLE(2)** ($\overline{CS_1}$ Controlled)



**TIMING WAVEFORM OF WRITE CYCLE(3)** ($\overline{UB}$, $\overline{LB}$ Controlled)

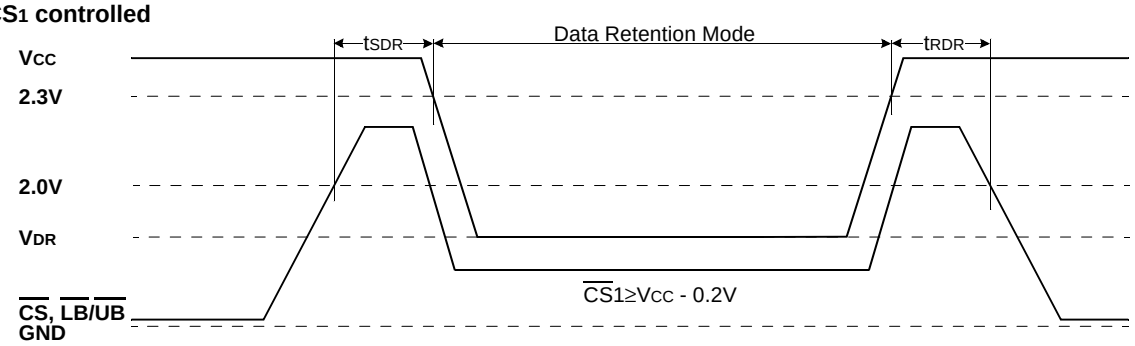



**NOTES** (WRITE CYCLE)

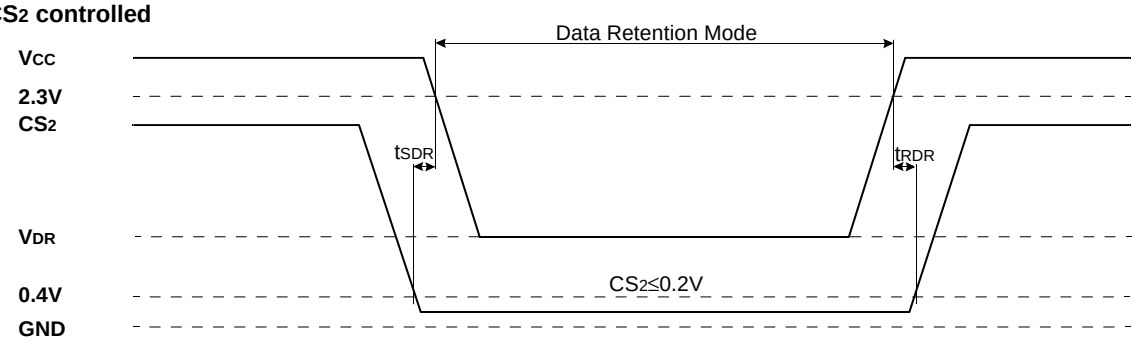
1. A write occurs during the overlap($t_{WP}$) of low $\overline{CS_1}$ and low $\overline{WE}$. A write begins when $\overline{CS_1}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS_1}$ goes high and $\overline{WE}$ goes high. The $t_{WP}$ is measured from the beginning of write to the end of write.
2. $t_{CW}$ is measured from the $\overline{CS_1}$ going low to end of write.
3. $t_{AS}$ is measured from the address valid to the beginning of write.
4. $t_{WR}$ is measured from the end or write to the address change. $t_{WR}$ applied in case a write ends as $\overline{CS_1}$ or $\overline{WE}$ going high.

## DATA RETENTION WAVE FORM

**$\overline{CS_1}$ controlled**

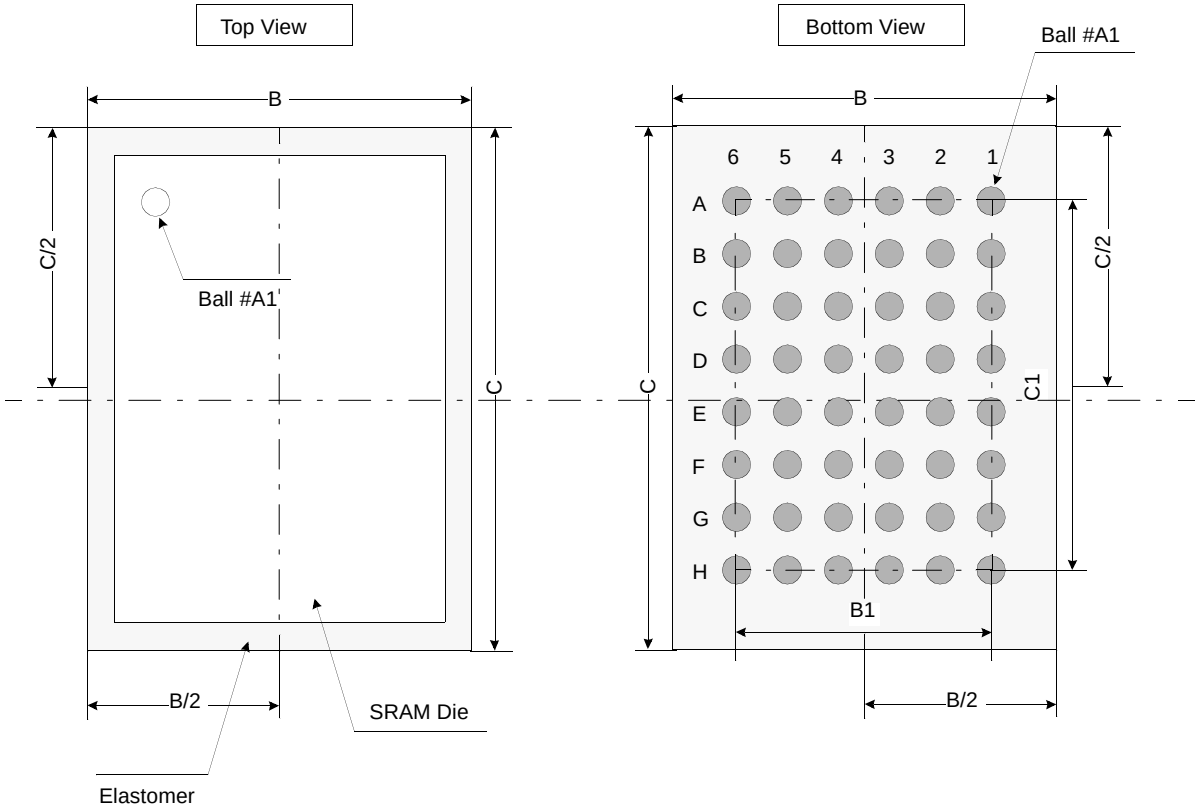


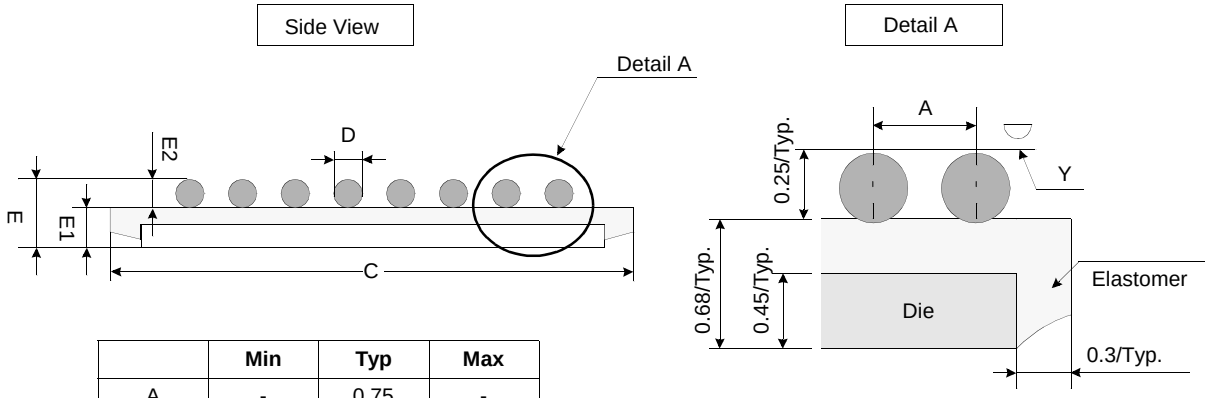

**$CS_2$ controlled**



## PACKAGE DIMENSIONS

Units : millimeter




| | Min | Typ | Max |
|---|---|---|---|
| A | - | 0.75 | - |
| B | 6.00 | 6.10 | 6.20 |
| B1 | - | 3.75 | - |
| C | 8.80 | 8.90 | 9.00 |
| C1 | - | 5.25 | - |
| D | 0.30 | 0.35 | 0.40 |
| E | - | 0.93 | 0.94 |
| E1 | - | 0.68 | - |
| E2 | - | 0.25 | - |
| Y | - | - | 0.08 |

Notes.

1. Bump counts : 48(8row x 6row)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerence are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. Y is coplanarity: 0.08(Max)