Features

- 72-Pin Small Outline Dual-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- High Performance CMOS process
- Single 3.3 ± 0.3V or 5.0 ± 0.25V Power Supply
- Low active current consumption
- All inputs & outputs are TTL(5V) or LVTTL(3.3V) compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only, CBR, Hidden and Self Refresh
- 4096 refresh cycles distributed across 256ms
- 12/8 Addressing (Row/Column)
- Optimized for use in byte-write non-parity applications.
- Au contacts

Description

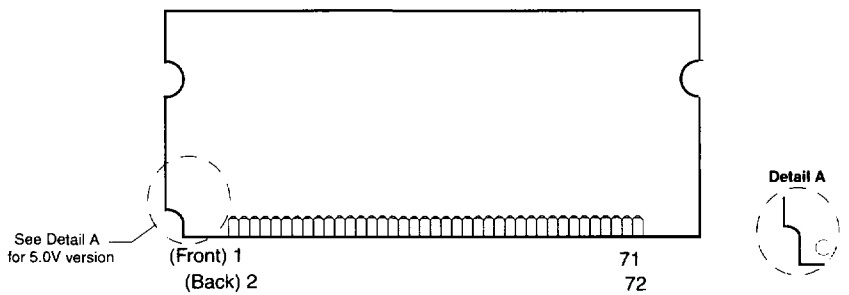
The IBM11S2320NP/M are 8MB industry standard 72-pin 4-byte small outline dual in-line memory modules (SO DIMMs). The modules are organized as 2Mx32 high speed memory arrays that are intended for use in 16, 32 and 64 bit applications. They are manufactured with four 1Mx16 TSOP devices, each in a 400mil package

The IBM11S1320NP/M are 4MB half populated versions, manufactured with two 1Mx16 TSOP devices.

These assemblies are intended for use in space constrained and or low power applications.

The IBM 72-Pin SO DIMMs provide a high performance, flexible 4-byte interface in a 2.35" long footprint.

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe (4MB)
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe (8MB)
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+3.3V or +5.0V)
V_{SS}	Ground
NC	No Connect
PD1 - PD7	Presence Detects

Pinout

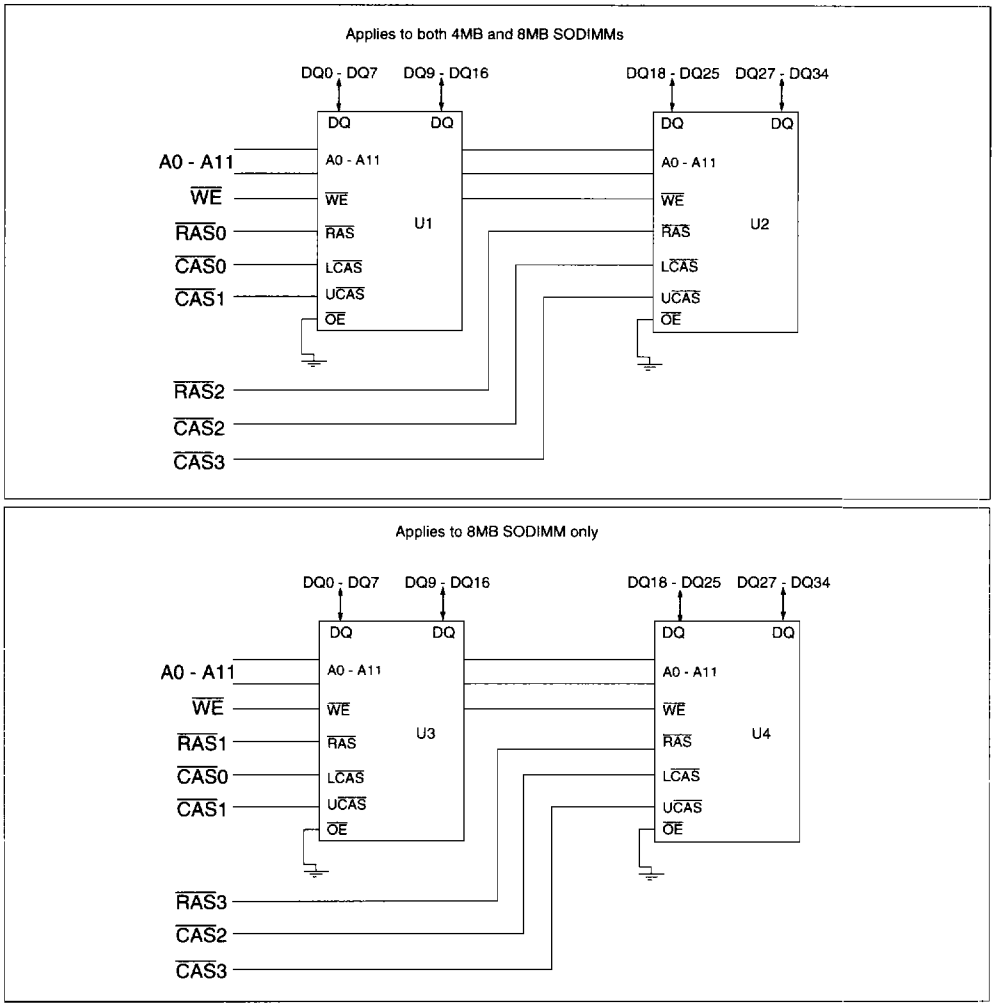
Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ13	37	DQ18	49	DQ20	61	V_{CC}
2	DQ0	14	A2	26	DQ14	38	DQ19	50	DQ21	62	DQ32
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ22	63	DQ33
4	DQ2	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ23	64	DQ34
5	DQ3	17	A5	29	A11	41	$\overline{CAS2}$	53	DQ24	65	NC
6	DQ4	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ25	66	PD2
7	DQ5	19	A10	31	A8	43	$\overline{CAS1}$	55	NC	67	PD3
8	DQ6	20	NC	32	A9	44	$\overline{RAS0}$	56	DQ27	68	PD4
9	DQ7	21	DQ9	33	$\overline{RAS3}$*	45	$\overline{RAS1}$*	57	DQ28	69	PD5
10	V_{CC}	22	DQ10	34	$\overline{RAS2}$	46	NC	58	DQ29	70	PD6
11	PD1	23	DQ11	35	DQ16	47	$\overline{WE}$	59	DQ31	71	PD7
12	A0	24	DQ12	36	NC	48	NC	60	DQ30	72	V_{SS}

4. * $\overline{RAS1}$ and $\overline{RAS3}$ are "NC" on 4MB SODIMM.

Ordering Information

Part Number	Organization	Speed	Dimensions	Power
IBM11S1320NP-60T	1M x 32	60ns	2.35" x 1" x .0965"	3.3V
IBM11S1320NP-70T	1M x 32	70ns	2.35" x 1" x .0965"	3.3V
IBM11S1320NM-60T	1M x 32	60ns	2.35" x 1" x .0965"	5.0V
IBM11S1320NM-70T	1M x 32	70ns	2.35" x 1" x .0965"	5.0V
IBM11S2320NP-60T	2M x 32	60ns	2.35" x 1" x .1496"	3.3V
IBM11S2320NP-70T	2M x 32	70ns	2.35" x 1" x .1496"	3.3V
IBM11S2320NM-60T	2M x 32	60ns	2.35" x 1" x .1496"	5.0V
IBM11S2320NM-70T	2M x 32	70ns	2.35" x 1" x .1496"	5.0V

Block Diagram



Truth Table

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby		H	X	X	X	X	High Impedance
Read		L	L	H	Row	Col	Valid Data Out
Early-Write		L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle		L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles		L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle		L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles		L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh		L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh		H→L	L	H	X	X	High Impedance
Hidden Refresh	Read	L→H→L	L	H	Row	Col	Data Out
	Write	L→H→L	L	H	Row	Col	Data In
Self Refresh		H→L	L	H	X	X	High Impedance

Presence Detect

	1M x 32		2M x 32	
Pin	-60	-70	-60	-70
PD1	NC	NC	NC	NC
PD2	V_{SS}	V_{SS}	V_{SS}	V_{SS}
PD3	NC	NC	NC	NC
PD4	NC	NC	V_{SS}	V_{SS}
PD5	NC	V_{SS}	NC	V_{SS}
PD6	NC	NC	NC	NC
PD7	V_{SS}	V_{SS}	V_{SS}	V_{SS}

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units	Notes
		3.3 Volt	5.0 Volt		
V_{CC}	Power Supply Voltage	-0.5 to + 4.6	-1.0 to + 7.0	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC} + 0.5, 4.6)	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} + 0.5, 4.6)	-0.5 to min (V_{CC} + 0.5, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +150C	-55 to +150C	°C	1
P_D	Power Dissipation	1.0 (4MB) 2.0 (8MB)	1.6 (4MB) 3.2 (8MB)	W	1, 2
I_{OUT}	Short Circuit Output Current	50	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	3.3 Volt			5.0 Volt			Units	Notes
		Min	Typ	Max	Min	Typ	Max		
V_{CC}	Supply Voltage	3.0	3.3	3.6	4.75	5.0	5.25	V	1
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.5	2.4	—	V_{CC} + 0.5	V	1, 2
V_{IL}	Input Low Voltage	-0.5	—	0.8	-0.5	—	0.8	V	1, 2

1. All voltages referenced to V_{SS}.
2. V_{IH} may overshoot to V_{CC} + 1.2V for pulse widths of ≤ 4.0ns with 3.3 Volt, or V_{CC} + 2.0V for pulse widths of ≤ 4.0ns (or V_{CC} + 1.0V for ≤ 8.0ns) with 5.0 Volt. Additionally, V_{IL} may undershoot to -2.0V for pulse widths ≤ 4.0ns (or -1.0V for ≤ 8.0ns) . Pulse widths measured at 50% points with amplitude measured peak to DC reference.

Capacitance (T_A = 0 to +70°C, V_{CC} = 3.3± 0.3V or 5.0 ± 0.25V)

Symbol	Parameter	1M x 32 Max	2M x 32 Max	Units
C_{I1}	Input Capacitance (A0-A9)	35	45	pF
C_{I2}	Input Capacitance (4MB: $\overline{RAS}$0, 8MB: $\overline{RAS}$0, 1)	16	16	pF
C_{I2}	Input Capacitance (4MB: $\overline{RAS}$2, 8MB: $\overline{RAS}$2, 3)	16	16	pF
C_{I4}	Input Capacitance ($\overline{CAS}$)	15	22	pF
C_{I5}	Input Capacitance ($\overline{WE}$)	36	50	pF
C_{IO}	Input - Output Capacitance (DQ0-DQ34)	16	23	pF

DC Electrical Characteristics (T_A = 0 to +70C, V_{CC} = 3.3 0.3V or 5.0 0.25V)

Symbol	Parameter		1Mx32 5.0 Volt Min	1Mx32 5.0 Volt Max	2Mx32 5.0 Volt Min	2Mx32 5.0 Volt Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	150	—	150	mA	1, 2, 3
		-70	—	130	—	130		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	4	—	8	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-60	—	150	—	150	mA	1, 3, 4
		-70	—	130	—	130		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$. Address Cycling: t_{PC} = t_{PC} min)	-60	—	130	—	130	mA	1. 2, 3
		-70	—	110	—	110		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	0.4	—	0.8	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$. $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	150	—	150	mA	1, 3, 4
		-70	—	130	—	130		
I_{CC7}	Self Refresh Current Average Power Supply Current during Self Refresh (CBR Cycle with $\overline{RAS}$ ≥ t_{RASS} (min))	3.3V	—	800	—	800	µA	4
		5.0V	—	1200	—	1200		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-10	+10	-10	+10	µA	
		$\overline{CAS}$	-10	+10	-20	+20		
		Address/ We	-20	+20	-40	+40		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.
4. Refresh current is specified for one bank

AC Characteristics

(T_A = 0 to +70C, V_{CC} = 3.3 0.3V or 5.0 0.25V)

1. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
2. AC measurements assume t_T=5ns.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. When both $\overline{CAS0}$ &$\overline{CAS1}$ or $\overline{CAS2}$ & $\overline{CAS3}$ go low at the same time, all 16 bits of data are read/written into the device. $\overline{CAS0}$ & $\overline{CAS1}$ or $\overline{CAS2}$ & $\overline{CAS3}$ (CAS'S TO THE SAME DRAM) cannot be staggered within the same read/write cycle.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10K	20	10K	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	10	—	10	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	1
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	3
t_{DH}	D_{IN} Hold Time	12	—	15	—	ns	3

1. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle. If the above condition is not satisfied, the condition of the data out (at access time) is indeterminate.
2. This timing parameter is not applicable to this product, but applies to a related product in this family.
3. These parameters are referenced to $\overline{CAS}$ 0,2 or $\overline{CAS}$ 1,3 leading edge in early write cycles.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2, 3
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 3
t_{AA}	Access Time from Address	—	30	—	35	ns	2, 3
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	4
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	ns	4
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	3
t_{OH}	Output Data Hold Time	3	—	3	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	15	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	—	15	—	15	ns	5

1. Operation within the t_{RCD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
3. Measured with the specified current load and 100pF.
4. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1

1. Measured with the specified current load and 100pF.

Refresh Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	5	—	5	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	5	—	5	—	ns	
t_{REF}	Refresh Period	—	256	—	256	ms	1

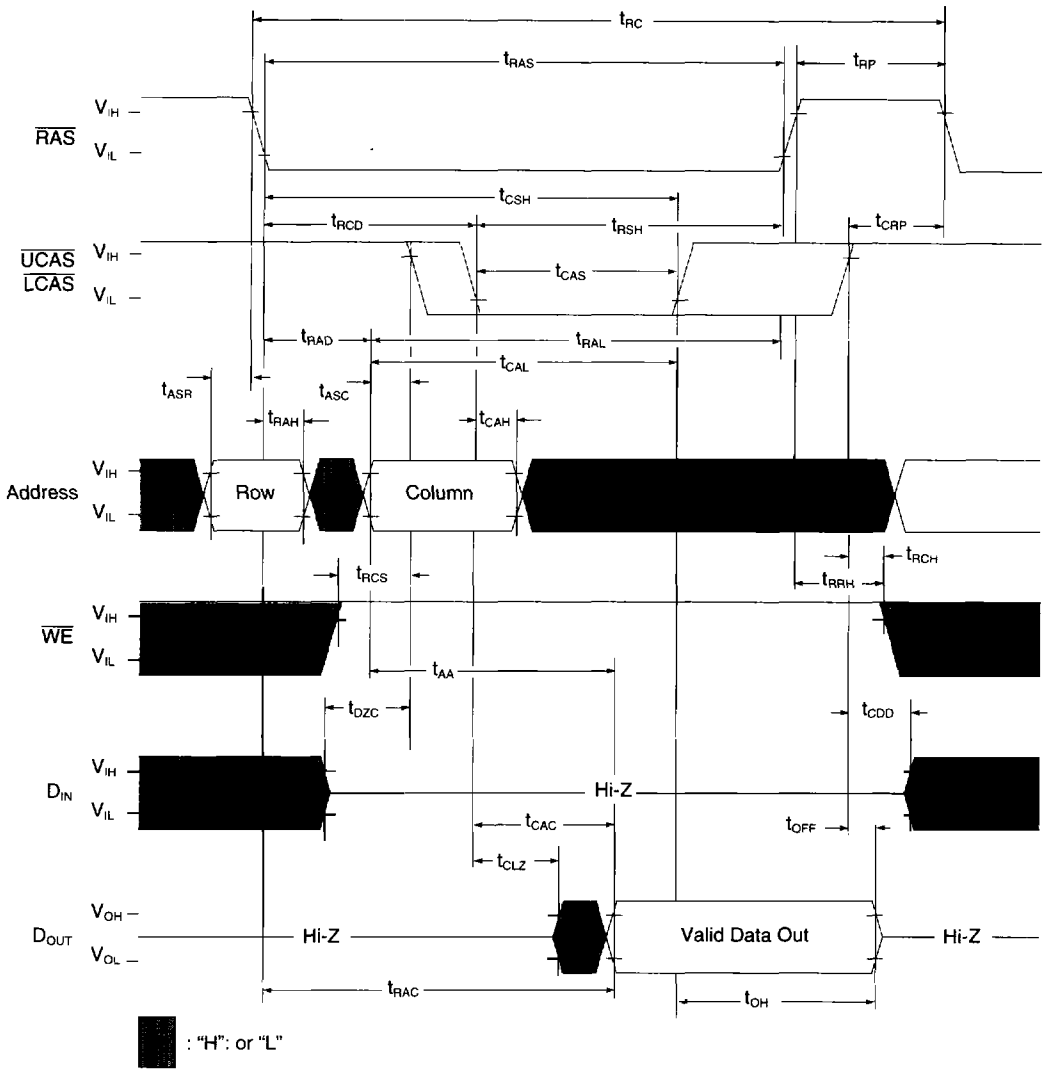
1. 4096 refreshes are required every 256ms.

Self Refresh Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RASS}	$\overline{RAS}$ Pulse Width During Self Refresh Cycle	100	—	100	—	µs	1
t_{RPS}	$\overline{RAS}$ Precharge Time During Self Refresh Cycle	104	—	124	—	ns	1
t_{CHS}	$\overline{CAS}$ Hold Time During Self Refresh Cycle	-50	—	-50	—	ns	1, 2
t_{CHD}	$\overline{CAS}$ Hold Time From RAS Falling During Self Refresh Cycle	350	—	350	—	µs	1, 2

1. When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation: If row addresses are being refreshed in a EVENLY DISTRIBUTED manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh. If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.
2. If $t_{RASS} > t_{CHD}$ (min) then t_{CHD} applies. If $t_{RASS} \leq t_{CHD}$ (min) then t_{CHS} applies.

Read


tRC
tRAS
tRP
VIH
RAS
VIL
tCSH
tRCD
tRSH
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UCAS
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tRAD
tRAL
tCAL
tASR
tASC
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tCAH
VIH
Address
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Row
Column
tRCS
tRCH
tRRH
VIH
WE
VIL
tAA
tDZC
tCDD
VIH
DIN
VIL
Hi-Z
tCAC
tOFF
tCLZ
VOH
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VOL
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Valid Data Out
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tRAC
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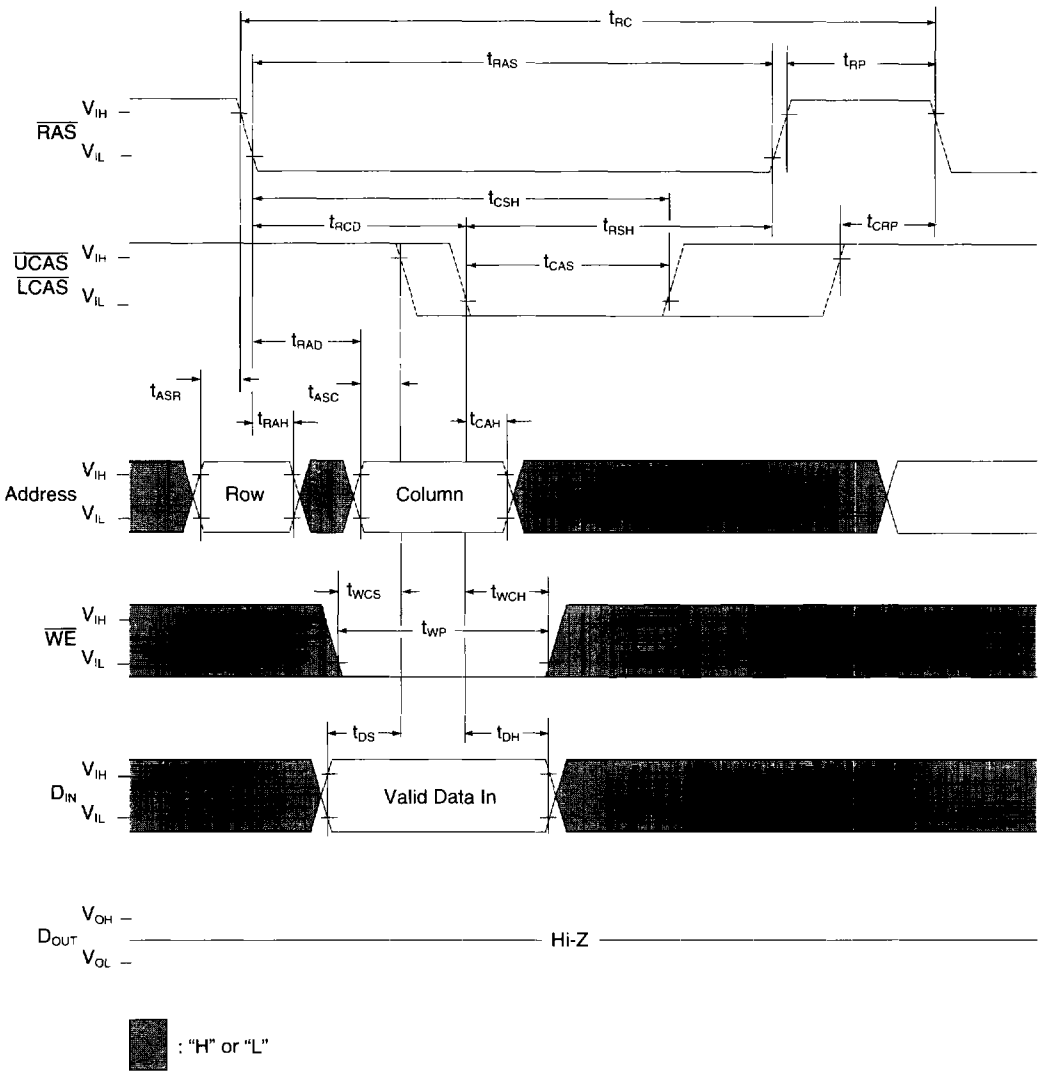
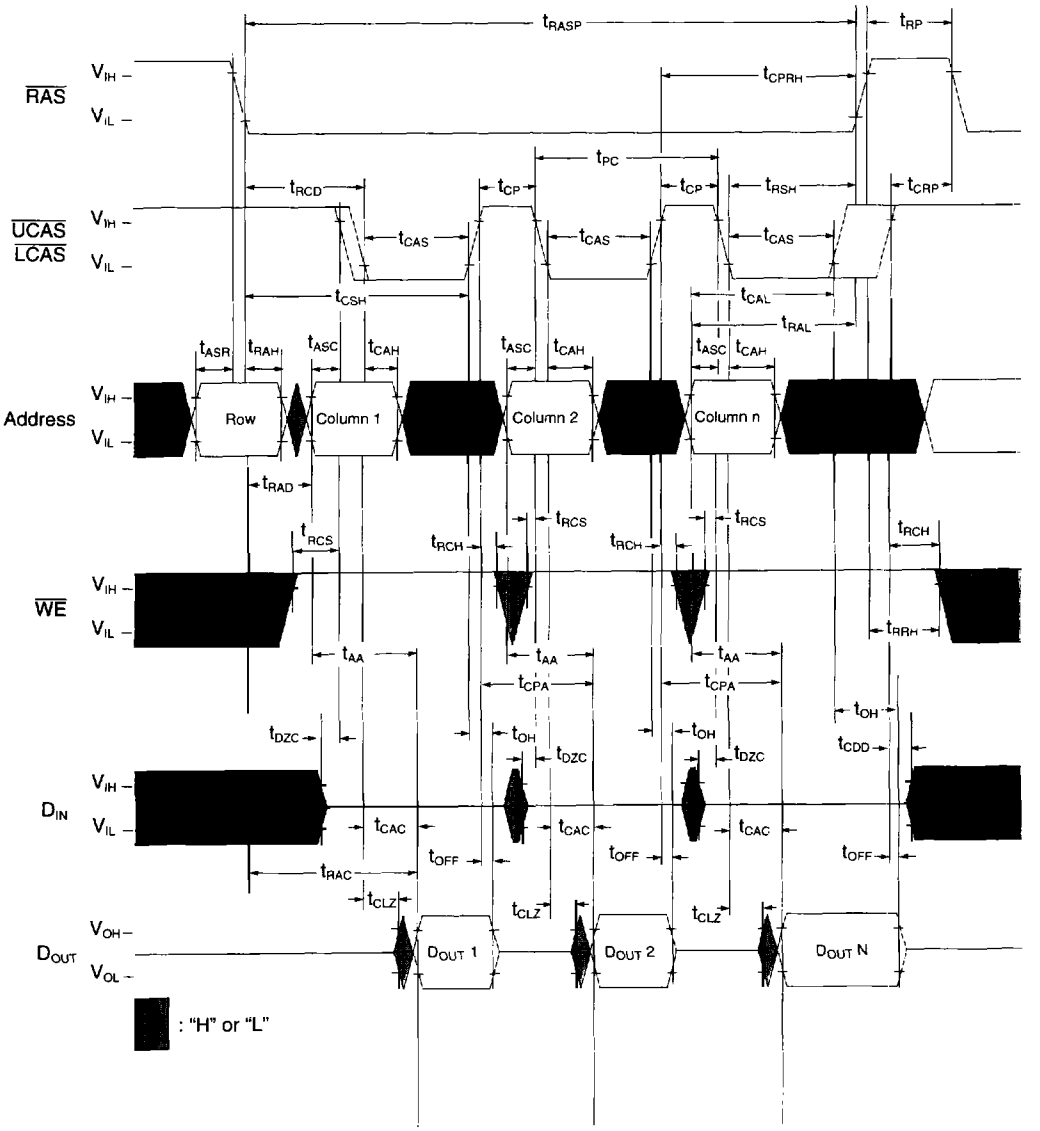
: "H": or "L"

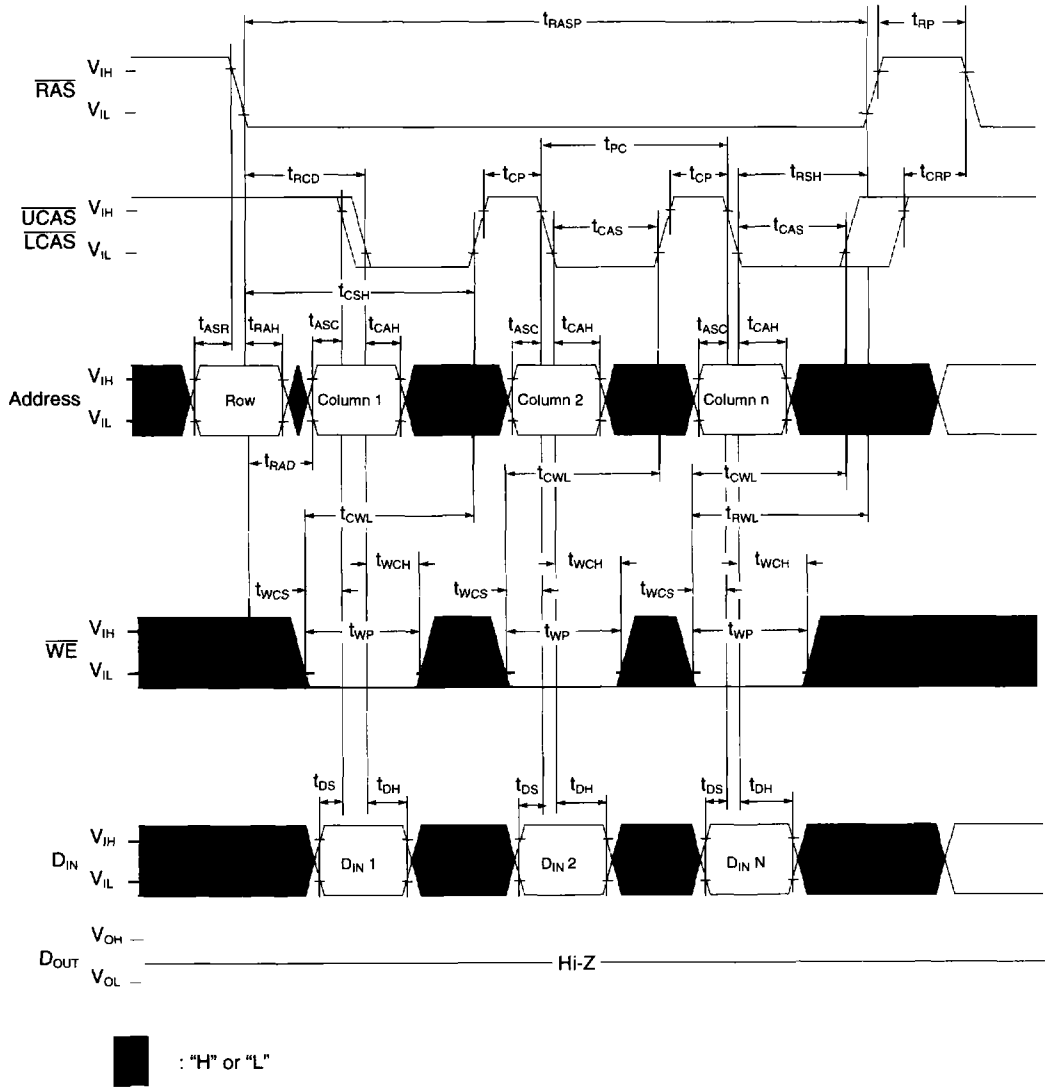
Write Cycle (Early Write)



Fast Page Mode Read Cycle

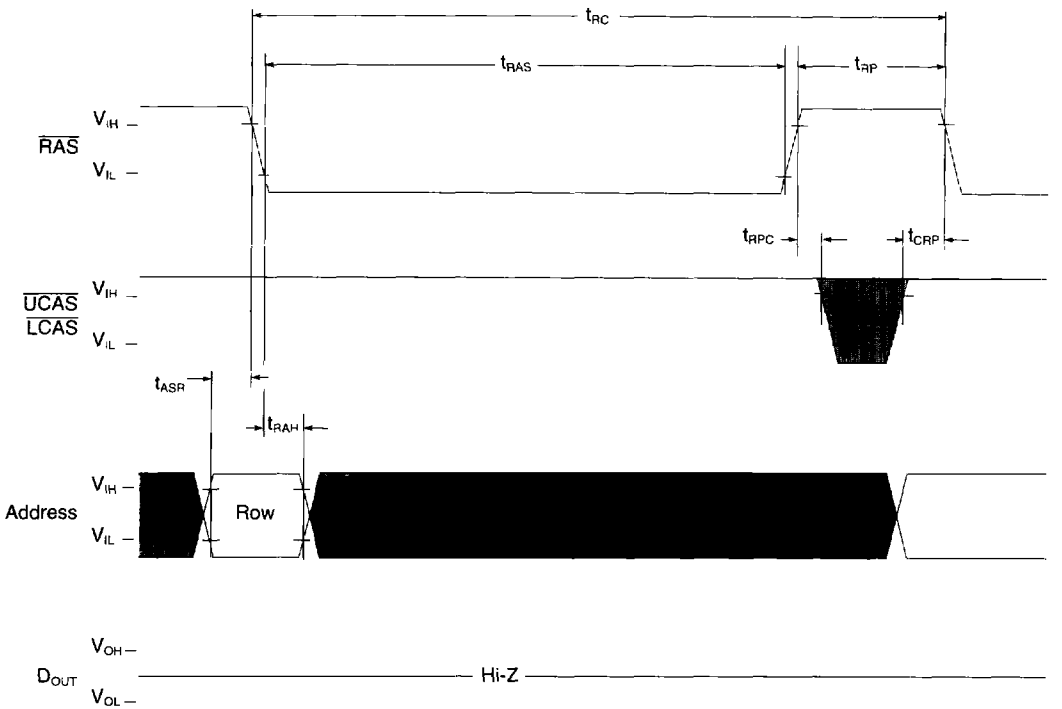


Fast Page Mode Write Cycle



: "H" or "L"

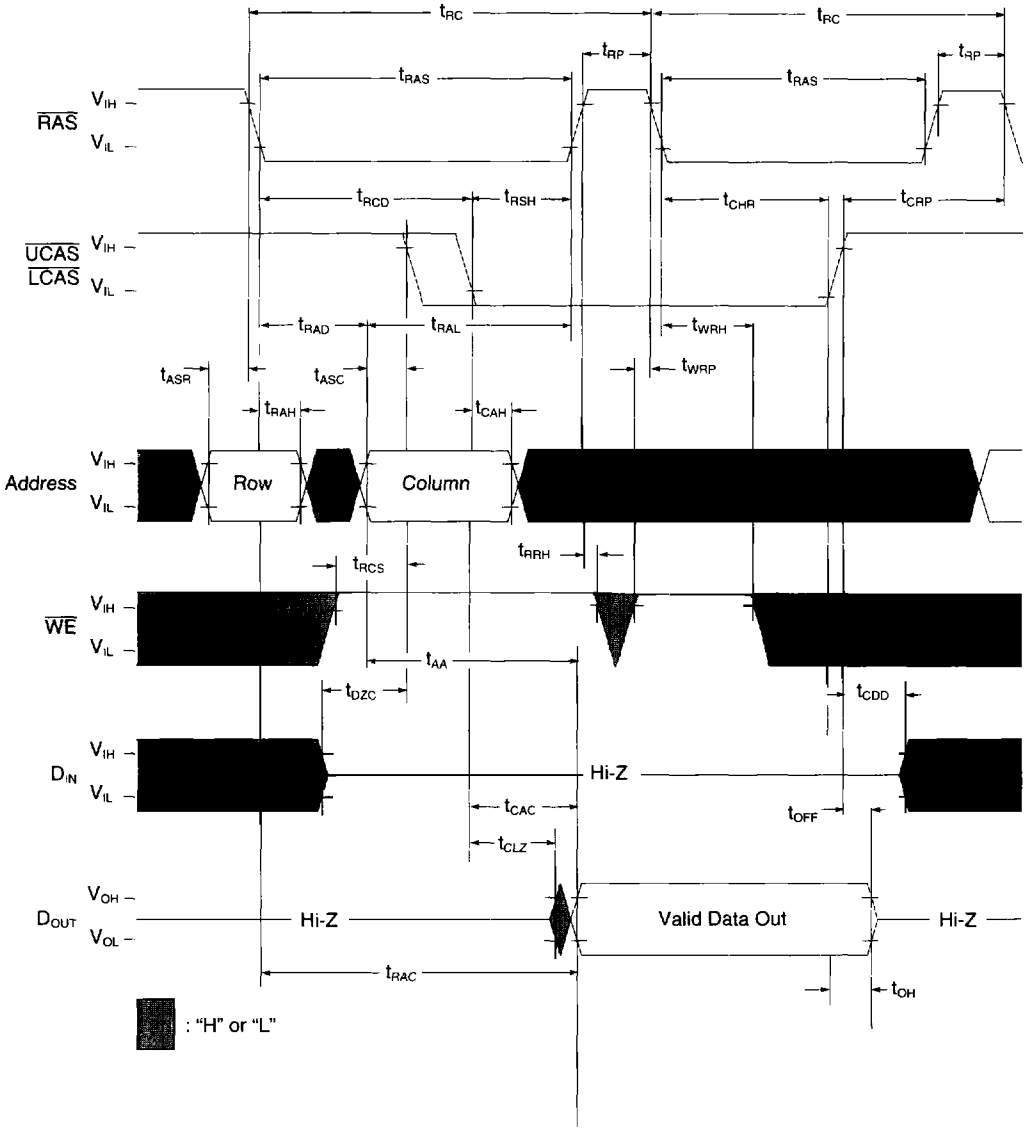
$\overline{RAS}$ Only Refresh Cycle



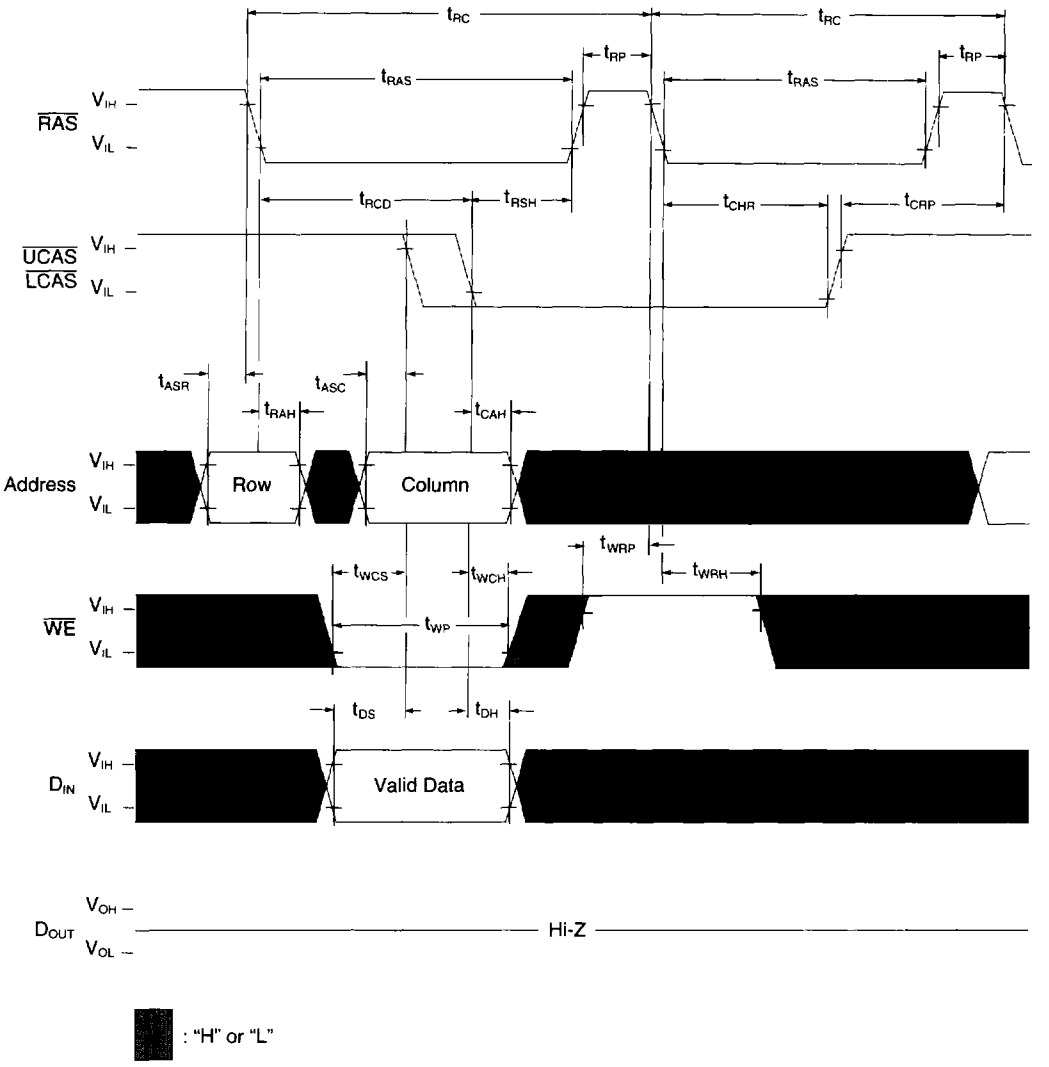
: "H" or "L"

NOTE: $\overline{WE}$ and D_{IN} are "H" or "L"

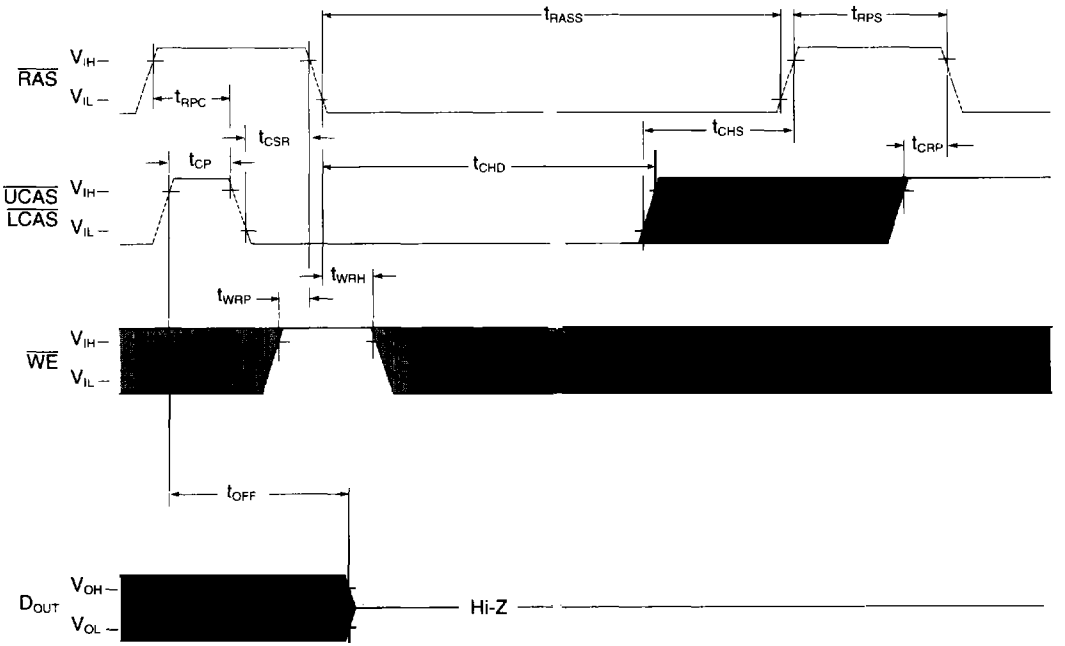
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)



Self Refresh Cycle (Sleep Mode)

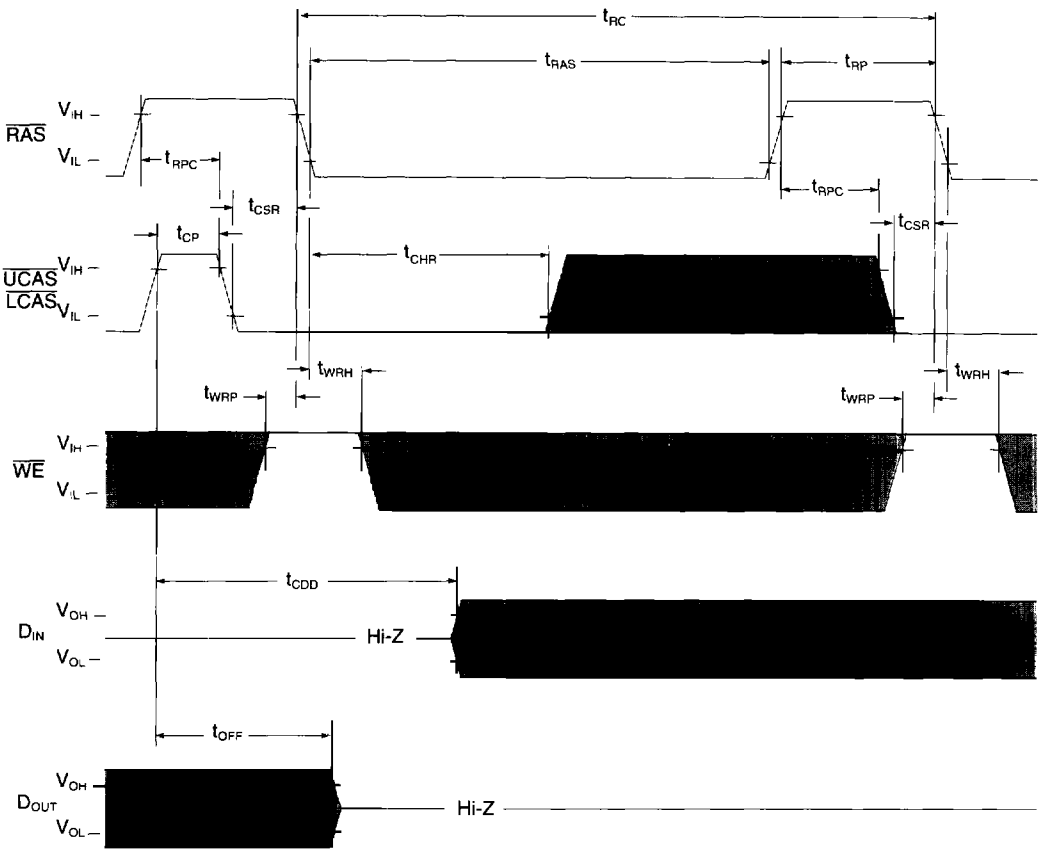


: "H" or "L"

NOTES:

1. Address is "H" or "L"
2. Once $\overline{RAS}$ (min) is provided and $\overline{RAS}$ remains low, the DRAM will be in Self Refresh, commonly known as "Sleep Mode."
3. If $t_{RASS} > t_{CHD}$ (min) then t_{CHD} applies.
   If $t_{RASS} \leq t_{CHD}$ (min) then t_{CHS} applies.

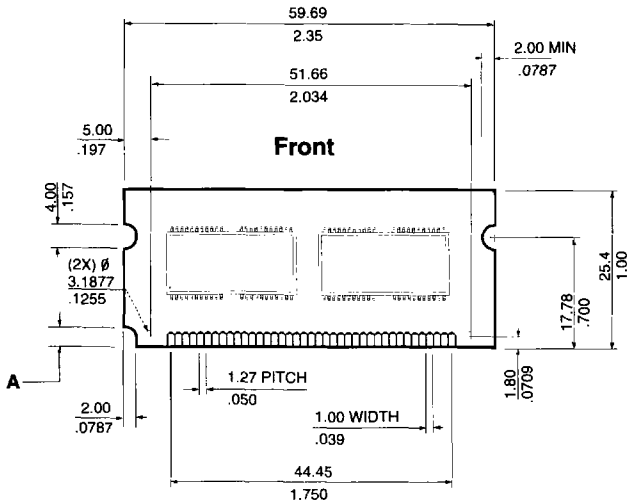
$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



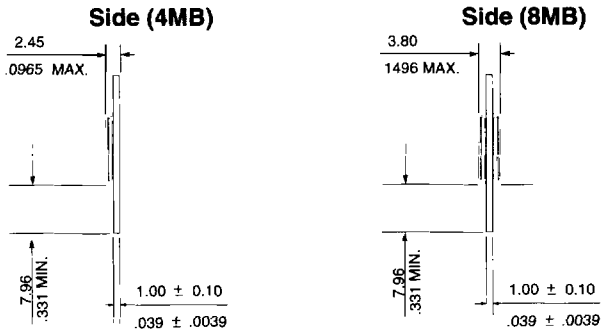
: "H" or "L"

NOTE: Address is "H" or "L"

Layout Drawing



A =	3.3V	5.0V
	3.175	6.35
	.125	.246



Note: All dimensions are typical unless otherwise stated. Millimeters / Inches