256 K x 4-Bit Dynamic RAM — HYB 514256B/BJ/BZ-60/-70/-80
Low Power 256 K × 4-Bit Dynamic RAM — HYB 514256BL/BJL/BZL-60/-70

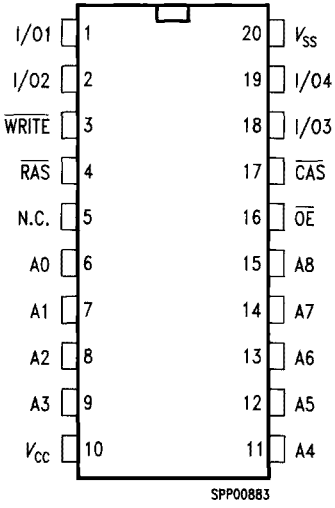
Advanced Information

- 262 144 words by 4-bit organization
- Fast access and cycle time
  60 ns access time
  110 ns cycle time (HYB 514256B/BL-60)
  70 ns access time
  130 ns cycle time (HYB 514256B/BL-70)
  80 ns access time
  150 ns cycle time (HYB 514256B-80)
- Fast page mode cycle time
  40 ns (HYB 514256B/BL-60)
  40 ns (HYB 514256B/BL-70)
  45 ns (HYB 514256B-80)
- Low power dissipation
  max. 495 mW active (HYB 514256B/BL-60)
  max. 440 mW active (HYB 514256B/BL-70)
  max. 385 mW active (HYB 514256B-80)
  max. 5.5 mW standby
  max. 1.1 mW standby for L-version
- Single + 5 V (± 10 %) supply with a built-in V_{BB} generator
- Output unlatched at cycle end allows two-dimensional chip selection
- Read-modify-write, $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, hidden-refresh and fast page mode capability
- All inputs, outputs and clocks TTL-compatible
- 512 refresh cycles/8 ms
  512 refresh cycles/64 ms
  for L-version only
- Plastic Packages: P-DIP-20-2,
  P-SOJ-26/20-1,
  P-ZIP-20/19-1

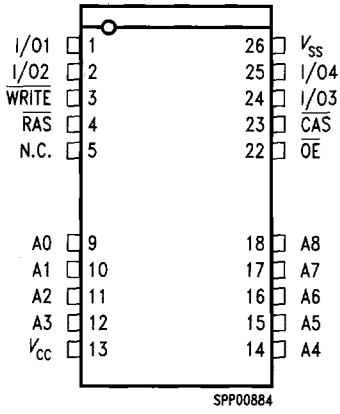
The HYB 514256B/BL is the new generation dynamic RAM organized as 262 144 words by 4-bit. The HYB 514256B/BL utilizes CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 514256B/BL to be packaged in a standard plastic P-DIP-20-2, plastic P-SOJ-26/20-1 or plastic P-ZIP-20/19. This package size provides high system bit densities and is compatible with commonly used automatic testing and insertion equipment. System oriented features include single + 5 V (± 10 %) power supply, direct interfacing with high-performance logic device families such as Schottky TTL. These HYB 514256BL are specially selected for battery backup applications.

Ordering Information

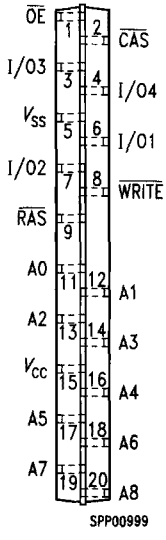
Type	Ordering Code	Package	Description
HYB 514256B-60	Q67100-Q530	P-DIP-20-2	DRAM (access time 60 ns)
HYB 514256B-70	Q67100-Q433	P-DIP-20-2	DRAM (access time 70 ns)
HYB 514256B-80	Q67100-Q434	P-DIP-20-2	DRAM (access time 80 ns)
HYB 514256BJ-60	Q67100-Q536	P-SOJ-26/20-1	DRAM (access time 60 ns)
HYB 514256BJ-70	Q67100-Q537	P-SOJ-26/20-1	DRAM (access time 70 ns)
HYB 514256BJ-80	Q67100-Q437	P-SOJ-26/20-1	DRAM (access time 80 ns)
HYB 514256BZ-60	Q67100-Q539	P-ZIP-20/19-1	DRAM (access time 60 ns)
HYB 514256BZ-70	Q67100-Q540	P-ZIP-20/19-1	DRAM (access time 70 ns)
HYB 514256BZ-80	Q67100-Q541	P-ZIP-20/19-1	DRAM (access time 80 ns)
HYB 514256BL-60	Q67100-Q542	P-DIP-20-2	DRAM (access time 60 ns)
HYB 514256BL-70	Q67100-Q543	P-DIP-20-2	DRAM (access time 70 ns)
HYB 514256BJL-60	Q67100-Q608	P-SOJ-26/20-1	DRAM (access time 60 ns)
HYB 514256BJL-70	Q67100-Q607	P-SOJ-26/20-1	DRAM (access time 70 ns)
HYB 514256BZL-60	Q67100-Q546	P-ZIP-20/19-1	DRAM (access time 60 ns)
HYB 514256BZL-70	Q67100-Q547	P-ZIP-20/19-1	DRAM (access time 70 ns)



P-DIP-20-2



P-SOJ-26/20-1

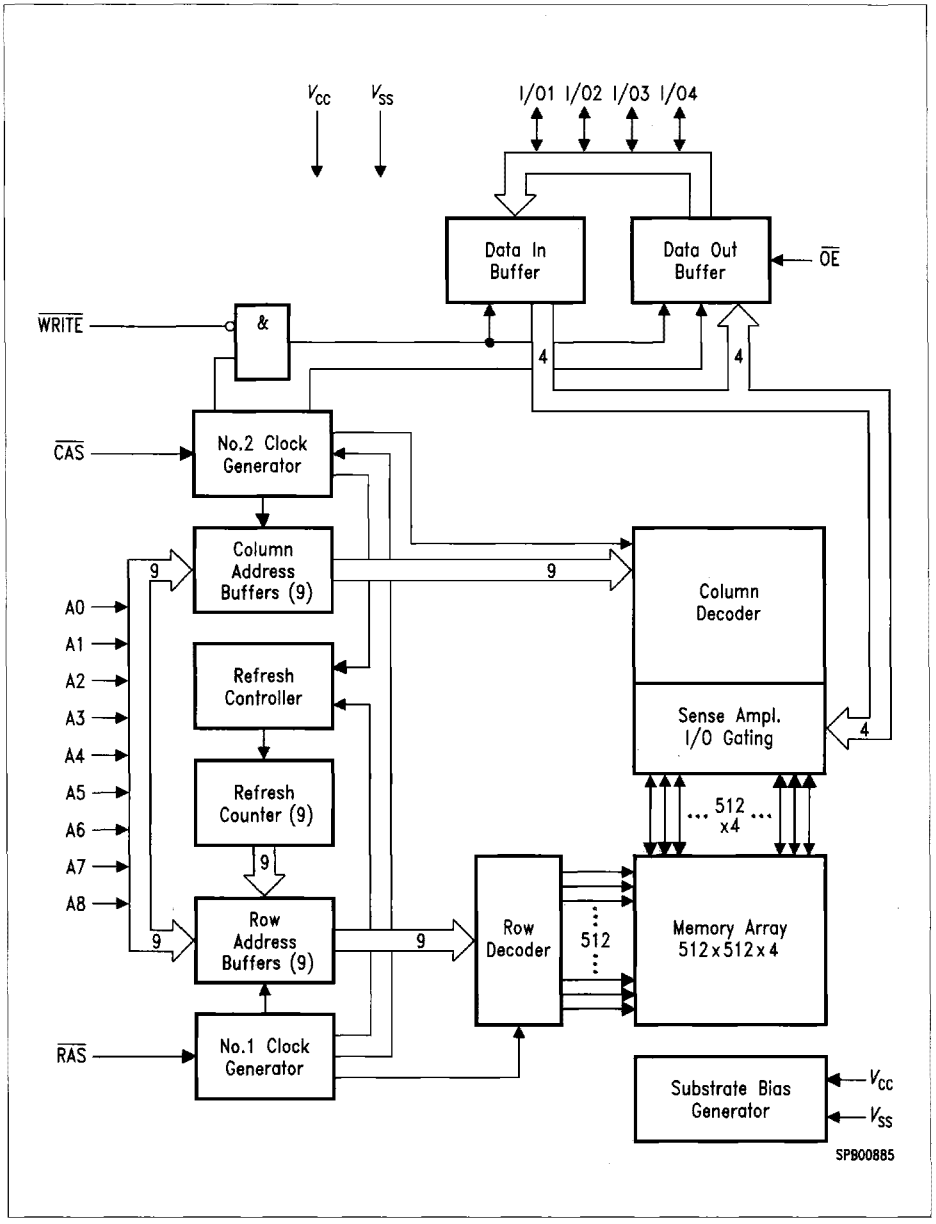


P-ZIP-20/19-1

Pin Names

A0-A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{OE}$	Output Enable
I/O1-I/O4	Data Input/Output
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground (0 V)
N.C.	No Connection

Pin Configuration



Block Diagram

Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 °C
Storage temperature range ..... – 55 to + 150 °C
Soldering temperature ..... 260 °C
Soldering time ..... 10 s
Input/output voltage ..... – 1 to + 7 V
Power supply voltage ..... – 1 to + 7 V
Power dissipation ..... 0.6 W
Data out current (short circuit) ..... 50 mA

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{CC} = 5 V ± 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	6.5	V	1)
Input low voltage	V_{IL}	– 1.0	0.8	V	1)
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	1)
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	1)
Input leakage current, any input (0 V ≤ V_{IN} ≤ 6.5 V, all other pins = 0 V)	$I_{I(L)}$	– 10	10	µA	1)
Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ V_{CC})	$I_{O(L)}$	– 10	10	µA	1)
Average V_{CC} supply current:	I_{CC1}				
HYB 514256B/BL-60		–	90	mA	2) 3)
HYB 514256B/BL-70		–	80	mA	2) 3)
HYB 514256B-80		–	70	mA	2) 3)
($\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC} = t_{RC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	2	mA	–
Average V_{CC} supply current, $\overline{RAS}$ only mode:	I_{CC3}				
HYB 514256B/BL-60		–	90	mA	2)
HYB 514256B/BL-70		–	80	mA	2)
HYB 514256B-80		–	70	mA	2)
($\overline{RAS}$ cycling: $\overline{CAS}$ = V_{IH} : t_{RC} = t_{RC} min.)					

Notes see page 62.

DC Characteristics (cont'd)

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{CC} = 5 V ± 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current, fast page mode:	I_{CC4}				
HYB 514256B/BL-60		–	70	mA	2) 3
HYB 514256B/BL-70		–	60	mA	2) 3)
HYB 514256B-80		–	50	mA	2) 3)
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: t_{PC} = t_{PC} min.)					
Standby V_{CC} supply current	I_{CC5}	–	1	mA	1)
L-Version		–	200	µA	1)
($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)					
Average V_{CC} supply current, $\overline{CAS}$-before-RAS refresh mode:	I_{CC6}				
		–	90	mA	2)
HYB 514256B/BL-60		–	80	mA	2)
HYB 514256B/BL-70		–	70	mA	2)
HYB 514256B-80					
($\overline{RAS}$, $\overline{CAS}$ cycling: t_{RC} = t_{RC} min.)					
For L-version only:					
Battery backup current:	I_{CC7}	–	300	µA	2) 13)
average power supply current,					
battery backup mode:					
($\overline{CAS}$ = $\overline{CAS}$ before $\overline{RAS}$ cycling or 0.2 V,					
$\overline{OE}$ = V_{CC} – 0.2 V					
$\overline{WRITE}$ = V_{CC} – 0.2 V or 0.2 V,					
A0 to A8 = V_{CC} – 0.2 V or 0.2 V,					
I/O1 to I/O4 = V_{CC} – 0.2 V or 0.2 V or open,					
t_{RC} = 125 µs, t_{RAS} = t_{RAS} min. ~ 1 µs)					

Notes see page 62.

AC Characteristics [4) 5)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		-60		-70		-80		
		min.	max.	min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	110	–	130	–	150	–	ns
Read-modify-write cycle time	t_{RMW}	165	–	185	–	205	–	ns
Fast page mode cycle time	t_{PC}	40	–	40	–	45	–	ns
Fast page mode read-modify-write cycle time	t_{PRMW}	95	–	95	–	100	–	ns
Access time from $\overline{RAS}$ [6) 11)]	t_{RAC}	–	60	–	70	–	80	ns
Access time from $\overline{CAS}$ [6) 11)]	t_{CAC}	–	20	–	20	–	20	ns
Access time from column address [6) 12)]	t_{AA}	–	30	–	35	–	40	ns
Access time from $\overline{CAS}$ precharge [6) 12)]	t_{CPA}	–	30	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z [4)]	t_{CLZ}	0	–	0	–	0	–	ns
Output buffer turn-off delay [7)]	t_{OFF}	0	20	0	20	0	20	ns
Transition time (rise and fall) [5)]	t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	40	–	50	–	60	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	60	10.000	70	10.000	80	10.000	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	60	100.000	70	100.000	80	100.000	ns
$\overline{RAS}$ hold time	t_{RSH}	20	–	20	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	60	–	70	–	80	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	20	10.000	20	10.000	20	10.000	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time [11)]	t_{RCD}	20	40	20	50	20	60	
$\overline{RAS}$ to column address delay time [12)]	t_{RAD}	15	30	15	35	15	40	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time	t_{CPN}	10	–	10	–	10	–	ns

Notes see page 62.

AC Characteristics (cont'd) [4] [5]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		-60		-70		-80		
		min.	max.	min.	max.	min.	max.	
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10	–	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns
Column address hold time	t_{CAH}	15	–	15	–	15	–	ns
Column address hold time referenced to $\overline{RAS}$	t_{AR}	50	–	55	–	60	–	ns
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	–	35	–	40	–	ns
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns
Read command hold time [8]	t_{RCH}	0	–	0	–	0	–	ns
Read command hold time referenced to $\overline{RAS}$ [8]	t_{RRH}	0	–	0	–	0	–	ns
Write command hold time	t_{WCH}	15	–	15	–	15	–	ns
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	50	–	55	–	60	–	ns
Write command pulse width	t_{WP}	15	–	15	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	–	20	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	–	20	–	20	–	ns
Data setup time [9]	t_{DS}	0	–	0	–	0	–	ns
Data hold time [9]	t_{DH}	15	–	15	–	15	–	ns
Data hold time referenced to $\overline{RAS}$	t_{DHR}	50	–	55	–	60	–	ns
Refresh period	t_{REF}	–	8	–	8	–	8	ms
Refresh period L-version	t_{REF}	–	64	–	64	–	–	ms
Write command setup time [10]	t_{WCS}	0	–	0	–	0	–	ns

Notes see page 62.

AC Characteristics (cont'd) [4) 5)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		-60		-70		-80		
		min.	max.	min.	max.	min.	max.	
$\overline{CAS}$ to $\overline{WRITE}$ delay time [10)]	t_{CWD}	50	–	50	–	50	–	ns
$\overline{RAS}$ to $\overline{WRITE}$ delay time [10)]	t_{RWD}	90	–	100	–	110	–	ns
Column address to $\overline{WRITE}$ delay time [10)]	t_{AWD}	60	–	65	–	70	–	ns
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CSR}	10	–	10	–	10	–	ns
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CHR}	30	–	30	–	30	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0	–	0	–	0	–	ns
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ counter test cycle)	t_{CPT}	40	–	40	–	40	–	ns
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	10	–	10	–	10	–	ns
$\overline{OE}$ access time	t_{OEA}	–	20	–	20	–	20	ns
$\overline{OE}$ to data delay	t_{OED}	20	–	20	–	20	–	ns
Output buffer turn-off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	20	0	20	ns
$\overline{OE}$ command hold time	t_{OEH}	20	–	20	–	20	–	ns

Notes see page 62.

Capacitance

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A8)	C_{I1}	–	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	C_{I2}	–	7	pF
Output capacitance (I/O1 ... I/O4)	C_O	–	7	pF

Notes for pages 57 to 61:

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} and I_{CC7} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.

4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

5) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

6) Measured with a load equivalent to 2 TTL loads and 100 pF.

7) t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open-circuit conditions and is not referenced to output voltage levels.

8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WRITE}$ leading edge in read-modify-write cycles.

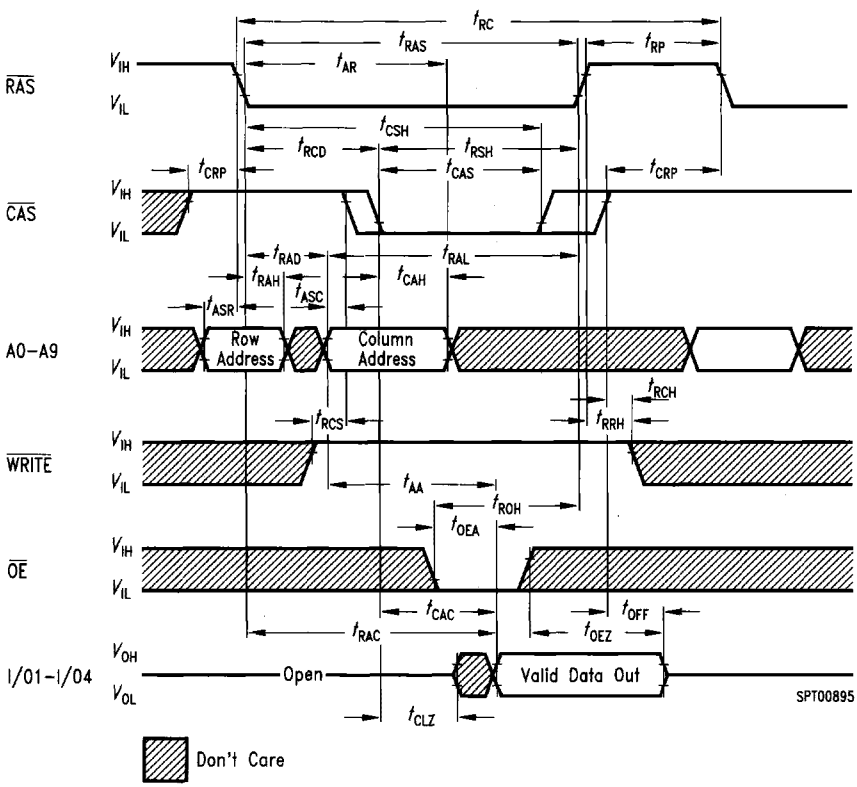
10) t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.) and $t_{AWD} \geq t_{AWD}$ (min.), the cycle is a read-modify-write cycle and DO will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out (at access time) is indeterminate.

11) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met, t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

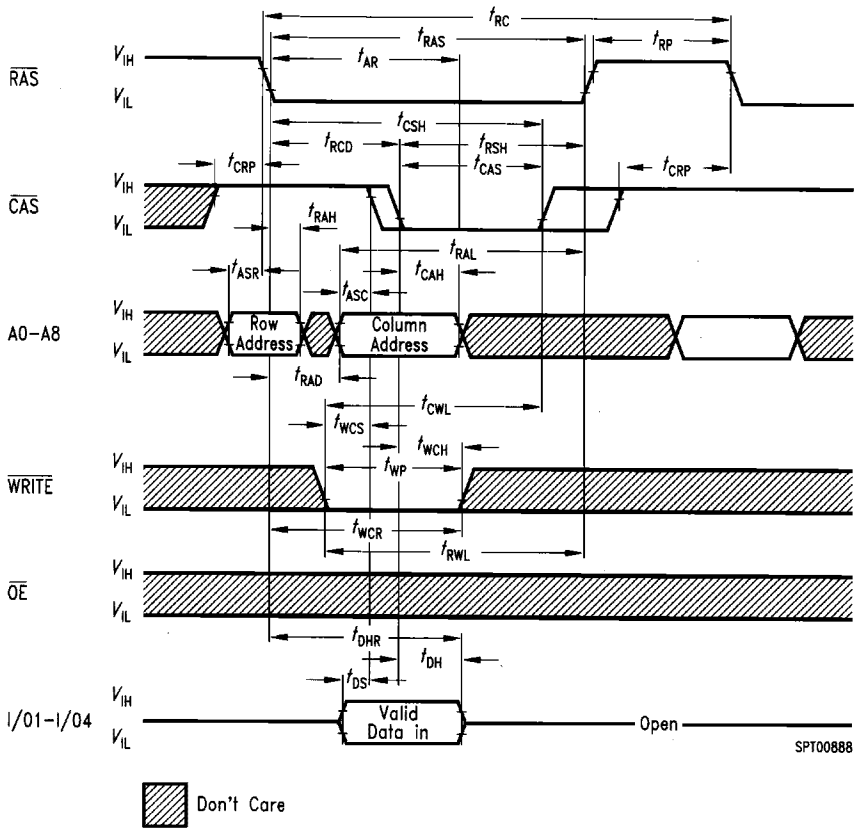
12) Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

13) t_{RAS} (max.) = 1 µs is only applied to refresh of battery-backup.
t_{RAS} (max.) = 10 µs is applied to functional operating.

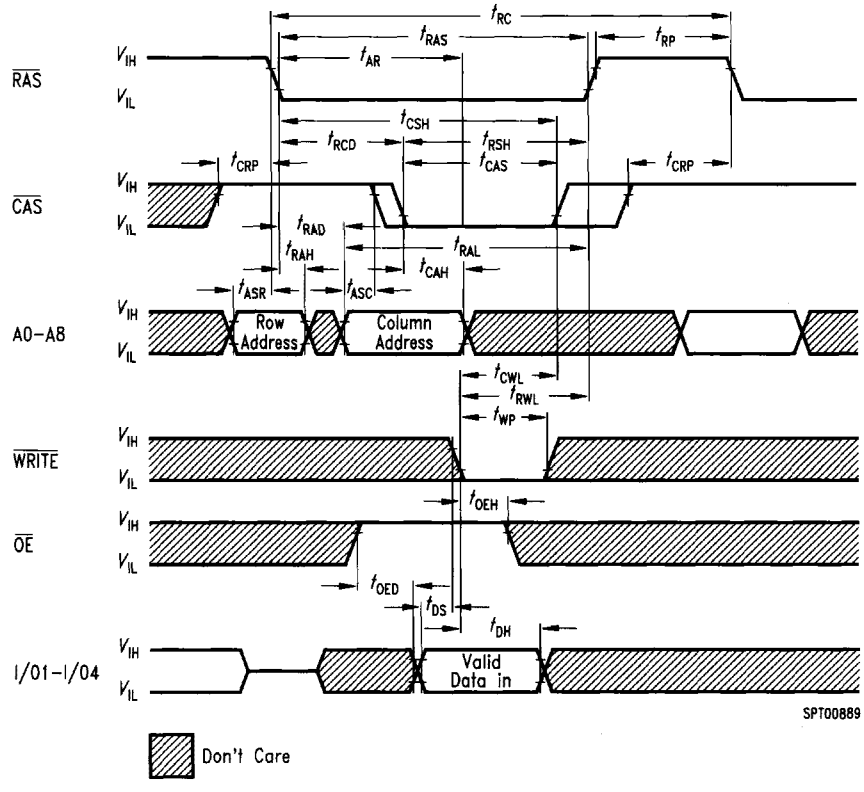
Waveforms



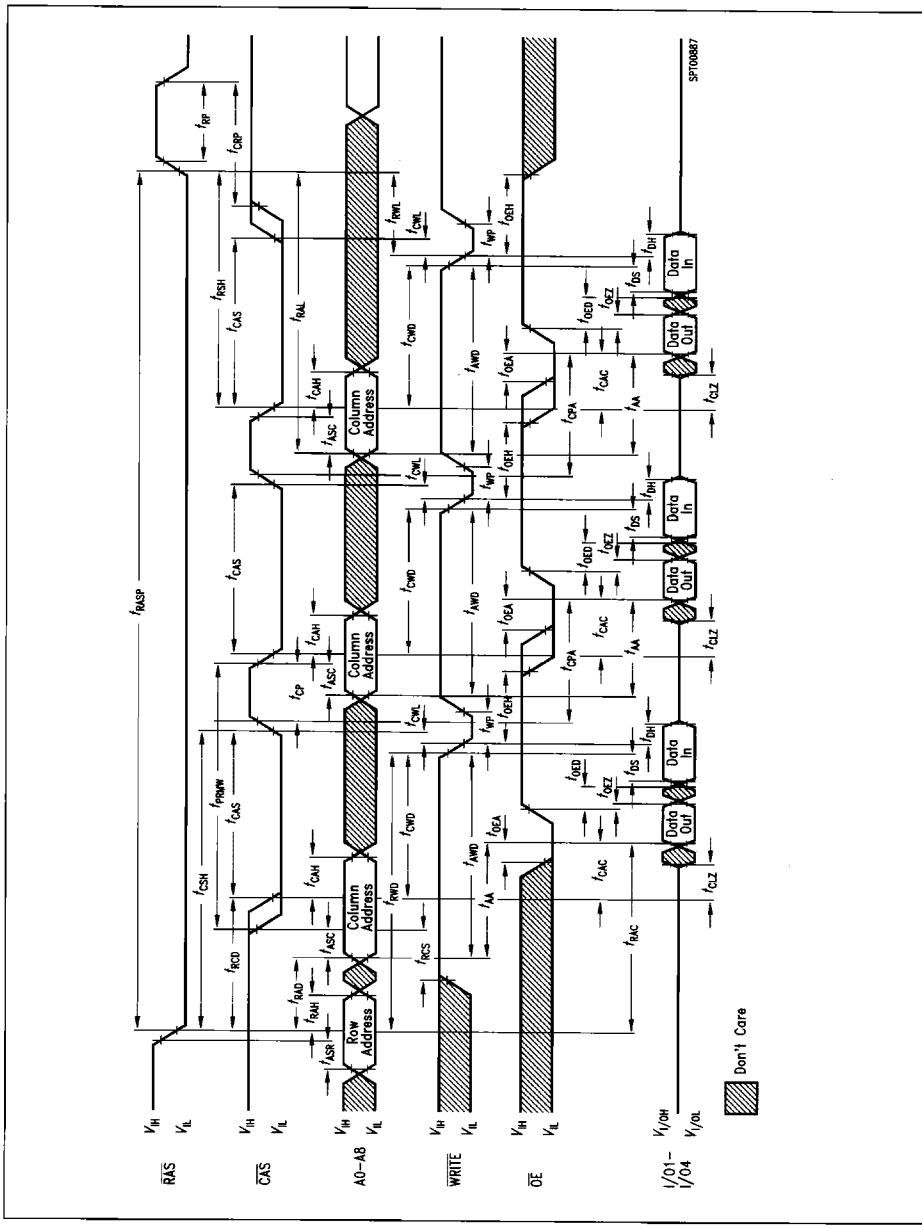
Read Cycle



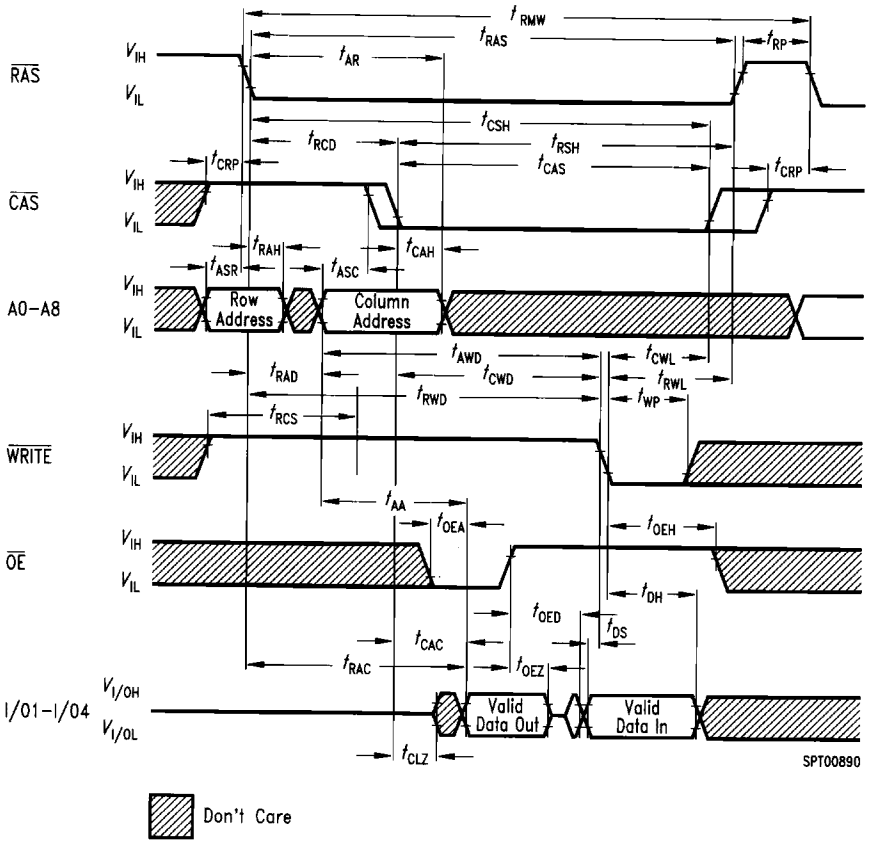
Write Cycle (Early Write)



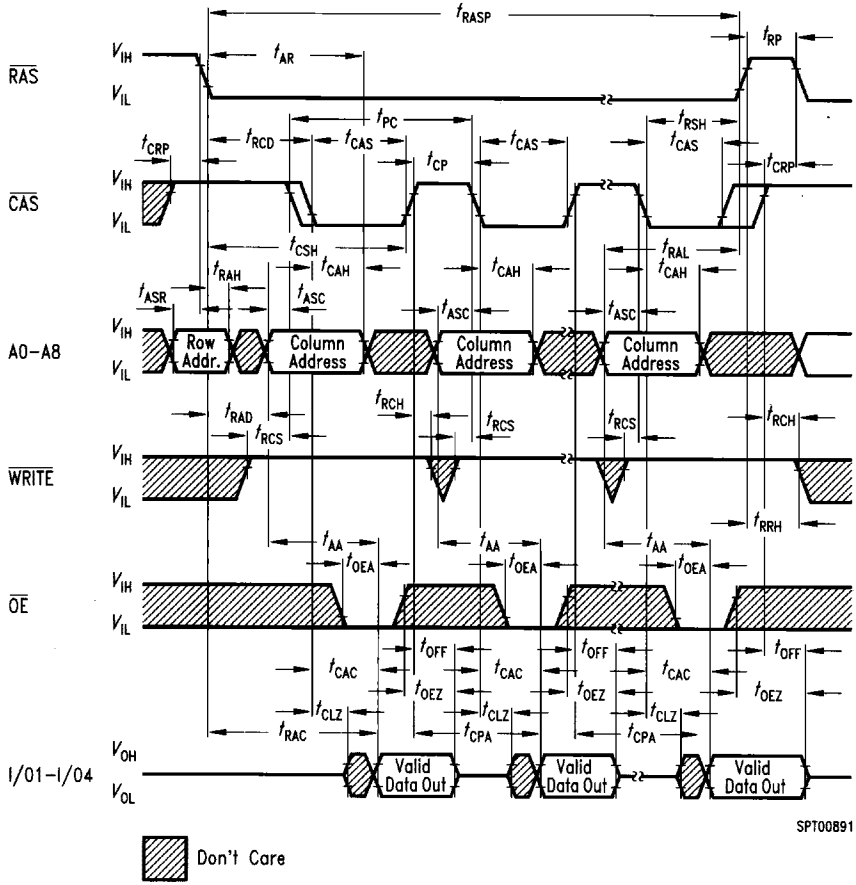
Write Cycle ($\overline{OE}$ Controlled Write)



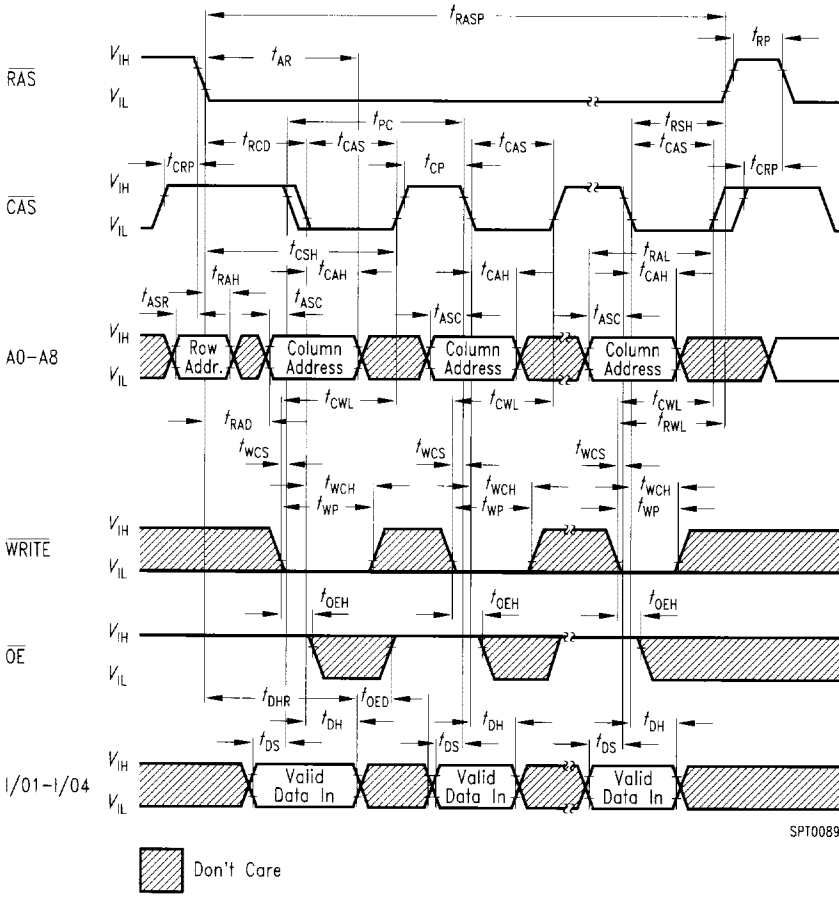
Fast Page Mode Read-Modify-Write Cycle



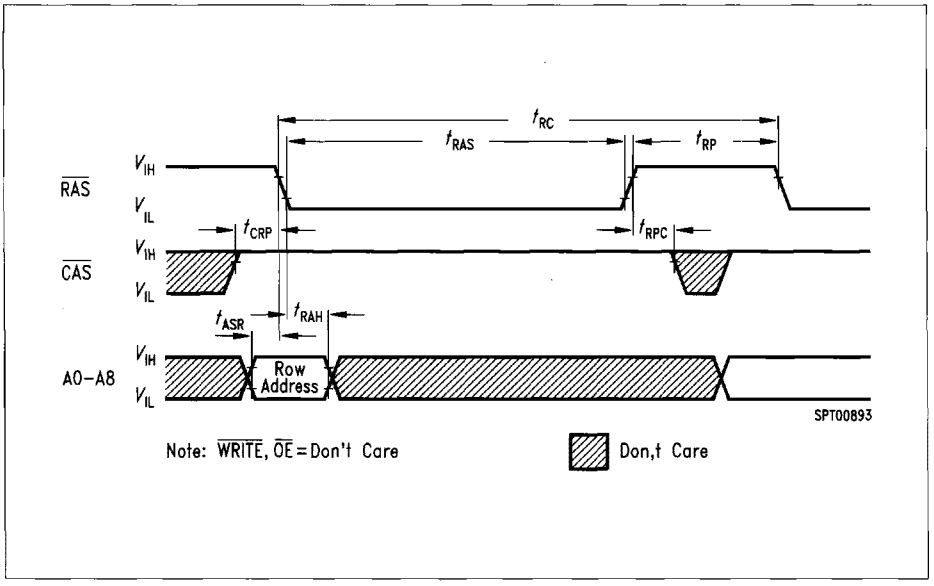
Read-Write (Read-Modify-Write) Cycle



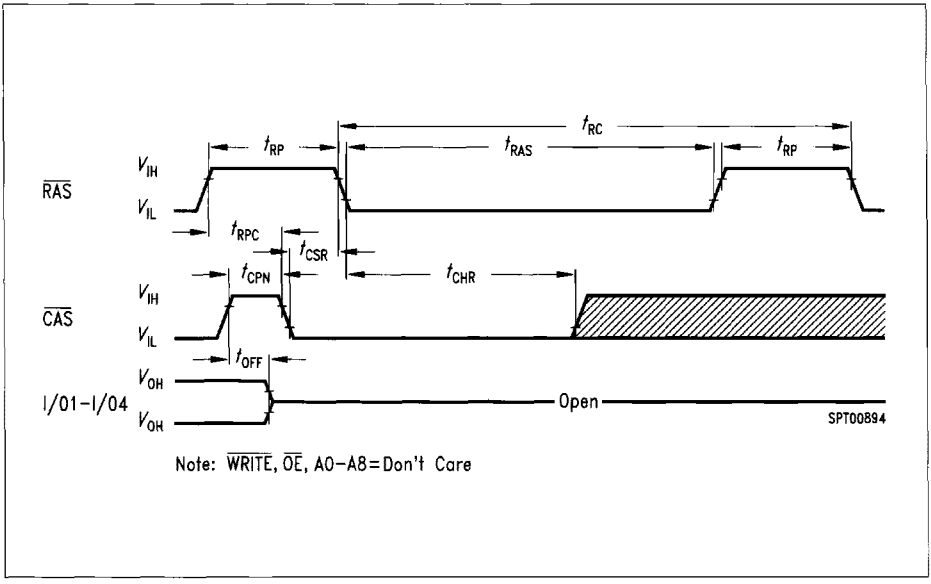
Fast Page Mode Read Cycle



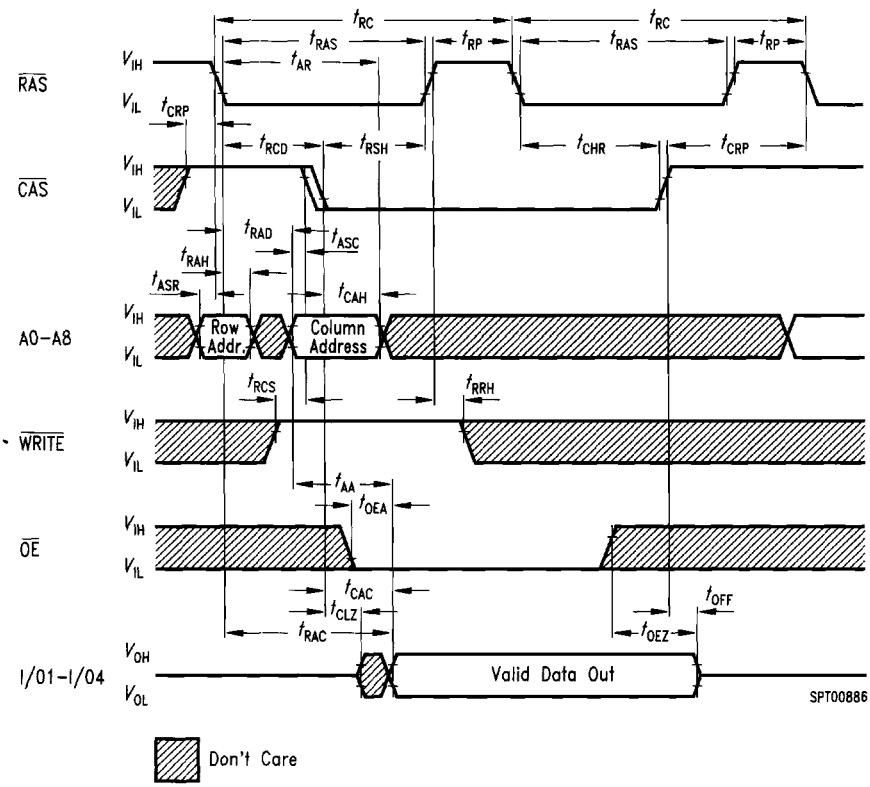
Fast Page Mode Write Cycle



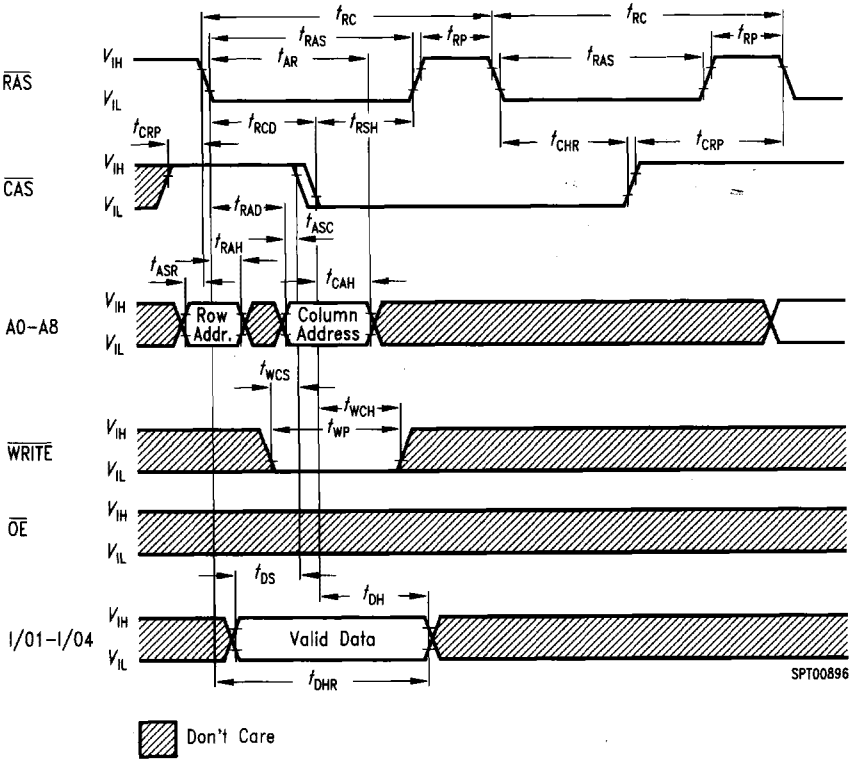
RAS-Only Refresh Cycle



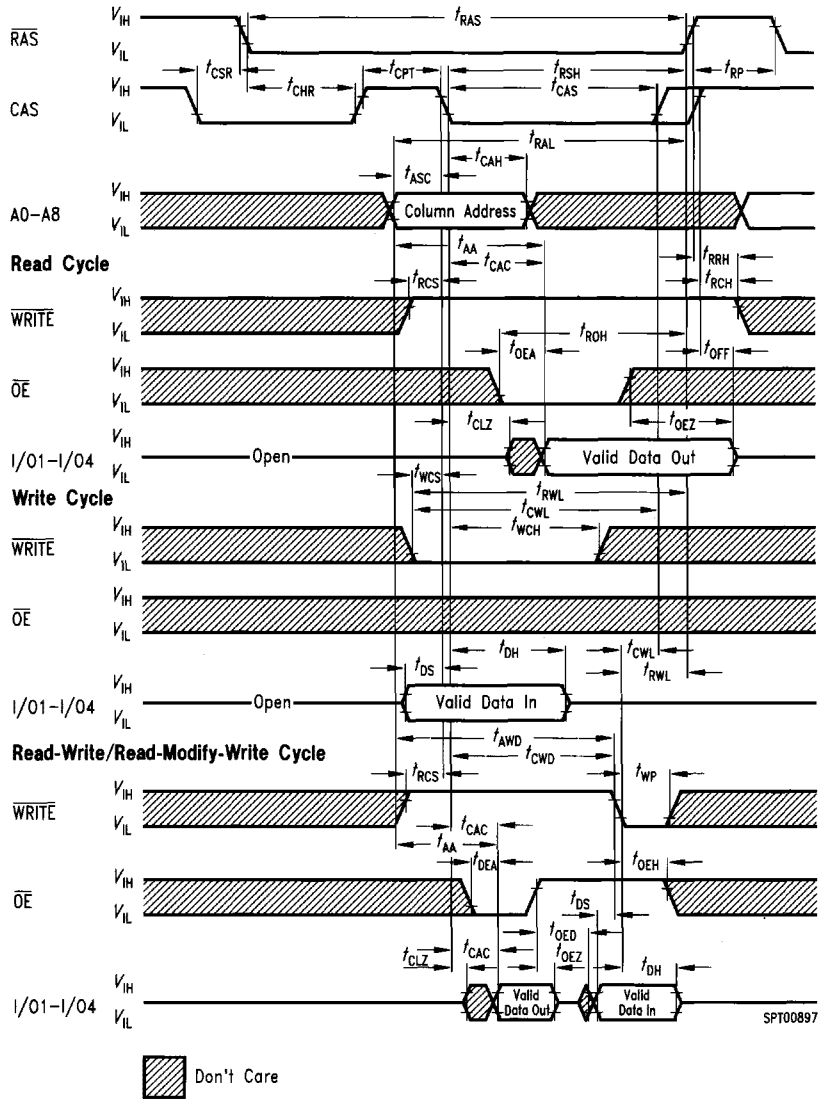
CAS-Before-RAS Refresh Cycle



Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)



CAS-Before-RAS Refresh Counter Test Cycle