

## FT6122, FT6122D

### Power MOS FET Arrays

Silicon N-channel Enhancement Mode Power MOS FET Arrays

#### ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Condition	Value	Unit
Drain Source Voltage	V <sub>DSS</sub>		120	V
Gate Source Voltage	V <sub>GS</sub>		±20	V
Drain Current	I <sub>D</sub>	T <sub>c</sub> = 25°C	4	A
	I <sub>DM</sub>		8	A
Reverse Drain Current (Continuous)	I <sub>DR</sub>		4	A
Fast Recovery Diode Forward Current	I <sub>FM</sub>	P <sub>w</sub> ≤ 0.5 ms, DR ≤ 25%	4	A
	I <sub>FSM</sub>	P <sub>w</sub> ≤ 100 ms, Single Pulse	8	A
Fast Recovery Diode Reverse Voltage	V <sub>R</sub>		130	V
Total Drain Power Dissipation	P <sub>T</sub>	T <sub>c</sub> = 25°C, 4-MOSFET operation	4	W
	P <sub>T</sub>	T <sub>c</sub> = 25°C, 4-MOSFET operation	36	W
Thermal Resistance Junction to Case	R <sub>thj-c</sub>	T <sub>c</sub> = 25°C, 4-MOSFET operation	3.5	°C/W
Channel Temperature	T <sub>ch</sub>		+150	°C
Storage Temperature	T <sub>stg</sub>		-55 ~ +150	°C

#### ELECTRICAL CHARACTERISTICS (Ta = 25°C) : for Single MOS FET

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Parameter	Symbol	Test Condition	Limit			Unit
			Min.	Typ.	Max.	
Drain to Source Breakdown Voltage	BV <sub>DSS</sub>	I <sub>D</sub> = 100 μA, V <sub>GS</sub> = 0 V	120	—	—	V
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V	—	—	100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 120 V, V <sub>GS</sub> = 0 V	—	—	100	μA
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	I <sub>D</sub> = 1 mA, V <sub>DS</sub> = 10 V	0.9	1.3	1.7	V
Static Drain to Source On-State Resistance	R <sub>DS(on)</sub>	I <sub>D</sub> = 3 A, V <sub>GS</sub> = 4 V	*	0.32	0.5	Ω
	R <sub>DS(on)</sub>	I <sub>D</sub> = 3 A, V <sub>GS</sub> = 10 V	*	0.25	0.4	Ω
Forward Transconductance	g <sub>f</sub>	I <sub>D</sub> = 3 A, V <sub>DS</sub> = 10 V	*	2.5	4.5	—
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 25 V	—	450	550	pF
	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	—	140	210	pF
Output Capacitance	C <sub>oss</sub>	f = 1 MHz	—	60	90	pF
	C <sub>oss</sub>		—	—	—	—
Reverse Transfer Capacitance	C <sub>ros</sub>		—	—	—	—
Turn-On Delay Time	t <sub>d(on)</sub>	I <sub>D</sub> = 3 A (See Test Circuit)	—	25	—	ns
Rise Time	t <sub>r</sub>	V <sub>DD</sub> = 60 V	—	30	—	ns
Turn-Off Delay Time	t <sub>d(off)</sub>	V <sub>GS</sub> = 10 V	—	75	—	ns
Fall Time	t <sub>f</sub>	R <sub>GS</sub> = 50 Ω	—	35	—	ns

\* Pulsed : Pulse Width ≤ 300 μs, D.R. ≤ 6%

#### SOURCE-DRAIN DIODE CHARACTERISTICS : for Single MOS FET

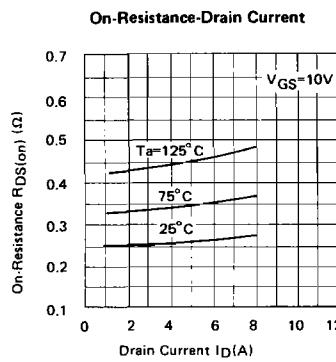
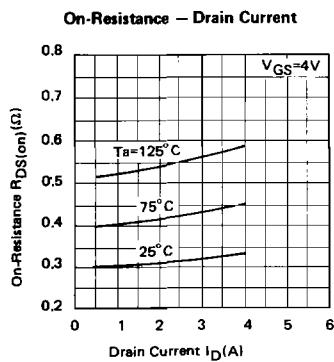
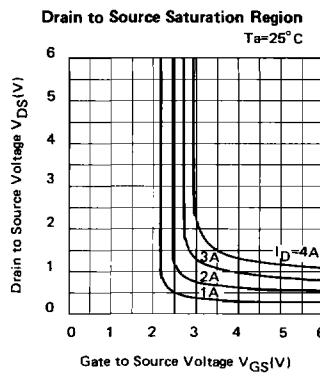
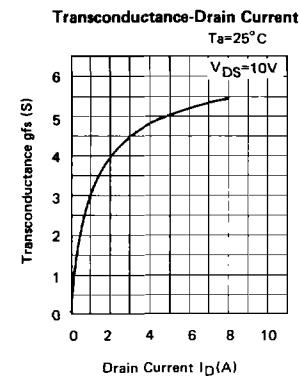
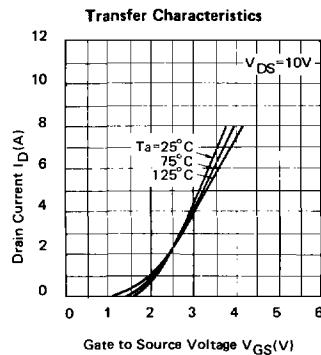
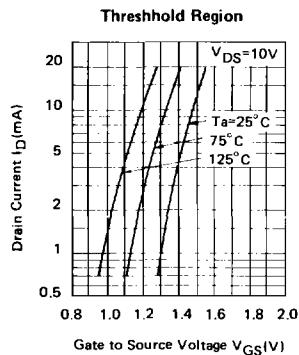
Forward On-Voltage	V <sub>SD</sub>	I <sub>DR</sub> = 3 A, V <sub>GS</sub> = 0 V	—	1.0	1.2	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>DR</sub> = 3 A, dI <sub>DR</sub> /dt = 100 A/μs	—	140	—	ns

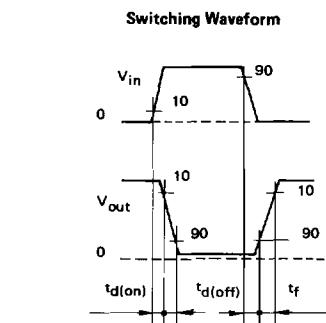
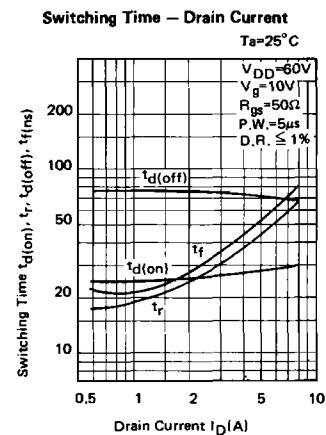
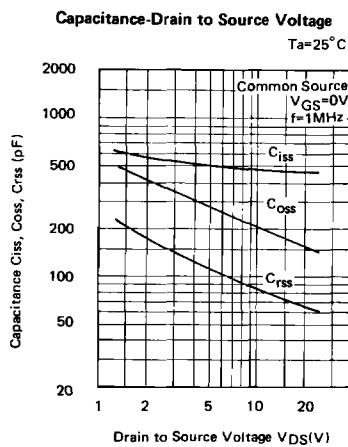
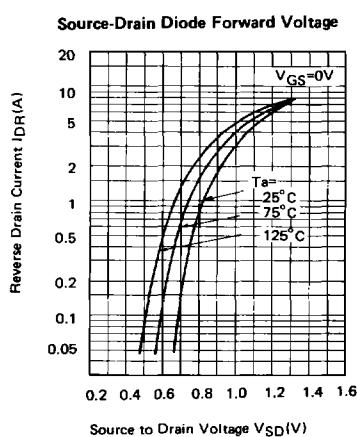
#### FAST RECOVERY DIODE CHARACTERISTICS : for Single Diode (FT6122D only)

Forward Voltage	V <sub>F</sub>	I <sub>F</sub> = 1 A	—	—	1.0	V
Reverse Current	I <sub>R</sub>	V <sub>R</sub> = 120 V	—	—	10	μA
Reverse Voltage	V <sub>R</sub>	I <sub>R</sub> = 15 μA	130	—	—	V

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**Test Circuit for Switching Time**

