SB600 Databook

Technical Reference Manual
Rev. 3.05

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Table of Contents

1 Introduction 7
1.1 Features of the SB600 7
1.2 Block Diagram and System Configuration 10
1.3 Part Number and Branding 13

2 Ball-out Assignment 14

3 Signal Description 16
3.1 A-Link Express II Interface 16
3.2 PCI Interface (PCI Host Bus and Internal PCI/PCI Bridge) 16
3.3 ATA66/100/133 17
3.4 LPC Interface 18
3.5 USB Interface 18
3.6 Serial ATA Interface 18
3.7 Power Management / North Bridge Interface 19
3.8 Processor Interface 23
3.9 SMBUS Interface / General Purpose Open Collector 23
3.10 Real Time Clock Interface 24
3.11 Reset / Clocks / ATE 24
3.12 General Purpose I/O 24
3.13 External Event / General Event / General Power Management / General Purpose Open Collector 26
3.14 AC '97 Link Interface 28
3.15 HD Audio Interface 28
3.16 XBUS ROM Access Interface 28
3.17 SPI ROM Interface 29
3.18 Hardware Monitor 29
3.19 Power and Ground 30
3.20 Pin Straps 31

4 Power Planes and Pin States 34
4.1 Power Up and Down Sequences 34
Power Up/Down Sequence Timing Notes 40
4.2 ACPI Timing 44
4.3 Pull-up/-down Requirements and Integrated Resistors 45

5 Functional Description 52
5.1 EHCI USB 2.0 and OHCI USB 1.1 Controllers 52
5.1.1 USB Architecture Overview 52
5.1.2 USB Power Management 53
5.2 SMI#/SCI Generation 54
5.3 LPC ISA Bridge 55
5.3.1 LPC Interface Overview 55
5.3.2 LPC Module Block Diagram 58
5.4 Real Time Clock 58
5.4.1 Functional Blocks of RTC 58
5.5 SATA (Serial ATA) Controller 59
5.6 AC '97 Controller 60
5.6.1 Output Data Stream 61

5.6.2 Input Data Stream 61
5.6.3 AC '97 Controller-Codec(s) Connections 62
5.7 High Definition Audio 65
5.7.1 HD Audio Codec Connections 65
5.7.2 HD Audio and AC '97 Codec Connections in Mixed Configurations 65
5.8 General Events and GPIOs 68

6 System Clock Specifications 69
6.1 System Clock Descriptions 69
6.2 System Clock Input Frequency Specifications 69
6.3 System Clock AC Specifications 69

7 States of Power Rails during ACPI S1 to S5 States 73

8 Electrical Characteristics 74
8.1 Absolute Maximum Ratings 74
8.2 Functional Operating Range 74
8.3 DC Characteristics 75
8.4 RTC Battery Current Consumption 79

9 Power Requirements 80

10 Package Information 85
10.1 Physical Dimensions 85
10.2 Pressure Specification 86

11 Thermal Information 87

12 Testability 88
12.1 Test Control Signals 88
12.2 XOR Chain Test Mode 89
12.2.1 Brief Description of an XOR Chain 89
12.2.2 Description of the SB600 XOR Chain 90
12.2.2.1 Unused Pins 92

Appendix A: Pin Listing 93

Appendix B: Revision History 105

List of Figures

Figure 1-1: SB600 Block Diagram 10
Figure 1-2: RS600/SB600/DDR2 “Marlin” Desktop System Block Diagram 11
Figure 1-3: RS600ME-SB600-DDR2 “Albacore” Mobile System Block Diagram 12
Figure 1-4: SB600 Branding Diagram 13
Figure 2-1: SB600 Ball-out Assignment (Left) 14
Figure 2-2: SB600 Ball-out Assignment (Right) 15
Figure 3-1: Straps Capture 31
Figure 4-1: SB600 Power Up/Down Sequence for Platforms with Intel Processors 36
Figure 4-2: SB600 S3/S0 Power Up/Down Sequence for Platforms Intel Processors 37
Figure 4-3: SB600 Power Up/Down Sequence for Platforms with AMD Processors 38
Figure 4-4: SB600 S3/S0 Power Up/Down Sequence for Platforms with AMD Processors 39
Figure 4-5: Circuit for Maintaining Proper Relationship between +V5_VREF and VDDQ 40
Figure 4-6: PCIE_PVDD vs. VDD Ramp Requirement 40
Figure 4-7: Timing for Latching of Straps 41
Figure 4-8: Timing for SB PWRGD De-asserted to RSM_RST# De-asserted 41
Figure 4-9: DPRSTP# Fully De-asserted when SB PWRGD Asserted 42
Figure 4-10: CPU_STP# De-asserted when SB PWRGD Asserted 42
Figure 4-11: Glitch on LDT_RST# 43
Figure 4-12: T13 Measurement Points 43
Figure 5-1: SB600 USB 2.0 System Block Diagram 52
Figure 5-2: A Typical LPC Bus System 55
Figure 5-3: LPC Host Controller Interfaces and Signals 56
Figure 5-4: Block Diagram of LPC Module 58
Figure 5-5: Block Diagram of Internal RTC 59
Figure 5-6: Block Diagram for the SATA Module 60
Figure 5-7: ACLINK AC_SDOUT Serial Stream 61
Figure 5-8: ACLINK ACZ_SDIN Serial Stream 62
Figure 5-9: Single AC ‘97 Codec Connection 63
Figure 5-10: Multiple AC ‘97 Codec Connection 64
Figure 5-11: HD Audio Codec Connections 65
Figure 5-12: HD Audio and AC ‘97 Codec Connections for Mixed Configurations 66
Figure 5-13: Schematic for HD Audio and AC ’97 Codec Connections in a Mixed Configuration 67
Figure 6-1: Timing Labels for AC Specifications of the SB600 Clocks 70
Figure 10-1: SB600 23 mm x 23 mm 0.8 mm Pitch 549-FCBGA Package Outline* 85
Figure 11-1 Test Mode Capturing Sequence Timing 89
Figure 11-2: A Generic XOR Chain 89
Figure 11-3: On-chip XOR Chain connectivity 90

List of Tables

Table 1-1: SB600 Part Numbers 13
Table 3-1: Standard Straps 31
Table 3-2: Debug Straps 32
Table 3-3: Additional Straps 33
Table 4-1: SB600 Power Up/Down Sequence Timing 34
Table 4-2: External Resistor Requirements and Integrated Pull Up/Down 45
Table 5-1: EHCI Support for Power Management States 53
Table 5-2: EHCI Power State Summary 53
Table 5-3: Causes of SMI# and SCI 54
Table 5-4: LPC Cycle List and Data Direction 57
Table 5-5: Pin Definitions 60
Table 5-6: AC_SDOUT Slots definitions 61
Table 5-7: ACZ_SDIN Slots Definitions 62
Table 5-8: SMI, SCI, and Wake Event Support by GPIO and General Event Pins 68
Table 5-9: Functionality of the General Events and GPIOs across ACPI States 68
Table 6-1: SB600 System Clock Descriptions 69
Table 6-2: SB600 System Clock Input Frequency Specifications 69
Table 6-3: 14 MHz OSC Reference Clock AC Specifications 70
Table 6-4: 48MHz USB/SIO Clock AC Specifications 70
Table 6-5: RTC X1 Clock AC Specifications 71
Table 6-6: LPC Clock AC Specifications 71
Table 6-7: PCI Clock AC Specifications 71
Table 6-8: AC 97 Clock AC Specifications 72
Table 7-1: State of Each Power Rail during ACPI S1 to S5 States 73
Table 8-1: Absolute Maximum Rating 74
Table 8-2: DC Characteristic for Power Supplies to the SB600 75
Table 8-3: DC Characteristics for Interfaces on the SB600 75
Table 8-4: GPIO/GEVENT Output DC Characteristics 76
Table 8-5: GPIO/GEVENT Input DC Characteristics 76
Table 8-6: RTC Battery Current Consumption 79
Table 9-1: Configuration Set Up for SB600 Power Activity Test 80
Table 9-2: Power Activity under Configuration 1 81
Table 9-3: Power Activity under Configuration 2 and 3 81
Table 9-4: Power Activity under Configuration 4 and 5 82
Table 9-5: Power Activity under Configuration 6 and 7 83
Table 9-6: Power Activity for SB600 under a Fully Loaded System Configuration 84
Table 10-1: SB600 Package Physical Dimensions 85
Table 11-1: SB600 Thermal Limits 87
Table 12-1: Signals for the Test Controller of the SB600 88
Table 12-2: Test Mode Signals 88
Table 12-3: TEST0 Bit Sequence 88
Table 12-4: Truth Table for an XOR Chain 89
Table 12-5: List of Pins on the SB600 XOR Chain and the Order of Connection 90
Table 12-6: Pins Excluded from the XOR Chain 92
Table 12-7: SB600 Pin List Sorted by Interface 93
Table 12-8: SB600 Pin List Sorted by Ball Reference 99

1 Introduction

AMD's SB600 is a south bridge that integrates key I/O, communications, and audio features required in a state-of-the-art PC into a single device. It is specifically designed to operate with AMD's families of integrated graphics processors (IGPs) in desktop and mobile PCs.

1.1 Features of the SB600

CPU Interface

- Supports the following Intel processors:
  - Desktop: Pentium 4, Pentium D, Pentium Extreme Edition, Prescott, Celeron, Celeron D, Cedar Mill, Presler, Conroe, Allendale
  - Mobile: Mobile Pentium 4, Pentium M, Mobile Prescott, Celeron M, Yonah, Yonah Celeron, Merom
- Supports the following AMD processors:
  - Desktop: Athlon 64, Athlon 64 FX, Athlon 64 X2, Sempron, Opteron, dual-core Opteron
  - Mobile: Athlon XP-M, Mobile Athlon 64, Turion 64, Mobile Sempron

A-Link Express II interface to the RADEON IGPs

- 1/2/4-lane A-Link Express II interface
- Dynamic detection of lane configuration
- High data transfer bandwidth

PCI Host Bus Controller

- Supports PCI Rev. 2.3 specification
- Supports PCI bus at 33MHz
- Supports up to 6 bus master devices
- Supports 40-bit addressing
- Supports interrupt steering for plug-n-play devices
- Supports concurrent PCI operations
- Supports hiding of PCI devices by BIOS/hardware
- Supports spread spectrum

USB controllers

- 5 OHCI and 1 EHCI Host controllers to support 10 USB ports
- All 10 ports are USB 1.1 ("Low Speed", "Full Speed") and 2.0 ("High Speed") compatible
- Supports ACPI S1~S5
- Supports legacy keyboard/mouse
- Supports USB debug port
- Supports port disable with individual control

SMBus Controller

- SMBus Rev. 2.0 compliant
- Support SMBALERT # signal / GPIO

Interrupt Controller

- Supports IOAPIC/X-IO APIC mode for 24 channels of interrupts
- Supports 8259 legacy mode for 15 interrupts
- Supports programmable level/edge triggering on each channels
- Supports serial interrupt on quiet and continuous modes

DMA Controller

- Two cascaded 8237 DMA controllers
- Supports PC/PCI DMA
- Supports LPC DMA
- Supports type F DMA

LPC host bus controller

- Supports LPC based super I/O and flash devices
- Supports two master/DMA devices

- Supports TPM version 1.1/1.2 devices for enhanced security
- Supports SPI devices up to 33MHz

SATA II AHCI Controller

- Supports four SATA ports, complying with the SATA 1.0a specification
- Supports SATA II 3.0Gbit/s PHY, with backward compatibility with 1.5Gbit/s
- Supports RAID striping (RAID 0) across all 4 ports
- Supports RAID mirroring (RAID 1) across all 4 ports
- Supports RAID 10 (4 ports needed)
- Supports both AHCI mode and IDE mode
- Supports NCQ
- Supports Hot Plug in AHCI mode only
- Supports advanced power management with AHCI mode
- Supports SATA port multiplier (only for ASIC revision A13 and above. The total number of SATA RAID drives connected directly to the host and behind the port multiplier should not exceed 4 drives.)

Note: The SB600 does **not** support eSATA configuration directly from the host controller.

IDE Controller

- Single PATA channel support
- Supports PIO, Multi-word DMA, and Ultra DMA 33/66/100/133 modes
- 32x32byte buffers on each channel for buffering
- Swap bay support by tri-state IDE signals
- Supports Message Signaled Interrupt (MSI)
- Integrated IDE series resistors

AC Link interface

- Supports for both audio and modem codecs
- Compliant with AC-97 codec Rev. 2.3
- 6/8 channel support on audio codec
- Multiple functions for audio and modem Codec operations
- Bus master logic
- Supports up to 3 codecs simultaneously
- Supports SPDIF output
- Separate bus from the HD audio

HD Audio

- 4 Independent output streams (DMA)
- 4 Independent input streams (DMA)
- Up to 16 channels of audio output per stream
- Supports up to 4 codecs
- Up to 192kHz sample rate
- Up to 32-bit per sample
- Message Signaled Interrupt (MSI) capability
- 64-bit addressing capability for MSI
- 64-bit addressing capability for DMA bus master
- Unified Audio Architecture (UAA) compatible
- HD Audio registers can be located anywhere in the 64-bit address space

Timers

- 8254-compatible timer
- Microsoft High Precision Event Timer (HPET)
- ACPI power management timer

RTC (Real Time Clock)

- 256-byte battery-backed CMOS RAM
- Hardware supported century rollover
- RTC battery monitoring feature

Power Management

- ACPI specification 2.0 compliant power management schemes
    - Supports C2, C3, C4
    - Support C1e and C3 pop-up (AMD platform only)
    - Supports S0, S1, S2, S3, S4, and S5

  Note: The SB600 only supports the ACPI scheme. APM is NOT supported.
- Wakeup events for S1, S2, S3, S4/S5 generated by:
    - Any GEVENT pin

- Any GPM pin
- USB
- Power button
- Internal RTC wakeup
- SMI# event

- Supports SpeedStep™
- Full support for On-Now™
- Supports CPU SMM, generating SMI# signal upon power management events
- GPIO supports on external wake up events
- Supports CLKRUN# on PCI power management
- Provides clock generator and CPU STPCLK# control
- Hardware Monitoring support
- Support for ASF

Hardware Monitor

- Supports 3 Independent FAN Control outputs
- Supports 1 AMDSI function

Note: SB600 does not support thermal diode temperature sensing function.

1.2 Block Diagram and System Configuration

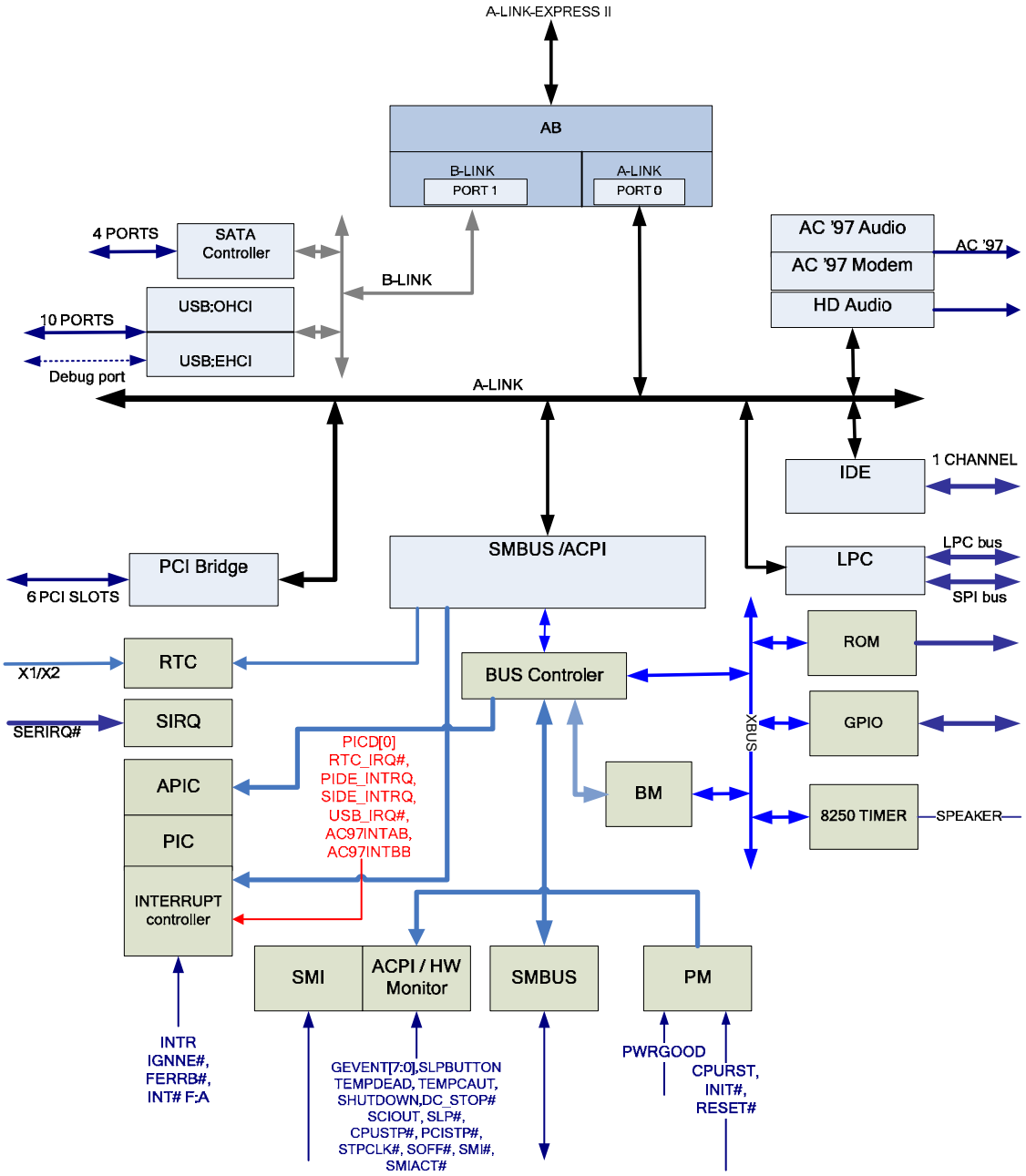


Figure 1-1: SB600 Block Diagram

Figure 1-1 is a block diagram for the SB600. *Figure 1-2* and *Figure 1-3* are configuration diagrams for sample systems utilizing a RADEON IGP and the SB600. These sample systems do not necessarily demonstrate all features of the SB600. Please refer to section *1.1*, *Features of the SB600*, for the full feature list of the device.

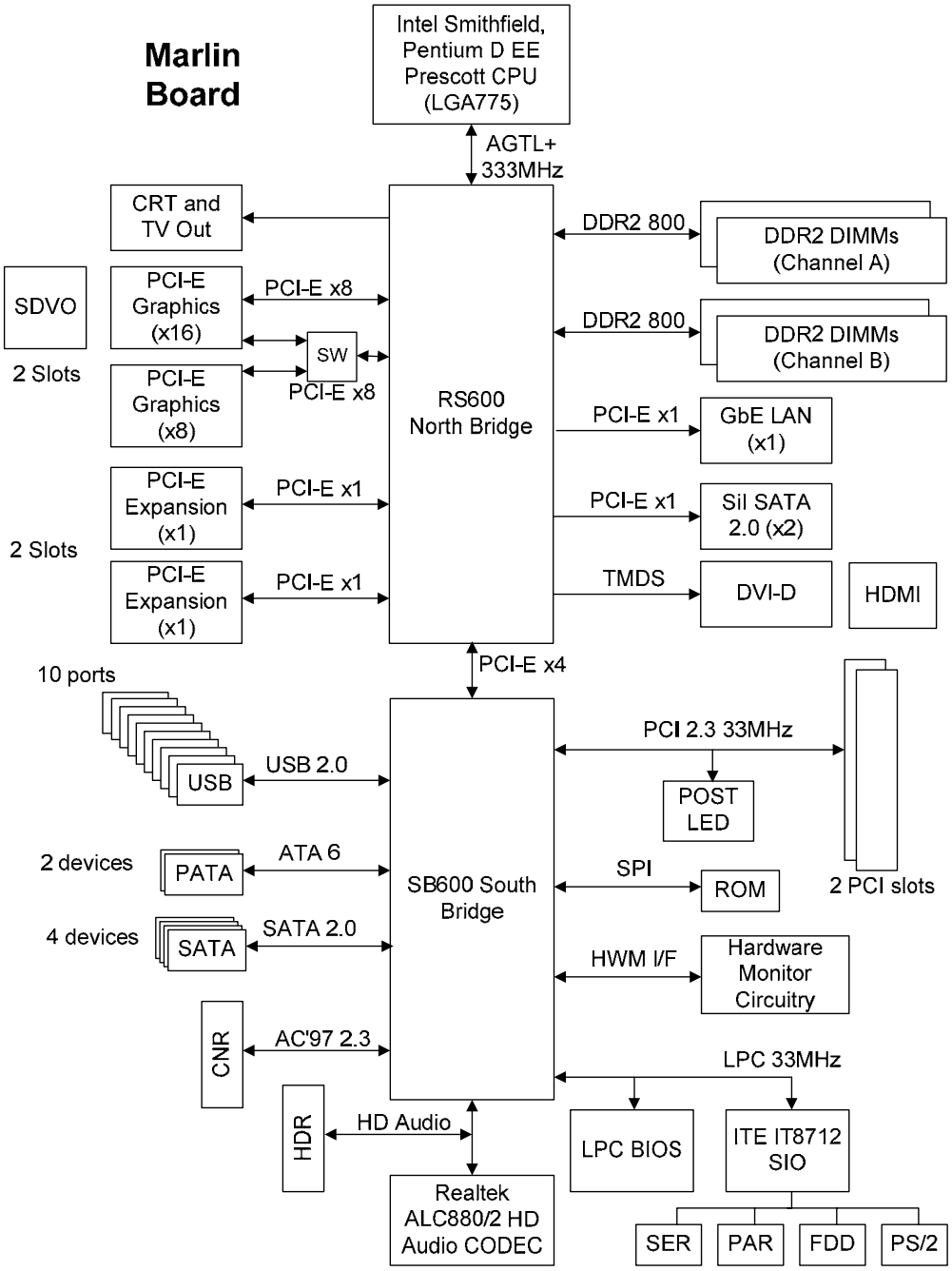


Figure 1-2: RS600/SB600/DDR2 "Marlin" Desktop System Block Diagram

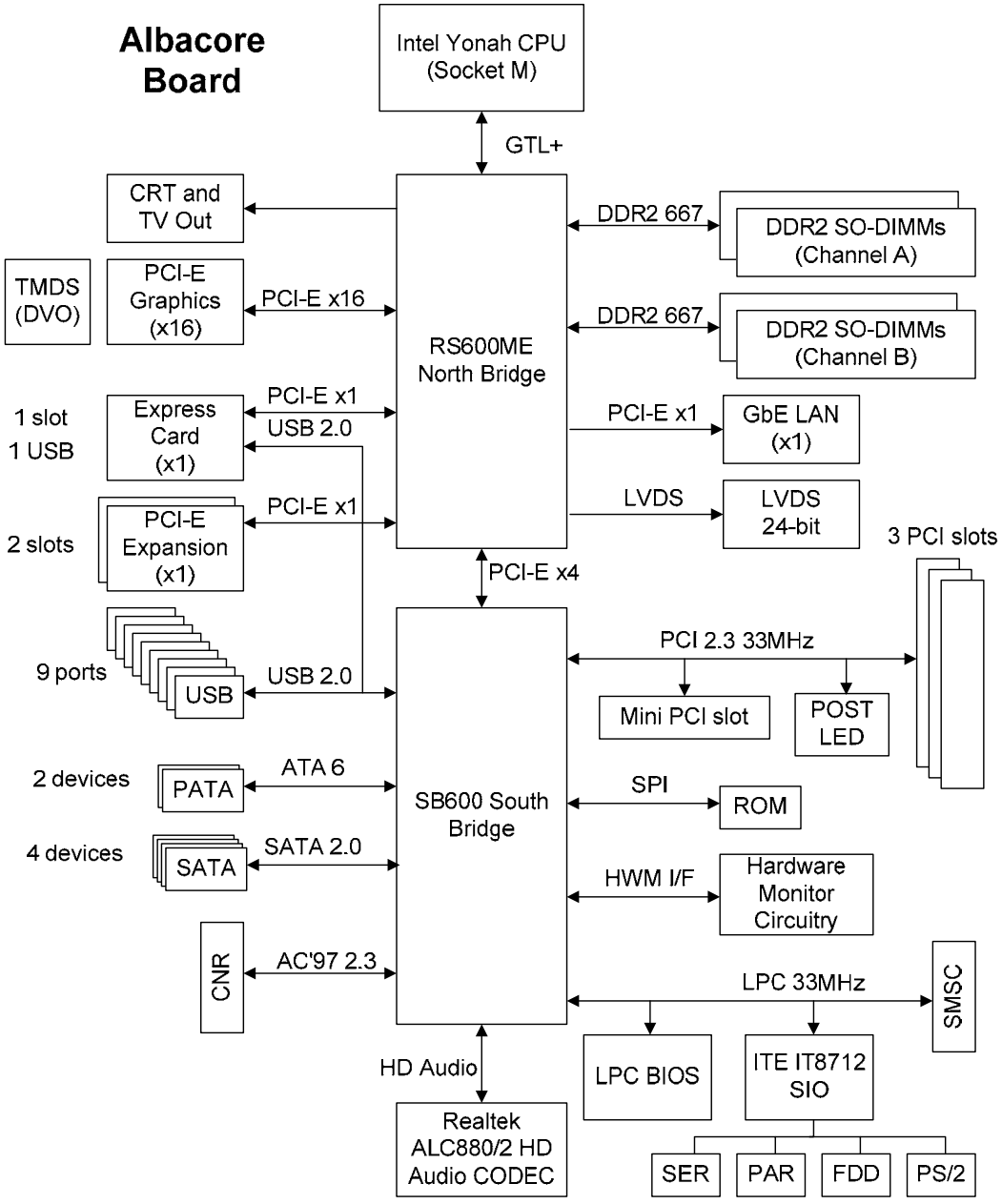
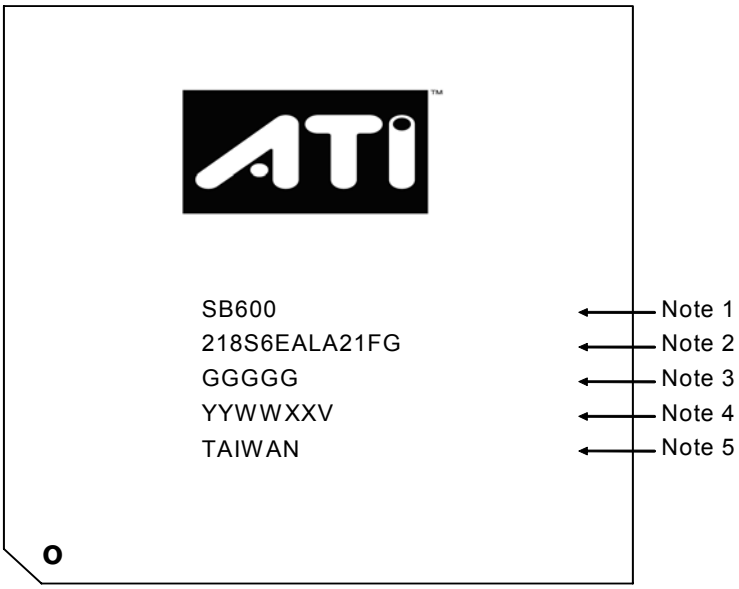


Figure 1-3: RS600ME-SB600-DDR2 "Albacore" Mobile System Block Diagram

1.3 Part Number and Branding



Note 1: Pre-production Marketing Name

Note 2: AMD Branded Part Number (see table below)

Note 3: Wafer foundry's lot ID and wafer ID: GGGGGG = Lot ID; Wxx = Wafer ID

Note 4: YY-assembly start year, WW-assembly start week, XX- assembly location

Note 5: Country of origin

Figure 1-4: SB600 Branding Diagram

Table 1-1: SB600 Part Numbers

ASIC Revision	Substrate Revision	AMD Part Number
		Lead Free
A12	C	218S6ECLA12FG
A13	C	218S6ECLA13FG
A21	C	218S6ECLA21FG

2 Ball-out Assignment

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	*Note*	S5_3.3V_1	PCI_PME#/GEVENT4#	LLB#/GPIO66	SLP_S5#	USB_OC4#/GPM4#	S5_3.3V_2	USB_OC0#/GPM0#	AVDDRX_0	USB_ATEST0	USB_ATEST1	AVDDC	AVSSC	USB_RCOMP	
B	VSS_5	RI#/EXTEVNT0#	SUS_STAT#	USB_OC6#/GEVENT6#	PWR_GOOD	USB_OC5#/DDR3_RST#/G	VSS_6	USB_OC1#/GPM1#	AVDDTX_0	AVDDRX_1	AVDDTX_1	AVDDRX_2	AVDDTX_2	AVDDRX_3	
C	X2	BLINK/GPM6#	SCL1/GPOC2#	USB_OC7#/GEVENT7#	USB_OC8#/AZ_DOCK_RS	USB_OC9#/SLP_S2/GPM9#	USB_OC2#/GPM2#	USB_OC3#/GPM3#	AVSS_USB_2	AVSS_USB_3	AVSS_USB_4	AVSS_USB_5	AVSS_USB_6	AVSS_USB_7	
D	RTC_GND	X1	RTCCLK	NC7		VSS_11	LPC_PME#/GEVENT3#		S3_STATE/GEVENT5#		AVSS_USB_13	USB_HSDM8-		USB_HSDM7-	
E	VBAT	RSMRST#	PWR_BTN#				WAKE#/GEVENT8#		TEST1		AVSS_USB_15	USB_HSDP8+		USB_HSDP7+	
F	S5_3.3V_3	VSS_13	SDA1/GPOC3#	SYS_RESET#/GPM7#	RTC_IRQ#/GPIO69		SLP_S3#		TEST2		AVSS_USB_17	AVSS_USB_18		AVSS_USB_19	
G	VSS_15	SPI_HOLD#/GPIO31	SPI_CLK/GPIO47	S5_1.2V_1	ROM_RST#/GPIO14	SPI_CS#/GPIO32	SMBALERT#/THRMTRIP#/		TEST0		AVSS_USB_24	USB_HSDM9-		USB_HSDP6+	
H	S5_1.2V_2	S5_1.2V_3	S5_1.2V_4								AVSS_USB_26	USB_HSDP9+		USB_HSDM6-	
J	VSS_16	ACZ_SDIN1/GPIO43	SPI_DI/GPIO12	ACZ_SDIN2/GPIO44	S5_3.3V_4	SPI_DO/GPIO11	S5_3.3V_5	VSS_17			AVSS_USB_28	AVSS_USB_29		AVSS_USB_30	
K	S5_3.3V_6	AZ_SDIN3/GPIO46	AZ_RST#												
L	AC_BITCLK/GPIO38	AC_SDOUT/GPIO39	AZ_SYNC	ACZ_SDIN0/GPIO42	AC_RST#/GPIO45	VSS_18	VIN1/GPIO54	VSS_19	VDDQ_5						
M	AVSS	AZ_SDOUT	AC_SYNC/GPIO40	FANOUT0/GPIO3	VDDQ_7	VIN4/GPIO57	VIN6/GPIO59	VIN2/GPIO55	VSS_20			VSS_21	VDD_1		VSS_22
N	AVDD	AZ_BITCLK	FANIN0/GPIO50									VDD_3	VSS_24		VDD_4
P	VSS_26	FANIN1/GPIO51	VDDQ_8	VIN5/GPIO58	TEMP_COMM	VSS_27	TEMPIN0/GPIO61	TEMPIN1/GPIO62	VDDQ_9						
R												VSS_29	VDD_6		VSS_30
T	SPDIF_OUT/PCICLK7/GPIO4	PCICLK1	FANOUT1/GPIO48	NC6	VDDQ_10	VSS_32	TEMPIN3/TALERT#/GPIO64	TEMPIN2/GPIO63	VSS_33						
U	PCICLK2	PCICLK0	PCICLK5									VDD_8	VSS_34		VDD_9
V	PCICLK6	PCICLK3	VSS_36	FANOUT2/GPIO49	VIN0/GPIO53	VIN3/GPIO56	VIN7/GPIO60	VSS_37	VDDQ_11			VSS_38	VDD_11		VSS_39
W	VSS_42	VDDQ_12	PCICLK4	FANIN2/GPIO52	AD3/ROMA15	VDDQ_13	AD0/ROMA18	AD2/ROMA16	VSS_43						
Y	AD1/ROMA17	STOP#	AD5/ROMA13												
AA	TRDY#/ROMOE#	FRAME#	AD16/ROMD0	NC5	AD4/ROMA14	AD6/ROMA12	AD8/ROMA9				VSS_45	VDDQ_16		VSS_46	
AB	AD18/ROMD2	AD20/ROMD4	AD22/ROMD6						CBE0#/ROMA10		AD13/ROMA4	GNT3#/GPIO72		AVSS_SATA_1	
AC	AD24	AD26	AD9/ROMA8	VDDQ_19	AD7/ROMA11	VSS_48	AD10/ROMA7		AD15/ROMA2		SERR#	SATA_ACT#/GPIO67		AVSS_SATA_4	
AD	AD30	AD28	INTE#/GPIO33	AD12/ROMA5			NC3		VSS_50		GNT0#	AVSS_SATA_7		PLLVDD_SATA_1	
AE	VDDQ_22	REQ1#	VSS_52			AD14/ROMA3	NC4		VDDQ_23		V5_VREF	AVSS_SATA_10		AVDD_SATA_1	
AF	INTF#/GPIO34	GNT1#	INTH#/GPIO36	INTG#/GPIO35		LOCK#	PAR/ROMA19		CBE1#/ROMA1		AVSS_SATA_12	SATA_CAL		AVSS_SATA_13	
AG	AD31	AD29	CBE3#	GNT4#/GPIO73	IRDY#	VSS_54	CLKRUN#	PERR#	REQ2#	A_RST#	AVSS_SATA_16	AVSS_SATA_17	AVSS_SATA_18	AVSS_SATA_19	
AH	AD27	AD25	AD23/ROMD7	AD19/ROMD3	REQ4#/GPIO71	DEVSEL#/ROMA0	GNT2#	REQ3#/GPIO70	CPU_STP#/DPSLP_3V#	AVSS_SATA_26	SATA_TX3-	SATA_RX3-	SATA_TX2+	SATA_TX2-	
AJ	VSS_55	VDDQ_26	AD21/ROMD5	AD17/ROMD1	CBE2#/ROMWE#	VDDQ_27	AD11/ROMA6	REQ0#	PCIRST#	PLLVDD_SATA_2	SATA_TX3+	AVDD_SATA_11	SATA_RX3+	AVDD_SATA_12	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Figure 2-1: SB600 Ball-out Assignment (Left)

***Note:** For ASIC A11, there is a VSS_1 ball at the A1 position. But for subsequent ASIC revisions, no ball exists there. However, references to the VSS_1 ball may continue to exist in AMD's reference schematics and other documents for the SB600, due to backward compatibility requirement with the SB460, which has a ground ball at the position. Those references can be safely ignored for any SB600 motherboard design that does not also support the SB460. See the product advisory titled *SB600 Ball-Out Change Notice* (AN_IXP600AA1) for details.

16	17	18	19	20	21	22	23	24	25	26	27	28	29	
AVSS_USB_1	USBCLK	USB_PHY_1.2V_1	USB_PHY_1.2V_2	VSS_2	VSS_3	AVDDCK_1.2V	WD_PWRGD/GPIO7	AVDDCK_3.3V	VDDQ_1	ROM_CS#/GPIO1	SSMUXSEL/SATA_IS3#/GPIO0	VDDQ_2	VSS_4	A
AVDDTX_3	AVDDRX_4	AVDDTX_4	USB_PHY_1.2V_3	USB_PHY_1.2V_4	USB_PHY_1.2V_5	AVSSCK	14M_OSC	DPSLP_OD#/GPIO37	VSS_7	SPKR/GPIO2	SMARTVOLT/SATA_IS2#/GPIO4	SDA0/GPOC1#	GHI#/SATA_IS1#/GPIO6	B
AVSS_USB_8	AVSS_USB_9	AVSS_USB_10	AVSS_USB_11	AVSS_USB_12	VSS_8	VSS_9	LAN_RST#/GPIO13	VSS_10	LPC_SMI#/EXTEVNT1#	DDC1_SDA/GPIO8	SCL0/GPOC0#	SATA_IS0#/GPIO10	VDDQ_3	C
USB_HSDP5+		USB_HSDP4+	USB_HSDP1+		AVSS_USB_14		SHUTDOWN#/GPIO5/SMARTVOLT2	VDDQ_4		DDC1_SCL/GPIO9	PCIE_VSS_1	PCIE_VSS_2	PCIE_VSS_3	D
USB_HSDM5-		USB_HSDM4-	USB_HSDM1-		AVSS_USB_16		NC1	VSS_12			PCIE_CALI	PCIE_CALRN	PCIE_CALRP	E
AVSS_USB_20		AVSS_USB_21	AVSS_USB_22		AVSS_USB_23		VSS_14			PCIE_VSS_4	PCIE_VDDR_1	PCIE_VDDR_2	PCIE_VDDR_3	F
USB_HSDP3+		USB_HSDP2+	USB_HSDP0+		AVSS_USB_25		PCIE_VSS_5	PCIE_VSS_6	PCIE_VSS_7	PCIE_VDDR_4	PCIE_VDDR_5	PCIE_VDDR_6	PCIE_VDDR_7	G
USB_HSDM3-		USB_HSDM2-	USB_HSDM0-		AVSS_USB_27						PCIE_VSS_8	PCIE_TX3N	PCIE_TX3P	H
AVSS_USB_31		AVSS_USB_32	AVSS_USB_33				PCIE_VSS_9	PCIE_RCLKP	PCIE_RCLKN	PCIE_VSS_10	PCIE_VDDR_8	PCIE_VSS_11	PCIE_VDDR_9	J
											PCIE_VSS_12	PCIE_TX2N	PCIE_TX2P	K
					VDDQ_6	PCIE_VSS_13	PCIE_VSS_14	PCIE_VSS_15	PCIE_VDDR_10	PCIE_VDDR_11	PCIE_VSS_16	PCIE_VSS_17	PCIE_VDDR_12	L
	VDD_2	VSS_23			PCIE_VSS_18	PCIE_RX3P	PCIE_RX3N	PCIE_VSS_19	PCIE_RX2P	PCIE_RX2N	PCIE_VSS_20	PCIE_TX1N	PCIE_TX1P	M
	VSS_25	VDD_5									PCIE_VSS_21	PCIE_VSS_22	PCIE_VDDR_13	N
					VSS_28	PCIE_VSS_23	PCIE_VSS_24	PCIE_VSS_25	PCIE_VSS_26	PCIE_VSS_27	PCIE_VSS_28	PCIE_TX0N	PCIE_TX0P	P
	VDD_7	VSS_31												R
					PCIE_VSS_29	PCIE_RX1P	PCIE_RX1N	PCIE_VSS_30	PCIE_RX0P	PCIE_RX0N	PCIE_VSS_31	PCIE_VSS_32	PCIE_VSS_33	T
	VSS_35	VDD_10									PCIE_VSS_34	PCIE_PVSS	PCIE_PVDD	U
	VDD_12	VSS_40			VSS_41	PCIE_VSS_35	PCIE_VSS_36	PCIE_VSS_37	PCIE_VSS_38	PCIE_VSS_39	PCIE_VSS_40	PCIE_VSS_41	PCIE_VSS_42	V
					VDDQ_14	BMREQ#/REQ5#/GPIO65	DPRSLPVR	NMI/LINT1	INIT#	INTR/LINT0	IDE_CS3#	IDE_CS1#	VDDQ_15	W
											FERR#	IDE_A2	VSS_44	Y
VDDQ_17		VSS_47	VDDQ_18			IGNNE#/SIC	SLP#/LDT_STP#	SMI#	STPCLK#/ALLOW_LDTSTP	A20M#/SID	CPU_PWR	IDE_IRQ	IDE_A0	AA
AVSS_SATA_2		AVSS_SATA_3	NC8								IDE_A1	IDE_DACK#	IDE_IORDY	AB
XTLVDD_SATA		AVSS_SATA_5	AVSS_SATA_6		NC2		VDDQ_20	VSS_49	LDT_RST#/DPRSTP#/PROC	CPU_PG/LDT_PG	IDE_DRQ	IDE_IOW#	IDE_IOR#	AC
SATA_X1		SATA_X2	AVSS_SATA_8		AVSS_SATA_9		VSS_51		IDE_D14/GPIO29	IDE_D1/GPIO16	VDDQ_21	IDE_D0/GPIO15	IDE_D15/GPIO30	AD
AVDD_SATA_2		AVDD_SATA_3	AVDD_SATA_4		AVSS_SATA_11		VDDQ_24				VSS_53	IDE_D13/GPIO28	IDE_D2/GPIO17	AE
AVSS_SATA_14		AVSS_SATA_15	AVDD_SATA_5		AVDD_SATA_6		SERIRQ	LFRAME#		GA20IN	IDE_D3/GPIO18	IDE_D11/GPIO26	IDE_D12/GPIO27	AF
AVSS_SATA_20	AVSS_SATA_21	AVSS_SATA_22	AVSS_SATA_23	AVSS_SATA_24	AVSS_SATA_25	AVDD_SATA_7	AVDD_SATA_8	LAD0	LAD1	KBRST#	IDE_D9/GPIO24	IDE_D10/GPIO25	IDE_D4/GPIO19	AG
SATA_RX2-	SATA_RX1-	SATA_TX1+	AVSS_SATA_27	SATA_RX0-	SATA_TX0+	AVDD_SATA_9	AVDD_SATA_10	LAD2	LAD3	LDRQ1#/GNT5#/GPIO68	IDE_D8/GPIO23	IDE_D5/GPIO20	VDDQ_25	AH
SATA_RX2+	SATA_RX1+	SATA_TX1-	AVDD_SATA_13	SATA_RX0+	SATA_TX0-	AVDD_SATA_14	AVDD_SATA_15	LDRQ0#	VSS_56	VDDQ_28	IDE_D7/GPIO22	IDE_D6/GPIO21	VSS_57	AJ
16	17	18	19	20	21	22	23	24	25	26	27	28	29	

Figure 2-2: SB600 Ball-out Assignment (Right)

3 Signal Description

Notes:
1. In the descriptions below, "[Intel]" indicates that the functions or descriptions apply only to Intel platforms and "[AMD]" indicates that they only apply to AMD platforms.
2. For ACPI timing details, refer to Section 4.2, "ACPI Timing for the SB600."
3. For multi-function pins, go to the relevant section for description of the relevant function (e.g., for SMALERT#/THRMTRIP#/GEVENT2#, the SMBus Alert function is described in section 3.9, "SMBUS Interface / General Purpose Open Collector" and the Thermal Trip function is described in section 3.7, "Power Management / North Bridge Interface").

3.1 A-Link Express II Interface

Pin Name	Type	Voltage	Functional Description
PCIE_TX[3:0]P	O	1.2V (Filtered)	A-Link Express II Lane 3-0 Transmit Positive
PCIE_TX[3:0]N	O		A-Link Express II Lane 3-0 Transmit Negative
PCIE_RX[3:0]P	I		A-Link Express II Lane 3-0 Receive Positive
PCIE_RX[3:0]N	I		A-Link Express II Lane 3-0 Receive Negative
PCIE_RCLKP	I		A-Link Express II Reference Clock Positive
PCIE_RCLKN	I		A-Link Express II Reference Clock Negative
PCIE_CALRP	O		A-Link Express II Calibration, TX termination reference resistor connection
PCIE_CALRN	O		A-Link Express II Calibration, RX termination reference resistor connection
PCIE_CALI	I		Reserved. Requires a pull-down to GND.

3.2 PCI Interface (PCI Host Bus and Internal PCI/PCI Bridge)

Pin Name	Type	Voltage	Functional Description
AD[15:0]/ROMA[18:11, 9:2]	I/O	3.3V (5V Tolerance)	PCI Bus Address/Data [15:0] / ROM Address [18:11, 9:2]
AD[23:16]/ROMD[7:0]	I/O	3.3V (5V Tolerance)	PCI Bus Address/Data [23:16] / ROM Data [7:0]
AD[31:24]	I/O	3.3V (5V Tolerance)	PCI Bus Address/Data [31:24]
BMREQ#/REQ5#/GPIO 65	I/O	3.3V (5V Tolerance)	Bus master REQ# (P4/K8) / PCI Request 5 Input / GPIO 65
CBE0#/ROMA10	I/O	3.3V (5V Tolerance)	Command/Byte Enable[0]/ ROM Address [10]
CBE1#/ROMA1	I/O	3.3V (5V Tolerance)	Command/Byte Enable[1]/ ROM Address [1]
CBE2#/ROMWE#	I/O	3.3V (5V Tolerance)	Command/Byte Enable[2]/ ROM WE #
CBE3#	I/O	3.3V (5V Tolerance)	Command/Byte Enable[3]
CLKRUN#	I/O	3.3V (5V Tolerance)	Clock running is de-asserted by the clock provider to indicate the system is about to shut down the PCI clock. When it is driven low by other agents, it means the agent is requesting the clock provider to not deactivate the clock.
DEVSEL#/ROMA0	I/O	3.3V (5V Tolerance)	Device Select / ROM Address [0] Device Select: driven by target to indicate it has decoded its address as the target of the current access.
FRAME#	I/O	3.3V (5V Tolerance)	Cycle Frame: driven by the current master to indicate the beginning and duration of an access.
GNT#[2:0]	O	3.3V (5V Tolerance)	PCI Bus Grant [2:0] from the SB600: indicates to the agent that access to the bus has been granted.
GNT3#/GPIO72	O	3.3V (5V Tolerance)	PCI Bus Grant 3 from SB600 / GPIO 72

Pin Name	Type	Voltage	Functional Description
GNT4#/GPIO73	I/O	3.3V (5V Tolerance)	PCI Bus Grant 4 from SB600 / GPIO 73
INT[H:E]#/GPIO[36:33]	I/O	3.3V (5V Tolerance)	PCI Interrupt [H:E] / GPIO [36:33]
IRDY#	I/O	3.3V (5V Tolerance)	Initiator Ready: indicates the initiating agent's ability to complete the current data phase of the transaction
LDRQ1#/GNT5#/GPIO68	I/O	3.3V (5V Tolerance)	Encoded DMA/Bus Master Request 1 / PCI bus Grant 5 from SB600 /GPIO 68
LOCK#	I/OD	3.3V (5V Tolerance)	PCI Bus Lock
PAR/ROMA[19]	I/O	3.3V (5V Tolerance)	PCI Bus Parity / ROM Address[19]
PCICLK[4:0]	O	3.3V (5V Tolerance)	33 MHz PCI clocks [4:0]
PCICLK5	O	3.3V (5V Tolerance)	33 MHz PCI clock 5 / LPC CLK 0
PCICLK6	O	3.3V (5V Tolerance)	33 MHz PCI clock 6 / LPC CLK 1
PCIRST#	O	3.3V (5V Tolerance)	Hardware Reset for PCI Slots Assertion: (a) at power on, (b) sometime after CPU_STP#'s assertion in S0, (c) after the system has transitioned into S4/S5. De-assertion: sometime after SB PWR_GOOD is asserted during power on or during a transition from S4/S5 to S0.
PERR#	I/O	3.3V (5V Tolerance)	Parity Error: reports data parity errors during all PCI transactions, except in a special cycle.
REQ#[2:0]	I	3.3V (5V Tolerance)	Request [2:0] Input: indicates that the agent desires use of the bus.
REQ3#/GPIO70	I	3.3V (5V Tolerance)	PCI Request 3 Input / GPIO 70
REQ4#/GPIO71	I	3.3V (5V Tolerance)	PCI Request 4 Input / GPIO 71
SERR#	I/OD	3.3V (5V Tolerance)	System Error: for reporting address parity errors and data parity errors on the special cycle command, or any other system error where the result will be catastrophic.
SPDIF_OUT/PCICLK7/GPIO41	I/O	3.3V (5V Tolerance)	SPDIF serial Out / 33 MHz PCI Clock 7 / GPIO 41
STOP#	I/O	3.3V (5V Tolerance)	Stop: indicates the current target is requesting the master to stop the current transaction
TRDY#/ROMOE#	I/O	3.3V (5V Tolerance)	Target Ready / ROM OE# Target Ready: indicates the target agent's ability to complete the current data phase of the transaction.

3.3 ATA66/100/133

Pin Name	Type	Voltage	Functional Description
IDE_IORDY	I	3.3V (5V Tolerance)	IDE IO Ready
IDE_IRQ	I	3.3V (5V Tolerance)	IDE Interrupt Request
IDE_A0	O	3.3V (5V Tolerance)	IDE Address bus bit 0
IDE_A1	O	3.3V (5V Tolerance)	IDE Address bus bit 1
IDE_A2	O	3.3V (5V Tolerance)	IDE Address bus bit 2
IDE_DACK#	O	3.3V (5V Tolerance)	IDE DMA Ack
IDE_DRQ	I	3.3V (5V Tolerance)	IDE DMA Request
IDE_IOR#	O	3.3V (5V Tolerance)	IDE IO Read
IDE_IOW#	O	3.3V (5V Tolerance)	IDE IO Write
IDE_CS1#	O	3.3V (5V Tolerance)	IDE chip select for I/O 1xxh address
IDE_CS3#	O	3.3V (5V Tolerance)	IDE chip select for I/O 3xxh address
IDE_D[15:0]/GPIO[30:15]	I/O	3.3V (5V Tolerance)	IDE data bus bit [15:0] / GPIO [30:15]

3.4 LPC Interface

Pin Name	Type	Voltage	Functional Description
GA20IN	I	3.3V (5V Tolerance)	A20 Gate Input from SIO
KBRST#	I	3.3V (5V Tolerance)	Keyboard reset#
LAD[3:0]	I/O	3.3V (5V Tolerance)	Multiplexed Command/Address/Data [3:0]
LFRAME#	O	3.3V (5V Tolerance)	Frame. Indicates start of a new cycle or termination of broken cycle.
LDRQ0#	I	3.3V (5V Tolerance)	Encoded DMA/Bus Master Request 0
LDRQ1#/GNT5#/GPIO68	I/O	3.3V (5V Tolerance)	Encoded DMA/Bus Master Request 1 / PCI bus Grant 5 from SB600 / GPIO 68
LPC_SMI#/EXTEVNT1#	I	3.3V (5V Tolerance)	LPC SMI / External Event 1
SERIRQ	I/O	3.3V (5V Tolerance)	Serial IRQ

3.5 USB Interface

Pin Name	Type	Voltage	Functional Description
USB_HSDP[9:0]+	I/O	AVDD_TX	USB Port 9 ~ 0 Positive I/O. See **Note**.
USB_HSDM[9:0]-	I/O	AVDD_TX	USB Port 9 ~ 0 Negative I/O
USBCLK	I	AVDDC	48MHz clock used for USB
USB_RCOMP	I	AVDDC	Compensating resistors input
USB_ATEST1	I/O	AVDD_TX	ATE Test Pin 1
USB_ATEST0	I/O	AVDD_TX	ATE Test Pin 0
USB_OC[4:0[#/GPM[4:0]#	I/O	S5_3.3V	USB Over Current [4:0] / GPM [4:0]
USB_OC5#/DDR3_RST#/GPM5#	I/O	S5_3.3V	USB Over Current 5 / DDR3 Memory Reset / GPM 5
USB_OC[7:6]#/ GEVENT[7:6]#	I/O	S5_3.3V	USB Over Current [7:6] / General Event [7:6]
USB_OC8#/AZ_DOCK_RST#/GPM8#	I/O	S5_3.3V	USB Over Current 8 / HD Audio Dock Reset / GPM 8
USB_OC9#/SLP_S2/GPM9#	I/O	S5_3.3V	USB Over Current 9 / Sleep S2 Indicator / GPM 9

Note: The USB_HSDP[9:0]+ and USB_HSDM[9:0]- signals are normally connected to the USB port connectors, in which case the USB ports are often handled by hand and the associated devices, connectors, or even the signal pins are subject directly to ESD events. The USB_HSDP+ and USB_HSDM- signals that may be exposed to the user through an USB port connection must have ESD protection. Please refer to the Product Advisory PA_SB600AU1 posted on the ORC for further details on ESD device specifications.

3.6 Serial ATA Interface

Pin Name	Type	Voltage	Functional Description
SATA_ACT#/GPIO67	OD	3.3V	SATA Channel Active / GPIO 67
SATA_CAL	I	1.2V (Filtered)	SATA Calibration
SATA_RX[3:0] -	I	1.2V (Filtered)	SATA Channel[3:0] Receive Negative
SATA_RX[3:0] +	I	1.2V (Filtered)	SATA Channel[3:0] Receive Positive
SATA_TX[3:0] -	O	1.2V (Filtered)	SATA Channel[3:0] Transmit Negative
SATA_TX[3:0] +	O	1.2V (Filtered)	SATA Channel[3:0] Transmit Positive
SATA_X1	I	3.3V (Filtered)	SATA Clock/Crystal Input.
SATA_X2	I	3.3V (Filtered)	SATA Crystal Input

Pin Name	Type	Voltage	Functional Description
SATA_IS0#/GPIO10	I/O	3.3V	SATA Interlock Switch Port 0 (Input) / GPIO 10
GHI#/SATA_IS1#/GPIO6	I/O	3.3V	GHI# output to CPU / SATA Interlock Switch Port 1 (Input) / GPIO 6
SMARTVOLT/SATA_IS2#/GPIO4	I/O	3.3V	Reduce system voltages / SATA Interlock Switch Port 2 (input) / GPIO 4
SSMUXSEL/SATA_IS3#/GPIO0	I/O	OD 3.3V (5V Tolerance)	SpeedStep Mux select (Output) / SATA Interlock Switch Port 3 (input) / GPIO0

Note: For each port there is a pin (SATA_IS) for sensing the status of the external interlock switch. If the motherboard implements SATA interlock switches, it should connect the statuses of the switches to those pins. The SB600 will sense the statuses of those pins and can generate a PME or interrupt when the states change. Normally, an inter-lock switch is required for supporting hot plug.

3.7 Power Management / North Bridge Interface

Pin Name	Type	Voltage	Functional Description
CPU_STP#/ DPSLP_3V#*	O	3.3V (5V Tolerance)	Stop CPU Clock [Intel] / Deep Sleep (3.3V) CPU_STP#: Stop CPU Clock [Intel]. Output to the external clock generator / NB to turn off the processor clock. It is used to support C3/C4 states and SpeedStep transitions. Assertion takes place at an interval (programmed by an SB register) after STPGNT message has been received by the system. De-assertion causes the NB or external clock generator to turn on the processor, and that takes place (a) in a sleep state: after a wake-up event is triggered; (b) in a C3/C4/SpeedStep transition: at a certain time interval after its own assertion. DPSLP_3V#: Deep Sleep (3.3V) [Banias/Dothan/Yonah platforms only]. This signal behaves identically with the CPU_STP# signal, only that it goes to the CPU directly (see **Note** below).
DPRSLPVR	O	3.3V	Deeper Sleep Voltage Regulator: [Intel] - Assertion causes the voltage regulator to output the lower "deeper sleep" core voltage to the CPU during C4 of S1-M states. Assertion takes place sometime after CPU_STP# is asserted. De-assertion causes the voltage regulator to output the normal CPU core voltage for the CPU to exit the C4 state. De-assertion takes place sometime after de-assertion of CPU_STP#
LPC_PME#/ GEVENT3#	I/O	S5_3.3V	LPC PME# Input / General Event 3
LPC_SMI#/ EXTEVNT1#	I/O	3.3V (5V tolerance)	LPC SMI# Input / External Event 1
PCI_PME#/ GEVENT4#	I/O	S5_3.3V	PCI PME# Input / General Event 4
DPSLP_OD#*/GPIO37	I/O	3.3V (5V Tolerance)	DPSLP_OD# / GPIO 37 DPSLP_OD#: Deep Sleep (Open Drain) [P4 platforms only]. Asserted by the SB600 to stop the processor's clock. This signal behaves identically with the CPU_STP#/DPSLP_3V# signal. This pin can also be used as GPIO 37.

Pin Name	Type	Voltage	Functional Description
PWR_BTN#	I	S5_3.3V	Power Button: The Power Button will cause an SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If PWRBTN# is pressed for more than 4 seconds, this will cause an unconditional transition (power button override) to the S5 state with only the PWRBTN# available as a wake event. Override will occur even if the system is in the S1 state. This signal has an internal pull-up resistor.
PWR_GOOD	I	S5_3.3V	SB power good input Assertion of PWR_GOOD by the SB power good circuit on the motherboard indicates that power supplies to the SB are valid. Assertion takes place sometime after NB Power Good is asserted. De-assertion of PWR_GOOD by the SB power good circuit indicates that the power supplies to the SB are NOT valid. De-assertion takes place sometime after SLP_S3# or SLP_S5#'s assertion, or after Power Supply Power Good is de-asserted.
RI#/EXTEVNT0#	I/O	S5_3.3V	Ring Indicator / External Event 0
SHUTDOWN#/GPIO5/ SMARTVOLT2	I/O	S0	System Shutdown / GPIO 5/SMARTVOLT2 System Shutdown: Assertion will cause the SB600 to assert SLP_S3# and SLP_S5# to force system to transition to S5 immediately, without waiting for the STPGNT message from the processor. SMARTVOLT2: Used for Smart power management
SLP_S3#	O	S5_3.3V	S3 Sleep Power plane control Assertion of SLP_S3# shuts off power to non-critical components when system transitions to S3, S4, or S5 states. Assertion takes place sometime after CPU_STP# is asserted. De-assertion of SLP_S3# turns on power to non-critical components when system transitions from S3, S4, or S5 back to S0. De-assertion takes place sometime after a wake-up event has been triggered.
SLP_S5#	O	S5_3.3V	S5 Sleep Power plane control - Assertion of SLP_S5# shuts power off to non-critical components when system transitions to S4 or S5 state. Assertion takes place sometime after CPU_STP# is asserted. De-assertion of SLP_S5# turns on power to non-critical components when transitioning from S4/S5 back to S0 state. De-assertion takes place sometime after a wake-up event is triggered.
SMBALERT#/ THRMTRIP#/ GEVENT2#	I/O	S5_3.3V	SMBus Alert / Thermal Trip / General Event 2 Thermal Trip: Signal indicates to the SB600 that a thermal trip has occurred. Its assertion will cause the SB600 to transition the system to S5 immediately, without waiting for the STPGNT message from the processor.

Pin Name	Type	Voltage	Functional Description
SUS_STAT#	OD	S5_3.3V	Suspend Status - Assertion by the SB600 indicates that the system will be entering a low-power state soon. The signal is monitored by those devices with memory that needs to switch from normal refresh to suspend refresh mode when the system transitions to a low-power state. Assertion takes place after the Stop Grant message from the CPU is received by the system. De-assertion by the SB600 indicates that the system is exiting a low power state now and is returning to S0. De-assertion timing for Intel platforms is as follows: (a) in S1: Following a wake-up event, after SLP# is de-asserted; (b) in S2/S3: Following a wake-up event, at a programmable interval after CPU_STP# is de-asserted; (c) in S4/S5: After a wake-up event is triggered. De-assertion for AMD platforms takes place after LDT_STP# is de-asserted.
TEMPIN3/ TALERT#/ GPIO64	I/O	3.3V	Temperature Monitor Input 3/ Thermal Alert / GPIO 64 Thermal Alert: The signal is a thermal alert to the SB600. SB600 can be programmed to generate an SMI#, SCI, or IRQ13 through GPE, or generate an SMI# without GPE in response to the signal's assertion. See the *SB600 Register Reference Manual* for details.
S3_STATE/GEVENT5#	I/O	S5_3.3V	K8 S3 State [AMD]: Assertion of S3_STATE by the SB600 indicates to the power supply that the system has transitioned into S3 state. Asserted after the Sleep S3 command is completed. De-assertion indicates that the system is leaving S3 state. De-assertion takes place after SUS_STAT# is de-asserted.
WAKE#/GEVENT8#	I/O	S5_3.3V	PCI Express Wake /General Event 8 WAKE# signal is required for PCI-E devices. The PCI-E interface is off the NB, but the ACPI WAKE# is controlled by SB. This signal is routed from the PCI-E device/slot to the SB. Note: the WAKE# is in S5 domain so it is active when the system is in S5 state. Care must be taken when plugging-in in the PCI-E devices: the system should be transitioned in to G3 state (S5 Power OFF) before a PCI-E device is installed. Plugging in a PCI-E device when the system is in S5 state may cause the system to wake up. That is because the WAKE# signal driven by the PCI-E device may transition momentarily to active state when the device is installed but has not been initialized to drive the signal in inactive state. (**Note:** Hot plugging of PCI-E devices is not supported in the PC architecture as, given the physical design of the interface, power will be interrupted during installation.)
USB_OC9#/SLP_S2/GPM9#	I/O	S5_3.3V	USB Over Current 9 / S2 Sleep Control / GPM9 S2 Sleep control: Assertion of SLP_S2 shuts off clocks when system transitions to S2 state, and it takes place sometime after CPU_STP# is asserted. De-assertion of SLP_S2 turns on clocks when system transitions from S2 back to S0, and it takes place sometime after a wake-up event has been triggered.

Pin Name	Type	Voltage	Functional Description
SLP#/LDT_STP#	OD [Intel]/ O [AMD]	CPU_PWR	Sleep [Intel] / LDT Stop [AMD] Sleep (Intel platforms only; not applicable to socket 775 platforms) - Assertion of SLP# causes the CPU to transition from Stop Grant state (C2) to Sleep state (C3/C4). The signal is also used during SpeedStep transitions. Assertion takes place at an interval (programmed by an SB register) after STPGNT message is received by the system. De-assertion of SLP# causes CPU to return from Sleep state (C3/C4) to Stop Grant state (C2). The signal is also used when bringing system from S1/S2/S3/S4/S5 back to S0. De-assertion takes place following a wake-up event: (a) in S1: at an interval (programmed by an SB register) after de-assertion of CPU_STP#; (b) in S2: after SLP_S2 is de-asserted; (c) in S3/S4/S5: after SLP_S3# is de-asserted; (d) in C3/C4, and during a SpeedStep transition: at an interval (programmed by an SB register) after de-assertion of CPU_STP#. LDT Stop [AMD] - Assertion of LDTSTOP_L on the CPU causes it to enter C3, or S1/S2/S3/S4/S5. Assertion takes place: (a) for S1/S2/S3/S4/S5: after SUS_STAT# is asserted; (b) for C3: after the STPGNT message is received by the system. De-assertion of LDTSTOP_L causes the CPU to return to C0 or S0 state. De-assertion takes place following a wake-up event: (a) in S1: at an interval (programmed by an SB register) after de-assertion of CPU_STP#; (b) in S2: after SLP_S2 is de-asserted; (c) in S3/S4/S5: after SB PWR_GOOD is asserted; (d) in C3: at an interval (programmed by an SB register)
STPCLK#/ ALLOW_LDTSTP	I/ O	CPU_PWR	Stop clock signal to CPU [Intel] / Allow LDT_STP# assertion [AMD] Stop Clock Signal to CPU [Intel]: Assertion of STPCLK# causes the CPU to issue a Stop Grant Acknowledge transaction and transition from the Normal (C0) sate to the Stop Grant state (C2). The assertion is initiated by software, during an ACPI or SpeedStep transition. De-assertion of STPCLK# brings the CPU back to the Normal (C0) sate. See Section 4.2 for detailed de-assertion timing. Allow LDT_STP# [AMD]: It is an input from NB to allow assertion of LDT_STOP#. When ALLOW_LDTSTP is de-asserted, SB600 cannot assert LDT_STOP#. ALLOW_LDTSTP can be used to implement stutter mode operation for the CPU.

* **Note:** DPSLP_3V# and DPSLP_OD# are the same signal, with the former being a push-pull and the latter an open drain signal. Either one or both of them can be used to implement the Deep Sleep function of the CPU. However, for output to a logic that does not have 3.3V input, using DPSLP_OD# will eliminate the need for a level shifter.

3.8 Processor Interface

Pin name	Type	Voltage	Functional Description
A20M#/SID	O	CPU_PWR	A20 mask [Intel] / SI Data [AMD], open-drain
CPU_PG/LDT_PG	O	CPU_PWR	Power Good to CPU [Intel] / LDT Power Good [AMD]
CPU_PWR	I	CPU_PWR	CPU I/O Voltage
FERR#	I	CPU_PWR	Floating Point Error pending at CPU [Intel]
IGNNE#/SIC	O	CPU_PWR	Ignore Numeric Exception [Intel] / SI Clock [AMD], open-drain
INIT#	O	CPU_PWR	CPU Initialization [Intel]
INTR/LINT0	O	CPU_PWR	INTR pin [Intel] / Interrupt signal to CPU's LINT0
LDT_RST#/DPRSTP#/ PROCHOT#	I/O	CPU_PWR	LDT Reset# [AMD] / CPU Deeper Stop# [Intel Yonah] / Processor Hot [Intel non-Yonah] LDT Reset# (AMD; 2.5V): Reset signal to the CPU. Assertion of LDT_RST# causes the CPU to transition into a low power state and to de-assert MEMCLKEA/B and assert MEMREST_L. Assertion of LDT_RST# takes place sometime after SB PWRGOOD has been de-asserted. De-assertion of LDT_RST# allows MEMRESET_L to be de-asserted and MEMCLK to be enabled. De-assertion of LDT_RST# takes place sometime after SB PWR_GOOD has been asserted. CPU Deeper Stop# [Intel Yonah]: Inverted DPRSLPVR Assertion takes place sometime after CPU_STP# is asserted. De-assertion takes place sometime after de-assertion of CPU_STP# Processor Hot [Intel, non-Yonah): Similar to TALERT#
NMI/LINT1	O	CPU_PWR	NMI pin[Intel] / Non Maskable Interrupt to CPU's LINT1
SMI#	O	CPU_PWR	System Management Interrupt to CPU [Intel]

3.9 SMBUS Interface / General Purpose Open Collector

Pin Name	Type	Voltage	Functional Description
SCL0/GPOC0# *	I/O	3.3V (5V Tolerance)	SMBus Clock 0 / General Purpose Open Collector 0
SDA0/GPOC1# *	I/O	3.3V (5V Tolerance)	SMBus Data 0 / General Purpose Open Collector 1
SCL1/GPOC2# *	I/O	S5_3.3V (to support ASF)	SMBus Clock 1 / General Purpose Open Collector 2
SDA1/GPOC3# *	I/O	S5_3.3V (to support ASF)	SMBus Data 1 / General Purpose Open Collector 3
SMBALERT#/ THRMTRIP#/ GEVENT2#	I/O	S5_3.3V	SMBus Alert# / Thermal Trip / General Event 2 SM Bus Alert: This signal is used to wake the system or generate an SMI#. If not used for SMBALERT#, it can be used for thermal trip or as a GEVENT.

*** Note:** SDA1 And SCL1 SMbus interface is dedicated for ASF devices only. It should not be used to connect to any other devices.

3.10 Real Time Clock Interface

Pin Name	Type	Voltage	Functional Description
RTC_GND	—	Analog GND	RTC Analog Ground
RTC_IRQ#/GPIO69	I/O	S5_3.3V/VBAT	RTC Interrupt / GPIO 69
RTCCLK	I/O	S5_3.3V/VBAT	32 kHz input for external RTC / 32 kHz output for internal RTC
VBAT	I	S5_3.3V/VBAT	RTC battery supply
X1	I	S5_3.3V/VBAT	RTC crystal oscillator input 1 (internal RTC)
X2	O	S5_3.3V/VBAT	RTC crystal oscillator input 2 (internal RTC)

3.11 Reset / Clocks / ATE

Pin Name	Type	Voltage	Functional Description
A_RST#	O	3.3V (5V Tolerance)	PCI Host Bus Reset. Asserted during transition to S3/S4/S5 to reset all devices in the SB600 or connected to it, except the ACPI logic in the SB600
14M_OSC	I	3.3V	14.318 MHz clock
RSMRST#	I	S5_3.3V	Resume Reset from Motherboard – Assertion of RSMRST# resets all SB600 registers to their default values. It also causes all reset signals originating from the SB600 (A_RST#, PCIRST#, LDT_RST#, AZ_RST#, AC_RST#) to be issued. RSRMT# should be asserted when system power is being applied. Type-I straps are captured on the rising edge of RSRMT# during its de-assertion. RSMRST# should be de-asserted sometime after S5 power is up, and should stay de-asserted until system power is removed.
SYS_RESET#/GPM7#	I/O	S5_3.3V	System Reset / GPM 7 System Reset: Signal coming from the power button circuit signaling a reset for the system. On receiving the signal, the SB600 asserts all reset signals that originate from the SB600 including: A_RST#, PCIRST#, LDT_RST#, AZ_RST#, and AC_RST#; it also resets all SB600 registers to their default values.
TEST0	I	S5_3.3V	ATE Test 0
TEST1	I	S5_3.3V	ATE Test 1
TEST2	I	S5_3.3V	ATE Test 2

3.12 General Purpose I/O

The GPIO pins of the SB600 are multiplexed with other functions. For information on how to configure the GPIO pins for the desired functions, see the *SB600 Register Reference Manual (OEM).*

The table below lists all the GPIO pins on the SB600. The Default Type column shows the state of the pin (default function) after de-assertion of the PCI host bus reset (A_RST#), which happens after power up or after system reset. Signals that are in input state after reset will be tri-state (TS) if they do not have any internal PU (pull up) or PD (Pull Down). For pins that have PU or PD internally, their states after reset will depend on the PU or PD: for signals with PU, the state will be HIGH and for signals with PD the state will be LOW. The PU and PD shown are enabled by default after PCI Reset and can be disabled by System BIOS.

Pin Name (Default function* in blue)	Type	Voltage	Power Domain	Default Type*	Functional Description
SSMUXSEL/ SATA_IS3#/GPIO0	I/OD	3.3V(5V Tolerance)	S0	Output (Low)	SpeedStep™ (GV1 only) Mux select / Serial ATA Interlock Switch Port 3 / GPIO 0
ROM_CS#/**GPIO1****	I/O	3.3V(5V Tolerance)	S0	Output (High) or Input (PU), depending on strapping	ROM Chip Enable / GPIO 1
SPKR/**GPIO2**	I/O	3.3V(5V Tolerance)	S0	Input (TS)	Speaker / GPIO 2
FANOUT0/**GPIO3**	I/O	3.3V(5V Tolerance)	S0	Input (PU)	Fan PWM Output 0 / GPIO 3
SMARTVOLT/ SATA_IS2#/**GPIO4**	I/O	3.3V(5V Tolerance)	S0	Input (TS)	SmartVoltage Select / Serial ATA Interlock Switch Port 2 / GPIO 4
SHUTDOWN#/**GPIO5**/SMARTVOLT2	I/O	3.3V(5V Tolerance)	S0	Input (TS)	System Shutdown / GPIO 5/SMARTVOLT2
GHI#/SATA_IS1#/GPIO6	I/OD	3.3V(5V Tolerance)	S0	Output (TS)	GHI# output to CPU (GV1 only)/ Serial ATA Interlock Switch Port 1 / GPIO 6
WD_PWRGD/**GPIO7*** **	I/O	3.3V(5V Tolerance)	S0	Output (High) or Input (TS), depending on strapping	Watchdog Power Good for NB / GPIO 7
DDC1_SDA/**GPIO8**	I/O	3.3V(5V Tolerance)	S0	Input (TS)	DDC1 Serial Data / GPIO 8
DDC1_SCL/**GPIO9**	I/O	3.3V(5V Tolerance)	S0	Input (TS)	DDC1 Serial Control / GPIO 9
SATA_IS0#/**GPIO10**	I/O	3.3V(5V Tolerance)	S0	Input (TS)	Serial ATA Interlock Switch Port 0 / GPIO 10
SPI_DO/GPIO11	I/O	S5_3.3V	S5	Input (PD)	SPI ROM Data Out / GPIO 11
SPI_DI/GPIO12	I/O	S5_3.3V	S5	Input (PD)	SPI ROM Data In / GPIO 12
LAN_RST#/GPIO13	O	3.3V(5V Tolerance)	S0	Output (Low)	LAN Reset / GPIO 13
ROM_RST#/GPIO14 ◊	I/O	3.3V(5V Tolerance)	S0	Output (Low)	ROM Reset ◊ / GPIO 14
IDE_D[15:0]/GPIO[30:15]	I/O	3.3V(5V Tolerance)	S0	Output (High)	IDE data [15:0] / GPIO [30:15]
SPI_HOLD#/GPIO31	I/O	S5_3.3V	S5	Input (PU)	SPI ROM Hold / GPIO 31
SPI_CS#/GPIO32	I/O	S5_3.3V	S5	Input (PU)	SPI ROM Chip Select / GPIO 32
INTE#/GPIO33	I/O	3.3V(5V Tolerance)	S0	Input (PU)	PCI Interrupt E / GPIO 33
INTF#/GPIO34	I/O	3.3V(5V Tolerance)	S0	Input (PU)	PCI Interrupt F / GPIO 34
INTG#/GPIO35	I/O	3.3V(5V Tolerance)	S0	Input (PU)	PCI Interrupt G / GPIO 35
INTH#/GPIO36	I/O	3.3V(5V Tolerance)	S0	Input (PU)	PCI Interrupt H / GPIO 36
DPSLP_OD#/GPIO37	I/O	3.3V(5V Tolerance)	S0	Output (TS)	Deep Sleep (Open Drain) / GPIO 37
AC_BITCLK/GPIO38	I/O	3.3V(5V Tolerance)	S0	Input (PD)	AC '97 Bit Clock / GPIO 38
AC_SDOUT/GPIO39	I/O	3.3V(5V Tolerance)	S0	Output (Low)	AC '97 Serial Data Out / GPIO 39
AC_SYNC/GPIO40	I/O	3.3V(5V Tolerance)	S0	Output (Low)	AC '97 Sync / GPIO 40

Pin Name (Default function* in blue)	Type	Voltage	Power Domain	Default Type*	Functional Description
SPDIF_OUT/ PCICLK7/GPIO41	I/O	3.3V(5V Tolerance)	S0	Output (Low)	SPDIF Serial Output / 33MHz PCI Clock 7 / GPIO41
ACZ_SDIN[2:0]/ GPIO[44:42]	I/O	S5_3.3V	S5	Input (PD)	AC '97 or HD Audio Serial Data In [2:0] / GPIO[44:42]
AC_RST#/GPIO45	I/O	S5_3.3V	S5	Output (Low)	AC '97 RESET# / GPIO45
AZ_SDIN3/GPIO46	I/O	S5_3.3V	S5	Input (PD)	HD Audio Serial Data In 3 / GPIO46
SPI_CLK/GPIO47	I/O	S5_3.3V	S5	Input (PD)	SPI ROM Clock / GPIO 47
FANOUT[2:1]/**GPIO[49:48]**	I/O	3.3V	S0	Input (PU)	Fan PWM Output [2:1] / GPIO [49:48]
FANIN[2:0]/**GPIO[52:50]**	I/O	3.3V	S0	Input (TS)	Fan Tachometer Input [2:0] / GPIO [52:50]
VIN[7:0]/**GPIO[60:53]**	I/O	3.3V	S0	Input (TS)	Voltage Input [7:0] / GPIO [60:53]
TEMPIN[2:0]/**GPIO[63:61]**	I/O	3.3V	S0	Input (TS)	Temperature Monitor Input [2:0] / GPIO [63:61]
TEMPIN3/TALERT#/ **GPIO64**	I/O	3.3V	S0	Input (TS)	Temperature Monitor Input 3 / Temperature Alert / GPIO64
BMREQ#/REQ5#/ **GPIO65**	I/O	3.3V	S0	Input (TS)	Bus Master Request / PCI Request 5 (Output) / GPIO 65
LLB#/**GPIO66**	I/O	S5_3.3V	S5	Input (PU)	Low-Low Battery / GPIO 66
SATA_ACT#/GPIO67	OD	3.3V	S0	Output (TS)	Serial ATA Activity / GPIO 67
LDRQ1#/GNT5#/ **GPIO68¤**	I/O	3.3V(5V Tolerance)	S0	Input (PU)	LPC DMA Req 1 / PCI Grant 5 / GPIO 68¤
RTC_IRQ#/**GPIO69†**	I/O	S5_3.3V/V BAT	S5	Input (PU)	RTC Interrupt / GPIO 69
REQ[4:3]#/GPIO[71:70]	I/O	3.3V(5V Tolerance)	S0	Input (PU)	PCI Request [4:3] (Input) / GPIO [71:70]
GNT[4:3]#/GPIO[73:72]	I/O	3.3V(5V Tolerance)	S0	Output (TS)	PCI Grant [4:3] / GPIO [73:72]

Notes: * The "default function" and the "default type" refer to function and type of the pin after de-assertion of PCI host bus reset (A_RST#), i.e., right after system power up or reset.
** ROM_CS# is the default function when the SB600 is strapped to use a PCI ROM (**PCI ROM is not supported for ASIC revision A21 and onwards**).
*** The function of WD_PWRGD (Watchdog Power Good) has not been qualified. This ball should only be used as GPIO7.
◊ PCI ROM is not supported for ASIC revision A21 and onwards, for which the default function of the pin is thus GPIO14.
¤ The GPIO68 and GNT5# functions are not present in ASIC versions A11-A13. In those versions, the default function is therefore LPC DMA Req 1#.
† RTC_IRQ# is the default function when the SB600 is strapped for external RTC mode.

3.13 External Event / General Event / General Power Management / General Purpose Open Collector

The EXTEVENT/GEVENT/GPM/GPOC pins of the SB600 are multiplexed with other functions. For information on how to configure the EXTEVENT/GEVENT/GPM/ GPOC pins for the desired functions, see the *SB600 Register Reference Manual (OEM).*

The table below lists all the EXTEVENT/GEVENT/GPM/GPOC pins on the SB600. The Default Type column shows the state of the pin (default function) after de-assertion of the PCI host bus reset (A_RST#), which happens after power up or after system reset. Signals that are in input state after reset

will be tri-state (TS) if they do not have any internal PU (pull up) or PD (Pull Down). For pins that have PU or PD internally, their states after reset will depend on the PU or PD: for signals with PU, the state will be HIGH and for signals with PD the state will be LOW. The PU and PD shown are enabled by default after PCI Reset and can be disabled by System BIOS.

Pin Name (Default function in blue)	Type	Voltage	Power Domain	Default Type	Functional Description
RI#/**EXTEVENT0#**	I/O	S5_3.3V	S5	Input (PU)	Ring Indicator / External Event 0
LPC_SMI#/ **EXTEVENT1#**	I/O	3.3V(5V Tolerance)	S0	Input (PU)	LPC SMI / External Event 1
SMBALERT#/**THRMTRIP#**/GEVENT2#	I/O	S5_3.3V	S5	Input (PU)	SM Bus Alert / Thermal Trip / General Event 2
LPC_PME#/ **GEVENT3#**	I/O	S5_3.3V	S5	Input (PU)	LPC PME (Input) / General Event 3
PCI_PME#/ **GEVENT4#**	I/O	S5_3.3V	S5	Input (PU)	PCI PME (Input) / General Event 4
S3_STATE/ **GEVENT5#** *	I/O	S5_3.3V	S5	Output (Low) or Input (PU), depending on strapping	AMD S3 State / General Event 5 See **Note 1** below.
USB_OC[7:6]#/ **GEVENT[7:6]#**	I/O	S5_3.3V	S5	Input (PU)	USB Over Current [7:6] / General Event [7:6]
WAKE#/**GEVENT8#**	I/O	S5_3.3V	S5	Input (PU)	PCI Express Wake / General Event 8
USB_OC[4:0]#/**GPM[4:0]#**	I/O	S5_3.3V	S5	Input (PU)	USB Over Current [4:0] / GPM [4:0]
USB_OC5#/DDR3_RST#/**GPM5#**	I/O/ OD	S5_3.3V	S5	Output (Low)	USB Over Current 5 / DDR3 Memory Reset / GPM 5
BLINK/**GPM6#**	I/O	S5_3.3V	S5	Input (PU)	LED Blink / GPM 6
SYS_RESET#/ **GPM7#**	I/O	S5_3.3V	S5	Input (PU)	System Reset / GPM 7
USB_OC8#/ AZ_DOCK_RST#/ **GPM8#**	I/O	S5_3.3V	S5	Input (PU)	USB Over Current 8 / HD Audio Dock Reset / GPM 8
USB_OC9#/SLP_S2/ **GPM9#**	I/O	S5_3.3V	S5	Input (PD)	USB Over Current 9 / Sleep S2 Indicator / GPM 9
SCL0/**GPOC0#**	I/O	3.3V(5V Tolerance)	S0	Input (TS)	SMBUS Clock 0 / General Purpose Open Collector 0
SDA0/**GPOC1#**	I/O	3.3V(5V Tolerance)	S0	Input (TS)	SMBUS Data 0 / General Purpose Open Collector 1
SCL1/**GPOC2#** **	I/O	S5_3.3V (to support ASF)	S5	Input (TS)	SMBUS Clock 1 (ASF) / General Purpose Open Collector 2 See **Note 2** below.
SDA1/**GPOC3#** **	I/O	S5_3.3V (to support ASF)	S5	Input (TS)	SMBUS Data 1 (ASF) / General Purpose Open Collector 3 See **Note 2** below.

*** Note 1:** S3_STATE is the default function when the SB600 is strapped for AMD CPU mode. If strapped for Intel CPU mode(GEVENT5#), default is Input (PU) for SB600 A11-A13 and Input (TS) for SB600 A21 and onwards.
**** Note 2:** SDA1 And SCL1 SMbus interface is dedicated for ASF devices only. It should not be used to connect to any other devices.

3.14 AC ’97 Link Interface

Pin Name	Type	Voltage	Functional Description
AC_BITCLK/GPIO38	I	3.3V (5V Tolerance)	AC ‘97 Interface Bit Clock / GPIO 38
AC_RST#/GPIO45	OD/ I	S5_3.3V	AC ’97 Interface Reset (OD) / GPIO45
ACZ_SDIN[2:0]/GPIO[44:42]	I/O	S5_3.3V	AC ‘97/HD Audio Serial Data Input from Codec [2:0] / GPIO [44:42]
AC_SDOUT/GPIO39	I/O	3.3V (5V Tolerance)	AC ‘97 Serial Data Output to Codec / GPIO 39
AC_SYNC/GPIO40	I/O	3.3V (5V Tolerance)	AC ‘97 Sync signal to Codec / GPIO40
SPDIF_OUT/PCICLK7/GPIO41	I/O	3.3V (5V Tolerance)	SPDIF Serial Output / 33MHz PCI Clock 7 / GPIO41

3.15 HD Audio Interface

Pin Name	Type	Voltage	Functional description
AZ_BITCLK	O	3.3V	HD Audio Interface Bit Clock
AZ_RST#	O	S5_3.3V	HD Audio interface Reset
ACZ_SDIN[2:0]/GPIO[44:42]	I/O	S5_3.3V	AC ‘97/HD Audio Serial Data Input from Codec [2:0] / GPIO [44:42]
AZ_SDIN3/GPIO46	I/O	S5_3.3V	HD Audio Serial Data Input from Codec 3/ GPIO 46
AZ_SDOUT	O	3.3V	HD Audio Serial Data Output to Codec
AZ_SYNC	O	3.3V	HD Audio Sync signal to Codec

3.16 XBUS ROM Access Interface

Note: XBUS Rom is **not** supported for ASIC revision A21 and onwards.

Pin Name	Type	Voltage	Functional Description
AD[15:0]/ROMA[18:11, 9:2]	I/O	3.3V (5V Tolerance)	PCI Bus Address/Data [15:0] / ROM Address [18:11, 9:2]
AD[23:16]/ROMD[7:0]	I/O	3.3V (5V Tolerance)	PCI Bus Address/Data [23:16] / ROM Data [7:0]
CBE0#/ROMA10	I/O	3.3V (5V Tolerance)	Command/Byte Enable[0] / ROM Address [10]
CBE1#/ROMA1	I/O	3.3V (5V Tolerance)	Command/Byte Enable[1] / ROM Address [1]
CBE2#/ROMWE#	I/O	3.3V (5V Tolerance)	Command/Byte Enable[2] / ROM WE #
DEVSEL#/ROMA0	I/O	3.3V (5V Tolerance)	Device Select / ROM Address [0]
PAR/ROMA19	I/O	3.3V (5V Tolerance)	PCI Bus PAR/ROM Address[19]
ROM_CS# / GPIO1	I/O	3.3V (5V Tolerance)	ROM chip enable; GPIO1

3.17 SPI ROM Interface

SPI ROM is supported up to 33 MHz. The burst read and fast read cycles are not supported.

Pin Name	Type	Voltage	Functional Description
SPI_DI/GPIO12	I/O	S5_3.3V	SPI Data In / GPIO 12
SPI_DO/GPIO11	I/O	S5_3.3V	SPI Data Output / GPIO 11
SPI_CLK/GPIO47	I/O	S5_3.3V	SPI Clock / GPIO 47
SPI_HOLD#/GPIO31	I/O	S5_3.3V	SPI HOLD# / GPIO 31
SPI_CS#/GPIO32	I/O	S5_3.3V	SPI Chip Select# / GPIO 32

3.18 Hardware Monitor

Pin Name	Type	Voltage	Functional Description
FANO0/GPIO3	I/O	3.3V (5V Tolerance)	Fan PWM Output 0 / GPIO 3
FANO1/GPIO48	I/O	3.3V (5V Tolerance)	Fan PWM Output 1 / GPIO 48
FANO2/GPIO49	I/O	3.3V (5V Tolerance)	Fan PWM Output 2 / GPIO 49
FANIN0/GPIO50	I/O	3.3V (5V Tolerance)	Fan Tachometer Input 0 / GPIO 50
FANIN1/GPIO51	I/O	3.3V(5V Tolerance)	Fan Tachometer Input 1 / GPIO 51
FANIN2/GPIO52	I/O	3.3V(5V Tolerance)	Fan Tachometer Input 2 / GPIO 52
TEMP_COMM	I	(Analog GND)	Temperature sensor diode current return path.
TEMPIN0/GPIO61	I/O	3.3V	Temperature Monitor Input 0 / GPIO 61
TEMPIN1/GPIO62	I/O	3.3V	Temperature Monitor Input 1 / GPIO 62
TEMPIN2/GPIO63	I/O	3.3V	Temperature Monitor Input 2 / GPIO 63
TEMPIN3/TALERT#/GPIO64	I/O	3.3V	Temperature Monitor Input 3 / Temperature has reached cautionary state / GPIO 64
VIN0/GPIO53	I/O	3.3V	Voltage Monitor Input 0 / GPIO 53
VIN1/GPIO54	I/O	3.3V	Voltage Monitor Input 1 / GPIO 54
VIN2/GPIO55	I/O	3.3V	Voltage Monitor Input 2 / GPIO 55
VIN3/GPIO56	I/O	3.3V	Voltage Monitor Input 3 / GPIO 56
VIN4/GPIO57	I/O	3.3V	Voltage Monitor Input 4 / GPIO 57
VIN5/GPIO58	I/O	3.3V	Voltage Monitor Input 5 / GPIO 58
VIN6/GPIO59	I/O	3.3V	Voltage Monitor Input 6 / GPIO 59
VIN7/GPIO60	I/O	3.3V	Voltage Monitor Input 7 / GPIO 60
AVDD	-	3.3V (Analog Power)	Hardware Monitor Analog PWR
AVSS	-	Analog Ground	Hardware Monitor Analog GND

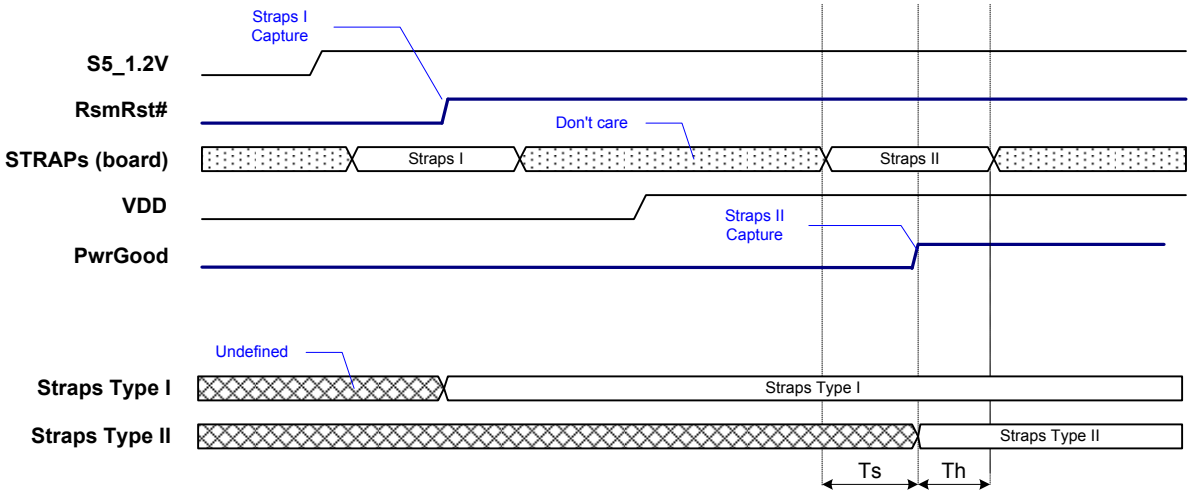
3.19 Power and Ground

Signal Name	Voltage/ Ground	ACPI STATE	GND reference	Note	Description
VDD_[12:1]	1.2V	S0-S2	VSS	-	Core power
VDDQ_[28:1]	3.3V	S0-S2	VSS	-	3.3V I/O Power
S5_1.2V_[4:1]	1.2V	S0-S5	VSS		1.2V S5 Power
S5_3.3V_[6:1]	S5_3.3V	S0-S5	VSS	-	3.3V S5 Power
AVDDCK_3.3V	3.3V	S0-S2	AVSSCK	1	3.3V power for analog PLLs
AVDDCK_1.2V	1.2V	S0-S2	AVSSCK		1.2V power for analog PLLs
PCIE_PVDD	1.2V	S0-S2	PCIE_VSS	1	A-Link Express II PLL Power
PCIE_VDDR[13:1]	1.2V	S0-S2	PCIE_VSS	1	A-Link Express II Analog power
AVDD_SATA[15:1]	1.2V	S0-S2	AVSS_SATA	1	SATA Analog Power
PLLVDD_SATA_[2:1]	1.2V	S0-S2	AVSS_SATA	1	SATA PLL Power
XTLVDD_SATA	3.3V	S0-S2	AVSS_SATA	1	SATA XTAL Power
VBAT	2.5 - 3.6V BAT	-	RTC_GND	-	RTC backup power
AVDDC	S5_3.3V	S0-S5 / S0-S3	AVSSC	1, 2	Analog Power for USB PHY PLL
AVDDRX[4:0]	S5_3.3V	S0-S5 / S0-S3	AVSS_USB	1, 2	Analog Power for USB PHY RX
AVDDTX[4:0]	S5_3.3V	S0-S5 / S0-S3	AVSS_USB	1, 2	Analog Power for USB PHY TX
USB_PHY_1.2V[5:1]	1.2V	S0-S5 / S0-S3	AVSS_USB	2	1.2V USB PHY standby Power
V5_VREF	5V	S0-S2	VSS	-	5V Reference voltage for PCI interface
CPU_PWR	CPU I/O Voltage	S0-S2	VSS	3	CPU I/O reference voltage
VSS_[57:1]	GND	-	-	-	Digital Ground
AVSSCK	GND	-	-	-	Common ground for analog PLLs
PCIE_PVSS	GND	-	-	-	A-Link Express II PLL Ground
PCIE_VSS[42:1]	GND	-	-	-	A-Link Express II Analog Ground
AVSS_SATA[27:1]	GND	-	-	-	SATA Analog Ground (Plane)
RTC_GND	Analog GND	-	-	-	RTC Analog Ground
AVSSC	GND	-	-	-	Analog Ground for USB PHY PLL.
AVSS_USB_[33:1]	GND_USB	-	-	-	Analog Ground for USB PHY

Note 1: These power rails should be filtered.
Note 2: These power rails can be tied to S0-S5 or S0-S3 power.
Note 3: CPU_PWR is 2.5V/1.8V for AMD platforms, and is CPU_PWR for Intel platforms.

3.20 Pin Straps

Straps are captured on the rising edge of RSMRST# and PWR_GOOD. There are two kinds of straps: Type I and Type II. Type I straps become valid immediately after capture on the rising edge of RSMRST#. This type of strap is used by modules in the S5 power well and is therefore captured only once, when power is first applied to the chip. All other straps (type II) become valid after PWR_GOOD is asserted in order to prevent the strap logic that resides in the standby power well from being driven by un-powered logic. Type II straps are captured every time the systems powers up from the S5 state. Transition from S3 to S0 does not trigger capture.



T	*Parameter*	*Min*	*Max*	*Unit*
Ts	Setup Time for capture	0		ns
Th	Hold Time for capture		1310.5	ns

Figure 3-1: Straps Capture

Straps are classified into two groups: Standard and Debug. Standard straps are required for selecting different chip options at power-up. Debug straps are used for debugging purposes only. Debug straps are not required to be populated for production boards. However, there should be provisions for connecting PUs or PDs on the debug strap signals if they are not used for normal system operation.

The *Description* column in *Table 3-1* and *Table 3-2* shows the function of every strap signal in the design. All straps are defined such that in the most likely scenario of operation, they will be set to the recommended (or safest) values. The values shown in the Description column are the external board strap values, with 3.3V being a pull-up and 0V a pull-down.

Table 3-1: Standard Straps

Pad Name	Strap Name	Type	Description
AC_SDOUT/ GPIO39	DefaultMode	**II**	Enable/Disable additional straps for debugging (see *Table 3-2*) 0V – Use hardcoded defaults for Debug Straps (**Default**) 3.3V – Enable additional Debug Straps

<table>
<tr><th>Pad Name</th><th>Strap Name</th><th>Type</th><th>Description</th></tr>
<tr><td>{ PCICLK1,
PCICLK0 }</td><td>{ ROMTYPE_1,
ROMTYPE_0 }</td><td>II</td><td>
<table>
<tr><td>ROMTYPE_1</td><td>ROMTYPE_0</td><td>ROM Type</td></tr>
<tr><td>3.3V</td><td>0V</td><td>LPC ROM (default)
(Supports both LPC and PMC ROM types)</td></tr>
<tr><td>3.3V</td><td>3.3V</td><td>PCI (X Bus) ROM
(Not supported for ASIC revision A21 and onwards.)</td></tr>
<tr><td>0V</td><td>0V</td><td>Firmware Hub</td></tr>
<tr><td>0V</td><td>3.3V</td><td>SPI ROM</td></tr>
</table>
</td></tr>
<tr><td>PCICLK6</td><td>CPU_Type</td><td>II</td><td>Defines the type of CPU
0V – Intel processors (default for Intel platform)
3.3V – AMD K8 processors (default for AMD platform</td></tr>
<tr><td>PCICLK4</td><td>SelUsbPll48</td><td>II</td><td>Select 48MHz USB clock or internal PLL
0V – Use external 48MHz clock (Default)
3.3V – Use internal PLL48</td></tr>
</table>

Table 3-2: Debug Straps

Pad Name	Strap Name	Type	Description
AD [28]	ShortReset	II	Generate a short reset 0V – Use short reset (reserved, do not use) 3.3V – Use long reset (**Default**) (Internal PU of 15kΩ)
AD [27]	PciPllByp	II	Bypass PCI PLL 0V – Bypass internal PLL clock . Use REQ3# as A-Link bypass clock Use GNT3# as B-Link bypass clock 3.3V – Use internal PLL-generated PLL CLK (**Default**) (Internal PU of 15kΩ)
AD[26]	AcpiBClkByP	II	Bypass ACPI_BCLK 0V – Bypass internal generated acpi_bclk. GNT0# as acpi_bclk bypass clock. 3.3 V – Use internal generated acpi_bclk (**Default**) (Internal PU of 15kΩ)
AD[25]	IdeClkByP	II	Bypass IDE CLK 0 V – Bypass internal Ide Clk Use GNT2# as Ide 66Mhz bypass clock. Use REQ2# as Ide 50Mhz bypass clock. Use REQ1# as Ide 33Mhz bypass clock. 3.3 V – Use internal PLL Ide Clk (**Default**) (Internal PU of 15kΩ).
AD[24]	I2CRomEn	II	A-Link Express-II core strap from I2C ROM enable 0V – Getting the value from I2C EPROM. I2C EPROM ADDRESS set to all zeroes. Use GNT4# as SDA Use REQ4# as SCL. 3.3 V – Use default value (**Default**) (Internal PU of 15kΩ)

Pad Name	Strap Name	Type	Description
AD[23]	BootFailTimerEn	**II**	BootFail Timer Enable 0V – Enable BootFail Timer 3.3V – Use default value (BootFail Timer off) (**Default**) (Internal PU resistor -15kΩ)

Table 3-3: Additional Straps

The following strap is not captured by the straps logic, but is required to set the correct RTC mode.

Pad Name	Strap Name	Description
RTCCLK	—	If a clock is applied to this pin and X1 is terminated, the chip will be set to external RTC mode. If this pin is pulled-up to S5_3.3V and a crystal is put on X1/X2, the chip will be set to internal RTC (**Default**)

4 Power Planes and Pin States

4.1 Power Up and Down Sequences

Simple diagrams of the SB600 power up sequences for both the Intel and AMD platforms are shown in *Figure 4-1* through *Figure 4-4* below. A power detection circuit is integrated into the SB600. This circuit will monitor SB PWRGD and will assert A_RST# (and LDT_RST# too on K8-based platforms) for as long as SB PWRGD is false. After SB PWRGD has been asserted, A_RST# (followed by LDT_RST# on K8-based platforms), will be de-asserted. Note that INIT# (to the CPU) is not asserted during the power up sequence *Table 4-1* shows the timing requirements referenced in *Figure 4-1* through *Figure 4-4*. Besides the illustrated requirements, it is also required that the ramp time for any rail be less than 40ms.

Table 4-1: SB600 Power Up/Down Sequence Timing

Symbol	Min.	Max.	Description
T1	**Note 1**		3.3V(S5) to 1.2V(S5)
T2	10 ms	–	S5 power to resume reset (RSM_RST#)
T2A	–	50 ms	Resume reset (RSM_RST#) rise time (10% to 90%). SB600 has a Schmitt trigger input with debouncing logic on this pin, so the value is relaxed relative to earlier ATI SB designs.
T3	31 ms	–	RSMRST# de-asserted to start of RTC Clock Out from pin D3 on SB600.
T6	**Note 15**		VRM_PG to NB_PWRGD / CORE_PWRGD to NB_PWRGD
T7	-22 ms	500 ms	NB Power Good to SB_PWRGD. SB_PWRGD should be qualified by 3.3V(S0), +1.2V(S0) at 90%, and Power Supply PWROK. The NB and SB are targeted to use the same Power Good signal. The time difference between Power Good and system reset's de-assertion is ~ 72ms. The NB requires 50ms, and that leaves ~22ms for the minimum lag between the NB and SB Power Goods. The 500ms maximum is an arbitrary number.
T7A	–	50 ms	SB_PWRGD rise time (10% to 90 %). See **Note 3**. SB600 has a Schmitt trigger with de-bouncing logic on this pin, so the value is relaxed relative to earlier ATI SB designs.
T7B	–	1 ms	SB_PWRGD fall time.
T8	47 ms	66 ms	SB_PWRGD to CPU_PG. CPU_PWRGD is driven by SB600
T8A	0 ns **Note 4**	100 ns	A_RST# (PCI host bus reset) to PCIRST#
T8B	–	**Note 5**	KB_RST# to A_RST#
T8C	1.9 ms	2.1 ms	PCIRST# to LDT_RST# (AMD Only) See **Note 14.**
T8D	47 ms	66 ms	SB_PWRGD to LDT_PG(AMD Only)
T9	71 ms	73 ms	SB_PWRGD to PCI_RST#
T9A	71ms	73 ms	SB_PWRGD to A_RST# (T9-T8A)
T10	-31 ms	–	PCIE_CLKP/N stable to SB_PWRGD asserted.
T11	36 ms	41 ms	SB_PWRGD to stable PCI CLOCK 33 MHz. See **Note 9**.
T12	1 ms	–	PCIRST# to CPU_RST# (CPU_RST# is driven by NB)
T13 **Note 16**	–	15ns	Wake Event (except PwrButton) to SLP_S3# / SLP_S5#
	200 ns	–	Wake Event (PwrButton) to SLP_S3# / SLP_S5#

Symbol	Min.	Max.	Description
T13A	80 ns	–	SB_PWRGD must be de-asserted before VDD(PS PWOK) drops more than 5% off the nominal value. **Note 10**
T14	1 ns	–	SB_PWRGD de-assertion to Resume Reset (RSM_RST#) assertion. See **Note 11**.
T15	5s	–	[Not illustrated] VBAT to VDD 3.3 and 1.2 (S5 power). Must be greater than 5 seconds to allow start time for the internal RTC.
T16	31 ms		SB_PWRGD to CPU_STP# de-assertion
T17	31 ms		SB_PWRGD to DPRSTP# de-assertion

See **Notes 1-16** in the Power Up/Down Sequence Timing Notes section following the power up/down sequence diagrams.

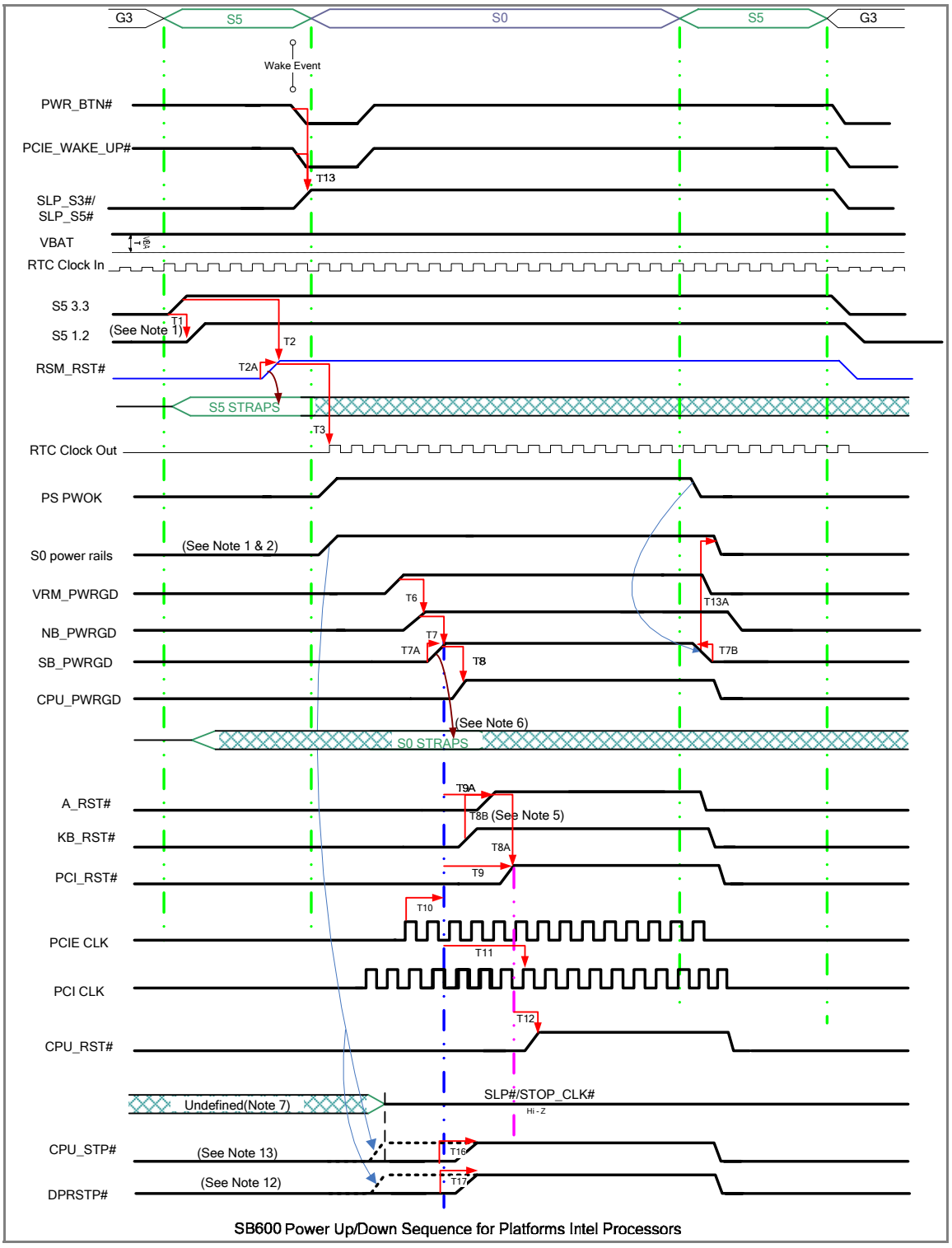


Figure 4-1: SB600 Power Up/Down Sequence for Platforms with Intel Processors

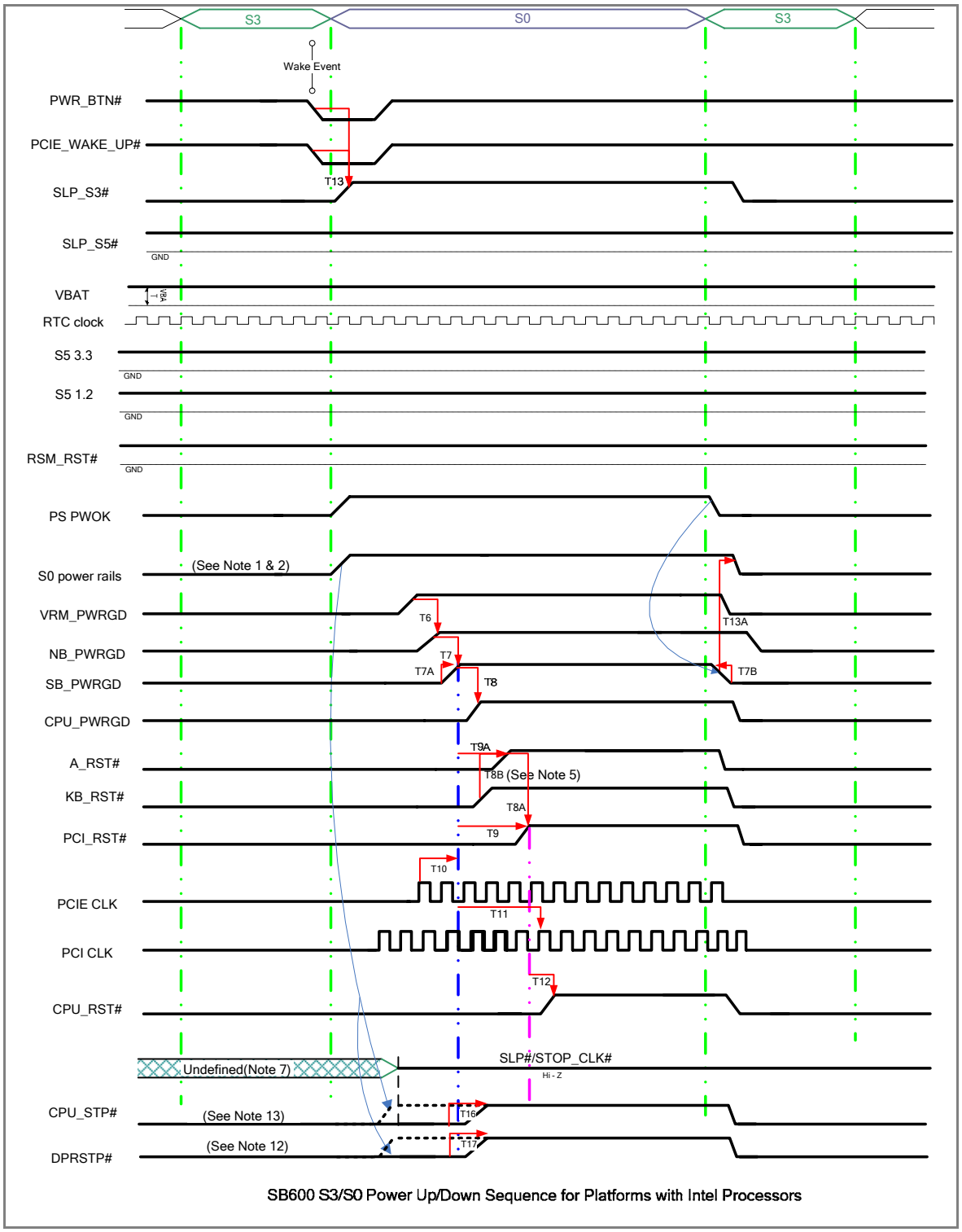


Figure 4-2: SB600 S3/S0 Power Up/Down Sequence for Platforms Intel Processors

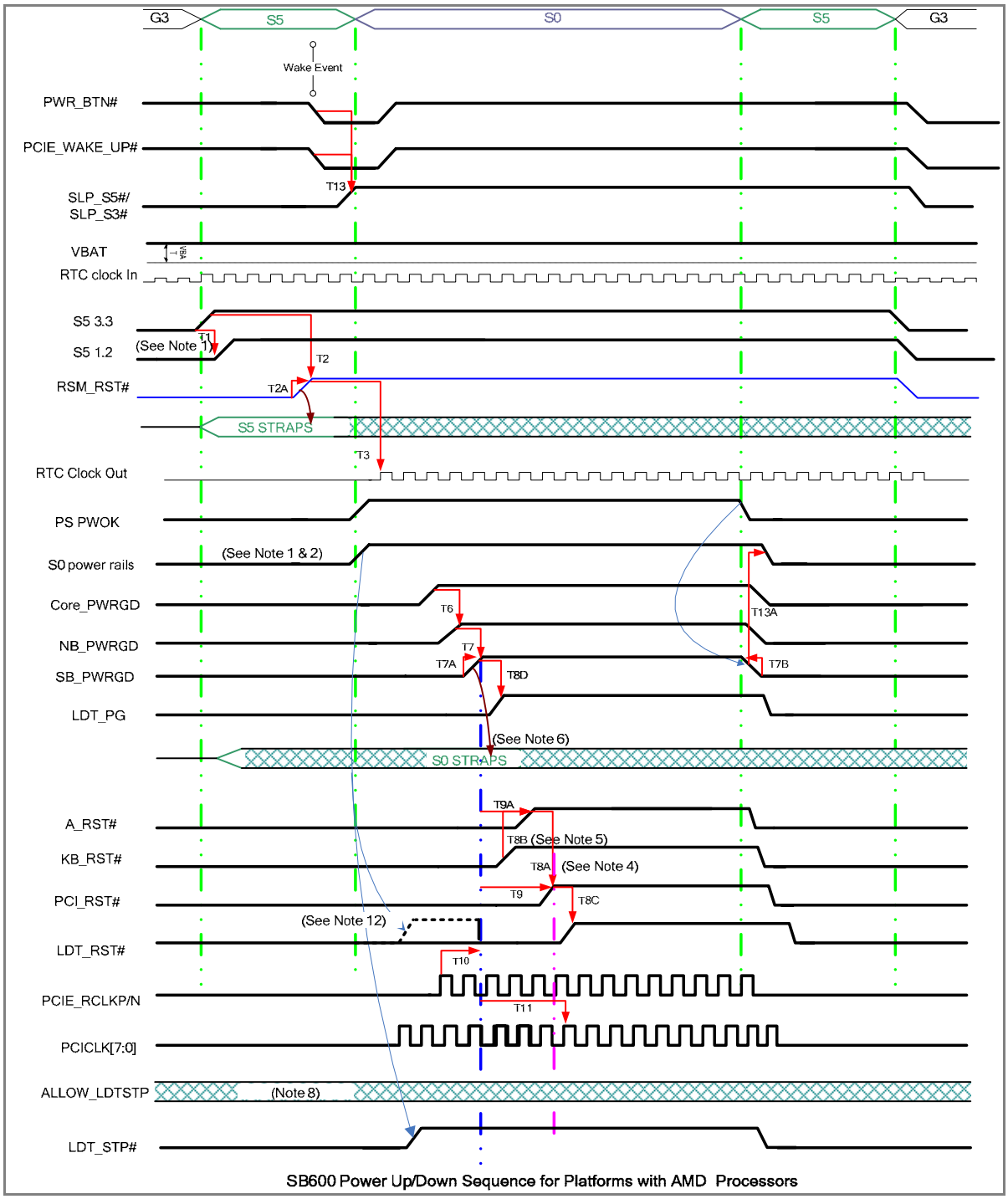


Figure 4-3: SB600 Power Up/Down Sequence for Platforms with AMD Processors

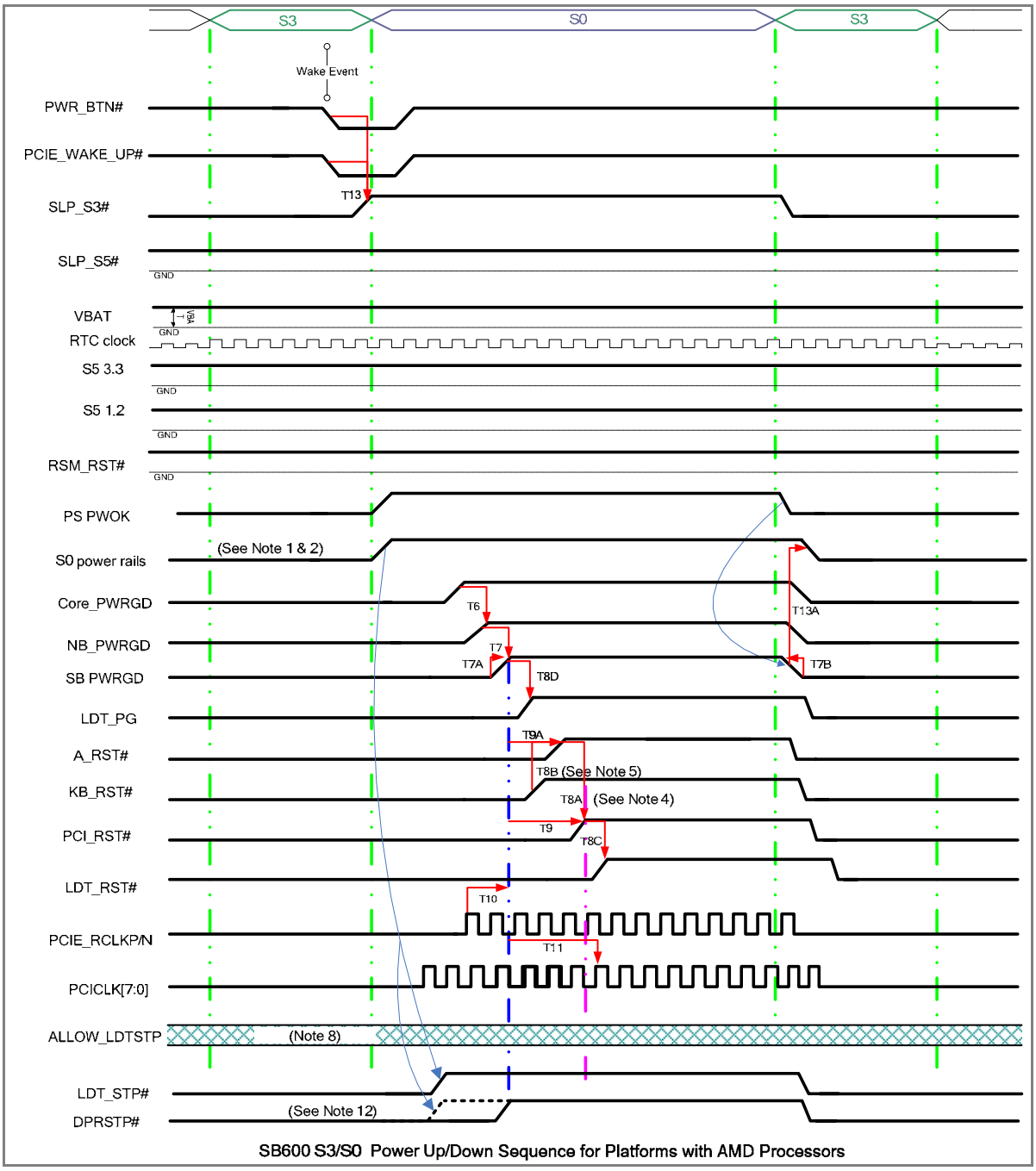


Figure 4-4: SB600 S3/S0 Power Up/Down Sequence for Platforms with AMD Processors

Power Up/Down Sequence Timing Notes

Note 1: There are no specific power sequencing requirements other than those indicated in Note 2 below (and potentially also in PA_SB600AH1, depending on the ASIC revision that is used). The SB600 power rails are grouped in four different voltages:

I. +5V, which includes V5_VREF
II. +3.3V, which includes VDDQ
III. +1.2V, which includes VDD, AVDDCK_1.2V, AVDD_SATA, PLLVDD_SATA PCIE_PVDD, PCIE_VDDR
IV. CPU_PWR (voltage is CPU-dependent)

Note 2:

A. V5_VREF is used in the SB600 for the 5V PCI signal tolerance. VDDQ (+3.3V) must not exceed V5_VREF by more than 0.6V at any time during ramp up, steady state, or ramp down. The suggested circuit below should be used to maintain relationship between V5_VREF and VDDQ.

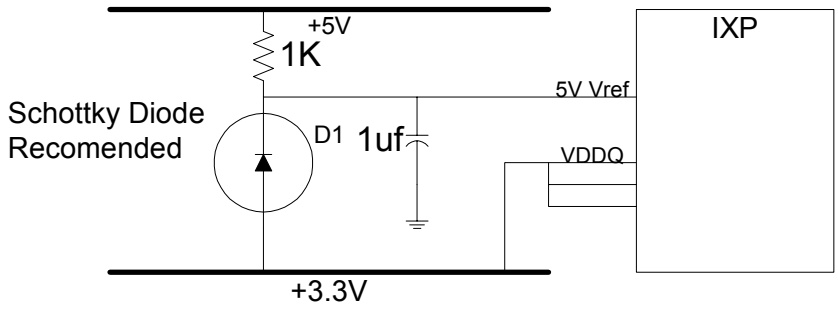


Figure 4-5: Circuit for Maintaining Proper Relationship between +V5_VREF and VDDQ

B. PCIE_PVDD must ramp between 3µs and 5ms later than VDD (core power) measured at 0.9V of each ramp as show below. See PA_SB600AT for a detailed description of this requirement.

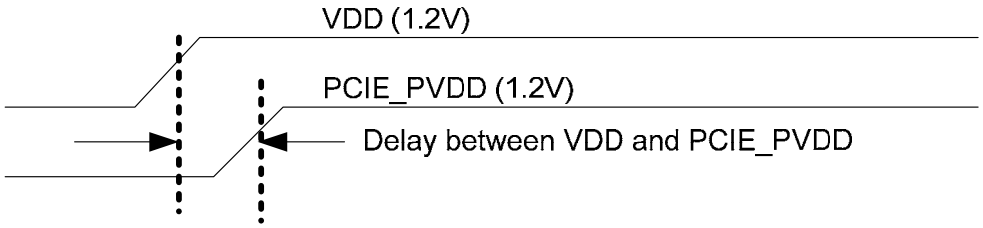


Figure 4-6: PCIE_PVDD vs. VDD Ramp Requirement

Note 3: The SB600 will latch the straps after rising edge of SB PWRGD only once. With debouncing of SB PWRGD, the latching of strap will occur at approximately ~10ms after the rising edge of SB PWRGD.

Note 4: Typical time between A_RST# and PCIRST# is 75ns. The measurement should be done at 10% of both signals. Loading on the motherboard may cause the measurement at 90% be more than the what is specified.

Note 5: The KB_RST# should be de-asserted before A_RST# (LDT_RST#) is de-asserted.

Note 6: Type II Standard and Debug straps will be latched after SB PWRGD is asserted. The straps will be latched in the window of TSc(min) = 10ms to TSc(max) = 10ms + 1050ns after SB PWRGD. Type I straps are latched on resume reset rising edge. See figure below.

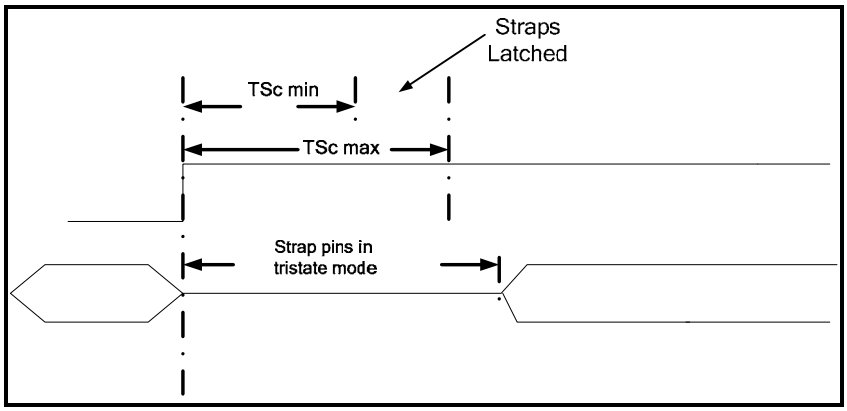


Figure 4-7: Timing for Latching of Straps

Note 7: SLP# and STOP_CLK# are tri-stated by the SB600 on power up. The voltages on these signals will depend on the external pull up supply.

Note 8: The SB600 will not monitor the ALLOW_LDTSTP signal on power up. This signal is only used on C3 transitions.

Note 9: The PCI Clock may be stable before T11 min. under some conditions; however in all cases, the PCI Clock is guaranteed to be stable only between T11 min. and max.

Note 10: The SB600 will monitor internally the power down event and protect the internal circuit during power down. This includes power down during the S3, S4, and S5 states. During an unexpected power failure or G3 state, the relationship between the 1.2V (VDD) and SB Power Good should be maintained to protect the SB600's internal logic.

Note 11: The following figure shows the timing of SB PWRGD de-asserted to RSM_RST# de-asserted during a power down sequence. However, this timing only applies to S0 to G3 state transition, because G3 state is when both signals are inactivated.

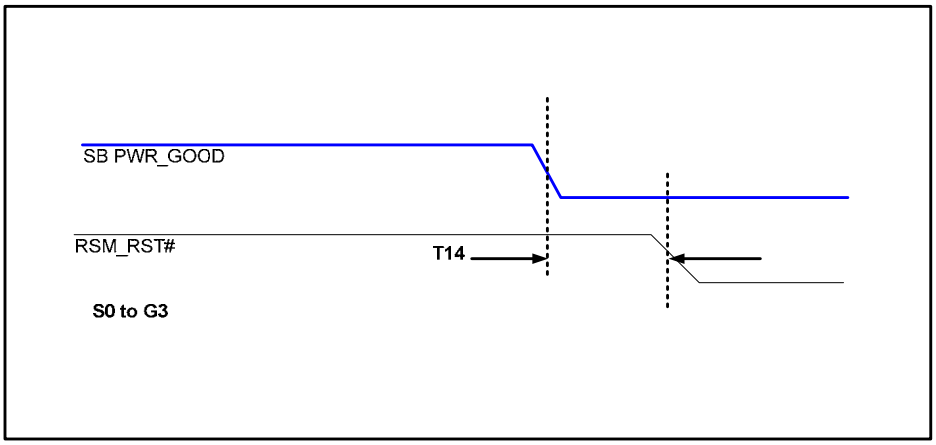


Figure 4-8: Timing for SB PWRGD De-asserted to RSM_RST# De-asserted

Note 12: DPRSTP# is asserted (low) until 32 ms after SB PWRGD is asserted. The signal may not be fully asserted to zero volt but may be seen at 300 mV max. This will still be considered a logic low by external logic. The DPRSTP# will be asserted only after the SB600 identifies the platform (which is done by reading the straps when SB PWRGD is asserted). See the following graph for details.

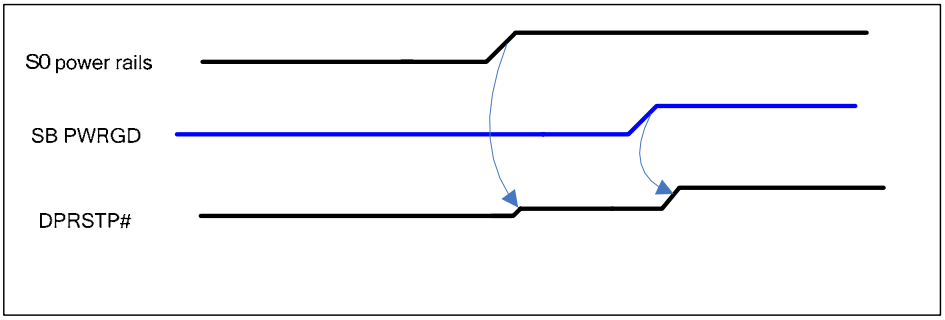


Figure 4-9: DPRSTP# Fully De-asserted when SB PWRGD Asserted

Note 13: Since the SB does not drive the signal until 32 ms after SB PWRGD, on some power up cycles, CPU_STP# may be asserted (low) until 32 ms after SB PWRGD is asserted. See the following figure for details.

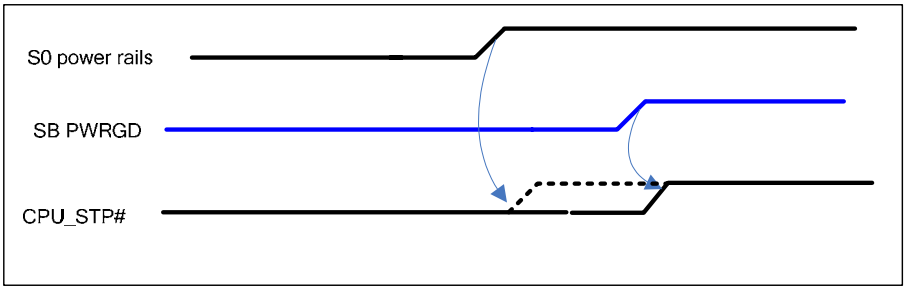


Figure 4-10: CPU_STP# De-asserted when SB PWRGD Asserted

Note 14: There is an approximately 200 ns max. glitch on LDT_RST# (label C in figure below), after the SB PWRGD is asserted. This glitch is caused by the logic not driving the signal for this period of time, as this multifunctional pin is being configured to support either an AMD or an INTEL CPU. This glitch happens right after SB PWRGD assertion, because this is the time when the SB straps are latched. The control signal will be in the process of being configured to either LDT_RST# (AMD platform) or DPRSTP#//PROCHOT (INTEL platform).

Prior to the SB_PWRGD assertion the LDT_RST# may be de-asserted as the internal logic is not initialized. The duration will depend on when the 3.3V or 1.2V rail ramps up. The de-assertion will be from the time when the 3.3.V or 1.2V rail ramps to 2.0V or 0.9 V respectively, to the time when SB_PWRGD ramps up to 2.0V.

Due to the following two timing features regarding the LDT_PG and LDT_RST#, the glitch on LDT_RST# should have no impact on the normal operation.

1. LDT_PG (CPU Power Good) is not asserted during the glitch and thereafter for at least 42 ms; see label A in the figure below.
2. LDT_RST# is also asserted again, after this glitch, for at least 74 ms (label B in the figure below), which will ensure that the CPU will be reset properly before actual de-assertion of LDT_RST# takes place.

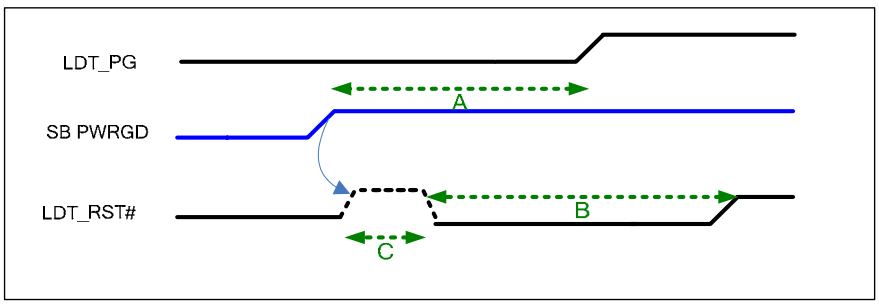


Figure 4-11: Glitch on LDT_RST#

Note 15: NB_PWRGD prerequisite timing is referred to in the power sequence section of the respective Northbridge Motherboard Design Guides.

Note 16: T13 is the duration between the time a Wake event is seen by the SB600 and the de-assertion of the SLP_S3# and SLP_S5# signals. The timing shown here is based on a minimum loading of 50 pf for both the SLP signals and the Wake event signals. If the system board has additional loading, the time measured will be longer due to the slow rise time of the signal. In this case the measurement is done at 90% of the fall time on Wake event signal and 10% of the rise time of the SLP signal rise time for a more accurate reading. See figure below.

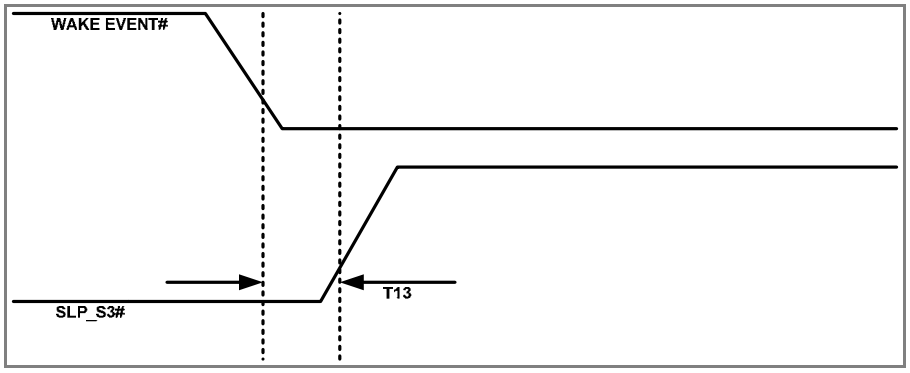


Figure 4-12: T13 Measurement Points

4.2 ACPI Timing

[TBA]

4.3 Pull-up/-down Requirements and Integrated Resistors

Table 4-2: External Resistor Requirements and Integrated Pull Up/Down

Interface	Signal Name	Value for Integrated / External Resistor	Resistor Type	Register for programming the integrated PU/PD
IDE	IDE_DRQ	Integrated 5.6K	Pull-down	—
	IDE_IORDY	Integrated 4.7K	Pull-up	—
	IDE_IRQ	Integrated 10K	Pull-down	—
	IDE_D7/GPIO22	Integrated 10K + integrated 27 Ω	See **Note**	(See GPIO section below)
	IDE_D[15:0]/GPIO[30:15]	Integrated 27Ω	Series	
	IDE_A[2:0]	Integrated 27Ω	Series	—
	IDE_CS[3,1]#	Integrated 27Ω	Series	—
	IDE_DACK#, IOW#, IOR#,	Integrated 27Ω	Series	——
PCIE	PCIE_CALRP	External 562 Ω (1% tolerance) Reference resistor for the Tx termination.	Pull-down to VSS_PCIE	
	PCIE_CALRN	External 2.05K (1% tolerance) Reference resistor for the Rx termination	Pull-UP to VDD_PCIE	—
USB	USB HSDM[9:0]-	Integrated 15K	Pull-down	—
	USB_HSDP[9:0]+	Integrated 15K	Pull-down	—
AC '97 /HD Audio	AC_BITCLK/GPIO38	Integrated 10K	Pull-down	(See GPIO section below)
	ACZ_SDIN[2:0]/ GPIO[44:42]	Integrated 50K	Pull-down	(See GPIO section below)
	AZ_SDIN3/GPIO46	Integrated 50K	Pull-down	(See GPIO section below)
	AC_SDOUT/GPIO39	Integrated 10K	Pull-down	(See GPIO section below)
Processor	A20M#/SID	AMD platforms: External 300Ω PU required. The PU should be tied to the same power used by the CPU I/O. Intel platforms: PU not required, as I/O is push-pull	Pull-up [AMD]	—
	CPU_PG/LDT_PG	AMD platforms: External 20K PD Intel platforms: PD not required, as I/O is push-pull	Pull-Down [AMD]	—

Interface	Signal Name	Value for Integrated / External Resistor	Resistor Type	Register for programming the integrated PU/PD
	FERR#	AMD platforms: Pin unused. Leave unconnected. Intel Platforms: External pull-up is required	Pull-up	—
Processor	IGNNE#/SIC	AMD platforms: External 300Ω PU required. Pull up should be tied to the same power used by the CPU I/O. Intel platforms: External PU not required, as I/O is push-pull	Pull-up [AMD]	—
	INIT#	PU not required, I/O is push-pull	—	—
	INTR/LINT0	PU not required, I/O is push-pull	—	—
	NMI/LINT1	PU not required, I/O is push-pull	—	—
	SMI#	PU not required, I/O is push-pull	—	—
	STPCLK#/ALLOW_LDTSTP	AMD platforms: External PU to CPU PWR Intel platforms: PU not required, I/O is push-pull	Pull-up [AMD]	—
	SLP#/LDT_STP#	AMD platforms: External 20K PD Intel platforms: Not required if paired with RS600's SLP# pin; otherwise, it requires an external PU to CPU_PWR.	Pull-up / pull-down	—
	DPRSLPVR	PU not required, I/O is push-pull (integrated PD when tri-stated)	Pull-down [integrated, when tri-stated]	—
	LDT_RST#/DPRSTP#/ PROCHOT#	AMD platforms: External 20K PD Intel platforms: Not required if it is configured as DPRSTP# (I/O is push-pull). For PROCHOT#, it requires external PU	Pull-down [AMD] / pull-up [Intel]	—
PCI	PCIRST#	External 8.2K pull-down is required	Pull-down	—
	INTE#/GPIO33	Integrated 8.2K	Pull-up	(See GPIO section below)
	INTF#/GPIO34	Integrated 8.2K	Pull-up	(See GPIO section below)
	INTG#/GPIO35	Integrated 8.2K	Pull-up	(See GPIO section below)

Interface	Signal Name	Value for Integrated / External Resistor	Resistor Type	Register for programming the integrated PU/PD
	INTH#/GPIO36	Integrated 8.2K	Pull-up	(See GPIO section below)
	AD[31:23]	Integrated 15K	Pull-up	PM_REG 41h / PM_REG 40h Default: PU enabled
	FRAME#	Integrated 8.2K	Pull-up	—
	TRDY#/ROMOE#	Integrated 8.2K	Pull-up	—
	IRDY#	Integrated 8.2K	Pull-up	—
	DEVSEL#/ROMA0	Integrated 8.2K	Pull-up	—
	STOP#	Integrated 8.2K	Pull-up	—
	SERR #	Integrated 8.2K	Pull-up	—
	PCI_PERR#	Integrated 8.2K	Pull-up	—
	LOCK#	Integrated 8.2K	Pull-up	—
	CLKRUN#	Integrated 8.2K	Pull-up	—
	REQ0#	Integrated 15K	Pull-up	—
	REQ1#	Integrated 15K	Pull-up	—
	REQ2#	Integrated 15K	Pull-up	—
	REQ3#/GPIO70	Integrated 15K	Pull-up	(See GPIO section below)
	REQ4#/GPIO71	Integrated 15K	Pull-up	(See GPIO section below)
	BMREQ#/REQ5#/GPIO65	External PU if used as REQ5#	Pull-up	(See GPIO section below)
LPC/ SIO/ SPI	LAD[3:0]	Integrated 15K	Pull-up	—
	LDRQ0#	Integrated 15K	Pull-up	—
	LDRQ1#/GNT5#/GPIO68	Integrated 15K	Pull-up	(See GPIO section below)
	LPC_SMI#/EXTEVNT1#	Integrated 8.2K	Pull-up	(See GEVENT section below)
	SERIRQ	Integrated 8.2K	Pull-up	—
	GA20IN	Integrated 8.2K	Pull-up	—
	KBRST#	Integrated 8.2K	Pull-up	—
	SPI_CLK/GPIO47	Integrated 10K	Pull-down	(See GPIO section below)
	SPI_DI/GPIO12	Integrated 10K	Pull-down	(See GPIO section below)
	SPI_DO/GPIO11	Integrated 10K	Pull-down	(See GPIO section below)
	SPI_HOLD#/GPIO31	Integrated 10K	Pull-up	—
	SPI_CS#/GPIO32	Integrated 10K	Pull-up	—
NB/ Power Manage-ment	USB_OC9#/SLP_S2/ GPM9#	Integrated 10K	Pull-down	PM2_Rg F8h Default: PD enabled
	PWR_BTN#	Integrated 10K	Pull-up	—
	PWR_GOOD	Integrated 10K	Pull-up	—
	TEST[1:0]	Integrated 10K	Pull-down	—
	TEST2	Integrated 10K	Pull-down	—

Interface	Signal Name	Value for Integrated / External Resistor	Resistor Type	Register for programming the integrated PU/PD
	RTCCLK	Integrated 10K	Pull-up	PM_Reg: 0Eh Default: PU enabled.
	RTC_IRQ#/GPIO69	Integrated 10K	Pull-up	(See GPIO section below)
	FANOUT0/GPIO3	Integrated 10K	Pull-up	—
	FANOUT1/GPIO48	Integrated 10K	Pull-up	—
	FANOUT2/GPIO49	Integrated 10K	Pull-up	—
	SPI_CLK/GPIO47	Integrated 10K	Pull-down	—
	RSMRST#	Integrated 10K	Pull-up	—
General Events/ GPM/ GPIO	RI#/EXTEVNT0#	Integrated 10K	Pull-up	PM2_Rg F5h Default: PU enabled
	LPC_SMI#/EXTEVNT1#	Integrated 8.2K	Pull-up	PM2_Rg F5h Default: PU enabled
	SMBALERT#/THRMTRIP#/GEVENT2#	Integrated 10K	Pull-up	PM2_Rg F3h Default: PU enabled
	LPC_PME#/GEVENT3#	Integrated 10K	Pull-up	PM2_Rg F3h Default: PU enabled
	PCI_PME#/GEVENT4#	Integrated 10K	Pull-up	PM2_Rg F4h Default: PU enabled
	S3_STATE/GEVENT5#	GEVENT5#: Integrated 10K S3_STATE: Push/Pull	Pull-up	PM2_Rg F4h Default: PU enabled
	USB_OC6#/GEVENT6#	Integrated 10K	Pull-up	PM2_Rg F4h Default: PU enabled
	USB_OC7#/GEVENT7#	Integrated 10K	Pull-up	PM2_Rg F4h Default: PU enabled
	WAKE#/GEVENT8#	Integrated 10K	Pull-up	PM2_Rg F5h Default: PU enabled
	USB_OC0#/GPM0#	Integrated 10K	Pull-up	PM2_Rg F6h Default: PU enabled
	USB_OC1#/GPM1#	Integrated 10K	Pull-up	PM2_Rg F6h Default: PU enabled
	USB_OC2#/GPM2#	Integrated 10K	Pull-up	PM2_Rg F6h Default: PU enabled
	USB_OC3#/GPM3#	Integrated 10K	Pull-up	PM2_Rg F6h Default: PU enabled
	USB_OC4#/GPM4#	Integrated 10K	Pull-up	PM2_Rg F7h Default: PU enabled
	USB_OC5#/DDR3_RST#/GPM5#	GPM5#: Integrated 10K DDR3_RST#: Open Drain	Pull-up	PM2_Rg F7h Default: PU not enabled
	BLINK/GPM6#	Integrated 10K	Pull-up	PM2_Rg F7h Default: PU enabled
	SYS_RESET#/GPM7#	Integrated 10K	Pull-up	PM2_Rg F7h Default: PU enabled
	USB_OC8#/AZ_DOCK_RST#/GPM8#	Integrated 10K	Pull-up	PM2_Rg F8h Default: PU enabled

Interface	Signal Name	Value for Integrated / External Resistor	Resistor Type	Register for programming the integrated PU/PD
	USB_OC9#/SLP_S2/ GPM9#	Integrated 10K	Pull-down	PM2_Rg F8h Default: PD enabled
GPIO	SSMUXSEL/SATA_IS3#/ GPIO0	Integrated 10K	Pull-down	PM2_Rg E0h Default: PD enabled
	ROM_CS#/GPIO1	Integrated 8.2K	Pull-up	PM2_Rg E0h Default: PU enabled
	SPKR/GPIO2	Integrated 10K	Pull-up	PM2_Rg E0h Default: PU/PD not enabled
	FANOUT0/GPIO3	Integrated 10K	Pull-up	PM2_Rg E0h Default: PU enabled
	SMARTVOLT/SATA_IS2#/ GPIO4	Integrated 8.2K	See **Note**	PM2_Rg E1h Default: PU/PD not enabled
	SHUTDOWN#/GPIO5/SM ARTVOLT2	Integrated 10K	See **Note**	PM2_Rg E1h Default: PU/PD not enabled
	GHI#/SATA_IS1#/GPIO6	Integrated 8.2K	See **Note**	PM2_Rg E1h Default: PU/PD not enabled
	WD_PWRGD/GPIO7	Integrated 10K	See **Note**	PM2_Rg E1h Default: PU/PD not enabled
	DDC1_SDA/GPIO8	Integrated 10K	See **Note**	PM2_Rg E2h Default: PU/PD not enabled
	DDC1_SCL/GPIO9	Integrated 10K	See **Note**	PM2_Rg E2h Default: PU/PD not enabled
	SATA_IS0#/GPIO10	Integrated 10K	See **Note**	PM2_Rg E2h Default: PU/PD not enabled
	SPI_DO/GPIO11	Integrated 10K	Pull down	PM2_Rg E2h Default: PD Enabled
	SPI_DI/GPIO12	Integrated 10K	Pull down	PM2_Rg E3h Default: PD Enabled
	LAN_RST#/GPIO13	Integrated 10K	See **Note**	PM2_Rg E3h Default: PU/PD not enabled
	ROM_RST#/GPIO14	Integrated 10K	See **Note**	PM2_Rg E3h Default: PU/PD not enabled
	IDE_D0/GPIO15	Integrated 10K	See **Note**	PM2_Rg E3h Default: PU/PD not enabled
	IDE_D1/GPIO16	Integrated 10K	See **Note**	PM2_Rg E4h Default: PU/PD not enabled
	IDE_D2/GPIO17	Integrated 10K	See **Note**	PM2_Rg E4h Default: PU/PD not enabled

Interface	Signal Name	Value for Integrated / External Resistor	Resistor Type	Register for programming the integrated PU/PD
	IDE_D3/GPIO18	Integrated 10K	See **Note**	PM2_Rg E4h Default: PU/PD not enabled
	IDE_D4/GPIO19	Integrated 10K	See **Note**	PM2_Rg E4h Default: PU/PD not enabled
	IDE_D5/GPIO20	Integrated 10K	See **Note**	PM2_Rg E5h Default: PD not enabled
	IDE_D6/GPIO21	Integrated 10K	See **Note**	PM2_Rg E5h Default: PU/PD not enabled
	IDE_D7/GPIO22	Integrated 10K	See **Note**	PM2_Rg E5h Default: PD not enabled
	IDE_D8/GPIO23	Integrated 10K	See **Note**	PM2_Rg E5h Default: PD not enabled
	IDE_D9/GPIO24	Integrated 10K	See **Note**	PM2_Rg E6h Default: PD not enabled
	IDE_D10/GPIO25	Integrated 10K	See **Note**	PM2_Rg E6h Default: PD not enabled
	IDE_D11/GPIO26	Integrated 10K	See **Note**	PM2_Rg E6h Default: PD not enabled
	IDE_D12/GPIO27	Integrated 10K	See **Note**	PM2_Rg E6h Default: PD not enabled
	IDE_D13/GPIO28	Integrated 10K	See **Note**	PM2_Rg E7h Default: PU/PD not enabled
	IDE_D14/GPIO29	Integrated 10K	See **Note**	PM2_Rg E7h Default: PU/PD not enabled
	IDE_D15/GPIO30	Integrated 10K	See **Note**	PM2_Rg E7h Default: PU/PD not enabled
	SPI_HOLD#/GPIO31	Integrated 10K	Pull-Up	PM2_Rg E7h Default: PU enabled
	SPI_CS#/GPIO32	Integrated 10K	Pull-up	PM2_Rg E8h Default: PU enabled
	INTE#/GPIO33	Integrated 10K	Pull-up	PM2_Rg E7h Default: PU enabled
	INTF#/GPIO34	Integrated 8.2K	Pull-up	PM2_Rg E7h Default: PU enabled
	INTG#/GPIO35	Integrated 8.2K	Pull-up	PM2_Rg E7h Default: PU enabled
	INTH#/GPIO36	Integrated 8.2K	Pull-up	PM2_Rg E8h Default: PU enabled

Interface	Signal Name	Value for Integrated / External Resistor	Resistor Type	Register for programming the integrated PU/PD
	DPSLP_OD#/GPIO37	Integrated 8.2K	See **Note**	PM2_Rg E8h Default: PU/PD not enabled
	AC_BITCLK/GPIO38	Integrated 10K	Pull-down	PM2_Rg E8h Default: PD enabled
	AC_SDOUT/GPIO39	Pull down (strap)	Pull-down	PM2_Rg E8h Default: PD enabled
	AC_SYNC/GPIO40	Integrated 10K	Pull-down	PM2_Rg E9h Default: PD enabled
	SPDIF_OUT/PCICLK7/ GPIO41	Integrated 10K	See **Note**	PM2_Rg EAh. Default: PU/PD not enabled
	ACZ_SDIN[2:0]/ GPIO[44:42]	Integrated 10K	Pull-down	PM2_Rg EAh Default: PD enabled
	AC_RST#/GPIO45	Push-pull. No external resistor required. Integrated 10K.	See **Note**	PM2_Rg EBh. Default: PD not enabled. Can be used to keep GPIO45 terminated on power up if pin is not used (NC).
	AZ_SDIN3/GPIO46	Integrated 50K	Pull-down	PM2_Rg EBh. Default: PD enabled
	SPI_CLK/GPIO47	Integrated 10K	Pull-down	PM2_Rg EBh. Default: PD enabled
	FANOUT1/GPIO48	Integrated 10K	Pull-up	PM2_Rg ECh. Default: PU enabled
	FANOUT2/GPIO49	Integrated 10K	Pull-up	PM2_Rg ECh. Default: PU enabled
	GPIO 65:50,67	Integrated 10K	See **Note**	PM2_rg F0h:ECh Default: PU/PD not enabled
	LLB#/GPIO66	Integrated 10K	Pull-up	PM2_Rg F0h Default: PU enabled
	LDRQ1#/GNT5#/GPIO68	Integrated 15K	Pull-up	PM2_Rg F1h Default: PU enabled
	RTC_IRQ#/GPIO69	Integrated 10K	Pull-up	PM2_Rg F1h Default: PU enabled
	REQ3#/GPIO70	Integrated 15K	Pull-up	PM2_Rg F1h Default: PU enabled
	REQ4#/GPIO71	Integrated 15K	Pull-up	PM2_Rg F1h Default: PU enabled
	GNT3#/GPIO72	Integrated 10K	See **Note**	PM2_rg F2h Default: PU/PD not enabled
	GNT4#/GPIO73	Integrated 10K	See **Note**	PM2_rg F2h Default PU/PD not enabled

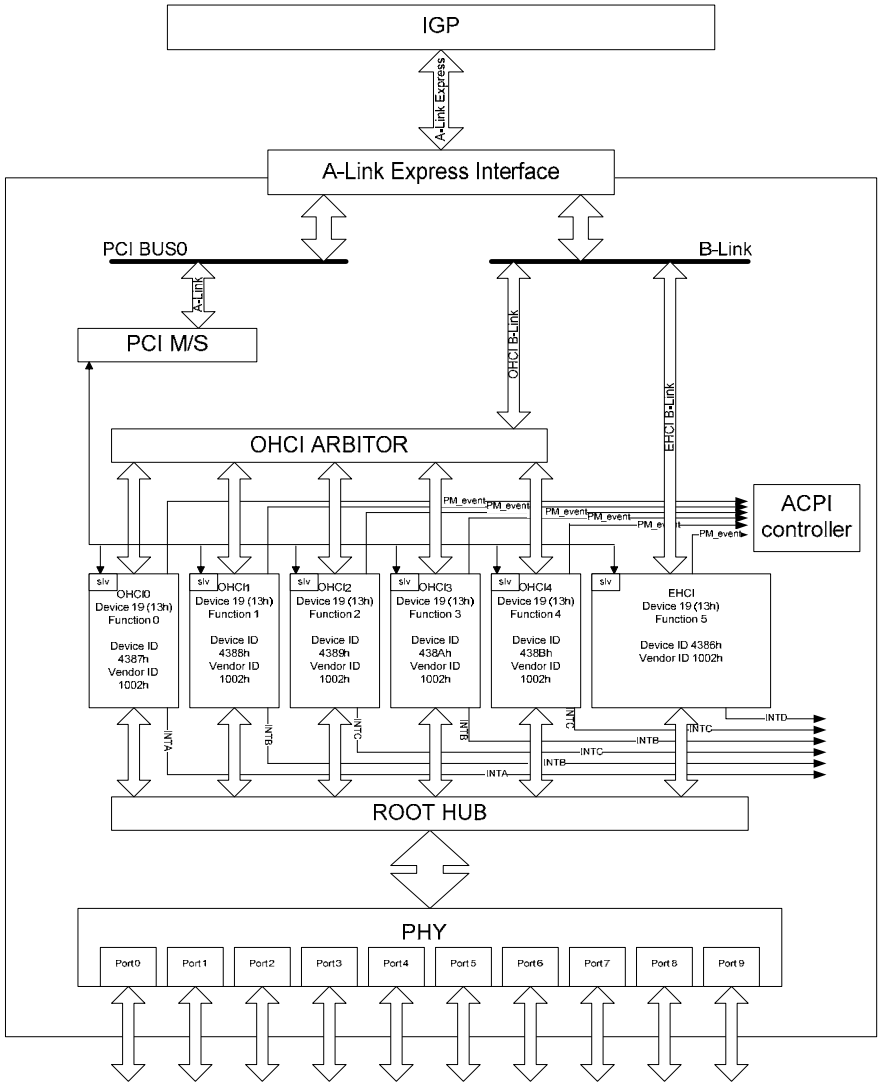
Note: The pin has an internal integrated pull-up or pull-down resistor that is not enabled by default. The pin's default function does not require a pull-up or pull-down. However, if the pin is used for an alternate function and a pull-up or pull-down is required, the internal resistor can be enabled by the indicated register.

5 Functional Description

5.1 EHCI USB 2.0 and OHCI USB 1.1 Controllers

5.1.1 USB Architecture Overview

A USB (Universal Serial Bus) Host System is composed of a number of hardware and software layers. Figure 16 illustrates block diagram of the OHCI and EHCI connectivity to USB ports.



Controller	Controls Port
OHCI0	Port 0/1
OHCI1	Port 2/3
OHCI2	Port 4/5
OHCI3	Port 6/7
OHCI4	Port 8/9
EHCI	Port 0 → 9

Figure 5-1: SB600 USB 2.0 System Block Diagram

5.1.2 USB Power Management

An advanced power management capability interface compliant with *PCI Bus Power Management Interface Specification Revision 1.1* is incorporated into the EHCI. This interface allows the EHCI to be placed in various power management states, offering a variety of power savings for a host system.

Table 5-1 highlights the EHCI support for power management states and features supported for each of the power management states. An EHCI implementation may internally gate-off USB clocks and suspend the USB transceivers (low power consumption mode) to provide these power savings.

Table 5-1: EHCI Support for Power Management States

PCI Power Management State	State Required/ Optional by Spec	Comments
D0	Required	**Supported in SB600.** Fully awake backward compatible state. All logic in full power mode.
D1	Optional	**Not supported in SB600.** USB Sleep state with EHCI bus master capabilities disabled. All USB ports in suspended state. All logic in low latency power savings mode because of low latency returning to D0 state.
D2	Optional	**Not supported in SB600.** USB Sleep state with EHCI bus master capabilities disabled. All USB ports in suspended state.
D3hot	Required	**Supported in SB600.** Deep USB Sleep state with EHCI bus master capabilities disabled. All USB ports in suspended state.
D3cold	Required	**Supported in SB600.** Fully asleep backward compatible state. All downstream devices are either suspended or disconnected based on the implementation's capability to supply downstream port power within the power budget.

The functional and wake-up characteristics for the EHCI power states are summarized in *Table 5-2* below.

Table 5-2: EHCI Power State Summary

Power State	Functional Characteristics	Wake-up Characteristics (Associated Enables must be Set)
D0	• Fully functional EHCI device state • Unmasked interrupts are fully functional	• Resume detected on suspended port • Connect or Disconnect detected on port Over Current detected on port
D1	• EHCI shall preserve PCI configuration • EHCI shall preserve USB configuration • Hardware masks functional interrupts • All ports are disabled or suspended	• Resume detected on suspended port • Connect or Disconnect detected on port • Over Current detected on port
D2	• EHCI shall preserve PCI configuration • EHCI shall preserve USB configuration • Hardware masks functional interrupts All ports are disabled or suspended	• Resume detected on suspended port • Connect or Disconnect detected on port • Over Current detected on port

Power State	Functional Characteristics	Wake-up Characteristics (Associated Enables must be Set)
D3hot	• EHCI shall preserve PCI configuration • EHCI shall preserve USB configuration • Hardware masks functional interrupts • All ports are disabled or suspended	• Resume detected on suspended port • Connect or Disconnect detected on port • Over Current detected on port
D3cold	• PME Context in PCI Configuration space is preserved • Wake Context in EHCI Memory • Space is preserved • All ports are disabled or suspended	• Resume detected on suspended port • Connect or Disconnect detected on port • Over Current detected on port

5.2 SMI#/SCI Generation

Certain system events are routable between SMI# or SCI. When an event is routed to SMI# and occurs, SMI# will be asserted by SB600 and the processor will enter SMM space. SMI# remains active until the EOS bit is set. When the EOS is set, SMI# will be de-asserted for at least 4 PCICLK. If the event is routed to SCI, then BIOS can route it to any of the legacy interrupts (except IRQ8) or INT21 in the case of IOAPIC.

Table 5-3: Causes of SMI# and SCI

Cause	SCI	SMI	Additional Enable	Where reported
SMI Command port	Yes	Yes	PM x0E, bit 2	PM x0F, bit 2
SERR# port	Yes	Yes	PCI config x64, bit 16	PCI config x04, bit 30; PM x0F, bit 1
GBLRLS written to	Yes	Yes	PM x0E, bit 0	PM x0F ,bit 0
PM Timer1	Yes	Yes	PM x00, bit 1; PM x08, x09, x0A	PM x01, bit 1
PM x00, bit 4 is written 1	Yes	Yes	PM x00, bit 4	PM x01, bit 4
IRQ[15:8] activity	Yes	Yes	PM x02	PM x05
IRQ[7:0] activity	Yes	Yes	PM x03	PM x06
Legacy IO activity	Yes	Yes	PM x04	PM x07
IO activity	Yes	Yes	PM x1C, PM xA8	PM x1D, PM xA9
Temperature Warning	Yes	Yes	XC50/C51, index x03, bit 1	XC50/C51, index x02, bit 1
Temperature Warning (this input can generate SMI# through this set of register)	Yes	Yes	AcpiGpe0Blk, index 00, bit 9	AcpiGpe0Blk, index 04, bit 9
GEVENT/GPM inputs	Yes	Yes	AcpiGpe0Blk, index 00, bits [7:0] for GEVENT, bits [29, 28, 26, 25, 22:19] for GPM	AcpiGpe0Blk, index 04, same bits
USB SMI#	Yes	Yes	AcpiGpe0Blk, index 00, bit 8	AcpiGpe0Blk, index 04, bit 8; PM x0F, bit 5
SMBus SMI#	Yes	Yes	AcpiGpe0Blk, index 00, bit 8	AcpiGpe0Blk, index 04, bit 8; PM x0F, bit 4
AC ‘97 wake	Yes	Yes	AcpiGpe0Blk, index 00, bit 12	AcpiGpe0Blk, index 04, bit 12
HDAudio wake	Yes	Yes	AcpiGpe0Blk, index 00, bit 27	–
USB wake	Yes	Yes	AcpiGpe0Blk, index 00, bit 11	AcpiGpe0Blk, index 04, bit 11
RTC	Yes	Yes	RTC_STS	RTC_EN
ACPI timer	Yes	Yes	TMR_STS	TMR_EN
GBL_STS	Yes	Yes	GBL_STS	GBL_EN
PowerButton	Yes	Yes	PWRBTN_STS	PWRBTN_EN

5.3 LPC ISA Bridge

5.3.1 LPC Interface Overview

The Low Pin Count (LPC) bus interface is a cost-efficient, low-speed interface designed to support low-speed legacy (ISA, X-bus) devices. The LPC interface essentially eliminates the need of ISA and X-bus in the system. A typical setup of the system with LPC interface is shown in Figure 5-2 below. Here the ISA bus is optional. The LPC host controller is typically integrated into the south bridge. It connects to the PCI bus on one side and the LPC bus on the other side.

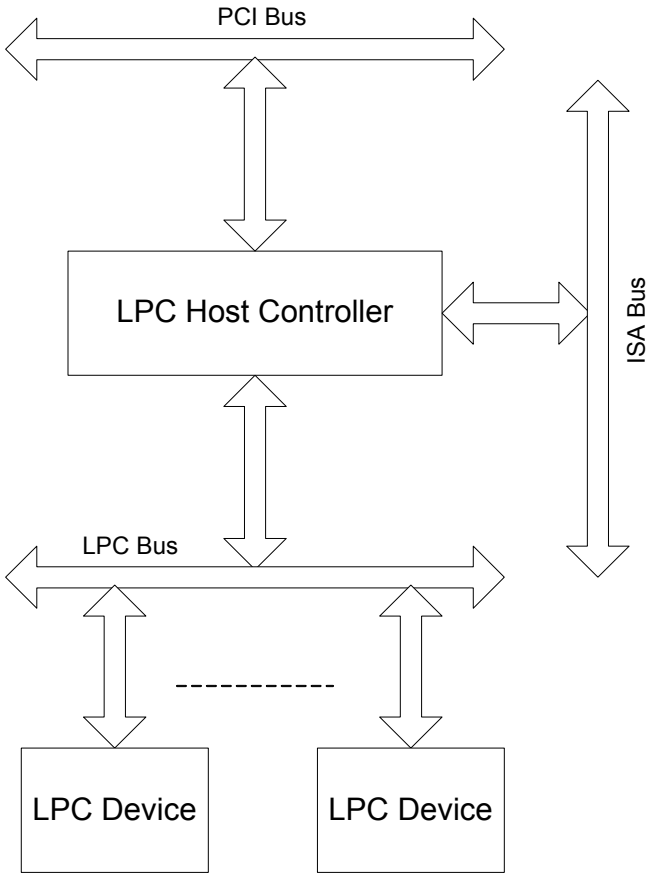


Figure 5-2: A Typical LPC Bus System

Examples of LPC devices include Super I/O (floppy-disk controller, keyboard controller), BIOS, audio, and system management controller. Figure 5-3 below shows the signals associated with the LPC host controller.

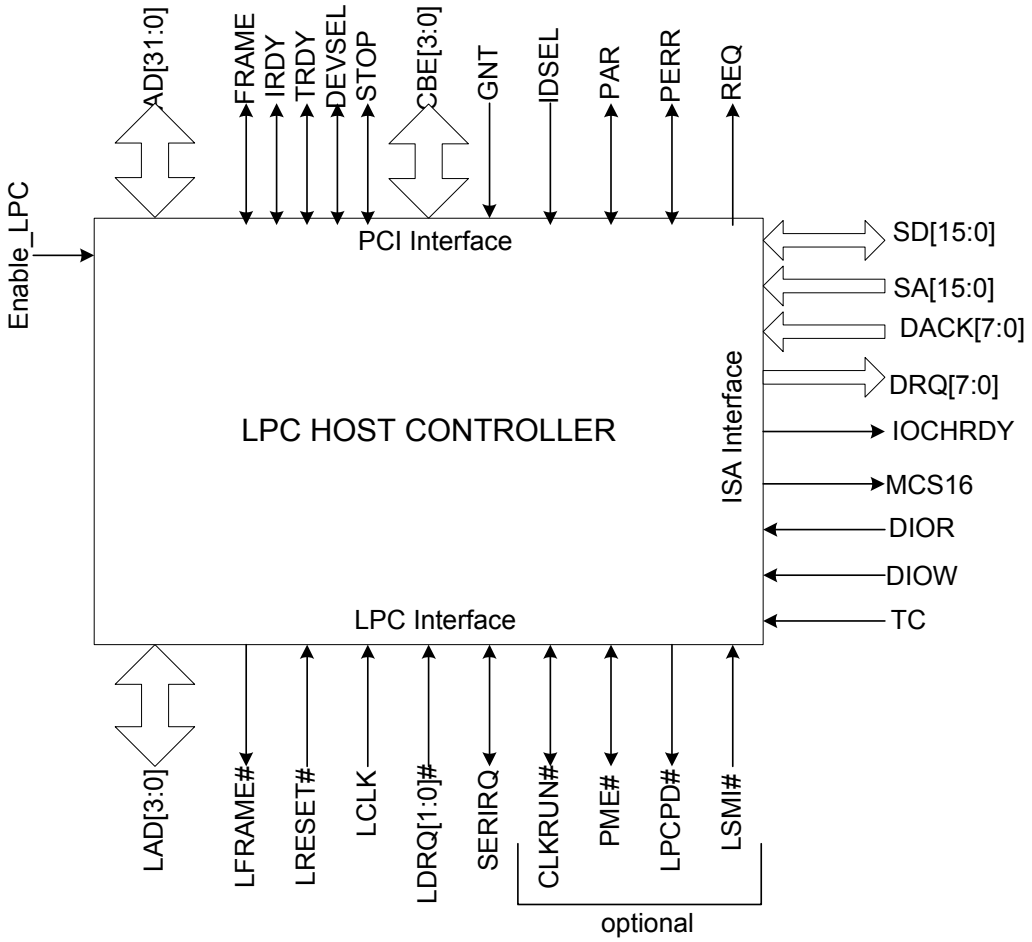


Figure 5-3: LPC Host Controller Interfaces and Signals

Note that the ISA interface is only used for legacy DMA operation. LPC host controller has standard PCI interface on one side and LPC interface on the other. Some LPC signals are used for power management in mobile systems and are therefore optional. A more detailed description of each signal is given later.

The host controller supports memory and IO read/write, DMA read/write, bus master memory/IO read/write. It supports up to two bus masters and 7 DMA channels. A bus master or DMA agent uses LDRQ pin to assert bus master or DMA request. The host controller uses LFRAME# to indicate the start or termination of a cycle. The following table shows a list of cycles supported by the host controller, initiator, data flow direction, and their PCI counterparts.

Table 5-4: LPC Cycle List and Data Direction

Cycle	Size (bytes)	Initiator	Data Direction	PCI counterpart
Memory read	1	Host	P-2-Host	MemRead to LPC range
Memory write	1	Host	Host-2-P	MemWrit to LPC range
I/O read	1	Host	P-2-Host	IORead to LPC range
I/O write	1	Host	Host-2-P	IOWrit to LPC range
DMA read	1,2,4	Peripheral	Host-2-P	DMA Cntrl Setup; DMA data fetch
DMA write	1,2,4	Peripheral	P-2-Host	DMA Cntrl Setup; DMA data store
BM Memory read	1,2,4	Peripheral	Host-2-P	DMA Cntrl Setup; DMA data fetch
BM Memory write	1,2,4	Peripheral	P-2-Host	DMA Cntrl Setup; DMA data store
BM I/O read	1,2,4	Peripheral	Host-2-P	DMA Cntrl Setup; IO data fetch
BM I/O write	1,2,4	Peripheral	P-2-Host	DMA Cntrl Setup; IO data store

The host controller has a SERIRQ (Serial IRQ) pin, which is used by peripherals that require interrupt support. All legacy interrupts are serialized on this pin, and then decoded by the host controller, and sent to the interrupt controller for processing. Please refer to the Serial IRQ Specification (Rev 5.4) for detailed description on serial IRQ protocol.

5.3.2 LPC Module Block Diagram

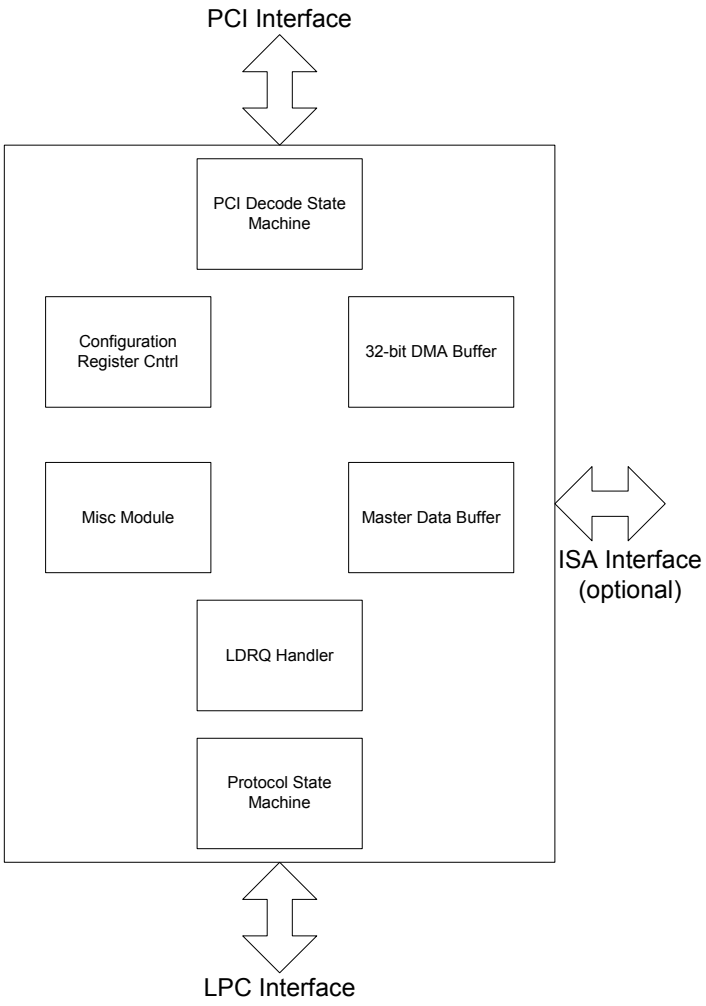


Figure 5-4: Block Diagram of LPC Module

5.4 Real Time Clock

The Real Time Clock (RTC) is used for updating a computer's time. In addition to that, it also generates interrupts for periodic events and pre-set alarm. The SB600's RTC includes a 256-byte CMOS RAM, which is used to store the configuration of a computer, such as the number and type of floppy drive, graphics adapter, base memory, checksum value, etc. Note that the RTC does make hardware leap year correction.

5.4.1 Functional Blocks of RTC

The internal RTC is made of two parts: one is an analog circuit, powered by a battery VBAT, and the other part is a digital circuit, powered by a main power VDD. *Figure 5-5* shows the block diagram of the internal RTC.

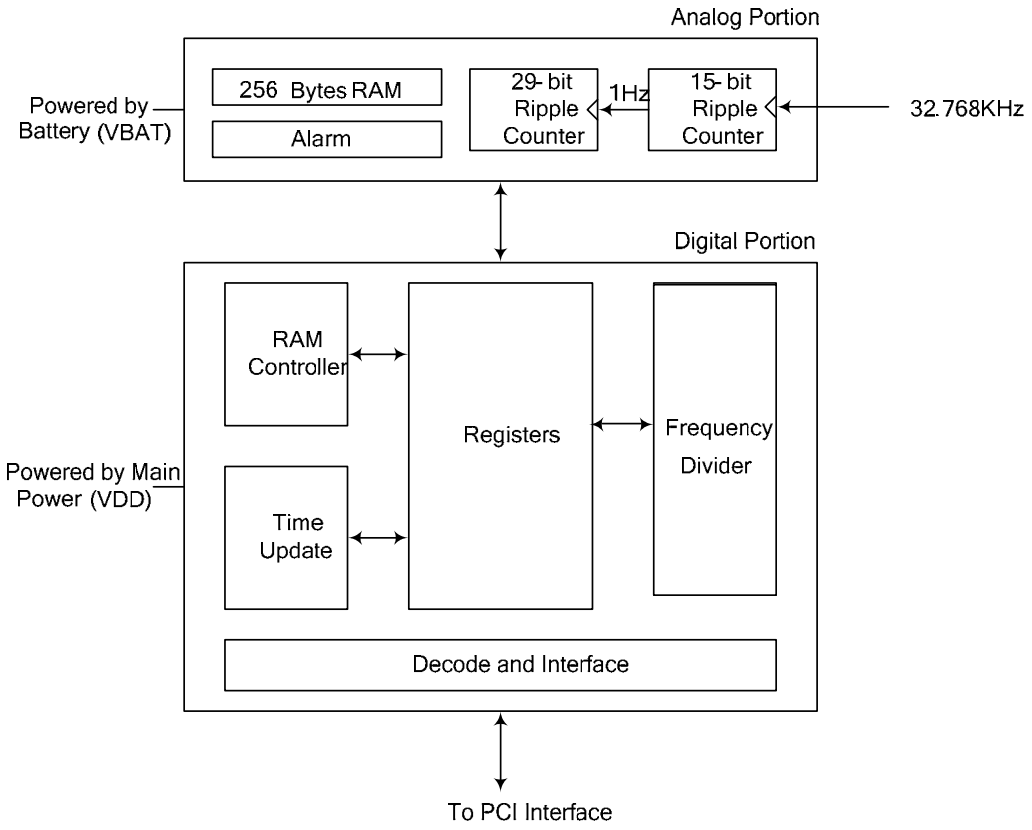


Figure 5-5: Block Diagram of Internal RTC

5.5 SATA (Serial ATA) Controller

The integrated Serial ATA controller processes host commands and transfers data between the host and Serial ATA devices. It supports four independent Serial ATA channels. Each channel has its own Serial ATA bus and supports one Serial ATA device. For transfer rate, SATA controller supports both Serial ATA Generation I (1.5Gb/s) and Generation II (3.0Gb/s). *Figure 5-6* below is a diagram for the SATA block.

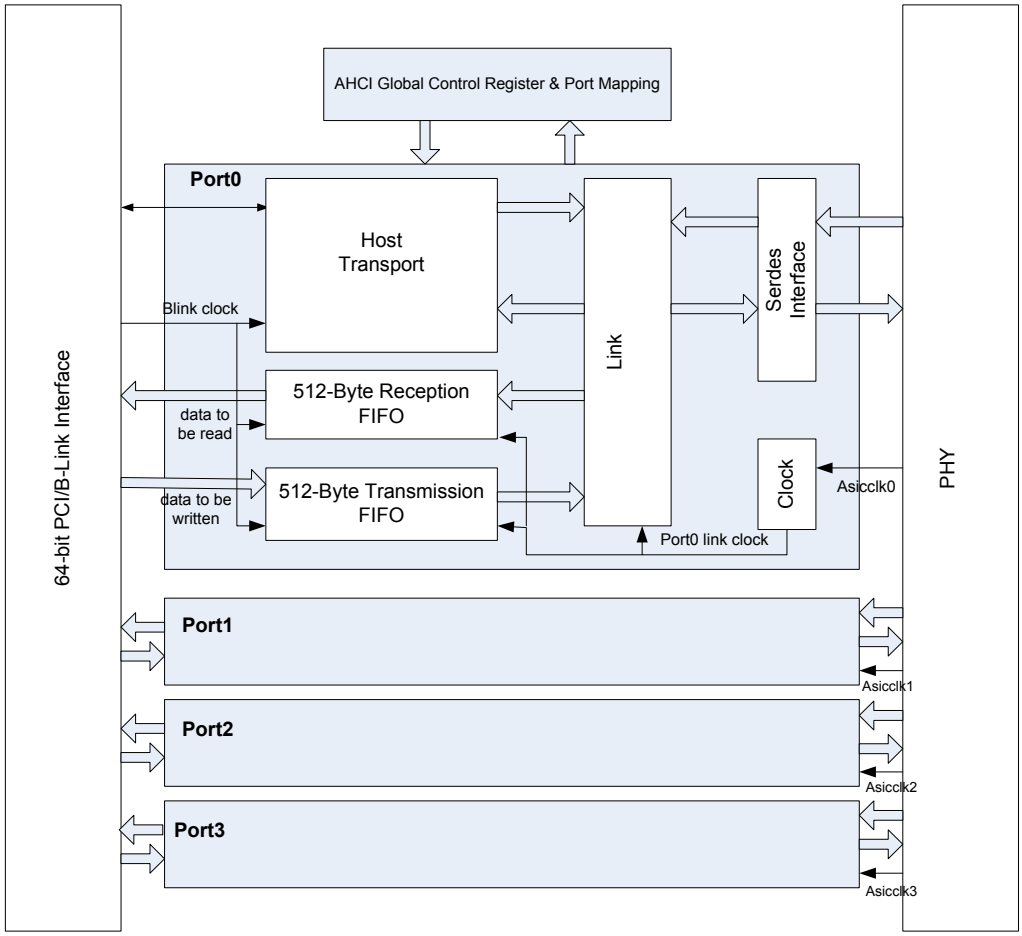


Figure 5-6: Block Diagram for the SATA Module

5.6 AC '97 Controller

A standard AC-Link digital serial interface is used in the SB600 AC '97 controller. This bi-directional time division multiplex serial PCM digital stream runs at a fixed rate with each frame being transmitted at 48 kHz. The interface for the SB600 AC '97 controller consists of six pins that transfer data in both directions. Data is transferred to the AC '97 codec through the AC_SDOUT port for audio playback, register access request, and modem data out. In the opposite direction, data is transferred from the AC '97 codec to the SB600 AC '97 Controller through the ACZ_SDIN for audio record, register status read back, and modem data in. The controller supports up to three AC '97 codecs.

Table 5-5: Pin Definitions

Pin name	I/O	Purpose
AC_BITCLK	In	Serial data transmission clock at 12.288MHz
ACZ_SDIN0	In	Data to the AC '97 Controller from primary codec
ACZ_SDIN1	In	Data to the AC '97 Controller from a secondary codec (slave 1)
ACZ_SDIN2	In	Data to the AC '97 Controller from a secondary codec (slave 2)
AC_SDOUT	Out	Data from the AC '97 Controller
AC_SYNC	Out	Synchronization signal at 48kHz
AC_RST#	Out	Reset to the codec(s)

5.6.1 Output Data Stream

The output data streams refer to the data going from the AC '97 controller to the codec(s). A timing diagram of the 13 slots is shown below. *Table 5-6* describes the use of each one of the slots. Each new bit position is presented into the AC-Link at the rising edge of the AC_ BITCLK. The data is subsequently sampled by the codec on the following falling edge of the AC_BITCLK.

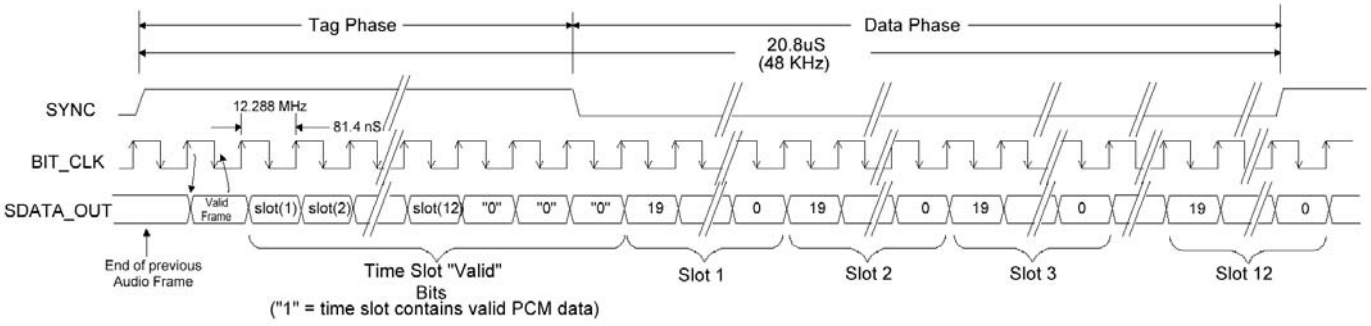


Figure 5-7: ACLINK AC_SDOUT Serial Stream

Table 5-6: AC_SDOUT Slots definitions

SDATA_OUT slots	Purpose
Slot 0	TAG: Bit 15: Identity the validity of the entire audio output frame Bit 14:3: Identity the validity of each slot Bit 2 : RESERVED Bit 1:0: Target codec ID of the current frame
Slot 1	Command Address Bit 19: Identity codec register read/write operation - 0 is write Bit 18:12 : Contains the target codec register address Bit 11:0 : RESERVED
Slot 2	Command Data 19:4 Data to be transferred to the register address identified by Slot 1 in case of a write operation 3:0 Reserved
Slot 3	PCM Playback Left Channel
Slot 4	PCM Playback Right Channel
Slot 5	Modem DAC Data
Slot 6	PCM center
Slot 7	PCM Left surround sound
Slot 8	PCM Right surround sound
Slot 9	PCM LFE
Slot 10	Modem 2 DAC Data or PCM Left for 96 MHz audio support
Slot 11	Hand set data (HSET DAC) or PCM Right for 96 MHz audio support
Slot 12	Modem GPIO Control Data or PCM Center data for 96 MHz audio support

5.6.2 Input Data Stream

The input data stream, ACZ_SDIN, refers to the data going from the codec(s) to the AC '97 Controller. A timing diagram of the 13 slots is shown in *Figure 5-8*. *Table 5-7* describes the use of each one of the slots. Each new bit position is presented into the AC Link at the rising edge of the BIT_CLK. The data is subsequently sampled by the AC '97 Controller during the following falling edge of the BIT_CLK.

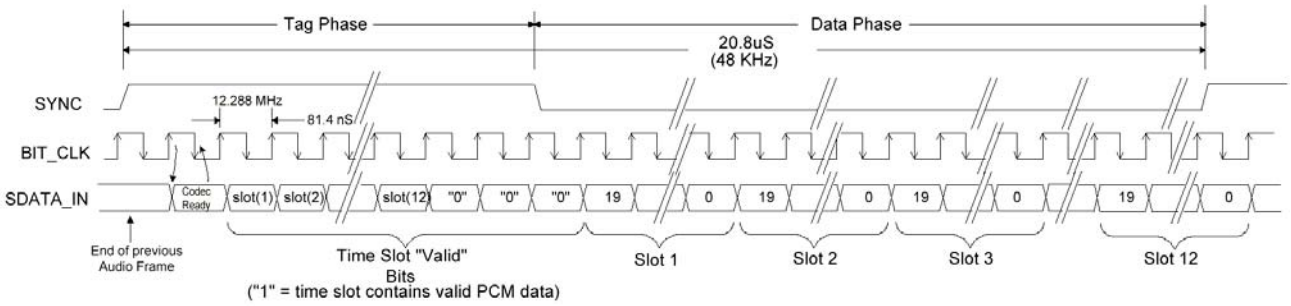


Figure 5-8: ACLINK ACZ_SDIN Serial Stream

Table 5-7: ACZ_SDIN Slots Definitions

SDATA_IN slots	Purpose
Slot 0	TAG Bit 15 : Codec ready Bit 14:3 : Identity the validity of each slot Bit 2:0 : RESERVED
Slot 1	Status Address Bit 19 : RESERVED Bit 18:12 : Echoes the command address slot Bit 11:2 : Slot request for supporting non-48kHz audio streams Bit 1:0 : RESERVED
Slot 2	Status Data Contains the register data of the register address indicated in slot 1
Slot 3	PCM Record Left Channel Left audio sample from ADC
Slot 4	PCM Record Right Channel Right audio sample from ADC
Slot 5	Modem ADC Data Modem audio sample from modem ADC
Slot 6	MIC ADC Microphone Data
Slot 7-9	Reserved - not used in 2.1 spec
Slot 10	Modem 2 ADC Data Modem audio sample from modem ADC
Slot 11	HSET DAC Hand set Data
Slot 12	Modem GPIO Status Contains current status of the GPIO pins on the codec

5.6.3 AC '97 Controller-Codec(s) Connections

The five AC Link pins on each codec are required to be connected with the AC ‘97 Controller. *Figure 5-9* shows a simple connection between a single codec (either AC ‘97 or AMC97) and the AC ‘97 Controller.

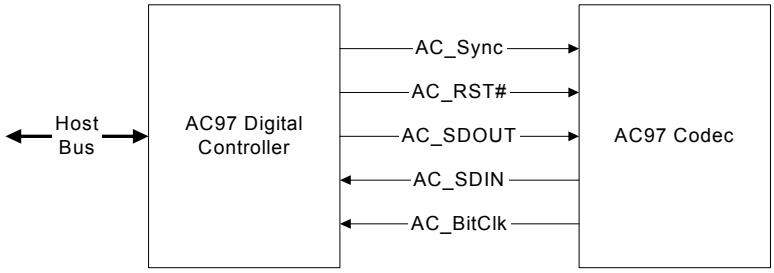


Figure 5-9: Single AC '97 Codec Connection

For a multiple codec configuration (see *Figure 5-10*), one of the codecs will act as the primary unit and provide the central master clock to the system. In this configuration, all three AC '97 codecs share the serial output data from the digital controller. Each codec will be responsible for parsing out the intended data from the stream based on the time slots. All codecs can send in data to the digital controller at the same time provided they do not share the same time slot.

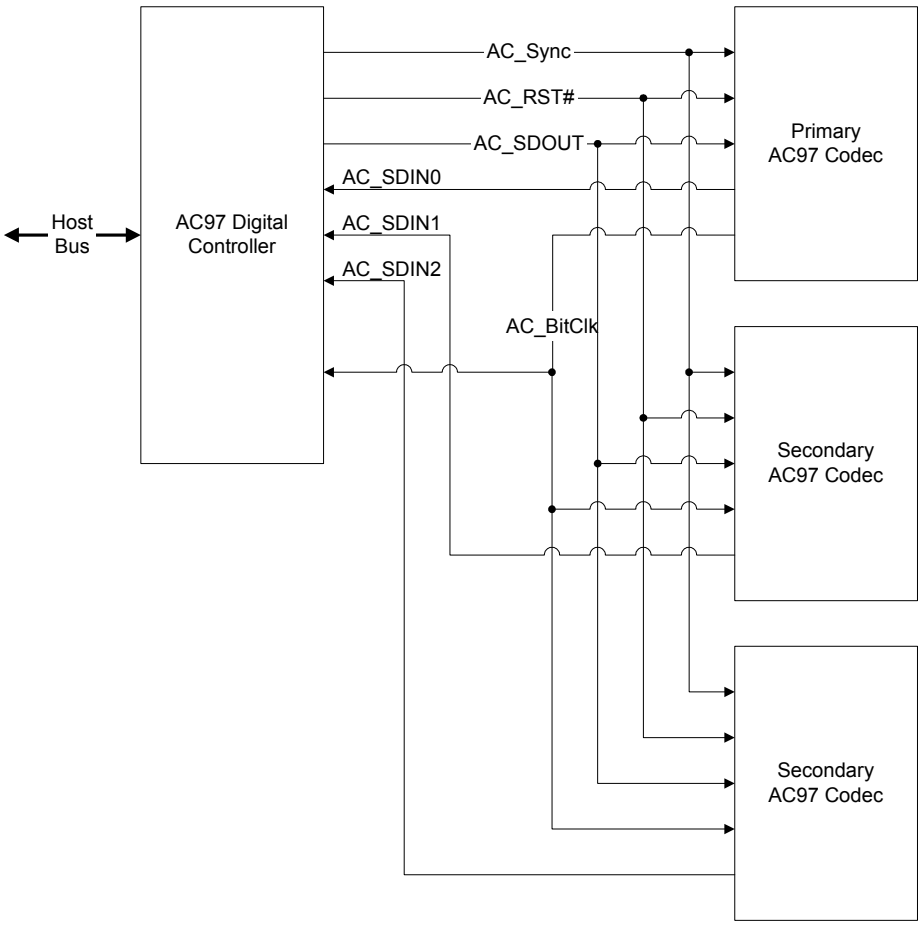


Figure 5-10: Multiple AC '97 Codec Connection

5.7 High Definition Audio

Intel® High Definition (HD) Audio is the next-generation PC audio technology intended for replacing the AC '97. The primary goal for developing HD Audio is to create a uniform programming interface and to provide capabilities beyond those supported by the AC '97. It is not intended to be backward compatible with the AC '97. The link protocols and operations of these two standards are not compatible, which means AC '97 and HD Audio codecs cannot be mixed on the same link.

The SB600 supports HD Audio with a separate engine from that of the AC '97. Also, the physical codec buses are separate, so that the AC '97 and HD engines can operate simultaneously. This allows mixed system configurations, supporting, for example, an HD Audio interface together with an AC '97 modem.

5.7.1 HD Audio Codec Connections

Figure 5-11 below shows the HD Audio interface connections to the HD Audio codecs. The AC '97 audio interface shares pins SDIN[2:0] with the HD Audio interface, and together with the dedicated SDIN3 pin, they support up to 4 HD Audio codecs. Those shared pins on the SB600 are named ACZ_SDIN[2:0] to indicate support for both interfaces and, together with AZ_SDIN3, they act as data input for the HD Audio interface. *Figure 5-11* shows the signals on both interfaces and their interrelationships.

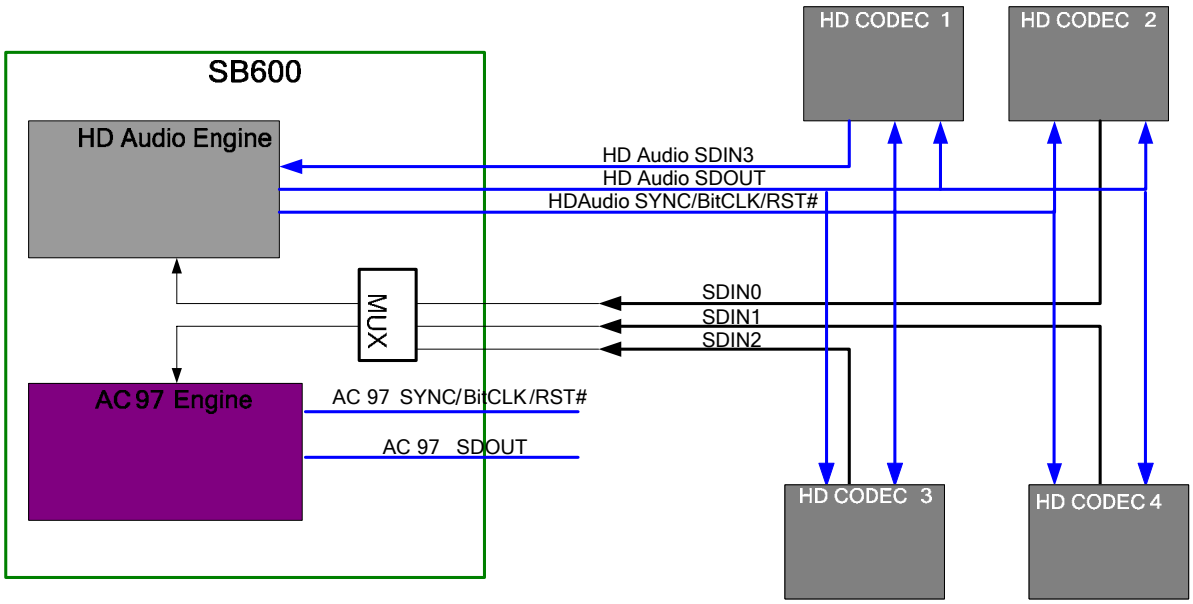


Figure 5-11: HD Audio Codec Connections

5.7.2 HD Audio and AC '97 Codec Connections in Mixed Configurations

SB600 also allows mixing AC' 97 and HD Audio codecs in a system. As discussed in section 3.15, AZ_SDIN3 can only be connected to an HD Audio codec, while ACZ_SDIN[2:0] can be connected to either an AC' 97 codec (audio / modem) or HD Audio codec. *Figure 5-12* and *Figure 5-13* below show some possible configurations combining HD Audio and AC' 97 codecs on the same system.

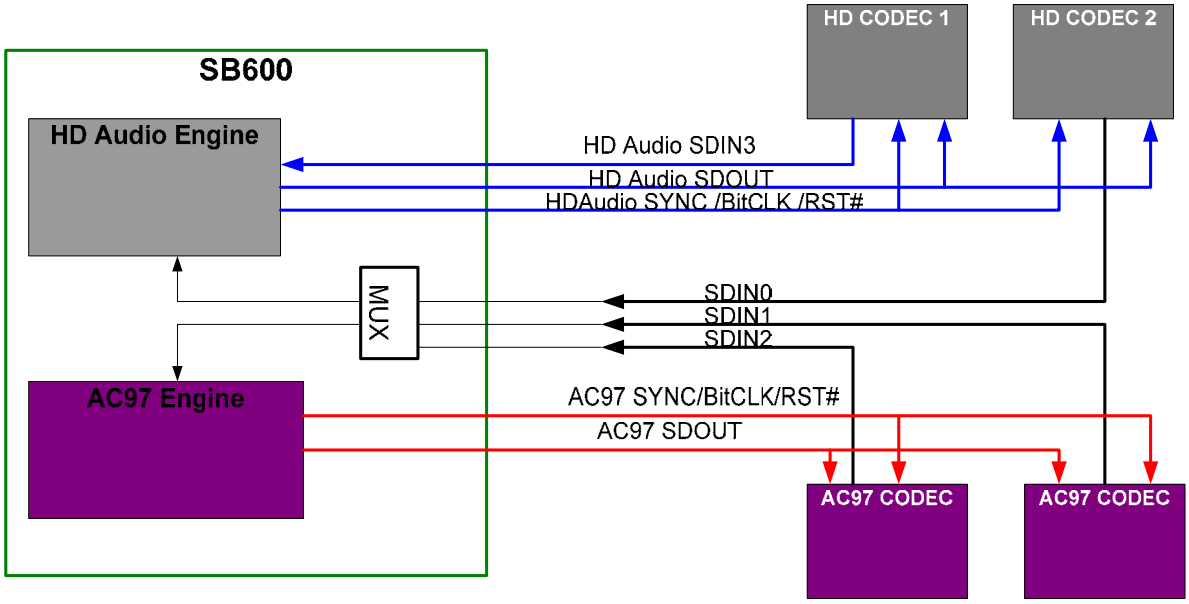


Figure 5-12: HD Audio and AC '97 Codec Connections for Mixed Configurations

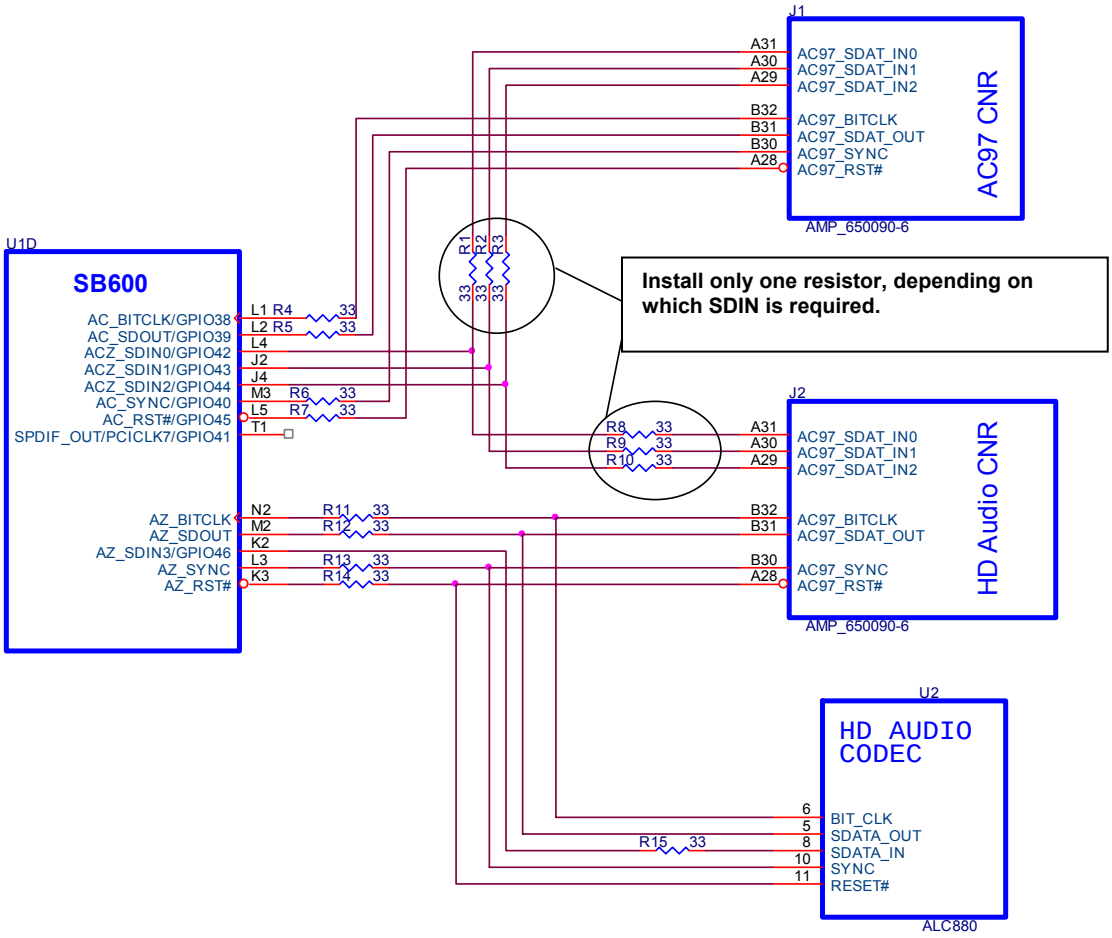


Figure 5-13: Schematic for HD Audio and AC '97 Codec Connections in a Mixed Configuration

5.8 General Events and GPIOs

Table 5-8: SMI, SCI, and Wake Event Support by GPIO and General Event Pins

Pin Name	SMI event	SCI event	Wake event
GPIO [0,2]	X	X	X
GPM [0:9]	X	X	X
GEVENTS [2:8]	X	X	X
EXTERNAL EVENTS [0:1]	X	X	X

The following table shows the state of the GPIO and GEVENT pins in different ACPI states. Note that even if some GPIOs are in the S5 domain, its functionality may not be maintained in the S5 state.

Table 5-9: Functionality of the General Events and GPIOs across ACPI States

GPIO / GEVENT	GPIO and G-Events Functionality across ACPI states			
	S0/S1	S2/S3	S4/S5	G3
EXTEVENT0#, GEVENT# [7:2]	Maintain state			Undefined
EXTEVENT1#	Maintain state		Undefined	
GPM [9:0]	Maintain state			Undefined
GPOC [1:0]	Maintain state		Undefined	
GPOC [3:2]	Maintain state			Undefined
GPIO [73:0]	Maintain state	Undefined		

Note: Except for GPIO1, all other GPIO and GPM pins are software configurable to assume alternate functions. Please refer to the GPIO section in the *SB600 Register Reference Guide* for information on how to configure the GPIO pins to alternate functions.

6 System Clock Specifications

6.1 System Clock Descriptions

Table 6-1: SB600 System Clock Descriptions

Clock Domain	Frequency	Source	Usage
PCIE_RCLKP, PCIE_RCLKN	100MHz	Main clock generator (external clock)	For PCIE differential input
SATA_X1, SATA_X2	25MHz	25MHz Crystal	For SATA Controllers
X1, X2	32KHz	32KHz Crystal	For RTC
14M_OSC	14.31818MHz	Main clock generator (external clock)	For Timer
USBCLK	48MHz	48MHz OSC or internal USB 48Mhz PLL	For USB Controllers and HD Audio
AC_BITCLK	12.288MHz	AC '97 codec	For AC '97 link generated by AC'97

6.2 System Clock Input Frequency Specifications

Table 6-2: SB600 System Clock Input Frequency Specifications

Clock	Frequency	Min	Max
14M_OSC	14.31818 MHz	14.315603 MHz	14.320757 MHz
USBCLK	48.000 MHz	47.995 MHz	48.005 MHz
SATA_X1, SATA_X2	25.000 MHz	24.997 MHz	25.005 MHz
AC_BITCLK	12.288MHz	The clock is supplied to SB by the external codec. 12.288MHz is its typical frequency.	

6.3 System Clock AC Specifications

Table 6-3 to *Table 6-8* list all the AC specifications of SB600 clocks at specific VIH/VIL combinations. The figure below illustrates the timing labels that appear in those tables.

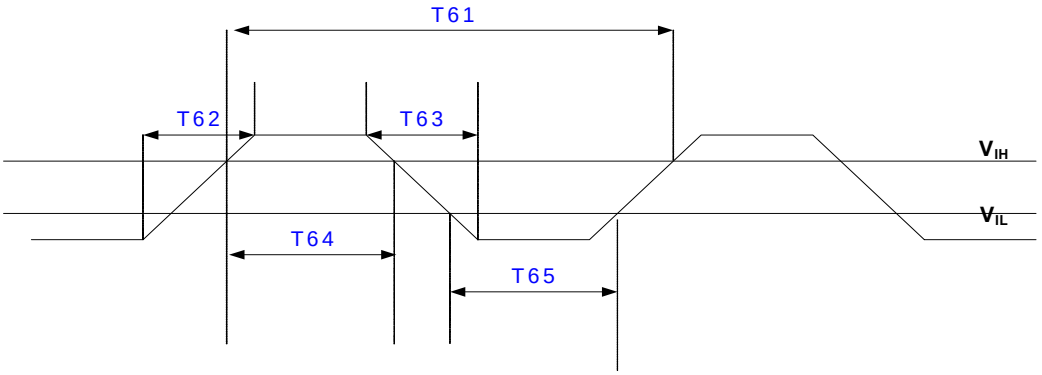


Figure 6-1: Timing Labels for AC Specifications of the SB600 Clocks

Table 6-3: 14 MHz OSC Reference Clock AC Specifications

14 MHz OSC Reference Clock					
Symbol	**Parameter**	**Min**	**Max**	**Units**	**Note**
T61	Clock Period	69.829	69.854	ns	1
T62	Clock/Data rise time	1	1.5	ns	2
T63	Clock/Data fall time	1	2	ns	
T64	Clock high period	30	38	ns	
T65	Clock low period	30	38	ns	
-	Cycle to Cycle Jitter	-	300	ps	-
-	Duty Cycle	40	60	%	-

Notes:
1 Clock frequency tolerance is +/- 180 ppm
2 VIL= 0.4V ; VILmax = 0.6V and VILmin = 0V
VIH = 2.4V; VIHmax=VDDR and VIHmin = 2.0V

Table 6-4: 48MHz USB/SIO Clock AC Specifications

48 MHz USB / SIO clock					
Symbol	**Parameter**	**Min**	**Max**	**Units**	**Note**
T61	Clock Period	20.831	20.836	ns	1
T62	Clock/Data rise time	0.5	1.5	ns	2
T63	Clock/Data fall time	0.5	1.5	ns	
T64	Clock high period	8.8	11	ns	
T65	Clock low period	7.7	10	ns	
-	Max Jitter	-	130	ps	-
-	Duty Cycle	45	55	%	-

Notes:
1 Clock frequency tolerance is +/- 100 ppm
2 VIL= 0.4V ; VILmax = 0.6V and VILmin = 0V
VIH = 2.4V; VIHmax=VDDR and VIHmin = 2.0V

Table 6-5: RTC X1 Clock AC Specifications

RTC X1 Clock					
Symbol	**Parameter**	**Min**	**Max**	**Units**	**Note**
T61	Clock Period	Typical at 32.7		KHz	1
T62	Clock/Data rise time	0.5	5	ns	2
T63	Clock/Data fall time	0.5	5	ns	
T64	Clock high period	13	17	ns	
T65	Clock low period	13	17	ns	
-	Cycle to Cycle Jitter		10	ns	
-	Duty Cycle	45	55	%	
-	Frequency Tolerance	-20	20	PPM	

Notes
1 Min/Max specifications depend on accuracy of the crystal used.
2 VIL= 0.25V ; VILmax = 250mV and VILmin = 0V
VIH = 0.75V; VIHmax=1V and VIHmin = 750mV

Table 6-6: LPC Clock AC Specifications

LPC Clock					
Symbol	**Parameter**	**Min**	**Max**	**Units**	**Note**
T61	Clock Period	30	33.3	ns	-
T62	Clock/Data rise time	-	3	ns	-
T63	Clock/Data fall time	-	3	ns	-
T64	Clock high period	12	-	ns	-
T65	Clock low period	12	-	ns	-

Table 6-7: PCI Clock AC Specifications

PCI Clock (8 clocks) PCICLK[7:0]					
Symbol	**Parameter**	**Min**	**Max**	**Units**	**Note**
T61	Clock Period	30	33.3	ns	-
T62	Clock/Data rise time	-	3.0	ns	-
T63	Clock/Data fall time	-	3.0	ns	-
T64	Clock high period	12	-	ns	-
T65	Clock low period	12	-	ns	-

Table 6-8: AC 97 Clock AC Specifications

AC97 Clock					
Symbol	**Parameter**	**Min**	**Max**	**Units**	**Note**
T61	Clock Period	Typical at 813.80		ns	1
T62	Clock/Data rise time	2.0	4.0	ns	-
T63	Clock/Data fall time	2.0	4.0	ns	-
T64	Clock high period	32.56	48.84	ns	-
T65	Clock low period	32.56	48.84	ns	-
-	Max Jitter	-	750	ps	-

Note 1: Nominal clock frequency is 12.288MHz.

7 States of Power Rails during ACPI S1 to S5 States

SB600 supports the ACPI states S1 to S5. Table 7-1 below shows the expected state of each power rail during these power states.

Table 7-1: State of Each Power Rail during ACPI S1 to S5 States

Pin name	Schematic Signal	ACPI STATE			
		S0	S1/S2	S3	S4/S5
VDDQ	3.3V I/O Power	+3.3V	+3.3V	0V	0V
VDD_CORE	VCORE_1.8	+1.2V	+1.2V	0V	0V
S5_1.2V	S5 Power	+1.2V	+1.2V	+1.2V	+1.2V
CPU_PWR	CPU Power	CPU	CPU	0V	0V
AVDDC	Analog USB 2.0 Pwr	+3.3V	+3.3V	+3.3V	+3.3V or 0V
AVDDTX[3:0] /AVDDRX[3:0]	USB_AVDD	+3.3V	+3.3V	+3.3V	+3.3V or 0V
USB_PHY_1.2V	USB Phy digital power	+1.2V	+1.2V	+1.2V	+1.2V or 0V
AVDD_SATA	SATA Power	+1.2V	+1.2V	0V	0V
PLLVDD_SATA	SATA PLL Power	+1.2V	+1.2V	0V	0V
XTLVDD_SATA	SATA XTAL Power	+3.3V	+3.3V	0V	0V
V5_VREF	+5V Ref Voltage	+5.0V	+5.0V	0V	0V
AVDDCK_3.3V	PLL Analog Power	+3.3V	+3.3V	0V	0V
AVDDCK_1.2V	PLL Digital Power	+1.2V	+1.2V	0V	0V
S5_3.3V	S5 I/O Power	+3.3V	+3.3V	+3.3V	+3.3V
PCIE_PVDD	PCI Express PLL Power	+1.2V	+1.2V	0V	0V
PCIE_VDDR	PCI Express I/O Power	+1.2V	+1.2V	0V	0V
SLP_S3#	SLP_S3#	+3.3V	+3.3V	0V	0V
SLP_S5#	SLP_S5#	+3.3V	+3.3V	+3.3V	0V
PWR_GOOD	SB_PWROK	+3.3V	+3.3V	0V	0V
SUS_STAT#	SUS_STAT#	0V	0V	0V	0V
RSMRST#	RSMRST#	+3.3V	+3.3V	+3.3V	+3.3V

8 Electrical Characteristics

Note: Values quoted in this section are preliminary and require further verification.

8.1 Absolute Maximum Ratings

Table 8-1 specifies the absolute maximum ratings that should never be exceeded. Exceeding the specified absolute maximum ratings may damage the ASIC. These ratings are guidelines for absolute worst case operating conditions and should not to be interpreted as recommended operating condition.

Table 8-1: Absolute Maximum Rating

Signal Name	Maximum Limits (V)	With respect to	Description
VDD_[12:1]	-0.5 to 1.32	VSS	Core power
VDDQ_[28:1]	-0.5 to 3.66	VSS	3.3V I/O Power
S5_1.2V_[4:1]	-0.5 to 1.32	VSS	1.2V S5 Power
S5_3.3V_[6:1]	-0.5 to 3.66	VSS	3.3V S5 Power
AVDDCK_3.3V	-0.5 to 3.66	AVSSCK	3.3V power for analog PLLs
AVDDCK_1.2V	-0.5 to 1.32	AVSSCK	1.2V power for analog PLLs
PCIE_PVDD	-0.5 to 1.32	PCIE_VSS	A-Link Express II PLL Power
PCIE_VDDR[13:1]	-0.5 to 1.32	PCIE_VSS	A-Link Express II Analog power
AVDD_SATA[15:1]	-0.5 to 1.32	AVSS_SATA	SATA Analog Power
PLLVDD_SATA_[2:1]	-0.5 to 1.32	AVSS_SATA	SATA PLL Power
XTLVDD_SATA	-0.5 to 1.32	AVSS_SATA	SATA XTAL Power
VBAT	-0.5 - 3.6V BAT	RTC_GND	RTC backup power
AVDDC	-0.5 to 3.66	AVSSC	Analog Power for USB PHY PLL
AVDDRX[4:0]	-0.5 to 3.66	AVSS_USB	Analog Power for USB PHY RX
AVDDTX[4:0]	-0.5 to 3.66	AVSS_USB	Analog Power for USB PHY TX
USB_PHY_1.2V[5:1]	-0.5 to 1.32	AVSS_USB	1.2V USB PHY standby Power
V5_VREF	-0.5 to 5.5	VSS	5V Reference voltage for PCI interface
Any 3.3V input signal	-0.5 to 3.66	VSS	See Section 3 for signal names
Any 3,3V 5V tolerant input signal	-05 to VREF+0.5	VSS	

8.2 Functional Operating Range

Use typical values between +/-5% on all input signals.

8.3 DC Characteristics

Table 8-2: DC Characteristic for Power Supplies to the SB600

Signal Name	Description	Min. Voltage	Typical Voltage	Max. Voltage	Unit
AVDDCK_1.2V	Core PLL digital power	1.14	1.2V	1.26	V
PCIE_PVDD	A-Link Express II PLL power	1.14	1.2V	1.26	V
PCIE_VDDR[13:1]	A-Link Express II power	1.14	1.2V	1.26	V
PLLVDD_SATA[2:1]	SATA PLL power	1.14	1.2V	1.26	V
AVDD_SATA[15:1]	SATA analog power	1.14	1.2V	1.26	V
S5_1.2V	Standby power	1.14	1.2V	1.26	V
USB_PHY_1.2V[5:1]	USB PHY standby power	1.14	1.2V	1.26	V
VDD[12:1]	Core voltage	1.14	1.2V	1.26	V
XTLVDD_SATA	SATA XTAL power	3.135	3.3V	3.465	V
VBAT	RTC backup power	2.5*	3.3	3.6	V
AVDDCK_3.3V	Core PLL analog power	3.135	3.3V	3.465	V
AVDDC	Analog power for USB PHY PLL	3.135	3.3V	3.465	V
AVDDRX[4:0]	Analog power for USB PHY	3.135	3.3V	3.465	V
AVDDTX[4:0]	Analog power for USB PHY	3.135	3.3V	3.465	V
S5_3.3v[6:1]	Core standby power	3.135	3.3V	3.465	V
VDDQ[28:1]	I/O power	3.135	3.3V	3.465	V
V5_VREF	5V reference voltage	4.75	5V	5.25	V

*** Note:** For VBAT below 2.5V, the battery-low error will occur. At 2.0V, the CMOS content may be lost.

Table 8-3: DC Characteristics for Interfaces on the SB600

Symbol	Parameter	Minimum	Maximum	Unit	Condition
GPIO					
VDD	Power Supply	3.135	3.46	V	
VIL	Input Low Voltage	-0.5	1.3	V	
VIH	Input High Voltage	1.8	VDD	V	
VOL	Output Low Voltage		0.4	V	IOL = 8.0mA
VOH	Output High Voltage	2.4		V	IOH = 8.0mA
ILI	Input Leakage Current		+/-10	µA	
CIN	Input Capacitance		10	pF	
PCI					
VDD	Power Supply	3.135	3.46	V	
V5REF	Reference	3.135	5.25	V	
VIL	Input Low Threshold	-0.5	0.3VDD	V	
VIH	Input High Threshold	0.5VDD	V5REF	V	
VOL	Output Low Voltage		0.4	V	IOL = 4.0mA
VOH	Output High Voltage	2.4		V	IOH=-4.0mA
ILI	Input Leakage Current		+/-10	µA	
CIN	Input Capacitance		10	pF	
IDE					

Symbol	Parameter	Minimum	Maximum	Unit	Condition
VDD	Power Supply (Driver & Receiver)	3.135	3.46	V	
VIH	Input High Voltage	0.5VDD	V5REF	V	
VIL	Input Low Voltage	-0.5	03VDD	V	
VOL	Output Low Voltage		0.662	V	IOL= 6mA
VOH	Output High Voltage	VDD-0.66		V	IOH=6mA
ILI	Input Leakage Current		+/-10	µA	Pull-up & pull-down Resistors disabled
CIN	Input Capacitance		10	pF	
CPU					
VCPU_IO	CPU IO Voltage	-	-	V	
VIL	Input Low Voltage	-0.15	0.58VCPU_IO	V	
VIH	Input High Voltage	0.73VCPU_IO	VCPU_IO	V	
VOL	Output Low Voltage	-0.15	0.25VCPU_IO	V	IOL = 4.0mA
VOH	Output High Voltage / Internal Pull-up Voltage		VCPU_IO	V	
ILI	Input Leakage Current		+/-10	µA	
CIN	Input Capacitance		10	pf	
LPC					
See values for the PCI pins.					
AC97					
AC_BITCLK—see values for IDE pins. AC_SDOUT, AC_STNC, SPIF_OUT—see values for PCI pins. ACZ_SDIN[2:0], AC_RST#—see values for GPIO pins.					

Table 8-4: GPIO/GEVENT Output DC Characteristics

Pin Name	Parameter	VOH	VOL
		Minimum	Maximum
All GPIO and GEVENT pins listed in Table 8-5	Output High Voltage	**2.4 V**	**—**
	Output Low Voltage	**—**	**0.4 V**
		Output Drive	
	Output Drive	**8 mA**	

Table 8-5: GPIO/GEVENT Input DC Characteristics

Pin Name	Voltage	VIL(V)		VIH (V)	
		Min	Max	Min	Max
SSMUXSEL/ SATA_IS3#/GPIO0	3.3V (5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
ROM_CS#/GPIO1	3.3V (5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
SPKR/GPIO2	3.3V (5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
FANOUT0/GPIO3	3.3V (5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
SMARTVOLT/ SATA_IS2#/GPIO4	3.3V(5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
SHUTDOWN#/ GPIO5/SMARTVOLT2	3.3V(5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
GHI#/ SATA_IS1#/GPIO6	3.3V(5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
WD_PWRGD/ GPIO7	3.3V(5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
DDC1_SDA/GPIO8	3.3V(5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25

Pin Name	Voltage	VIL(V)		VIH (V)	
		Min	Max	Min	Max
DDC1_SCL/GPIO9	3.3V(5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
SATA_IS0#/GPIO10	3.3V(5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
SPI_DO/GPIO11	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
SPI_DI/GPIO12	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
LAN_RST#/GPIO13	3.3V(5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
ROM_RST#/ GPIO14	3.3V(5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
IDE_D[15:0]/GPIO[30:15]	3.3V(5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
SPI_HOLD#/ GPIO31	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
SPI_CS#/GPIO32	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
INTE#/GPIO33	3.3V(5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
INTF#/GPIO34	3.3V(5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
INTG#/GPIO35	3.3V(5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
INTH#/GPIO36	3.3V(5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
DPSLP_OD#/ GPIO37	3.3V(5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
AC_BITCLK/ GPIO38	3.3V(5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
AC_SDOUT/ GPIO39	3.3V(5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
AC_SYNC/GPIO40	3.3V(5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
SPDIF_OUT/ PCICLK7/GPIO41	3.3V(5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
ACZ_SDIN0/ GPIO42	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
ACZ_SDIN1/ GPIO43	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
ACZ_SDIN2/ GPIO44	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
AC_RST#/GPIO45	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
AZ_SDIN3/GPIO46	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
SPI_CLK/GPIO47	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
FANOUT1/GPIO48	3.3V	-0.5	0.3* VDDQ	0.7*VDDQ	VDDQ + 0.25
FANOUT2/GPIO49	3.3V	-0.5	0.3* VDDQ	0.7*VDDQ	VDDQ + 0.25
FANIN0/GPIO50	3.3V	-0.5	0.3* VDDQ	0.7*VDDQ	VDDQ + 0.25
FANIN1/GPIO51	3.3V	-0.5	0.3* VDDQ	0.7*VDDQ	VDDQ + 0.25
FANIN2/GPIO52	3.3V	-0.5	0.3* VDDQ	0.7*VDDQ	VDDQ + 0.25
VIN[7:0]/GPIO[60:53]	3.3V	-0.5	0.3* VDDQ	0.7*VDDQ	VDDQ + 0.25
TEMPIN[2:0]/GPIO[63:61]	3.3V	-0.5	0.3* VDDQ	0.7*VDDQ	VDDQ + 0.25
TEMPIN3/TALERT#/GPIO 64	3.3V	-0.5	0.3* VDDQ	0.7*VDDQ	VDDQ + 0.25
BMREQ#/REQ5#/ GPIO65	3.3V	-0.5	0.3* VDDQ	0.7*VDDQ	VDDQ + 0.25
LLB#/GPIO66	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
SATA_ACT#/ GPIO67	3.3V	-0.5	0.3* VDDQ	0.7*VDDQ	VDDQ + 0.25
LDRQ1#/GNT5#/ GPIO68	3.3V(5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25

Pin Name	Voltage	VIL(V)		VIH (V)	
		Min	Max	Min	Max
RTC_IRQ#/GPIO69	S5_3.3V/VBAT	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
REQ3#/GPIO70	3.3V(5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
REQ4#/GPIO71	3.3V(5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
GNT3#/GPIO72	3.3V(5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
GNT4#/GPIO73	3.3V(5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
USB_OC[4:0]#/GPM[4:0]#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
USB_OC5#/DDR3_RST#/ GPM5#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
BLINK/GPM6#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
SYS_RESET#/ GPM7#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
USB_OC8#/ AZ_DOCK_RST#/ GPM8#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
USB_OC9#/SLP_S2/GPM 9#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
RI#/EXTEVENT0#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
LPC_SMI#/ EXTEVENT1#	3.3V(5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
SMBALERT#/THRMTRIP# /GEVENT2#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
LPC_PME#/ GEVENT3#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
PCI_PME#/ GEVENT4#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
S3_STATE/ GEVENT5#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
USB_OC6#/ GEVENT6#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
USB_OC7#/ GEVENT7#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
WAKE#/GEVENT8#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
SCL0/GPOC0#	3.3V(5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
SDA0/GPOC1#	3.3V(5V Tolerance)	-0.5	0.3* VDDQ	0.7*VDDQ	V5_Ref + 0.25
SCL1/GPOC2#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25
SDA1/GPOC3#	S5_3.3V	-0.5	0.3* S5_3.3V	0.7* S5_3.3V	S5_3.3V + 0.25

8.4 RTC Battery Current Consumption

The RTC battery current consumption is measured as follows:

Table 8-6: RTC Battery Current Consumption

Power States	RTC Battery Current	
	Typical	Maximum
G3 (Off), S0-S5	< 0.5 µA	< 3 µA

RTC battery life is calculated using the rated capacity of the battery and the measured maximum current consumption. RTC battery's are normally rated for 170 mAh and the worst case current consumption for the SB600 is 3.0 µA. Thus, the expected minimum life of battery will be as follows:

170,000 µA / 3 µA = 56,667 h = 6.5 years

9 Power Requirements

Table 9-3 to *Table 9-5* indicate the power activity of the SB600 Rev A13 for each of configurations 1 to 7, described in *Table 9-1* below. Configuration 1 gives measurements for idle status on a mobile system. Configuration 2, 4, and 6 give measurements of minimum activity with system idle status for specific hardware setups, and configuration 3, 5, and 7 give measurements of maximum power activity for the same setups.

Measurements are divided into two categories:

Average Power Dissipation—calculated average power based on sample readings taken every 2 seconds during the test.

Maximum (Peak) Power Dissipation—measured maximum power reading recorded among the sample readings.

In each category, two subcategories are used to record power data: Normal Activity indicates power recording with system running normally, and Maximum Activity shows SB600's maximum power affordability.

All test measurements are taken at 25 °C with no CPU airflow, and the measurement tolerance is ± 5%.

Note: A heat sink is required for the SB600 if the case temperature exceeds 105 ºC. The case temperature should be measured using a thermal couple diode connected to the centre at the top of the SB600 with the system in the enclosed production case and configured with all internal and external devices enabled. Application software or a test utility should be used to exercise all devices and interfaces connected to the SB600 when measuring the case temperature. More details on how to select the correct heat sink can be found in the *SB600 Thermal Design Guide* (TDG-SB600-01) that is available at AMD's Partner Resource Center.

Table 9-1: Configuration Set Up for SB600 Power Activity Test

Configuration #	Hardware	System Activity
1	USB and SATA disabled in BIOS 1 HDD IDE Drive connected Enabled A-Link X2	Windows idle for mobile
2	USB and SATA Controllers* enabled in BIOS 2 USB 1.1 devices connected to the system 1IDE ODD Drive + 1x1.5G SATA Drive connected Enabled A-Link X2	Windows idle for mobile/desktop
3		Third party and internal AMD software used to create maximum activity on a mobile system.
4	USB and SATA Controllers * enabled in BIOS 4 USB 2.0 devices (2xUSB1.1 and 2xUSB 2.0)connected to the system 1 IDE ODD Drive + 1x1.5G SATA Drive connected Enabled A-Link X2.	Windows idle for mobile.
5		Third party and internal AMD software used to create maximum activity on a mobile system.
6	USB and SATA Controllers * enabled in BIOS 4 USB 2.0 devices (2xUSB1.1 and 2xUSB 2.0)connected to the system 1 IDE ODD Drive + 1x1.5G SATA Drive connected Enabled A-Link X2 1 External PCI(LAN) connected	Windows idle for desktop.
7		Third party and internal AMD software used to create maximum activity on a desktop system.

Note: *The SATA controller supports 4 ports, but only one port is active.

Table 9-2: Power Activity under Configuration 1

	Average power (mA)	Maximum Power (mA)
S0 1.2V		
VDD	185.61	189.7
PCIE_PVDD	28.2	28.49
PCIE_VDDR	177.25	177.55
PLLVDD_SATA	4.25	4.41
AVDD_SATA	3.13	3.32
AVDDCK_1.2V	31.67	31.91
TOTAL S0_1.2V	**430.11**	**435.38**
S5 1.2V		
S5_1.2V	17.64	21.81
USB_PHY_1.2V	0.23	2.42
TOTAL S5 1.2V	**17.87**	**24.23**
S0 3.3V		
AVDDC	0.12	0.46
XTLVDD_SATA	0	0
VDDQ	81.01	85.17
AVDD	0	0.17
TOTAL S0_3.3 V	**81.13**	**85.8**
S5 3.3V		
S5_3.3V	6.88	8.94
AVDDTX	0.1	0.42
AVDDRX	0	0.18
AVDDCK_3.3V	4.68	4.85
TOTAL S5 3.3V	**11.66**	**14.39**
Other Voltages		
CPU_PWR (1.05V)	0.11	2.2
V5_VREF (5V)	0.15	2.27
Total Current (mA)	**541.03**	**564.27**
Total Power (W)	**0.845**	**0.868**
Case Temp (ºC)	**28.4**	**28.5**

Table 9-3: Power Activity under Configuration 2 and 3

	Average power (mA)		Maximum Power (mA)	
	Minimum Activity	Maximum Activity	Minimum Activity	Maximum Activity
S0 1.2V				
VDD	301.3	306.43	312.23	314.71
PCIE_PVDD	27.83	28.04	28.38	28.6
PCIE_VDDR	252.46	252.51	252.86	252.88
PLLVDD_SATA	53.1	53.56	54.08	54.1
AVDD_SATA	75.06	75.29	75.79	75.84
AVDDCK_1.2V	31.5	31.46	31.91	32.03
TOTAL S0_1.2V	**741.25**	**747.29**	**755.25**	**758.16**
S5 1.2V				
S5_1.2V	59.77	59.88	66.71	67.79
USB_PHY_1.2V	5.25	10.56	17.31	18.21
TOTAL S5 1.2V	**65.02**	**70.44**	**84.02**	**86**
S0 3.3V				
AVDDC	9.86	10.39	10.38	10.48

	Average power (mA)		Maximum Power (mA)	
	Minimum Activity	Maximum Activity	Minimum Activity	Maximum Activity
XTLVDD_SATA	1.11	1.36	1.43	1.45
VDDQ	80.32	81.41	88.88	89.37
AVDD	0	0.02	0.35	0.36
TOTAL S0_3.3 V	**91.29**	**93.18**	**101.04**	**101.66**
S5 3.3V				
S5_3.3V	6.59	6.55	11.33	11.5
AVDDTX	7.73	8.93	8.28	11.55
AVDDRX	15.6	15.87	16.05	16.12
AVDDCK_3.3V	4.7	4.97	5	5.06
TOTAL S5 3.3V	**34.62**	**36.32**	**40.66**	**44.23**
Other Voltages				
CPU_PWR (1.05V)	0.07	0.09	4.67	4.74
V5_VREF (5V)	0.01	0.14	4.5	4.71
Total Current (mA)	**932.26**	**947.46**	**990.14**	**999.5**
Total Power (W)	**1.39**	**1.4**	**1.45**	**1.47**
Case Temp (ºC)	**30.4**	**30.9**	**30.9**	**31**

Table 9-4: Power Activity under Configuration 4 and 5

	Average power (mA)		Maximum Power (mA)	
	Minimum Activity	Maximum Activity	Minimum Activity	Maximum Activity
S0 1.2V				
VDD	307.63	315.63	317.67	325.11
PCIE_PVDD	28.23	28.82	28.33	28.34
PCIE_VDDR	252.44	252.45	252.76	252.82
PLLVDD_SATA	53.31	53.39	54.09	54.1
AVDD_SATA	75.26	75.78	75.78	75.79
AVDDCK_1.2V	31.39	31.27	31.91	31.97
TOTAL S0_1.2V	**748.26**	**757.34**	**760.54**	**768.13**
S5 1.2V				
S5_1.2V	67.6	67.61	69.6	73.87
USB_PHY_1.2V	27.59	27.96	32	32.61
	95.19	**95.57**	**101.6**	**106.48**
S0 3.3V				
AVDDC	10.08	10.43	10.43	10.43
XTLVDD_SATA	1.34	1.39	1.41	1.42
VDDQ	80.93	83.53	88.13	89.09
AVDD	0.01	0.05	0.34	0.36
TOTAL S0_3.3 V	**92.36**	**95.4**	**100.31**	**101.3**
S5 3.3V				
S5_3.3V	9.29	9.66	11.4	11.52
AVDDTX	50.76	52.46	51.45	57.34
AVDDRX	57.82	58.01	58.35	58.91
AVDDCK_3.3V	4.27	4.45	5.15	5.2
TOTAL S5 3.3V	**122.14**	**124.58**	**126.35**	**132.97**
Other Voltages				
CPU_PWR (1.05V)	0.19	0.19	4.38	4.58
V5_VREF (5V)	0.17	0.19	4.43	4.78

	Average power (mA)		Maximum Power (mA)	
	Minimum Activity	Maximum Activity	Minimum Activity	Maximum Activity
Total Current (mA)	1058.31	1073.27	1097.61	1118.24
Total Power (W)	1.72	1.74	1.76	1.78
Case Temp (ºC)	31.4	31.6	31.5	31.7

Table 9-5: Power Activity under Configuration 6 and 7

	Average power (mA)		Maximum Power (mA)	
	Minimum Activity	Maximum Activity	Minimum Activity	Maximum Activity
S0 1.2V				
VDD	310.92	322.78	332.19	334.19
PCIE_PVDD	27.63	27.91	28.28	28.37
PCIE_VDDR	250.2	250.28	250.58	250.59
PLLVDD_SATA	53.37	53.56	54.02	54.12
AVDD_SATA	90.04	90.43	90.51	90.52
AVDDCK_1.2V	31.57	31.57	31.87	31.92
TOTAL S0_1.2V	**763.73**	**776.53**	**787.45**	**789.71**
S5 1.2V				
S5_1.2V	65.14	65.85	73.07	73.91
USB_PHY_1.2V	47.17	45.86	53.32	54.1
	112.31	**111.71**	**126.39**	**128.01**
S0 3.3V				
AVDDC	10.2	10.22	10.62	10.66
XTLVDD_SATA	1.33	1.37	1.4	1.45
VDDQ	83.64	84.64	95.66	96.13
AVDD	0	0.04	0.38	0.39
TOTAL S0_3.3 V	**95.17**	**96.27**	**108.06**	**108.63**
S5 3.3V				
S5_3.3V	6.92	7.97	11.23	12.78
AVDDTX	110.02	110.43	110.78	112.59
AVDDRX	119.95	120.08	120.49	121.17
AVDDCK_3.3V	4.45	4.72	5.08	5.18
TOTAL S5 3.3V	**241.34**	**243.2**	**247.58**	**251.72**
Other Voltages				
CPU_PWR (1.05V)	0.17	0.25	4.31	4.81
V5_VREF (5V)	0.15	0.36	4.95	5.14
Total Current (mA)	1212.87	1228.32	1278.74	1288.02
Total Power (W)	2.17	2.18	2.22	2.46
Case Temp (ºC)	32.6	32.8	32.7	33

Table 9-6 below lists results of power consumption measurements for a fully loaded system (testing configuration: 4 x SATA 3.0G drives, 9x USB devices, 2 x IDE devices , 1 Floppy Drive, 2x PCI add on cards, on board AC97 Audio enabled).

Table 9-6: Power Activity for SB600 under a Fully Loaded System Configuration

	Average power (mA)		Maximum Power (mA)			
	Normal Activity	Maximum Activity	Minimum Activity	Maximum Activity	S3	S5
S0 1.2V						
VDD	403.45	406.39	414.93	423.12	0	0
PCIE_PVDD	27.65	27.72	27.92	27.86	0	0
PCIE_VDDR	388.16	390.71	391.01	390.82	0	0
PLLVDD_SATA	53.77	54.04	54.33	54.17	0	0
AVDD_SATA	242.94	243.86	244.62	244.53	0	0
AVDDCK_1.2V	31.16	31.25	31.41	31.28	0	0
TOTAL S0_1.2V	**1147.13**	**1153.97**	**1164.22**	**1171.78**	**0**	**0**
S5 1.2V						
S5_1.2V	66.27	66.4	67.46	70.73	1.25	1.2
USB_PHY_1.2V	75.41	75.44	76.42	77.55	0	0
TOTAL S5 1.2V	**141.68**	**141.84**	**143.88**	**148.28**	**1.25**	**1.2**
S0 3.3V						
AVDDC	10.44	10.44	10.47	10.71	0	0
XTLVDD_SATA	1.03	1.04	1.05	1.19	0	0
VDDQ	96.06	96.77	100.36	117.6	0	0
AVDD	0.01	0.03	0.07	0.19	0	0
TOTAL S0_3.3 V	**107.54**	**108.28**	**111.95**	**129.69**	**0**	**0**
S5 3.3V						
S5_3.3V	6.77	6.85	11.03	7.2	5.87	5.84
AVDDTX	190.56	190.59	190.73	191.49	11.52	11.51
AVDDRX	201.28	201.29	201.4	203.34	0	0
AVDDCK_3.3V	4.69	4.7	4.79	4.86	0	0
TOTAL S5 3.3V	**403.3**	**403.43**	**407.95**	**406.89**	**17.39**	**17.35**
Other Voltages						
CPU_PWR (1.05V)	0.06	0.14	1.55	4.24	0	0
V5_VREF (5V)	0.19	0.68	0.56	2.53	0	0
Total Current (mA)	**1799.9**	**1808.34**	**1830.11**	**1863.41**	**18.64**	**18.55**
Total Power (W)	**3.239**	**3.242**	**3.262**	**3.314**	**0.059**	**0.059**
Case Temp (ºC)	**38.6**	**39.8**	**39.9**	**40.3**	**25.8**	**25.8**

10 Package Information

10.1 Physical Dimensions

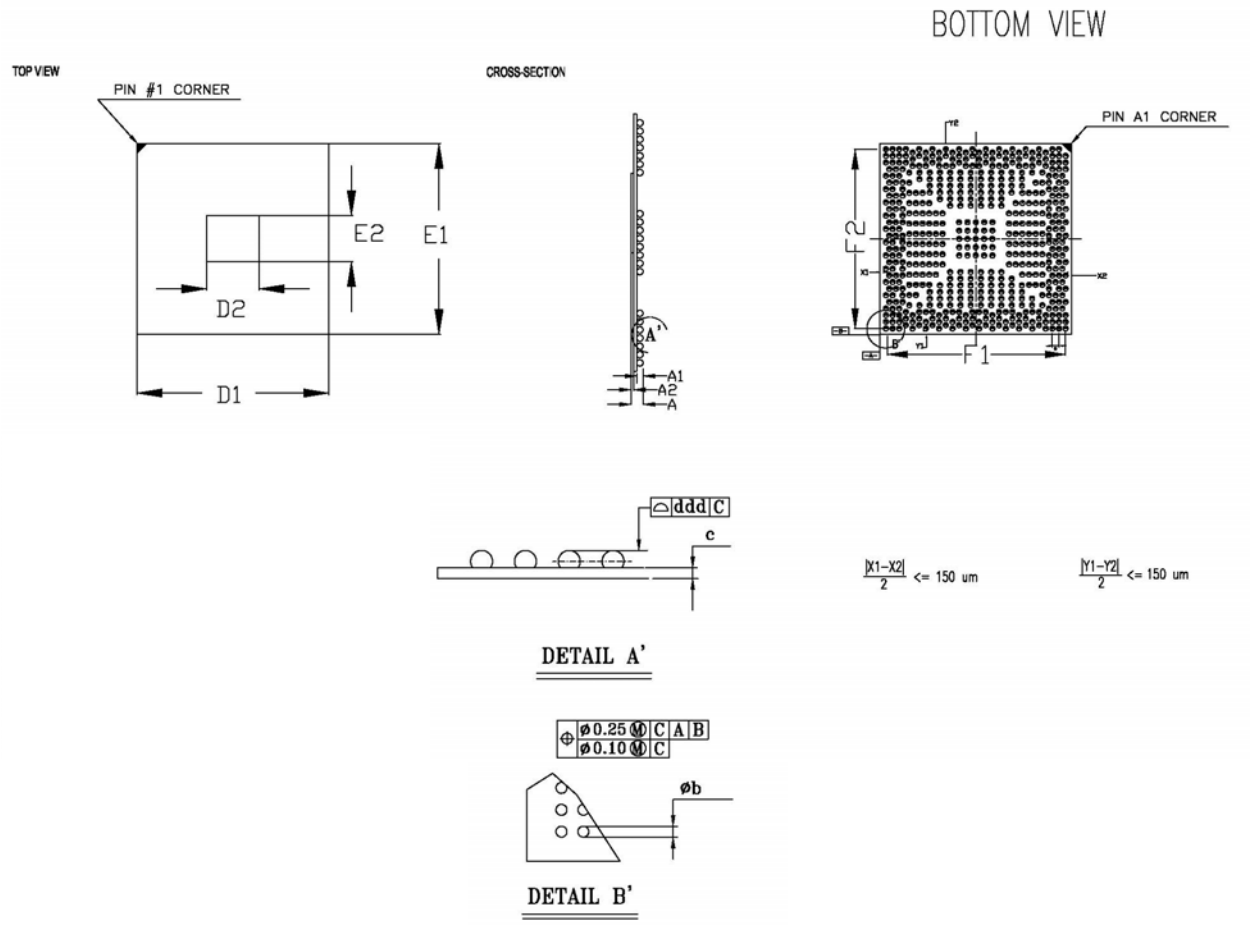


Figure 10-1: SB600 23 mm x 23 mm 0.8 mm Pitch 549-FCBGA Package Outline*

* **Note:** This diagram does not show the ball at position A1, which only exists on ASIC A11. See the product advisory titled *SB600 Ball-Out Change Notice* (AN_IXP600AA1) for details.

Table 10-1: SB600 Package Physical Dimensions

Ref.	Min(mm)	Nominal (mm)	Max. (mm)
c	0.96	1.06	1.16
A**	2.18	2.33	2.48
A1	0.30	0.40	0.50
A2	0.84	0.87	0.90
ϕb	0.40	0.50	0.60
D1	22.80	23.00	23.20
D2	-	6.37	-
E1	22.80	23.00	23.20
E2	-	5.62	-
F1	-	21.60	-
F2	-	21.60	-
e	-	0.80	-
ddd	-	-	0.15

**Note: Dimension of "A" subject to change according to actual measurement.

10.2 Pressure Specification

To avoid damages to the ASIC (die or solder ball joint cracks) caused by improper mechanical assembly of the cooling device, follow the recommendations below:

- It is recommended that the maximum pressure which is evenly applied across the contact area between the thermal management device and the die does not exceed 40 PSI. Note that a contact pressure of 30-40 PSI is adequate to secure the thermal management device and achieve the lowest thermal contact resistance with a temperature drop across the thermal interface material of no more than 3°C. Also, the surface flatness of the metal spreader should be 0.001 inch/1 inch.
- Pre-test the assembly fixture with a strain gauge to make sure that the flexing of the final assembled board and the pressure applying around the ASIC package will not exceed 600 micron strain under any circumstances.
- Ensure that any distortion (bow or twist) of the board after SMT and cooling device assembly is within industry guidelines (IPC/EIA J-STD-001). For measurement method, refer to the industry approved technique described in the manual IPC-TM-650, section 2.4.22.

11 Thermal Information

This section describes some key thermal parameters of the SB600. For a detailed discussion on these parameters and other thermal design descriptions including package level thermal data and analysis, please consult the *Thermal Design and Analysis Guidelines for SB600.*

Table 11-1: SB600 Thermal Limits

Parameter	Minimum	Nominal	Maximum	Unit	Note
Operating Case Temperature	0	—	105	°C	1
Absolute Rated Junction Temperature	—	—	125	°C	2
Storage Temperature	-40	—	60	°C	
Ambient Temperature	0	—	45	°C	3
Thermal Design Power	—	4.0	—	W	4

Notes:
1 - The maximum operating case temperature is the die geometric top-center temperature measured through proper thermal contact to the back side of the die based on the methodology given in the document *Thermal Design and Analysis Guidelines for SB600* (Chapter 11). This is the temperature at which the functionality of the chip is qualified.
2 - The maximum absolute rated junction temperature is the junction temperature at which the device can operate without causing damage to the ASIC. This temperature can be measured via the integrated thermal diode described in the next section.
3 - The ambient temperature is defined as the temperature of the local intake air to the thermal management device. The maximum ambient temperature is dependent on the heat sink's local ambient conditions as well as the chassis' external ambient, and the value given here is based on AMD's reference desktop heat sink solution for the SB600. Refer to Chapter 5 in the *Thermal Design and Analysis Guidelines for SB600* for heatsink and thermal design guidelines. Refer to Chapter 6 of the above mentioned document for details of ambient conditions.
4 - Thermal Design Power (TDP) is defined as the highest power dissipated while running currently available worst case applications at nominal voltages. Since the core power of modern ASICs using 65nm and smaller process technology can vary significantly, parts specifically screened for higher core power were used for TDP measurement. The TDP is intended only as a design reference, and the value given here is preliminary.

12 Testability

12.1 Test Control Signals

Table 12-1 below shows the signals used for the integrated test controller of the SB600.

Table 12-1: Signals for the Test Controller of the SB600

Signal Name	Ball Ref.	Description
14M_OSC	A23	14.318Mhz Reference Clock.
TEST0	G9	Test0 input.
TEST1	E9	Test1 input.
TEST2	F9	Test2 input.

Table 12-2 shows how Test[2:0] are used to select the normal operation, ASIC debug, or test mode.

Table 12-2: Test Mode Signals

TEST2	TEST1	TEST0	Test Mode	Description
0	0	0	None	Normal operation
0	0	1	Reserved	Reserved for ASIC debug
0	1	x	Test Mode	EnableTest Mode
1	X	X	Reserved	Reserved for ASIC debug

When TEST2 is low, a low on TEST1 will reset all test logic and allow TEST0 to choose between normal operation and the reserved debug mode. A high on TEST1 should be followed by a bit sequence on TEST0 to define the test mode into which the SB600 will enter. A new test mode can be entered when a new bit sequence is transmitted. In addition to resetting the test controller asynchronously with TEST1, a bit sequence can also be used to synchronously change the test mode. *Table 12-3* shows the legal bit sequences for TEST0.

Table 12-3: TEST0 Bit Sequence

TEST0 bit sequence	Test Mode
11111	Look for first 0 to define a new test mode
00000	Reserved
00001	Alt Pull High Test
00010	Pull Outputs High
00011	Pull Outputs Low
00100	Pull Outputs to Z
00101	XOR Test Mode

Figure 12-1 illustrates the data timing for the test signals with respect to the OSC clock. Note that once TEST1 is set to one, TEST0 needs to be asserted to one for at least 8 clocks before transmitting the test mode bit sequence. The rising of “Internal Test Mode” in the diagram indicates the time when the SB600 enters into test mode.

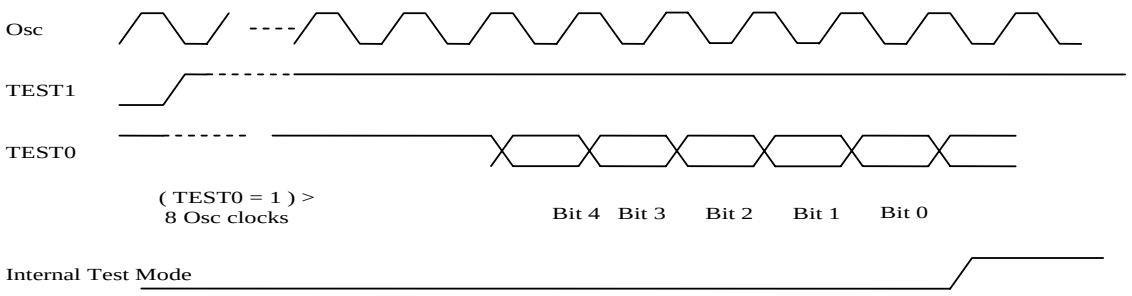


Figure 12-1 Test Mode Capturing Sequence Timing

12.2 XOR Chain Test Mode

12.2.1 Brief Description of an XOR Chain

A sample of a generic XOR chain is shown in the figure below.

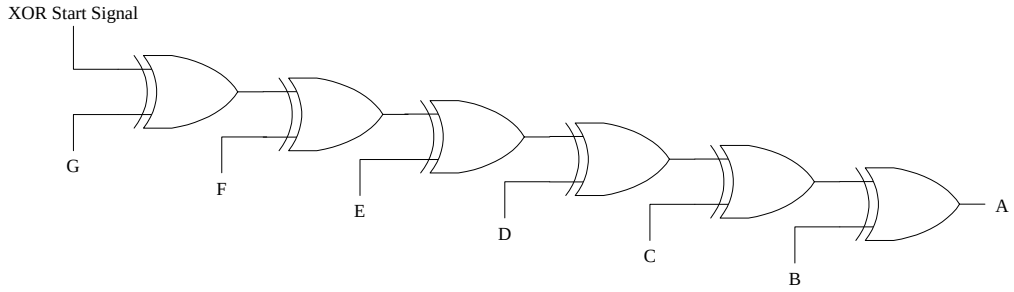


Figure 12-2: A Generic XOR Chain

Pin A is assigned to the output direction, and pins B through F are assigned to the input direction. It can be seen that after all pins from B to F are assigned to logic 0 or 1, a logic change in any one of these pins will toggle the output pin A.

The following is the truth table for the XOR Chain shown in *Figure 12-2.* The XOR start signal is assumed to be logic 1.

Table 12-4: Truth Table for an XOR Chain

Test Vector number	Input Pin G	Input Pin F	Input Pin E	Input Pin D	Input Pin C	Input Pin B	Output Pin A
1	0	0	0	0	0	0	1
2	1	0	0	0	0	0	0
3	1	1	0	0	0	0	1
4	1	1	1	0	0	0	0
5	1	1	1	1	0	0	1
6	1	1	1	1	1	0	0
7	1	1	1	1	1	1	1

12.2.2 Description of the SB600 XOR Chain

During XOR Chain Test Mode, most of the chip pads on the SB600 are connected together using XOR gates as shown in *Figure 12-3*. The first input of the chain is connected to a logic level high, and all pads are configured as inputs except for the last pad in the chain, which is configured as an output. AD6/ROMA12 is the start of the chain and FRAME# is the end of the chain. *Table 12-5* lists all pads that are on the SB600 XOR chain, as well as and their order of connection. Pads are chained together in the shown order, i.e., pad number 1 is the first pad on the XOR chain, pad number 2 the second, and so on.

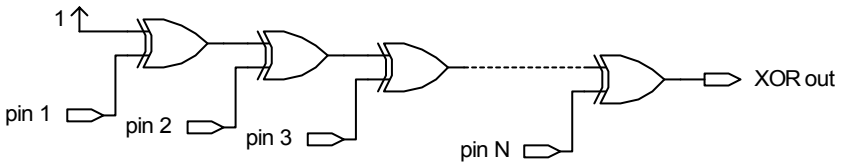


Figure 12-3: On-chip XOR Chain connectivity

Table 12-5: List of Pins on the SB600 XOR Chain and the Order of Connection

XOR #	Pin Name	Pin #
1	AD6/ROMA12	AA6
2	AD31	AG1
3	AD27	AH1
4	AD8/ROMA9	AA7
5	AD23/ROMD7	AH3
6	GNT1#	AF2
7	INTH#/GPIO36	AF3
8	AD25	AH2
9	AD28	AD2
10	AD29	AG2
11	INTG#/GPIO35	AF4
12	AD7/ROMA11	AC5
13	INTF#/GPIO34	AF1
14	AD21/ROMD5	AJ3
15	AD12/ROMA5	AD4
16	IRDY#	AG5
17	AD10/ROMA7	AC7
18	AD15/ROMA2	AC9
19	REQ1#	AE2
20	AD19/ROMD3	AH4
21	LOCK#	AF6
22	CBE2#/ROMWE#	AJ5
23	GNT4#/GPIO73	AG4
24	REQ4#/GPIO71	AH5
25	AD11/ROMA6	AJ7
26	CPU_STP#/DPSLP_3V#	AH9
27	GNT0#	AD11
28	CLKRUN#	AG7
29	AD14/ROMA3	AE6
30	CBE3#	AG3
31	DEVSEL#/ROMA0	AH6
32	A_RST#	AG10

XOR #	Pin Name	Pin #
33	AD13/ROMA4	AB11
34	GNT2#	AH7
35	SATA_ACT#/GPIO67	AC12
36	SERR#	AC11
37	AD17/ROMD1	AJ4
38	PCIRST#	AJ9
39	REQ0#	AJ8
40	PERR#	AG8
41	CBE1#/ROMA1	AF9
42	GNT3#/GPIO72	AB12
43	REQ2#	AG9
44	REQ3#/GPIO70	AH8
45	LAD1	AG25
46	LAD3	AH25
47	SERIRQ	AF23
48	LDRQ0#	AJ24
49	LAD2	AH24
50	KBRST#	AG26
51	LAD0	AG24
52	GA20IN	AF26
53	LDRQ1#/GNT5#/GPIO68	AH26
54	LFRAME#	AF24
55	IDE_D7/GPIO22	AJ27
56	IDE_D14/GPIO29	AD25
57	IDE_D9/GPIO24	AG27
58	IDE_D10/GPIO25	AG28
59	IDE_D8/GPIO23	AH27
60	IDE_D1/GPIO16	AD26
61	IDE_D3/GPIO18	AF27
62	IDE_D13/GPIO28	AE28
63	IDE_D6/GPIO21	AJ28
64	IDE_D12/GPIO27	AF29

XOR #	Pin Name	Pin #
65	IDE_IOR#	AC29
66	IDE_CS1#	W28
67	IDE_DRQ	AC27
68	IDE_D5/GPIO20	AH28
69	IDE_D11/GPIO26	AF28
70	IDE_D4/GPIO19	AG29
71	IDE_D2/GPIO17	AE29
72	IDE_IOW#	AC28
73	IDE_CS3#	W27
74	IDE_IRQ	AA28
75	IDE_DACK#	AB28
76	IDE_A1	AB27
77	IDE_A2	Y28
78	IDE_D0/GPIO15	AD28
79	IDE_D15/GPIO30	AD29
80	IDE_A0	AA29
81	IDE_IORDY	AB29
82	STPCLK#/ ALLOW_LDTSTP	AA25
83	A20M#/SID	AA26
84	SLP#/LDT_STP#	AA23
85	FERR#	Y27
86	LDT_RST#/ DPRSTP#/PROCHOT#	AC25
87	DDC1_SCL/GPIO9	D26
88	DPRSLPVR	W23
89	BMREQ#/REQ5#/GPIO65	W22
90	ROM_CS#/GPIO1	A26
91	SPKR/GPIO2	B26
92	LPC_SMI#/EXTEVNT1#	C25
93	DPSLP_OD#/GPIO37	B24
94	DDC1_SDA/GPIO8	C26
95	SHUTDOWN#/GPIO5/ SMARTVOLT2	D23
96	LAN_RST#/GPIO13	C23
97	SDA0/GPOC1#	B28
98	SATA_IS0#/GPIO10	C28
99	SSMUXSEL/ SATA_IS3#/GPIO0	A27
100	SCL0/GPOC0#	C27
101	WD_PWRGD/GPIO7	A23
102	SMARTVOLT/ SATA_IS2#/GPIO4	B27
103	GHI#/SATA_IS1#/GPIO6	B29
104	RTC_IRQ#/GPIO69	F5
105	SUS_STAT#	B3
106	USB_OC8#/AZ_DOCK _RST#/GPM8#	C5
107	LPC_PME#/GEVENT3#	D7
108	USB_OC5#/DDR3_RST# /GPM5#	B6
109	USB_OC9#/SLP_S2/ GPM9#	C6

XOR #	Pin Name	Pin #
110	BLINK/GPM6#	C2
111	USB_OC2#/GPM2#	C7
112	PWR_BTN#	E3
113	PCI_PME#/GEVENT4#	A3
114	USB_OC6#/GEVENT6#	B4
115	USB_OC0#/GPM0#	A8
116	SPI_CS#/GPIO32	G6
117	SPI_CLK/GPIO47	G3
118	SPI_DI/GPIO12	J3
119	SPI_DO/GPIO11	J6
120	RI#/EXTEVNT0#	B2
121	USB_OC7#/GEVENT7#	C4
122	USB_OC1#/GPM1#	B8
123	SPI_HOLD#/GPIO31	G2
124	USB_OC4#/GPM4#	A6
125	ROM_RST#/GPIO14	G5
126	SMBALERT#/THRM TRIP#/GEVENT2#	G7
127	SYS_RESET#/GPM7#	F4
128	S3_STATE/GEVENT5#	D9
129	SDA1/GPOC3#	F3
130	SCL1/GPOC2#	C3
131	LLB#/GPIO66	A4
132	WAKE#/GEVENT8#	E7
133	AC_RST#/GPIO45	L5
134	ACZ_SDIN0/GPIO42	L4
135	ACZ_SDIN2/GPIO44	J4
136	ACZ_SDIN1/GPIO43	J2
137	AZ_RST#	K3
138	AZ_SDIN3/GPIO46	K2
139	TEMPIN1/GPIO62	P8
140	TEMPIN0/GPIO61	P7
141	VIN6/GPIO59	M7
142	VIN1/GPIO54	L7
143	VIN2/GPIO55	M8
144	VIN4/GPIO57	M6
145	VIN0/GPIO53	V5
146	VIN5/GPIO58	P4
147	TEMPIN2/GPIO63	T8
148	VIN7/GPIO60	V7
149	VIN3/GPIO56	V6
150	TEMPIN3/TALERT#/ GPIO64	T7
151	AZ_SYNC	L3
152	AZ_BITCLK	N2
153	AZ_SDOUT	M2
154	FANIN0/GPIO50	N3
155	FANIN1/GPIO51	P2
156	FANIN2/GPIO52	W4
157	FANOUT1/GPIO48	T3
158	FANOUT2/GPIO49	V4
159	AC_SDOUT/GPIO39	L2
160	AC_BITCLK/GPIO38	L1

XOR #	Pin Name	Pin #
161	AC_SYNC/GPIO40	M3
162	SPDIF_OUT/PCICLK7/ GPIO41	T1
163	PCICLK6	V1
164	PCICLK0	U2
165	PCICLK5	U3
166	PCICLK2	U1
167	PCICLK1	T2
168	PCICLK4	W3
169	PCICLK3	V2
170	AD1/ROMA17	Y1
171	AD0/ROMA18	W7
172	AD4/ROMA14	AA5
173	AD3/ROMA15	W5
174	STOP#	Y2
175	TRDY#/ROMOE#	AA1

XOR #	Pin Name	Pin #
176	AD20/ROMD4	AB2
177	AD16/ROMD0	AA3
178	AD18/ROMD2	AB1
179	INTE#/GPIO33	AD3
180	AD2/ROMA16	W8
181	AD22/ROMD6	AB3
182	AD9/ROMA8	AC3
183	AD24	AC1
184	AD5/ROMA13	Y3
185	CBE0#/ROMA10	AB9
186	PAR/ROMA19	AF7
187	AD30	AD1
188	AD26	AC2
189	FRAME#	AA2

12.2.2.1 Unused Pins

The pins that are part of the XOR chain (see *Table 12-5*) but are not used for testing must be pulled up or down before the XOR chain is activated. No pins in the XOR chain should be left floating.

All digital or analog pins not included in *Table 12-5* are not part of the XOR chain and can be left floating during an XOR test. That includes the output of the XOR chain, FANOUT0/GPIO3, and other pads shown in *Table 12-6* below.

Table 12-6: Pins Excluded from the XOR Chain

Pin Name	Pin #	Description
RSMRST#	E2	Used for capturing straps
PWR_GOOD	B5	Used for capturing straps
SLP_S5#	A5	In S5 power well. No test support.
SLP_S3#	F7	In S5 power well. No test support.
CPU_PG/LDT_PG	AC26	No test support
IGNNE#/SIC	AA22	No test support
SMI#	AA24	No test support
NMI/LINT1	W24	No test support
INTR/LINT0	W26	No test support
INIT#	W25	No test support
USB_OC3#/GPM3#	B7	No test support
TEST0	G9	Test controller data input
TEST1	E9	Test controller mode
TEST2	F9	Reserved Test Input
14M_OSC	B23	Test control clock
RTCCLK	D3	No test support
FANOUT0/GPIO3	M4	Output of the XOR chain

Appendix A: Pin Listing

Table 12-7: SB600 Pin List Sorted by Interface

Ball No.	Signal Name
	CPU Interface
AC26	CPU_PG/LDT_PG
W26	INTR/LINT0
W24	NMI/LINT1
W25	INIT#
AA24	SMI#
AA23	SLP#/LDT_STP#
AA22	IGNNE#/SIC
AA26	A20M#/SID
Y27	FERR#
AA25	STPCLK#/ALLOW_LDTSTP
W23	DPRSLPVR
AA27	CPU_PWR
AC25	LDT_RST#/DPRSTP#/PROCHOT#
	LPC Interface
AG24	LAD0
AG25	LAD1
AH24	LAD2
AH25	LAD3
AF24	LFRAME#
AJ24	LDRQ0#
AH26	LDRQ1#/GNT5#/GPIO68
C25	LPC_SMI#/EXTEVNT1#
AF23	SERIRQ
AF26	GA20IN
AG26	KBRST#
	PCI Express Interface
J24	PCIE_RCLKP
J25	PCIE_RCLKN
P29	PCIE_TX0P
P28	PCIE_TX0N
M29	PCIE_TX1P
M28	PCIE_TX1N
K29	PCIE_TX2P
K28	PCIE_TX2N
H29	PCIE_TX3P
H28	PCIE_TX3N
T25	PCIE_RX0P
T26	PCIE_RX0N
T22	PCIE_RX1P
T23	PCIE_RX1N
M25	PCIE_RX2P
M26	PCIE_RX2N
M22	PCIE_RX3P
M23	PCIE_RX3N
E29	PCIE_CALRP
E28	PCIE_CALRN
E27	PCIE_CALI
	PCI 33 Interface
U2	PCICLK0
T2	PCICLK1
U1	PCICLK2
V2	PCICLK3
W3	PCICLK4
U3	PCICLK5
V1	PCICLK6
T1	SPDIF_OUT/PCICLK7/GPIO41
AJ9	PCIRST#
AD3	INTE#/GPIO33
AF1	INTF#/GPIO34
AF4	INTG#/GPIO35
AF3	INTH#/GPIO36
W7	AD0/ROMA18
Y1	AD1/ROMA17
W8	AD2/ROMA16
W5	AD3/ROMA15
AA5	AD4/ROMA14
Y3	AD5/ROMA13
AA6	AD6/ROMA12
AC5	AD7/ROMA11
AA7	AD8/ROMA9
AC3	AD9/ROMA8
AC7	AD10/ROMA7
AJ7	AD11/ROMA6
AD4	AD12/ROMA5
AB11	AD13/ROMA4
AE6	AD14/ROMA3
AC9	AD15/ROMA2
AA3	AD16/ROMD0
AJ4	AD17/ROMD1
AB1	AD18/ROMD2
AH4	AD19/ROMD3
AB2	AD20/ROMD4
AJ3	AD21/ROMD5
AB3	AD22/ROMD6
AH3	AD23/ROMD7
AC1	AD24
AH2	AD25
AC2	AD26
AH1	AD27
AD2	AD28
AG2	AD29
AD1	AD30
AG1	AD31
AB9	CBE0#/ROMA10
AF9	CBE1#/ROMA1
AJ5	CBE2#/ROMWE#
AG3	CBE3#
AA2	FRAME#
AH6	DEVSEL#/ROMA0
AG5	IRDY#

Ball No.	Signal Name
AA1	TRDY#/ROMOE#
AF7	PAR/ROMA19
Y2	STOP#
AG8	PERR#
AC11	SERR#
AF6	LOCK#
AJ8	REQ0#
AE2	REQ1#
AG9	REQ2#
AH8	REQ3#/GPIO70
AH5	REQ4#/GPIO71
W22	BMREQ#/REQ5#/GPIO65
AD11	GNT0#
AF2	GNT1#
AH7	GNT2#
AB12	GNT3#/GPIO72
AG4	GNT4#/GPIO73
AH26	LDRQ1#/GNT5#/GPIO68
AG7	CLKRUN#
	USB Interface
H12	USB_HSDP9+
G12	USB_HSDM9-
E12	USB_HSDP8+
D12	USB_HSDM8-
E14	USB_HSDP7+
D14	USB_HSDM7-
G14	USB_HSDP6+
H14	USB_HSDM6-
D16	USB_HSDP5+
E16	USB_HSDM5-
D18	USB_HSDP4+
E18	USB_HSDM4-
G16	USB_HSDP3+
H16	USB_HSDM3-
G18	USB_HSDP2+
H18	USB_HSDM2-
D19	USB_HSDP1+

Ball No.	Signal Name
E19	USB_HSDM1-
G19	USB_HSDP0+
H19	USB_HSDM0-
A17	USBCLK
A14	USB_RCOMP
A11	USB_ATEST1
A10	USB_ATEST0
	ATA66/100/133
AB29	IDE_IORDY
AA28	IDE_IRQ
AA29	IDE_A0
AB27	IDE_A1
Y28	IDE_A2
AB28	IDE_DACK#
AC27	IDE_DRQ
AC29	IDE_IOR#
AC28	IDE_IOW#
W28	IDE_CS1#
W27	IDE_CS3#
AD28	IDE_D0/GPIO15
AD26	IDE_D1/GPIO16
AE29	IDE_D2/GPIO17
AF27	IDE_D3/GPIO18
AG29	IDE_D4/GPIO19
AH28	IDE_D5/GPIO20
AJ28	IDE_D6/GPIO21
AJ27	IDE_D7/GPIO22
AH27	IDE_D8/GPIO23
AG27	IDE_D9/GPIO24
AG28	IDE_D10/GPIO25
AF28	IDE_D11/GPIO26
AF29	IDE_D12/GPIO27
AE28	IDE_D13/GPIO28
AD25	IDE_D14/GPIO29
AD29	IDE_D15/GPIO30
	Serial ATA
AH21	SATA_TX0+

Ball No.	Signal Name
AJ21	SATA_TX0-
AH20	SATA_RX0-
AJ20	SATA_RX0+
AH18	SATA_TX1+
AJ18	SATA_TX1-
AH17	SATA_RX1-
AJ17	SATA_RX1+
AH13	SATA_TX2+
AH14	SATA_TX2-
AH16	SATA_RX2-
AJ16	SATA_RX2+
AJ11	SATA_TX3+
AH11	SATA_TX3-
AH12	SATA_RX3-
AJ13	SATA_RX3+
AF12	SATA_CAL
AD16	SATA_X1
AD18	SATA_X2
AC12	SATA_ACT#/GPIO67
C28	SATA_IS0#/GPIO10
B29	GHI#/SATA_IS1#/GPIO6
B27	SMARTVOLT/SATA_IS2#/GPIO4
A27	SSMUXSEL/SATA_IS3#/GPIO0
	AC '97 Interface
L1	AC_BITCLK/GPIO38
L2	AC_SDOUT/GPIO39
L4	ACZ_SDIN0/GPIO42
J2	ACZ_SDIN1/GPIO43
J4	ACZ_SDIN2/GPIO44
M3	AC_SYNC/GPIO40
L5	AC_RST#/GPIO45
T1	SPDIF_OUT/PCICLK7/GPIO41
	HD Interface
N2	AZ_BITCLK
M2	AZ_SDOUT
L3	AZ_SYNC

Ball No.	Signal Name
K3	AZ_RST#
K2	AZ_SDIN3/GPIO46
	Real Time Clock
D2	X1
C1	X2
D1	RTC_GND
E1	VBAT
F5	RTC_IRQ#/GPIO69
D3	RTCCLK
	Hardware Monitor
M4	FANOUT0/GPIO3
T3	FANOUT1/GPIO48
V4	FANOUT2/GPIO49
N3	FANIN0/GPIO50
P2	FANIN1/GPIO51
W4	FANIN2/GPIO52
P5	TEMP_COMM
P7	TEMPIN0/GPIO61
P8	TEMPIN1/GPIO62
T8	TEMPIN2/GPIO63
T7	TEMPIN3/TALERT#/GPIO64
V5	VIN0/GPIO53
L7	VIN1/GPIO54
M8	VIN2/GPIO55
V6	VIN3/GPIO56
M6	VIN4/GPIO57
P4	VIN5/GPIO58
M7	VIN6/GPIO59
V7	VIN7/GPIO60
N1	AVDD
M1	AVSS
	SPI ROM Interface
J3	SPI_DI/GPIO12
J6	SPI_DO/GPIO11
G3	SPI_CLK/GPIO47
G2	SPI_HOLD#/GPIO31
G6	SPI_CS#/GPIO32

Ball No.	Signal Name
	NB / Power Mgmt
B24	DPSLP_OD#/GPIO37
AH9	CPU_STP#/DPSLP_3V#
F7	SLP_S3#
A5	SLP_S5#
C6	USB_OC9#/SLP_S2/GPM9#
E3	PWR_BTN#
B5	PWR_GOOD
B3	SUS_STAT#
G9	TEST0
E9	TEST1
F9	TEST2
	General Events
B2	RI#/EXTEVNT0#
C25	LPC_SMI#/EXTEVNT1#
G7	SMBALERT#/THRMTRIP#/GEVENT2#
D7	LPC_PME#/GEVENT3#
A3	PCI_PME#/GEVENT4#
D9	S3_STATE/GEVENT5#
B4	USB_OC6#/GEVENT6#
C4	USB_OC7#/GEVENT7#
E7	WAKE#/GEVENT8#
A8	USB_OC0#/GPM0#
B8	USB_OC1#/GPM1#
C7	USB_OC2#/GPM2#
C8	USB_OC3#/GPM3#
A6	USB_OC4#/GPM4#
B6	USB_OC5#/DDR3_RST#/GPM5#
C2	BLINK/GPM6#
F4	SYS_RESET#/GPM7#
C5	USB_OC8#/AZ_DOCK_RST#/GPM8#
C6	USB_OC9#/SLP_S2/GPM9#
	SM Bus/ GPOC
C27	SCL0/GPOC0#

Ball No.	Signal Name
B28	SDA0/GPOC1#
C3	SCL1/GPOC2#
F3	SDA1/GPOC3#
	General Purpose I/O
A27	SSMUXSEL/SATA_IS3#/GPIO0
A26	ROM_CS#/GPIO1
B26	SPKR/GPIO2
M4	FANOUT0/GPIO3
B27	SMARTVOLT/SATA_IS2#/GPIO4
D23	SHUTDOWN#/GPIO5/SMARTVOLT2
B29	GHI#/SATA_IS1#/GPIO6
A23	WD_PWRGD/GPIO7
C26	DDC1_SDA/GPIO8
D26	DDC1_SCL/GPIO9
C28	SATA_IS0#/GPIO10
J6	SPI_DO/GPIO11
J3	SPI_DI/GPIO12
C23	LAN_RST#/GPIO13
G5	ROM_RST#/GPIO14
AD28	IDE_D0/GPIO15
AD26	IDE_D1/GPIO16
AE29	IDE_D2/GPIO17
AF27	IDE_D3/GPIO18
AG29	IDE_D4/GPIO19
AH28	IDE_D5/GPIO20
AJ28	IDE_D6/GPIO21
AJ27	IDE_D7/GPIO22
AH27	IDE_D8/GPIO23
AG27	IDE_D9/GPIO24
AG28	IDE_D10/GPIO25
AF28	IDE_D11/GPIO26
AF29	IDE_D12/GPIO27
AE28	IDE_D13/GPIO28
AD25	IDE_D14/GPIO29
AD29	IDE_D15/GPIO30
G2	SPI_HOLD#/GPIO31

Ball No.	Signal Name
G6	SPI_CS#/GPIO32
AD3	INTE#/GPIO33
AF1	INTF#/GPIO34
AF4	INTG#/GPIO35
AF3	INTH#/GPIO36
B24	DPSLP_OD#/GPIO37
L1	AC_BITCLK/GPIO38
L2	AC_SDOUT/GPIO39
M3	AC_SYNC/GPIO40
T1	SPDIF_OUT/PCICLK7/GPIO41
L4	ACZ_SDIN0/GPIO42
J2	ACZ_SDIN1/GPIO43
J4	ACZ_SDIN2/GPIO44
L5	AC_RST#/GPIO45
K2	AZ_SDIN3/GPIO46
G3	SPI_CLK/GPIO47
T3	FANOUT1/GPIO48
V4	FANOUT2/GPIO49
N3	FANIN0/GPIO50
P2	FANIN1/GPIO51
W4	FANIN2/GPIO52
V5	VIN0/GPIO53
L7	VIN1/GPIO54
M8	VIN2/GPIO55
V6	VIN3/GPIO56
M6	VIN4/GPIO57
P4	VIN5/GPIO58
M7	VIN6/GPIO59
V7	VIN7/GPIO60
P7	TEMPIN0/GPIO61
P8	TEMPIN1/GPIO62
T8	TEMPIN2/GPIO63
T7	TEMPIN3/TALERT#/GPIO64
W22	BMREQ#/REQ5#/GPIO65
A4	LLB#/GPIO66
AC12	SATA_ACT#/GPIO67

Ball No.	Signal Name
AH26	LDRQ1#/GNT5#/GPIO68
F5	RTC_IRQ#/GPIO69
AH8	REQ3#/GPIO70
AB12	GNT3#/GPIO72
AH5	REQ4#/GPIO71
AG4	GNT4#/GPIO73
	Reset / Clocks
AG10	A_RST#
E2	RSMRST#
B23	14M_OSC
	No Connects (empty balls)
E23	NC1
AC21	NC2
AD7	NC3
AE7	NC4
AA4	NC5
T4	NC6
D4	NC7
AB19	NC8
	Special Power / Gnd
A24	AVDDCK_3.3V
A22	AVDDCK_1.2V
B22	AVSSCK
AE11	V5_VREF
	USB Analog Pwr
B9	AVDDTX_0
B11	AVDDTX_1
B13	AVDDTX_2
B16	AVDDTX_3
B18	AVDDTX_4
A9	AVDDRX_0
B10	AVDDRX_1
B12	AVDDRX_2
B14	AVDDRX_3
B17	AVDDRX_4
A12	AVDDC
A13	AVSSC

Ball No.	Signal Name
	USB Analog GND
A16	AVSS_USB_1
C9	AVSS_USB_2
C10	AVSS_USB_3
C11	AVSS_USB_4
C12	AVSS_USB_5
C13	AVSS_USB_6
C14	AVSS_USB_7
C16	AVSS_USB_8
C17	AVSS_USB_9
C18	AVSS_USB_10
C19	AVSS_USB_11
C20	AVSS_USB_12
D11	AVSS_USB_13
D21	AVSS_USB_14
E11	AVSS_USB_15
E21	AVSS_USB_16
F11	AVSS_USB_17
F12	AVSS_USB_18
F14	AVSS_USB_19
F16	AVSS_USB_20
F18	AVSS_USB_21
F19	AVSS_USB_22
F21	AVSS_USB_23
G11	AVSS_USB_24
G21	AVSS_USB_25
H11	AVSS_USB_26
H21	AVSS_USB_27
J11	AVSS_USB_28
J12	AVSS_USB_29
J14	AVSS_USB_30
J16	AVSS_USB_31
J18	AVSS_USB_32
J19	AVSS_USB_33
	PCI Express Analog Power
U29	PCIE_PVDD
F27	PCIE_VDDR_1

Ball No.	Signal Name
F28	PCIE_VDDR_2
F29	PCIE_VDDR_3
G26	PCIE_VDDR_4
G27	PCIE_VDDR_5
G28	PCIE_VDDR_6
G29	PCIE_VDDR_7
J27	PCIE_VDDR_8
J29	PCIE_VDDR_9
L25	PCIE_VDDR_10
L26	PCIE_VDDR_11
L29	PCIE_VDDR_12
N29	PCIE_VDDR_13
	PCI-E Analog Ground
U28	PCIE_PVSS
D27	PCIE_VSS_1
D28	PCIE_VSS_2
D29	PCIE_VSS_3
F26	PCIE_VSS_4
G23	PCIE_VSS_5
G24	PCIE_VSS_6
G25	PCIE_VSS_7
H27	PCIE_VSS_8
J23	PCIE_VSS_9
J26	PCIE_VSS_10
J28	PCIE_VSS_11
K27	PCIE_VSS_12
L22	PCIE_VSS_13
L23	PCIE_VSS_14
L24	PCIE_VSS_15
L27	PCIE_VSS_16
L28	PCIE_VSS_17
M21	PCIE_VSS_18
M24	PCIE_VSS_19
M27	PCIE_VSS_20
N27	PCIE_VSS_21
N28	PCIE_VSS_22
P22	PCIE_VSS_23

Ball No.	Signal Name
P23	PCIE_VSS_24
P24	PCIE_VSS_25
P25	PCIE_VSS_26
P26	PCIE_VSS_27
P27	PCIE_VSS_28
T21	PCIE_VSS_29
T24	PCIE_VSS_30
T27	PCIE_VSS_31
T28	PCIE_VSS_32
T29	PCIE_VSS_33
U27	PCIE_VSS_34
V22	PCIE_VSS_35
V23	PCIE_VSS_36
V24	PCIE_VSS_37
V25	PCIE_VSS_38
V26	PCIE_VSS_39
V27	PCIE_VSS_40
V28	PCIE_VSS_41
V29	PCIE_VSS_42
	Serial ATA Analog Pwr
AE14	AVDD_SATA_1
AE16	AVDD_SATA_2
AE18	AVDD_SATA_3
AE19	AVDD_SATA_4
AF19	AVDD_SATA_5
AF21	AVDD_SATA_6
AG22	AVDD_SATA_7
AG23	AVDD_SATA_8
AH22	AVDD_SATA_9
AH23	AVDD_SATA_10
AJ12	AVDD_SATA_11
AJ14	AVDD_SATA_12
AJ19	AVDD_SATA_13
AJ22	AVDD_SATA_14
AJ23	AVDD_SATA_15
AC16	XTLVDD_SATA
AD14	PLLVDD_SATA_1

Ball No.	Signal Name
AJ10	PLLVDD_SATA_2
	Serial ATA Analog Ground
AB14	AVSS_SATA_1
AB16	AVSS_SATA_2
AB18	AVSS_SATA_3
AC14	AVSS_SATA_4
AC18	AVSS_SATA_5
AC19	AVSS_SATA_6
AD12	AVSS_SATA_7
AD19	AVSS_SATA_8
AD21	AVSS_SATA_9
AE12	AVSS_SATA_10
AE21	AVSS_SATA_11
AF11	AVSS_SATA_12
AF14	AVSS_SATA_13
AF16	AVSS_SATA_14
AF18	AVSS_SATA_15
AG11	AVSS_SATA_16
AG12	AVSS_SATA_17
AG13	AVSS_SATA_18
AG14	AVSS_SATA_19
AG16	AVSS_SATA_20
AG17	AVSS_SATA_21
AG18	AVSS_SATA_22
AG19	AVSS_SATA_23
AG20	AVSS_SATA_24
AG21	AVSS_SATA_25
AH10	AVSS_SATA_26
AH19	AVSS_SATA_27
	Core Pwr
M13	VDD_1
M17	VDD_2
N12	VDD_3
N15	VDD_4
N18	VDD_5
R13	VDD_6
R17	VDD_7

Ball No.	Signal Name
U12	VDD_8
U15	VDD_9
U18	VDD_10
V13	VDD_11
V17	VDD_12
	3.3V I/O Pwr
A25	VDDQ_1
A28	VDDQ_2
C29	VDDQ_3
D24	VDDQ_4
L9	VDDQ_5
L21	VDDQ_6
M5	VDDQ_7
P3	VDDQ_8
P9	VDDQ_9
T5	VDDQ_10
V9	VDDQ_11
W2	VDDQ_12
W6	VDDQ_13
W21	VDDQ_14
W29	VDDQ_15
AA12	VDDQ_16
AA16	VDDQ_17
AA19	VDDQ_18
AC4	VDDQ_19
AC23	VDDQ_20
AD27	VDDQ_21
AE1	VDDQ_22
AE9	VDDQ_23
AE23	VDDQ_24
AH29	VDDQ_25
AJ2	VDDQ_26
AJ6	VDDQ_27
AJ26	VDDQ_28
	3.3V Standby Pwr
A2	S5_3.3V_1
A7	S5_3.3V_2

Ball No.	Signal Name
F1	S5_3.3V_3
J5	S5_3.3V_4
J7	S5_3.3V_5
K1	S5_3.3V_6
	1.2V Standby Pwr
G4	S5_1.2V_1
H1	S5_1.2V_2
H2	S5_1.2V_3
H3	S5_1.2V_4
	USB Phy Digital Power
A18	USB_PHY_1.2V_1
A19	USB_PHY_1.2V_2
B19	USB_PHY_1.2V_3
B20	USB_PHY_1.2V_4
B21	USB_PHY_1.2V_5
	Digital Ground
A1	ASIC A11: VSS_1 ASIC A12 and after: No ball at the position
A20	VSS_2
A21	VSS_3
A29	VSS_4
B1	VSS_5
B7	VSS_6
B25	VSS_7
C21	VSS_8
C22	VSS_9
C24	VSS_10
D6	VSS_11
E24	VSS_12
F2	VSS_13
F23	VSS_14
G1	VSS_15
J1	VSS_16
J8	VSS_17
L6	VSS_18
L8	VSS_19
M9	VSS_20

Ball No.	Signal Name
M12	VSS_21
M15	VSS_22
M18	VSS_23
N13	VSS_24
N17	VSS_25
P1	VSS_26
P6	VSS_27
P21	VSS_28
R12	VSS_29
R15	VSS_30
R18	VSS_31
T6	VSS_32
T9	VSS_33
U13	VSS_34
U17	VSS_35
V3	VSS_36
V8	VSS_37
V12	VSS_38
V15	VSS_39
V18	VSS_40
V21	VSS_41
W1	VSS_42
W9	VSS_43
Y29	VSS_44
AA11	VSS_45
AA14	VSS_46
AA18	VSS_47
AC6	VSS_48
AC24	VSS_49
AD9	VSS_50
AD23	VSS_51
AE3	VSS_52
AE27	VSS_53
AG6	VSS_54
AJ1	VSS_55
AJ25	VSS_56
AJ29	VSS_57

Table 12-8: SB600 Pin List Sorted by Ball Reference

Ball No.	Signal Name
A1	ASIC A11: VSS_1 ASIC A12 and after: No ball at the position
A10	USB_ATEST0
A11	USB_ATEST1
A12	AVDDC
A13	AVSSC
A14	USB_RCOMP
A16	AVSS_USB_1
A17	USBCLK
A18	USB_PHY_1.2V_1
A19	USB_PHY_1.2V_2
A2	S5_3.3V_1
A20	VSS_2
A21	VSS_3
A22	AVDDCK_1.2V
A23	WD_PWRGD/GPIO7
A24	AVDDCK_3.3V
A25	VDDQ_1
A26	ROM_CS#/GPIO1
A27	SSMUXSEL/SATA_IS3#/GPIO0
A28	VDDQ_2
A29	VSS_4
A3	PCI_PME#/GEVENT4#
A4	LLB#/GPIO66
A5	SLP_S5#
A6	USB_OC4#/GPM4#
A7	S5_3.3V_2
A8	USB_OC0#/GPM0#
A9	AVDDRX_0
AA1	TRDY#/ROMOE#
AA11	VSS_45
AA12	VDDQ_16
AA14	VSS_46
AA16	VDDQ_17

Ball No.	Signal Name
AA18	VSS_47
AA19	VDDQ_18
AA2	FRAME#
AA22	IGNNE#/SIC
AA23	SLP#/LDT_STP#
AA24	SMI#
AA25	STPCLK#/ALLOW_LDTSTP
AA26	A20M#/SID
AA27	CPU_PWR
AA28	IDE_IRQ
AA29	IDE_A0
AA3	AD16/ROMD0
AA4	NC5
AA5	AD4/ROMA14
AA6	AD6/ROMA12
AA7	AD8/ROMA9
AB1	AD18/ROMD2
AB11	AD13/ROMA4
AB12	GNT3#/GPIO72
AB14	AVSS_SATA_1
AB16	AVSS_SATA_2
AB18	AVSS_SATA_3
AB19	NC8
AB2	AD20/ROMD4
AB27	IDE_A1
AB28	IDE_DACK#
AB29	IDE_IORDY
AB3	AD22/ROMD6
AB9	CBE0#/ROMA10
AC1	AD24
AC11	SERR#
AC12	SATA_ACT#/GPIO67
AC14	AVSS_SATA_4
AC16	XTLVDD_SATA
AC18	AVSS_SATA_5

Ball No.	Signal Name
AC19	AVSS_SATA_6
AC2	AD26
AC21	NC2
AC23	VDDQ_20
AC24	VSS_49
AC25	LDT_RST#/DPRSTP#/PROCHOT#
AC26	CPU_PG/LDT_PG
AC27	IDE_DRQ
AC28	IDE_IOW#
AC29	IDE_IOR#
AC3	AD9/ROMA8
AC4	VDDQ_19
AC5	AD7/ROMA11
AC6	VSS_48
AC7	AD10/ROMA7
AC9	AD15/ROMA2
AD1	AD30
AD11	GNT0#
AD12	AVSS_SATA_7
AD14	PLLVDD_SATA_1
AD16	SATA_X1
AD18	SATA_X2
AD19	AVSS_SATA_8
AD2	AD28
AD21	AVSS_SATA_9
AD23	VSS_51
AD25	IDE_D14/GPIO29
AD26	IDE_D1/GPIO16
AD27	VDDQ_21
AD28	IDE_D0/GPIO15
AD29	IDE_D15/GPIO30
AD3	INTE#/GPIO33
AD4	AD12/ROMA5
AD7	NC3
AD9	VSS_50

Ball No.	Signal Name
AE1	VDDQ_22
AE11	V5_VREF
AE12	AVSS_SATA_10
AE14	AVDD_SATA_1
AE16	AVDD_SATA_2
AE18	AVDD_SATA_3
AE19	AVDD_SATA_4
AE2	REQ1#
AE21	AVSS_SATA_11
AE23	VDDQ_24
AE27	VSS_53
AE28	IDE_D13/GPIO28
AE29	IDE_D2/GPIO17
AE3	VSS_52
AE6	AD14/ROMA3
AE7	NC4
AE9	VDDQ_23
AF1	INTF#/GPIO34
AF11	AVSS_SATA_12
AF12	SATA_CAL
AF14	AVSS_SATA_13
AF16	AVSS_SATA_14
AF18	AVSS_SATA_15
AF19	AVDD_SATA_5
AF2	GNT1#
AF21	AVDD_SATA_6
AF23	SERIRQ
AF24	LFRAME#
AF26	GA20IN
AF27	IDE_D3/GPIO18
AF28	IDE_D11/GPIO26
AF29	IDE_D12/GPIO27
AF3	INTH#/GPIO36
AF4	INTG#/GPIO35
AF6	LOCK#
AF7	PAR/ROMA19
AF9	CBE1#/ROMA1

Ball No.	Signal Name
AG1	AD31
AG10	A_RST#
AG11	AVSS_SATA_16
AG12	AVSS_SATA_17
AG13	AVSS_SATA_18
AG14	AVSS_SATA_19
AG16	AVSS_SATA_20
AG17	AVSS_SATA_21
AG18	AVSS_SATA_22
AG19	AVSS_SATA_23
AG2	AD29
AG20	AVSS_SATA_24
AG21	AVSS_SATA_25
AG22	AVDD_SATA_7
AG23	AVDD_SATA_8
AG24	LAD0
AG25	LAD1
AG26	KBRST#
AG27	IDE_D9/GPIO24
AG28	IDE_D10/GPIO25
AG29	IDE_D4/GPIO19
AG3	CBE3#
AG4	GNT4#/GPIO73
AG5	IRDY#
AG6	VSS_54
AG7	CLKRUN#
AG8	PERR#
AG9	REQ2#
AH1	AD27
AH10	AVSS_SATA_26
AH11	SATA_TX3-
AH12	SATA_RX3-
AH13	SATA_TX2+
AH14	SATA_TX2-
AH16	SATA_RX2-
AH17	SATA_RX1-
AH18	SATA_TX1+

Ball No.	Signal Name
AH19	AVSS_SATA_27
AH2	AD25
AH20	SATA_RX0-
AH21	SATA_TX0+
AH22	AVDD_SATA_9
AH23	AVDD_SATA_10
AH24	LAD2
AH25	LAD3
AH26	LDRQ1#/GNT5#/GPIO68
AH27	IDE_D8/GPIO23
AH28	IDE_D5/GPIO20
AH29	VDDQ_25
AH3	AD23/ROMD7
AH4	AD19/ROMD3
AH5	REQ4#/GPIO71
AH6	DEVSEL#/ROMA0
AH7	GNT2#
AH8	REQ3#/GPIO70
AH9	CPU_STP#/DPSLP_3V#
AJ1	VSS_55
AJ10	PLLVDD_SATA_2
AJ11	SATA_TX3+
AJ12	AVDD_SATA_11
AJ13	SATA_RX3+
AJ14	AVDD_SATA_12
AJ16	SATA_RX2+
AJ17	SATA_RX1+
AJ18	SATA_TX1-
AJ19	AVDD_SATA_13
AJ2	VDDQ_26
AJ20	SATA_RX0+
AJ21	SATA_TX0-
AJ22	AVDD_SATA_14
AJ23	AVDD_SATA_15
AJ24	LDRQ0#
AJ25	VSS_56
AJ26	VDDQ_28

Ball No.	Signal Name
AJ27	IDE_D7/GPIO22
AJ28	IDE_D6/GPIO21
AJ29	VSS_57
AJ3	AD21/ROMD5
AJ4	AD17/ROMD1
AJ5	CBE2#/ROMWE#
AJ6	VDDQ_27
AJ7	AD11/ROMA6
AJ8	REQ0#
AJ9	PCIRST#
B1	VSS_5
B10	AVDDRX_1
B11	AVDDTX_1
B12	AVDDRX_2
B13	AVDDTX_2
B14	AVDDRX_3
B16	AVDDTX_3
B17	AVDDRX_4
B18	AVDDTX_4
B19	USB_PHY_1.2V_3
B2	RI#/EXTEVNT0#
B20	USB_PHY_1.2V_4
B21	USB_PHY_1.2V_5
B22	AVSSCK
B23	14M_OSC
B24	DPSLP_OD#/GPIO37
B24	DPSLP_OD#/GPIO37
B25	VSS_7
B26	SPKR/GPIO2
B27	SMARTVOLT/SATA_IS2#/GPIO4
B28	SDA0/GPOC1#
B29	GHI#/SATA_IS1#/GPIO6
B3	SUS_STAT#
B4	USB_OC6#/GEVENT6#
B5	PWR_GOOD
B6	USB_OC5#/DDR3_RST#/GPM5#

Ball No.	Signal Name
B7	VSS_6
B8	USB_OC1#/GPM1#
B9	AVDDTX_0
C1	X2
C10	AVSS_USB_3
C11	AVSS_USB_4
C12	AVSS_USB_5
C13	AVSS_USB_6
C14	AVSS_USB_7
C16	AVSS_USB_8
C17	AVSS_USB_9
C18	AVSS_USB_10
C19	AVSS_USB_11
C2	BLINK/GPM6#
C20	AVSS_USB_12
C21	VSS_8
C22	VSS_9
C23	LAN_RST#/GPIO13
C24	VSS_10
C25	LPC_SMI#/EXTEVNT1#
C26	DDC1_SDA/GPIO8
C27	SCL0/GPOC0#
C28	SATA_IS0#/GPIO10
C29	VDDQ_3
C3	SCL1/GPOC2#
C4	USB_OC7#/GEVENT7#
C5	USB_OC8#/AZ_DOCK_RST#/GPM8#
C6	USB_OC9#/SLP_S2/GPM9#
C7	USB_OC2#/GPM2#
C8	USB_OC3#/GPM3#
C9	AVSS_USB_2
D1	RTC_GND
D11	AVSS_USB_13
D12	USB_HSDM8-
D14	USB_HSDM7-
D16	USB_HSDP5+

Ball No.	Signal Name
D18	USB_HSDP4+
D19	USB_HSDP1+
D2	X1
D21	AVSS_USB_14
D23	SHUTDOWN#/GPIO5/SMARTVOLT2
D24	VDDQ_4
D26	DDC1_SCL/GPIO9
D27	PCIE_VSS_1
D28	PCIE_VSS_2
D29	PCIE_VSS_3
D3	RTCCLK
D4	NC7
D6	VSS_11
D7	LPC_PME#/GEVENT3#
D9	S3_STATE/GEVENT5#
E1	VBAT
E11	AVSS_USB_15
E12	USB_HSDP8+
E14	USB_HSDP7+
E16	USB_HSDM5-
E18	USB_HSDM4-
E19	USB_HSDM1-
E2	RSMRST#
E21	AVSS_USB_16
E23	NC1
E24	VSS_12
E27	PCIE_CALI
E28	PCIE_CALRN
E29	PCIE_CALRP
E3	PWR_BTN#
E7	WAKE#/GEVENT8#
E9	TEST1
F1	S5_3.3V_3
F11	AVSS_USB_17
F12	AVSS_USB_18
F14	AVSS_USB_19
F16	AVSS_USB_20

Ball No.	Signal Name
F18	AVSS_USB_21
F19	AVSS_USB_22
F2	VSS_13
F21	AVSS_USB_23
F23	VSS_14
F26	PCIE_VSS_4
F27	PCIE_VDDR_1
F28	PCIE_VDDR_2
F29	PCIE_VDDR_3
F3	SDA1/GPOC3#
F4	SYS_RESET#/GPM7#
F5	RTC_IRQ#/GPIO69
F7	SLP_S3#
F9	TEST2
G1	VSS_15
G11	AVSS_USB_24
G12	USB_HSDM9-
G14	USB_HSDP6+
G16	USB_HSDP3+
G18	USB_HSDP2+
G19	USB_HSDP0+
G2	SPI_HOLD#/GPIO31
G21	AVSS_USB_25
G23	PCIE_VSS_5
G24	PCIE_VSS_6
G25	PCIE_VSS_7
G26	PCIE_VDDR_4
G27	PCIE_VDDR_5
G28	PCIE_VDDR_6
G29	PCIE_VDDR_7
G3	SPI_CLK/GPIO47
G4	S5_1.2V_1
G5	ROM_RST#/GPIO14
G6	SPI_CS#/GPIO32
G7	SMBALERT#/THRMTRIP#/ GEVENT2#
G9	TEST0
H1	S5_1.2V_2

Ball No.	Signal Name
H11	AVSS_USB_26
H12	USB_HSDP9+
H14	USB_HSDM6-
H16	USB_HSDM3-
H18	USB_HSDM2-
H19	USB_HSDM0-
H2	S5_1.2V_3
H21	AVSS_USB_27
H27	PCIE_VSS_8
H28	PCIE_TX3N
H29	PCIE_TX3P
H3	S5_1.2V_4
J1	VSS_16
J11	AVSS_USB_28
J12	AVSS_USB_29
J14	AVSS_USB_30
J16	AVSS_USB_31
J18	AVSS_USB_32
J19	AVSS_USB_33
J2	ACZ_SDIN1/GPIO43
J23	PCIE_VSS_9
J24	PCIE_RCLKP
J25	PCIE_RCLKN
J26	PCIE_VSS_10
J27	PCIE_VDDR_8
J28	PCIE_VSS_11
J29	PCIE_VDDR_9
J3	SPI_DI/GPIO12
J4	ACZ_SDIN2/GPIO44
J5	S5_3.3V_4
J6	SPI_DO/GPIO11
J6	SPI_DO/GPIO11
J7	S5_3.3V_5
J8	VSS_17
K1	S5_3.3V_6
K2	AZ_SDIN3/GPIO46
K27	PCIE_VSS_12

Ball No.	Signal Name
K28	PCIE_TX2N
K29	PCIE_TX2P
K3	AZ_RST#
L1	AC_BITCLK/GPIO38
L2	AC_SDOUT/GPIO39
L21	VDDQ_6
L22	PCIE_VSS_13
L23	PCIE_VSS_14
L24	PCIE_VSS_15
L25	PCIE_VDDR_10
L26	PCIE_VDDR_11
L27	PCIE_VSS_16
L28	PCIE_VSS_17
L29	PCIE_VDDR_12
L3	AZ_SYNC
L4	ACZ_SDIN0/GPIO42
L5	AC_RST#/GPIO45
L6	VSS_18
L7	VIN1/GPIO54
L8	VSS_19
L9	VDDQ_5
M1	AVSS
M12	VSS_21
M13	VDD_1
M15	VSS_22
M17	VDD_2
M18	VSS_23
M2	AZ_SDOUT
M21	PCIE_VSS_18
M22	PCIE_RX3P
M23	PCIE_RX3N
M24	PCIE_VSS_19
M25	PCIE_RX2P
M26	PCIE_RX2N
M27	PCIE_VSS_20
M28	PCIE_TX1N
M29	PCIE_TX1P

Ball No.	Signal Name
M3	AC_SYNC/GPIO40
M4	FANOUT0/GPIO3
M5	VDDQ_7
M6	VIN4/GPIO57
M7	VIN6/GPIO59
M8	VIN2/GPIO55
M9	VSS_20
N1	AVDD
N12	VDD_3
N13	VSS_24
N15	VDD_4
N17	VSS_25
N18	VDD_5
N2	AZ_BITCLK
N27	PCIE_VSS_21
N28	PCIE_VSS_22
N29	PCIE_VDDR_13
N3	FANIN0/GPIO50
P1	VSS_26
P2	FANIN1/GPIO51
P21	VSS_28
P22	PCIE_VSS_23
P23	PCIE_VSS_24
P24	PCIE_VSS_25
P25	PCIE_VSS_26
P26	PCIE_VSS_27
P27	PCIE_VSS_28
P28	PCIE_TX0N
P29	PCIE_TX0P
P3	VDDQ_8
P4	VIN5/GPIO58
P5	TEMP_COMM
P6	VSS_27
P7	TEMPIN0/GPIO61
P8	TEMPIN1/GPIO62
P9	VDDQ_9
R12	VSS_29

Ball No.	Signal Name
R13	VDD_6
R15	VSS_30
R17	VDD_7
R18	VSS_31
T1	SPDIF_OUT/PCICLK7/ GPIO41
T2	PCICLK1
T21	PCIE_VSS_29
T22	PCIE_RX1P
T23	PCIE_RX1N
T24	PCIE_VSS_30
T25	PCIE_RX0P
T26	PCIE_RX0N
T27	PCIE_VSS_31
T28	PCIE_VSS_32
T29	PCIE_VSS_33
T3	FANOUT1/GPIO48
T4	NC6
T5	VDDQ_10
T6	VSS_32
T7	TEMPIN3/TALERT#/ GPIO64
T8	TEMPIN2/GPIO63
T9	VSS_33
U1	PCICLK2
U12	VDD_8
U13	VSS_34
U15	VDD_9
U17	VSS_35
U18	VDD_10
U2	PCICLK0
U27	PCIE_VSS_34
U28	PCIE_PVSS
U29	PCIE_PVDD
U3	PCICLK5
V1	PCICLK6
V12	VSS_38
V13	VDD_11

Ball No.	Signal Name
V15	VSS_39
V17	VDD_12
V18	VSS_40
V2	PCICLK3
V21	VSS_41
V22	PCIE_VSS_35
V23	PCIE_VSS_36
V24	PCIE_VSS_37
V25	PCIE_VSS_38
V26	PCIE_VSS_39
V27	PCIE_VSS_40
V28	PCIE_VSS_41
V29	PCIE_VSS_42
V3	VSS_36
V4	FANOUT2/GPIO49
V5	VIN0/GPIO53
V6	VIN3/GPIO56
V7	VIN7/GPIO60
V8	VSS_37
V9	VDDQ_11
W1	VSS_42
W2	VDDQ_12
W21	VDDQ_14
W22	BMREQ#/REQ5#/GPIO65
W23	DPRSLPVR
W24	NMI/LINT1
W25	INIT#
W26	INTR/LINT0
W27	IDE_CS3#
W28	IDE_CS1#
W29	VDDQ_15
W3	PCICLK4
W4	FANIN2/GPIO52
W5	AD3/ROMA15
W6	VDDQ_13
W7	AD0/ROMA18
W8	AD2/ROMA16

Ball No.	Signal Name
W9	VSS_43
Y1	AD1/ROMA17
Y2	STOP#
Y27	FERR#
Y28	IDE_A2
Y29	VSS_44
Y3	AD5/ROMA13

Appendix B: Revision History

Note: The revision number of the manual reflects either one of the two release states defined below:

Preliminary Release — Revision numbers from 0.1 to 0.9. Generally with incomplete information and/or information subject to change.

Full Release — Revision numbers from 1.0 onwards. Occurring after essential elements have been reviewed, typically after tape-out.

Date	Rev.	Comment
July 2, 2008	3.05	Changed "AMD Confidential" to "Proprietary" in document footers. Also changed file name of the document.
Nov 30, 2007	3.04	Updated Section 4.1: Added VDD in Note 1, and added VDD vs. PCIE_PVDD power sequence requirement in Note 2. Added Chapter 11, "Thermal Information."
April 20, 2007	3.03	Updated Section 3.5, "USB Interface": Added Note on ESD protection for USB_HSDP[9:0]+ and USB_HSDM[9:0]- signals. Updated Section 8.4, "RTC Battery Current Consumption": updated statement on expectancy of RTC battery life.
April 11, 2007	3.02	Added references to SMARTVOLT2 Corrected header of Table 8-4, "GPIO/GEVENT Output DC Characteristics." Updated Table 8-6, "RTC Battery Current Consumption." Updated the Note on heat sink in Ch.9, "Power Requirements."
Jan 8, 2007	3.01	Updated the following: Section 3.9, "SMBUS Interface / General Purpose Open Collector": Added Note. Section 3.13, "External Event / General Event / General Power Management / General Purpose Open Collector": Added Note 2 and see notes. Section 3.19, "Power and Ground": Modified Note 3. "Table 4-1: SB600 Power Up/Down Sequence Timing": Modified the T2 Min value. Section 4.1, "Power Up/Down Sequence Timing Notes": Modified Note 15 and 16. "Table 6-3: 14 MHz OSC Reference Clock AC Specifications": Modified the Duty Cycle Min value.
Dec 19, 2006	3.00	Revised general format and styles to reflect new corporate identity. Raised revision number to 3.00 according to the AMD scheme. Updated 1.1, "Features of the SB600": Added Hot Plug support by SATA controller (AHCI mode only); removed support for thermal diode temperature sensing function. Updated Section 4.1, "Power Up and Down Sequences." Updated Table 6-2, "System Clock Input Frequency Specifications": Revised specifications for 14M_OSC; added AC_BITCLK specification. Updated Table 6-3, "14 MHz OSC Reference Clock AC Specifications": and Table 6-4, "48MHz USB/SIO Clock AC Specifications": Revised clock period specifications and added clock frequency tolerance. Updated Table 8-2, "DC Characteristics for Power Supplies to the SB600": Added note on minimum value of VBAT. Updated Section 10.2, "Pressure Specification."
Oct 27, 2006	1.2	Updated section 4.1, "Power Up and Down Sequences." Updated Table 4.2, "External Resistor Requirements and Integrated Pull Up/Down": Clarified description for FEER# (leave unconnected for AMD platforms).
Aug 25, 2006	1.1	Updated section 1.2, "Part Number and Branding": Revised branding diagram and removed part numbers for leaded parts. Updated section 3.12, "General Purpose I/O": Added notes regarding pins

Date	Rev.	Comment
		with PCI ROM functions and LDRG1#/GNT65#/GPIO68. Updated section 3.13, "General Event/…": Expanded note on S3_STATE/GEVENT5#. Updated section 4.1, "Power Up and Down Sequences": Added T9A, removed T14A, and made other minor changes. Added Table 9-1, "Power Activity under Configuration 1."
Aug 21, 2006	1.0	Specified that PCI (X Bus) ROM is not supported for ASIC revision A21 and onwards. Revised section 1.1, "Features of the SB600": Added SATA port multiplier support and a note on eSATA support. Revised Table 1-1, "SB600 Part Numbers": Added part numbers for ASIC revision A13 and A21. Revised section 3.15, "HD Audio Interface": Changed I/O type to "O" for AZ_BITCLK, AZ_RST#, AZ_SDOUT, and AZ_SYNC. Added section 6.3, "System Clock AC Specifications." Updated section 4.1, "Power Up and Down Sequences": Revised some numbers and combined the original sections on power up and power down sequences into one. Made "Power requirements" a separate chapter, and updated it with new numbers.
June 23, 2006	0.6	Updated section 1.1, "Features of the SB600": Corrected feature list for SATA II support. Updated Table 4.1-1 "SB600 Power On Sequence Timing": Revised values for T8D and T13. Added Table 6-2:"SB600 System Clock Input Frequency Specifications."
May 9, 2006	0.5	Clarified that pin A1 (VSS_1) only exists on ASIC A11. Affected the following: Figure 5, SB600 Ball-out Assignment", Figure 27, "SB600 Package Outline"; Appendix A, "Pin Listing." Updated Section 1.1, "Features of the SB600": Restricted the LPC controller's SPI device support to 33MHz maximum. Updated Section 3.7, "Power Management/North Bridge Interface": Corrected pin type for SUS_STAT# to simply "OD," and that of LDT_STP# [AMD] to "O". Updated Table 3.20-3, "Additional Straps": Corrected pull-up rail for RTCCLK strap to S5_3.3V. Updated Table 4.1-1, "SB600 Power On Sequence Timing": Added Note 9 to the description of T11.
April 2006	0.4	Updated Section 1.1, "Features of the SB600": Added that APM is not supported. Updated Table 4.1-1, "SB600 Power On Sequence Timing": Revised maximum time between SB PWR_GOOD and LDT PG (T8D) to 48.15ms. Updated Table 4.2-1: "SB600 Power Down Timing": Revised maximum SB PWR_GOOD fall time (T7B) to 1µs. Revised Table 5.8-2, "Functionality of the General Events and GPIOs across ACPI States": Changed functionality for GPIO [73:0].
April 2006	0.3	Updated Table 4.1-1, "SB600 Power On Sequence Timing": Revised values for T8C, T8D, T9, and T11; corrected label T14 to T15. Updated Figure 13 and Table 4.2-1: "SB600 Power Down Timing": Added fall time for RSM_RST# (T14A). Updated Table 3.20-1: "Standard Straps": Changed default value for strap on PCICLK4 to that of "0V." Updated Section 3.12, "General Purpose I/O": Changed I/O type of LAN_RST#/GPIO13 to "O." Updated Section 3.6, "Serial ATA Interface": Added a note to the end of the table. Updated Table 4.4-1, "External Resistors Requirements and Integrated Pull Up/Down": Made various corrections and additions to the table. Revised Table 5.8-2, "Functionality of the General Events and GPIOs across ACPI States." Updated Table 8.4.1, "Power Estimates for the SB600": Put in "TBD" for power estimates.

Date	Rev.	Comment
		Updated Table 9-1.1, “SB600 Package Physical Dimensions”: Revised minimum and maximum values of substrate thickness (parameter “c”). Updated Section 9.2, “Pressure Specification”: Elaborated on the specification. Updated Table 10.1-1, “Signals for the Test Controller of the SB600”: Corrected ball references for TEST0 and TEST1.
Feb 2006	0.2	Updated Table 1.3.-1, “SB600 Part Number”: Added part numbers for ASIC A11, substrate revision B, and ASIC A12. Updated Section 3.1, “A-Link Express II Interface”: Changed description for PCIE_CALI. Updated Section 3.12, “General Purpose I/O”: Corrected information on various pins. Updated Section 3.13,, “External Event / General Event / General Power Management / General Purpose Open Collector“: Corrected information on various pins. Updated Section 3.7, “Power Management / North Bridge Interface”: Updated pin description for WAKE#/GEVENT8#. Updated Section 4.1, “Power Up Sequences”: Put in new details and requirements. Updated Table 4.4-1, “External Resistor Requirements and Integrated Pull Up/Down”: Corrected external resistor requirement for USB_OC9#/SLP_S2/GPM9# to 10K pull-down. Updated Section 9.1, “Physical Dimensions”: Updated package diagram to show substrate rev. B; added detailed dimension figures. Added Section 9.2, “Pressure Specification.”
Nov 2005	0.1	Replaced Table 5.8-3 with a reference to the RRG
Oct 2005	0.09	Preliminary release