Z84C90 CMOS Z80®KIO Serial/Parallel/Counter/Timer

FEATURES:

- Two independent synchronous/asynchronous serial channels.
- Three 8-bit parallel ports.
- Four independent counter/timer channels.
- On-chip clock oscillator/driver.
- Software/Hardware Resets.
- Designed in CMOS for low power operations.
- Supports Z80 Family interrupt daisy chain.
- Programmable interrupt priorities.
- 8, 10 and 12.5 MHz bus clock frequency.
- Single +5 Volt Power Supply.

GENERAL DESCRIPTION:

Zilog's Z84C90 Serial/Parallel I/O /Counter/Timer (KIO) is a multi-channel, multi-purpose I/O device designed to provide the end-user with a cost effective and powerful solution to meet his peropheral needs. The Z84C90 combines the features of one Z84C30 CTC, one Z84C4xSIO, one Z84C20 PIO, a byte-wide bit-programmable I/O port, and a crystal oscillator into a single 84-pin PLCC package. The block diagram for the Z84C90 is shown in Figure 1 while the pinout is shown in Figure 2. Utilizing fifteen internal registers for data and programming information, the KIO can easily be configured to any given system environment. Although the optimum performance is obtained with a Z84C00 CPU, the KIO can just as easily be used with any other CPU.

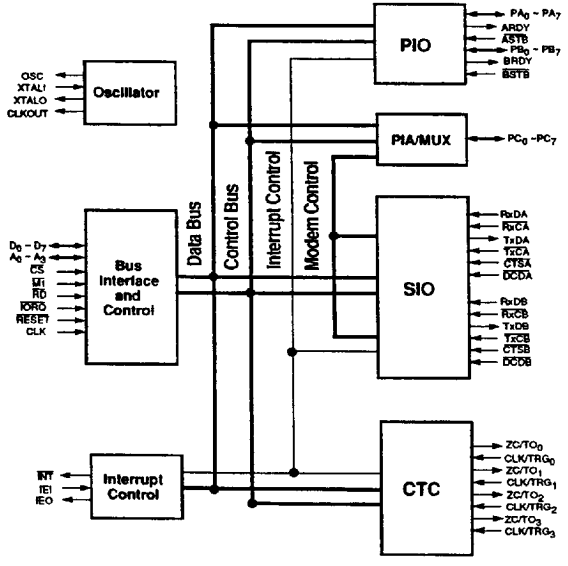


Figure 1: KIO Block Diagram

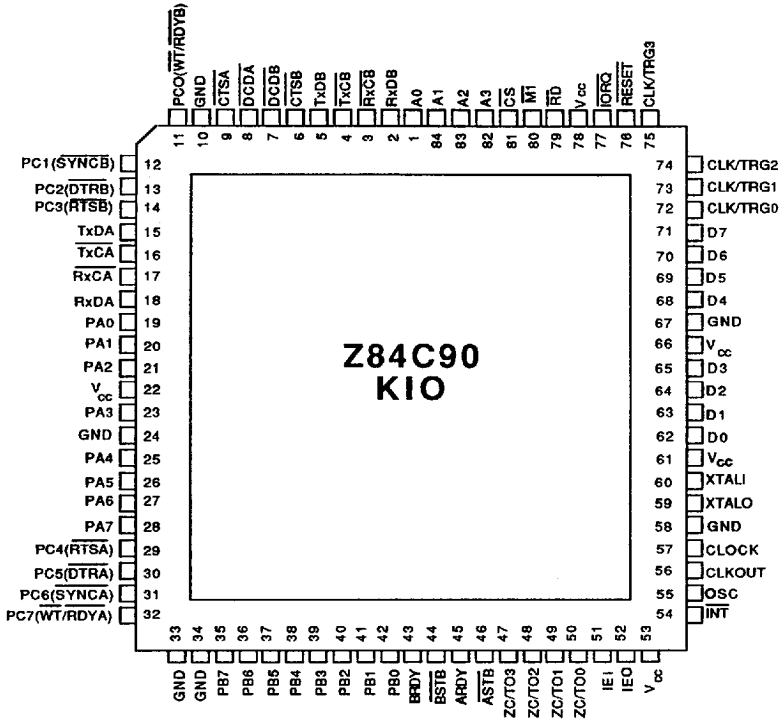


Figure 2: PLCC Pinout

Z84C20 Parallel Input/Output Logic Unit: This logic unit provides both TTL- and CMOS-compatible interfaces between peripheral devices and a CPU through the use of two 8-bit parallel ports. The CPU configures the logic to interface to a wide range of peripheral devices with no external logic. Typical devices that are compatible with this interface are keyboards, printers, and EPROM/PAL programmers.

The parallel ports (designated Port A and Port B) are byte-wide and completely compatible with the Z84C20 PIO (see Figure 3.). These two ports have several modes of operation; input, output, bidirectional, or bit control mode. Each port has two handshake signals (RDY and $\overline{STB}$) which can be used to control data transfers. The RDY (ready) indicates that the port is ready for data transfer while $\overline{STB}$ (strobe) is an input to the port that indicates when data transfer has occurred. Each of the ports can also be programmed to interrupt the CPU upon the occurrence of specified status conditions and generate unique interrupt vectors when the CPU responds. (For more information on the operation of this portion of the logic, please refer to the Z84C20 PIO Product Specification and Technical Manual.)

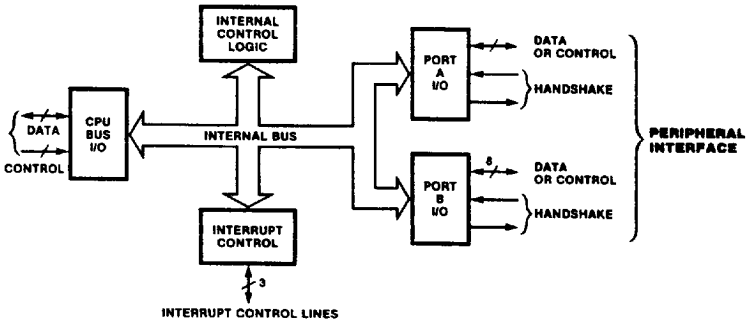


Figure 3: PIO Block Diagram

Parallel Interface Adapter (PIA) Logic Unit: This logic also offers an additional 8-bits of I/O, referred to as the PIA port (see Figure 4), to the user. This port, designated as Port C, is bit-programmable for data transfers; each bit can be individually programmed as either an input or an output. Bit direction control is accomplished through the programming of the PIA Control Register. When programmed as outputs, the output data latches are programmed with an I/O write cycle and their state can be read with an I/O read cycle. When programmed as inputs, the state of the external pin is read with the I/O read cycle. This port does not have handshake capabilities and offers no interrupt capabilities. This port is multiplexed to provide, when desired, the additional modem and CPU control signals for the serial I/O logic unit.

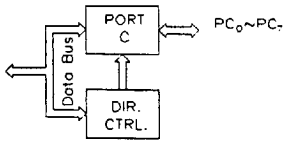


Figure 4: PIA Block Diagram

When a read from the PIA port is done, input data will be latched when $\overline{IORQ}$, $\overline{CS}$, and $\overline{RD}$ are all detected active. The data bus will display this data as a result of the rising edge of the CLOCK input after this occurrence. When a write to the PIA port is done, data will be written as a result of the rising edge of the CLOCK input after $\overline{IORQ}$ and $\overline{CS}$ have been detected active and $\overline{RD}$ has been detected inactive.

Counter/Timer Logic Unit: This logic unit provides the user with four individual 8-bit counter/timer channels that are compatible with the Z84C30 CTC (see Figure 5). The counter/timers can be programmed by the CPU for a broad range of counting and timing applications. Typical applications include event counting, interrupt and interval timing, and serial baud rate clock generation.

Each of the counter/timer channels, designated Channels 0 through 3, have an 8-bit prescaler (when used in timer mode) as well as its own 8-bit counter to provide a wide range of count resolution. Each of the channels also have their own clock/trigger input to quantify the counting process and an output to indicate zero crossing/timeout conditions. With only one interrupt vector programmed into this logic unit, each channel can generate a unique interrupt vector in response to the interrupt acknowledge cycle.

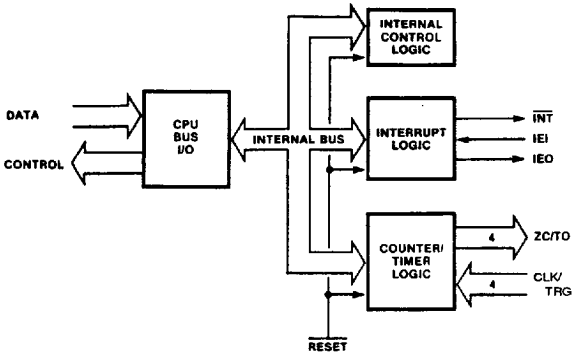


Figure 5: CTC Block Diagram

Serial I/O Logic Unit: This logic unit provides the user with two separate serial I/O channels that are completely compatible with the Z84C4x SIO (see Figure 6). Their basic functions as serial-to-parallel and parallel-to-serial converters can be programmed by a CPU for a broad range of serial communications applications. Each channel, designated Channel A and Channel B, is capable of supporting all common asynchronous and synchronous protocols (Monosync, Bisync, and SDLC/HDLC), byte- or bit-oriented.

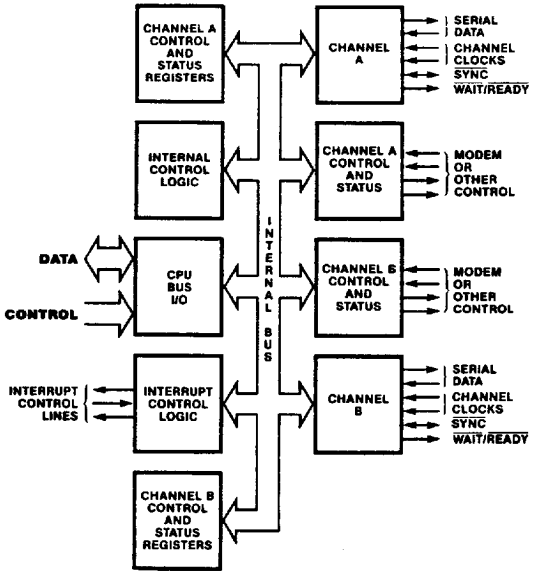


Figure 6: SIO Block Diagram

In the default state of the KIO, each serial channel supports full duplex communication with seperate transmit and receive data lines, two modem control signals ($\overline{CTS}$ and $\overline{DCD}$), and seprate transmit and receive clock inputs. Optionally, additional modem and CPU/DMA control signals can be obtained through the PIA port. (For more information on the operation of this portion of the logic, please refer to the Z84C40 SIO Product Specification and Technical Manual).

Clock Oscillator/Driver Logic Unit: A clock oscillator/driver is also available that will allow the user to eliminate that circuitry within his new design, or for use as another oscillator within the system. This logic will accept either a crystal, ceramic resonator, or TTL-compatible clock input and generate a MOS-compatible clock output and also an oscillator reference output. A fundamental parallel resonant crystal (Figure 7) is recommended. The preferred value of the two capacitors - C1 and C2 is 33 pf each.

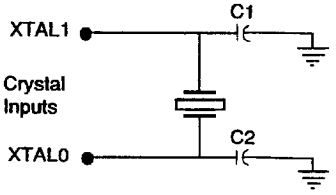


Figure 7: Crystal Connection

Command Logic Unit: This logic unit provides for much more than just controlling the interface between the KIO and the CPU. The main function provided by this unit is to allow the user to configure the internal interrupt daisy chain of the KIO into the order in which he would like the peripherals to interrupt. Any one of the three devices (SIO, CTC, PIO) can be the highest priority while another can be second and the remaining one third. The user can even configure the daisy chain such that no internal peripherals are involved in the chain. Programming of the daisy chain configuration is done by programming the Command Register with the appropriate 3-bit pattern in D_0-D_2 and D_3 set to "1".

A second function of this logic unit is to provide software controllable "hardware" resets to each of the individual devices. This allows an individual peripheral to be reset without having to reset the entire KIO. Requiring bit D_3 to be set to a "1" in order to program the daisy chain configuration allows the user to reset the individual devices without changing the daisy chain. The software reset commands for the individual devices still remain available to the user.

A third function of the Command Register allows the user to obtain use of the additional control signals of the SIO logic instead of the PIA Port. This is done by programming bit D_7 of the Command Register with "1".

PIN DESCRIPTIONS:

A_0-A_3. Address Bus (inputs, active high, 3-state). Use to select which port/register the current transaction cycle is for.

ARD, BRDY. Port Ready (outputs, active high). these signals indicate that the port is ready for a data transfer. Inmode 0, it indicates that the port has data available for the peripheral device. In mode 1, it indicates that the port is ready to accept data from the peripheral device. In mode2, ARDY indicates that Port A has available for the peripheral device, but that it will not be placed onto PA_0-PA_7 until the $\overline{ASTB}$ signal is active, while BRDY indicates that Port A is able to accept data from a peripheral device. Note that Port B does not support mode 2 operation and can only be used in mode 3 operation when Port A is programmed for mode 2. These signals are not used in mode 3 operation.

$\overline{ASTB}$, $\overline{BSTB}$. Port Strobe (inputs, active low). These signals indicate that the peripheral device has performed a transfer. In mode 0, it indicates that the peripheral device has accepted the data present on the port pins. In mode 1, it causes the data on the port pins to be latched into Port A. In mode 2, the $\overline{ASTB}$ signal causes the data in the output data latch of Port A to be placed onto the Port A pins while the $\overline{BSTB}$ signal will cause the data present on the Port A pins to be latched into the Port A input data latch. The end of the current transaction is noted by the rising edge of these signals. Note that Port B does not support mode 2 operation and can only be used in mode 3 operation when Port A is programmed for mode 2. These signals are not used in mode 3 operation.

CLK/TRG_0-CLK/TRG_3. External Clock/Timer Trigger (inputs, user selectable active high or low). These four pins correspond to the four counter/timer channels of the KIO. In counter mode, each active edge will cause the downcounter to decrement. In timer mode, an active edge will start the timer.

CLKOUT. Clock Out (output, active high). This output is a divide-by-two of the oscillator (XTAL) input.

CLOCK. System Clock (input, active high). This clock should be the same as (or a derivative of) the CPU clock. If the CLKOUT is to be used as the system clock, then these two pins should be connected together.

$\overline{CS}$. Chip Select (input, active low). Used to activate the internal register decoding mechanism and allow the KIO to perform a data transfer to/from the CPU.

$\overline{CTSA}$, $\overline{CTSB}$. Clear to Send (inputs, active low). These signals are modem control signals to their serial channels. When programmed for Auto Enables, a low on these pins will enable their respective transmitters. If not programmed as Auto Enables, these pins may be used as general-purpose input signals.

D_0-D_7. Data Bus (bidirectional, active high, 3-state). Used for data exchanges between the CPU and the KIO for programming and data transfer. The KIO also monitors the data bus during the RETI instruction cycle to resolve its

$\overline{DCDA}$,$\overline{DCDB}$. Data Carrier Detect (inputs, active low). These signals are modem control signals to their serial channels. When programmed for Auto Enables, a low on these pins will enable their respective receivers. If not programmed as Auto Enables, these pins may be used as general-purpose input signals.

$\overline{DTRA}$, $\overline{DTRB}$. Data Terminal Ready (outputs, active low). These signals are modem control signals for their serial channels. They will follow the state programmed into their respective serial channels. They are multiplexed with Port C, bits 5 and 2 respectively.

IEI. Interrupt Enable In (input, active high). This signal is used with IEO to form a priority daisy chain when there is more than one interrupt-driven device. A high on this line indicates that no higher priority device is requesting an interrupt.

IEO. Interrupt Enable Out (output, active high). This signal is used with IEI to form a priority daisy chain when there is more than one interrupt-driven device. A high on this line indicates that this device and no higher priority device is requesting an interrupt. A low will block any lower priority devices from requesting an interrupt.

$\overline{INT}$. Interrupt Request (output, active low, open-drain). When any of the devices within the KIO requests interrupt servicing, this line will be active.

$\overline{IORQ}$. I/O Request (input, active low). $\overline{IORQ}$ is used with $\overline{RD}$, A0-A3, and $\overline{CS}$ to transfer data between the KIO and the CPU. When $\overline{IORQ}$, $\overline{RD}$, and $\overline{CS}$ are all active, the device selected by A0-A3 transfers data to the CPU. When $\overline{IORQ}$ and $\overline{CS}$ are active, but $\overline{RD}$ is inactive, the device selected by A0-A3 is written into by the CPU, When IORQ and $\overline{M1}$ are both active the KIO will respond with an interrupt vector from the highest priority interrupting device.

$\overline{M1}$. Machine Cycle 1 (input, active low). When $\overline{M1}$ is active and $\overline{RD}$ is active, the Z80 CPU is fetching an instruction from memory; the KIO decodes this cycle to determine if the RETI instruction sequence is being executed. When $\overline{M1}$ and $\overline{IORQ}$ are both active, the KIO decodes the cycle to be an interrupt acknowledge and will respond with a vector from the highest priority interrupting device.

OSC. Oscillator (output, active high). This output is a reference clock for the oscillator.

PA_0-PA_7. Port A Bus (bidirectional, active high, 3-state). This 8-bit bus transfers data between the peripheral device and the port. PA_0 is the least significant bit of the bus.

PB_0-PB_7. Port B Bus (bidirectional, active high, 3-state). This 8-bit bus transfers data between the peripheral device and the port. PB_0 is the least significant bit of the bus. This port can also supply 1.5 mA at 1.5 volts to drive Darlington transistors.

PC_0-PC_7. Port C Bus (bidirectional, active high, 3-state). This 8-bit bus transfers data between the peripheral device and the port. PC_0 is the least significant bit of the bus. These pins are multiplexed to provide either an 8-bit parallel port or additional modem control signals for the serial channels.

$\overline{RD}$. Read (input, active low). when $\overline{RD}$ is active, a memory or I/O read operation is in progress. $\overline{RD}$ is used with A0-A3, $\overline{CS}$ and $\overline{IORQ}$ to transfer data between the KIO and CPU.

$\overline{RESET}$. Reset (input, active low). A low on this pin will force the KIO into a reset condition. This signal must be active for a minimum of three CLOCK cycles. The reset state of the KIO is with the PIO ports in Mode 1 operation and handshakes inactive and interrupts disabled; PIA port in input mode and active; CTC channel counting terminated and interrupts disabled; SIO channels disabled and marking with interrupts disabled. All control registers should be rewritten after a hardware reset.

$\overline{RTSA}$, $\overline{RTSB}$. Request to Send (outputs, active low). These signals are modem control signals for their serial channels. They will follow the inverse state programmed into their respective serial channels. They are multiplexed with Port C, bits 4 and 3 respectively.

$\overline{RxCA}$, $\overline{RxCB}$. Receive Clock (inputs, active low). These clock are used to assemble data in the receiver shift register for their serial channels. Data is sampled on the rising edge of the clock.

RxDA, RxDB. Receive Data (inputs, active high). These are the input data pins to the receive shift register for their serial channels.

$\overline{SYNCA}$,$\overline{SYNCB}$. Synchronization (bidirectional, active low). In the asynchronous mode of operation, these pins act much like the $\overline{CTS}$ and $\overline{DCD}$ pins. Transitions affect the Sync/Hunt status bit for their respective serial channel but serve no other purpose. They are multiplexed with Port C, bits 6 and 1 respectively.

$\overline{TxCA}$, $\overline{TXCA}$. Transmit Clock (inputs, active low). These clocks are used to transmit data from the transmit shift register for their serial channels. Data is transmitted on the falling edge of the clock.

TxDA, TxDB. Transmit Data (outputs, active high). These are the output data pins from the transmitter for their serial channels.

$\overline{WT/RDYA}$, $\overline{WT/RDYB}$. Wait/Ready (outputs, open-drain when programmed as Wait, active high when programmed as Ready). These pins may be programmed as Ready lines for a DMA controller or Wait lines for interface to a CPU. As a Ready line, it indicates (when active) that transmitter or receiver is able to perform a transfer between the serial channel and the DMA. As a Wait line, in dictates (when active), that the CPU should wait until the transmitter or receiver can complete the requested transaction. They are multiplexed with Port C, bits 7 and 0 respectively.

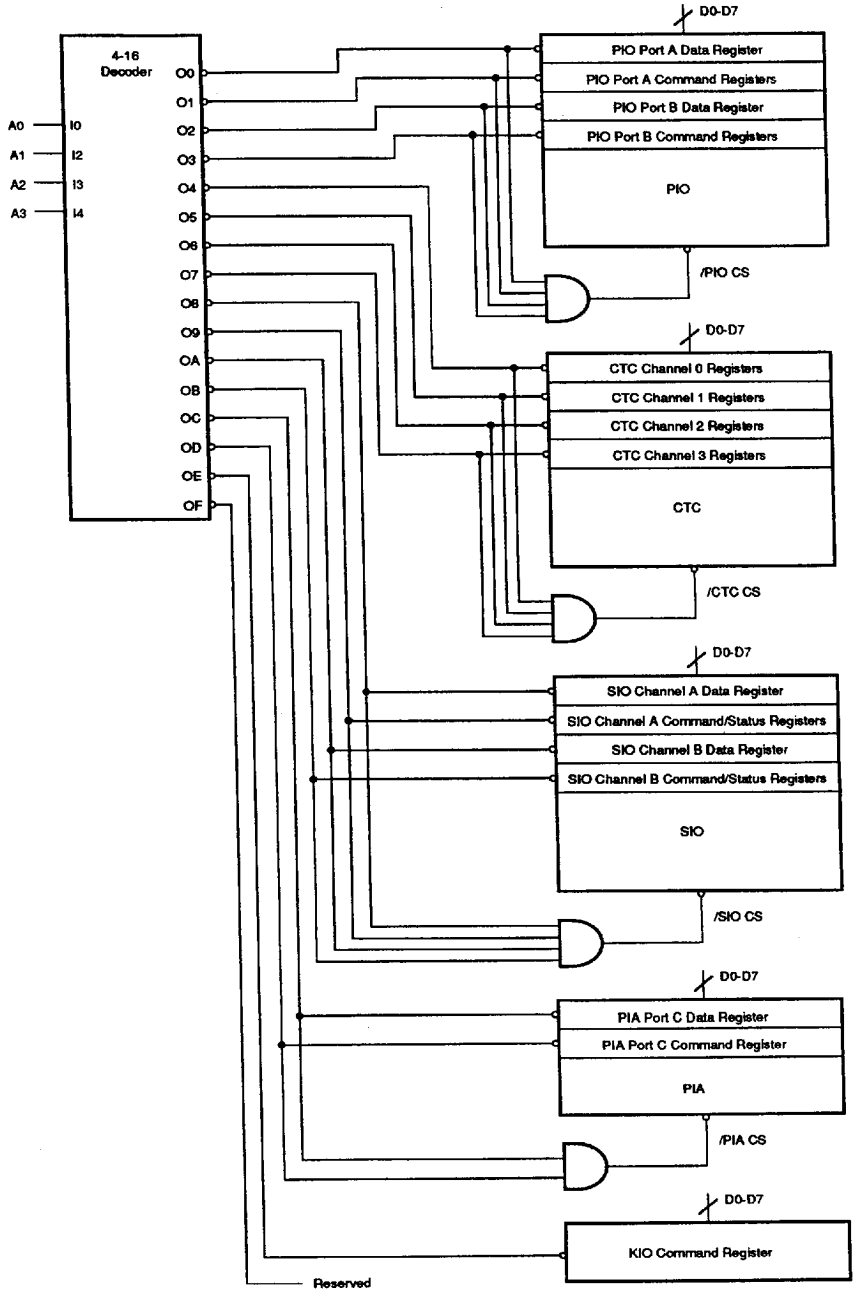
XTALI. Crystal/Clock Connection (input, active high).

XTALO. Crystal Connection (output, active high).

ZC/TO_0-ZC/TO_3. Zero Count/Timeout (outputs, active high). These four pins correspond to the four counter/timer channels of the KIO. Each pin will become active when its corresponding downcounter reaches a zero count.

Address	A3, A2, A1, A0	/IORQ	/CS	/Rd CPU Read	/Rd CPU Write
Register 0: PIO Port A Data	0000	0	0	0	1
Register 1: PIO Port A Command	0001	0	0	0	1
Register 2: PIO Port B Data	0010	0	0	0	1
Register 3: PIO Port B Command	0011	0	0	0	1
Register 4: CTC Channel 0	0100	0	0	0	1
Register 5: CTC Channel 1	0101	0	0	0	1
Register 8: SIO Port A Data	1000	0	0	0	1
Register 9: SIO Port A Command/Status	1001	0	0	0	1
Register 10: SIO Channel B Data	1010	0	0	0	1
Register 11: SIO Channel B Command Status	1011	0	0	0	1
Register 12: PIA Port C Data	1100	0	0	0	1
Register13: PIA Port C Command	1101	0	0	0	1
Register 14: KIO Command	1110	0	0	0	1
Register 15: Reserved	1111	0	0	0	1

REGISTER ADDRESS DECODING FOR THE KIO



REGISTER PROGRAMMING:

PIO Registers: For more detailed information, please consult the PIO Technical Manual. These registers apply to channels A and B (see register address decoding).

Interrupt Vector Word (Figure 8). The PIO logic unit is designed to work with the Z80 CPU in Interrupt Mode 2. This word must be programmed if interrupts are to be used and bit D_0 must be a zero.

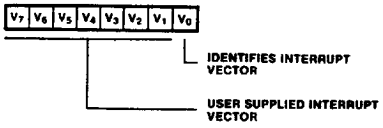


Figure 8: PIO Interrupt Vector Word

Mode Control Word (Figure 9). Selects the port operating mode. This word is required and may be written at any time.

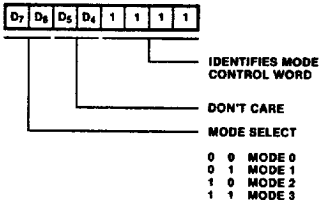


Figure 9: PIO Mode Control Word

I/O Register Control Word (Figure 10). When Mode 3 is selected, the Mode Control Word must be followed by the I/O Register Control Word. This word configures the I/O register, which defines which port lines are inputs or outputs. A "1" indicates input while a "0" indicates output. This word is required when in Mode 3.

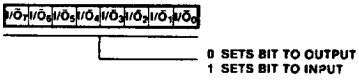


Figure 10: PIO I/O Register Control Word

Interrupt Control Word (Figure 11). In Mode 3 operation, handshake signals are not used. Interrupts are generated as a logic function of the input signal levels. The Interrupt Control Word sets the logic conditions and the logic levels required for generating an interrupt. Two logic conditions or functions are available: AND (if all input bits change to the active level, an interrupt is triggered), and OR (if any one of the input bits change to the active logic level, an interrupt is triggered). The user can also program which input bits are to be considered as part of this logic function. Bit D_6 sets the logic function, bit D_5 sets the logic level, and bit D_4 specifies a mask control word to follow.

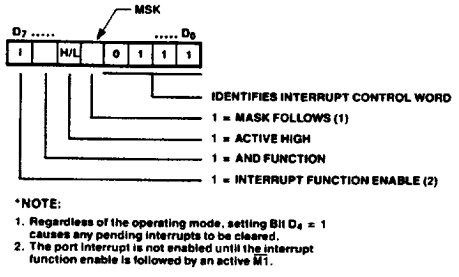


Figure 11: PIO Interrupt Control Word

Mask Control Word (Figure 12). This word sets the mask control register, thus allowing any unused bits to be masked off. If any bits are to be masked, then bit D4 of the interrupt Control Word must be set. When bit D4 of the Interrupt Control Word is set, then the next word programmed must be the Mask Control Word. To mask an input bit, the corresponding Mask Control Word bit must be a "1".

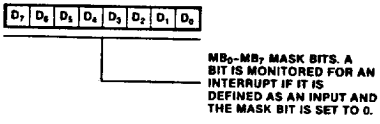


Figure 12: PIO Mask Control Word

Interrupt Disable Word (Figure 13). This word can be used to enable or disable a port's interrupts without changing the rest of the port's interrupt conditions.

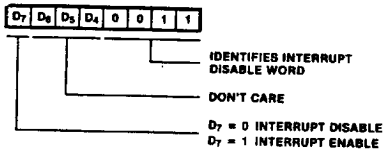


Figure 13: PIO Interrupt Disable Word

CTC Registers: For more detailed information, please consult the CTC Technical Manual. These registers apply to channels 0, 1, 2 and 3 (see register address decoding).

Channel Control Word (Figure 14). This word sets the operating modes and parameters as described below. Bit D_0 must be a "1" to indicate that this is a Control Word.

Interrupt Enable. Bit D7 enables the interrupt logic so that an interrupt output ($\overline{INT}$) can be generated at zero count. Interrupts can be programmed in either mode and may be enabled or disabled at any time.

Mode. Bit D_6 selects either Timer Mode or Counter Mode.

Prescale Factor. Bit D_5 selects the prescale factor for use in the timer mode. Either divide-by-16 or divide-by-256 is available.

Clock/Trigger Edge Selector. Bit D_4 selects the active edge of the CLK/TRG input pulses.

Timer Trigger. Bit D_3 selects the trigger mode for timer operation. Either automatic or external trigger may be selected.

Time Constant. Bit D_2 indicates that the next word programmed is time constant data for the downcounter.

Software Reset. Setting bit D_1 indicates a software reset operation.

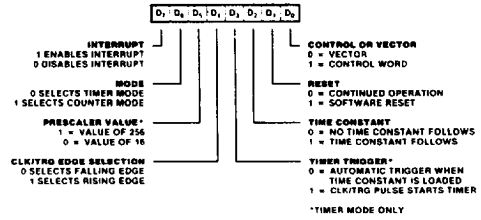


Figure 14: CTC Channel Control Word

Time Constant Word (Figure 15). Before a channel can start counting, it must receive a time constant word. The time constant value may be anywhere between 1 and 256, with "0" being accepted as a count of 256.

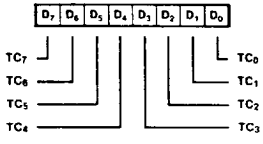


Figure 15: CTC Time Constant Word

Interrupt Vector Word (Figure 16). If one or more of the CTC channels have interrupts enabled, then the Interrupt Vector Word must be programmed. Only the five most significant bits of this word are programmed, and bit D_0 must be "0". Bits D_2-D_1 are automatically modified by the CTC channel when it responds with an interrupt vector.

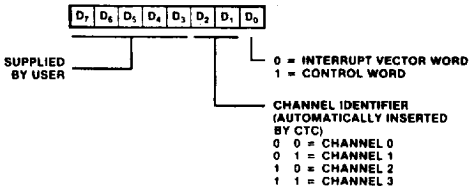


Figure 16: CTC Interrupt Vector Word

SIO Registers: For more detailed information, please consult the PIO Technical Manual. These registers apply to channels A and B (see register address decoding).

Read Registers (Figure 17). The SIO channel B contains three read registers while channel A contains only two that can be read to obtain status information. To read the contents of a register (other than RR_0), the program must first write a pointer to WR_0 in exactly the same manner as a write register operation. The next I/O read cycle will place the contents of the selected read register onto the data bus.

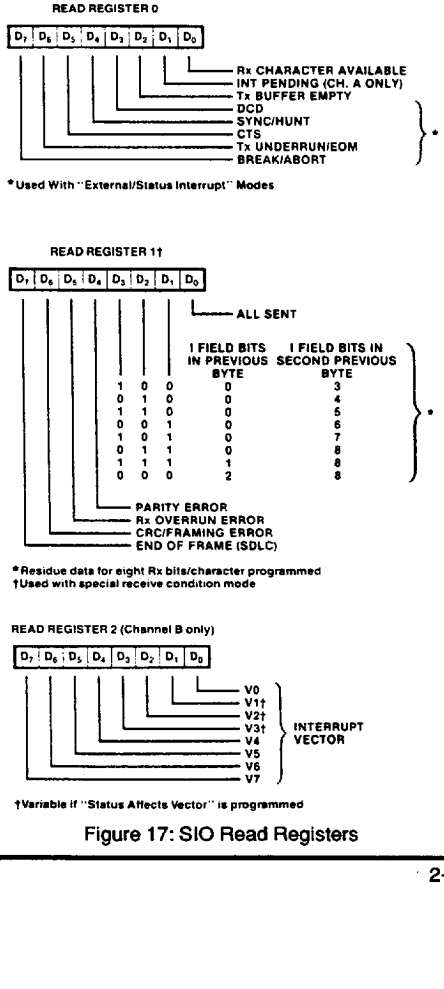


Figure 17: SIO Read Registers

Write Registers (Figure 18). The SIO channel B contains eight write registers while channel A contains only seven that are programmed to configure the operating modes and characteristics of each channel. With the exception of WR_0, programming the write registers is a two step operation. The first operation is a pointer written to WR_0 that point to the selected register. The second operation is the actual control word that is written into the register to configure the SIO channel.

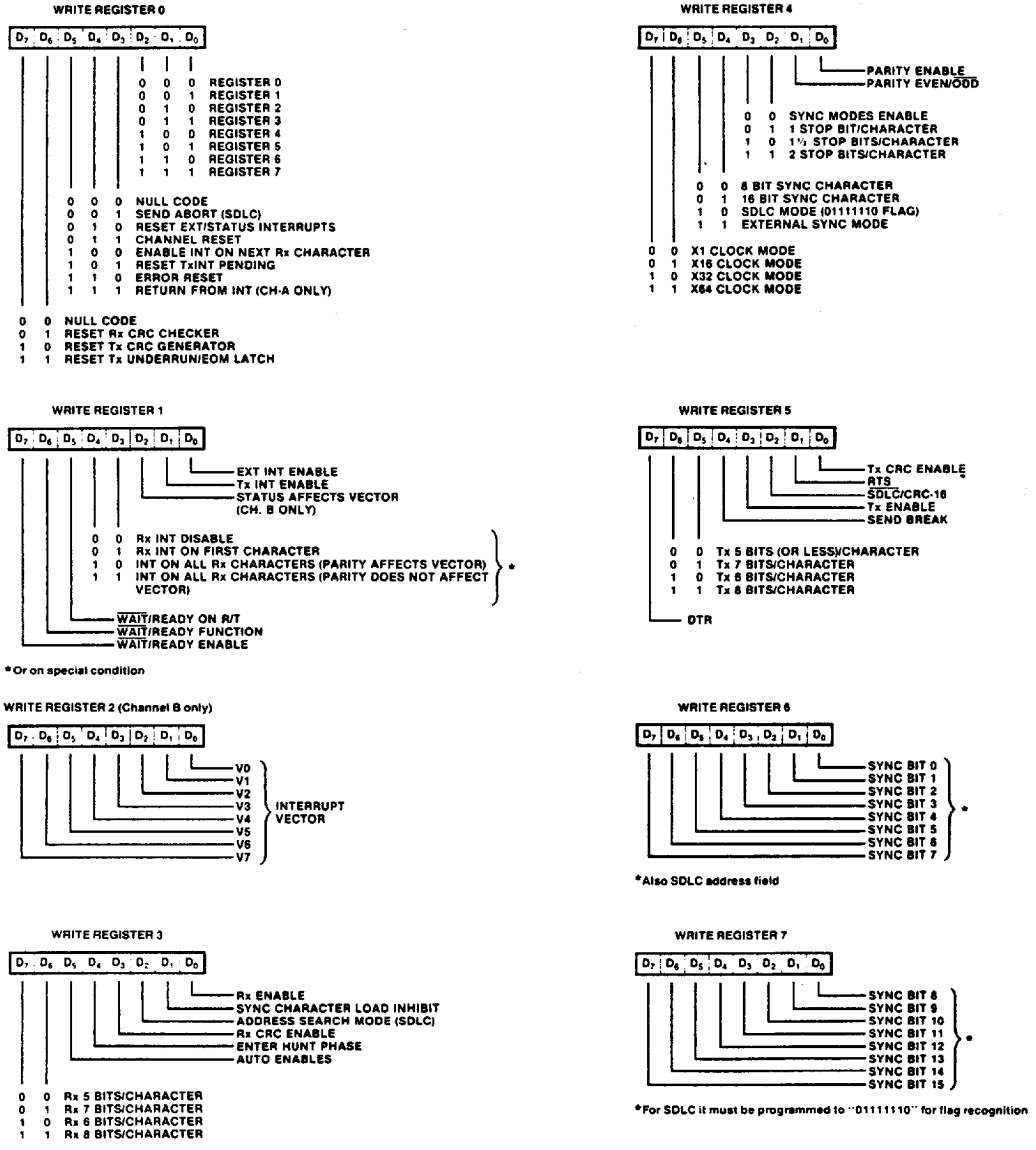


Figure 18: SIO Write Registers

PIA Registers:

The PIA port can be configured for any combination of input and output bits. The direction is controlled by writing to the PIA Control Register. A "1" written to a bit position will indicate that the respective bit should be an input (Figure 19). All bits are inputs on reset.

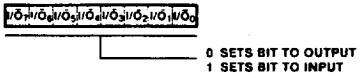


Figure 19: PIA Control Register

KIO Command Register:

The KIO Command Register is used to program software resets and to configure the internal interrupt daisy chain priority (Figure 20). This register should be programmed before all others. The reset control bits are momentary, writing a "1" will pulse an internal reset signal to the appropriate device.

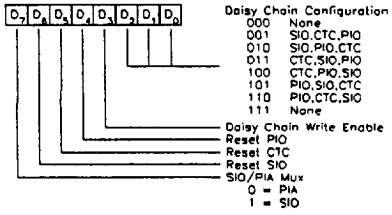


Figure 20: KIO Command Register

2

Z84C90 KIO - ENHANCED VERSION

The new revision of the Z84C90 has a enhancement which allows you to 'simulate' the Return From Interrupt sequence, by software. This feature allows interfacing the CPU to other devices in addition to the Z80 CPU (or, Z180/ Z280).

Enhancement - Software RETI.

Writing "1" to a particular command bit location of the KIO, generates a "RETI sequence" internally. Everytime RETI is needed, a "1" is written to this bit.

Programming of this feature

This revision has one newly assigned register at Register address 15 (this location is "Reserved" on current rev.).

Bit assignment for this register is shown in Figure 21.

Writing "1" to Bit D0 location of this register enables the KIO to simulate a RETI sequence. Writing "0" to this bit has no effect. The upper 7 bits of this register (D7-D1) are reserved and should be programmed as "0". If this register is read, unpredictable data is returned.

Note:
[1] After writing "1" to this bit, 8 clock cycles of access recovery time is required before making another access to the KIO. If accessing the KIO within this access recovery time, the KIO ignores the transaction on the bus.

[2] When simulating "RETI", the status of the IEI pin is ignored with an internally forced "H". If there are other peripherals on the upper interrupt daisy chain, care must be taken.

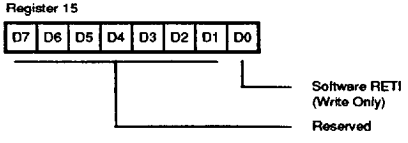


Figure 21. KIO Register 15 - KIO Command Register B

ABSOLUTE MAXIMUM RATINGS:

Voltage on Vcc with respect to Vss
. . . . . -0.3V to +7.0V
Voltages on all inputs with respect to Vss
. . . . . -0.3V to Vcc+0.3V
Operating Ambient Temperature
. . . . . See Ordering Information
Storage Temperature
. . . . . -65 C to +150 C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS:

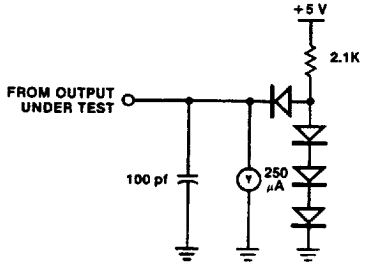
The DC Characteristics and Capacitance sections below apply to the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

Available operating temperature ranges are:
- S = 0 C to +70 C
- E = -40 C to +100 C

Voltage Supply Range: +5.0V ± 10%

All AC parameters assume a load capaitance of 100 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 200pF for the data bus. AC timing measurements are referenced to 1.5 volts (except for CLOCK, which is referenced to the 10% and 90% points).

The Ordering Information section lists temperature ranges and product numbers. Package drawings are in the Package Information section. Refer to the Literature List for additional documentation.

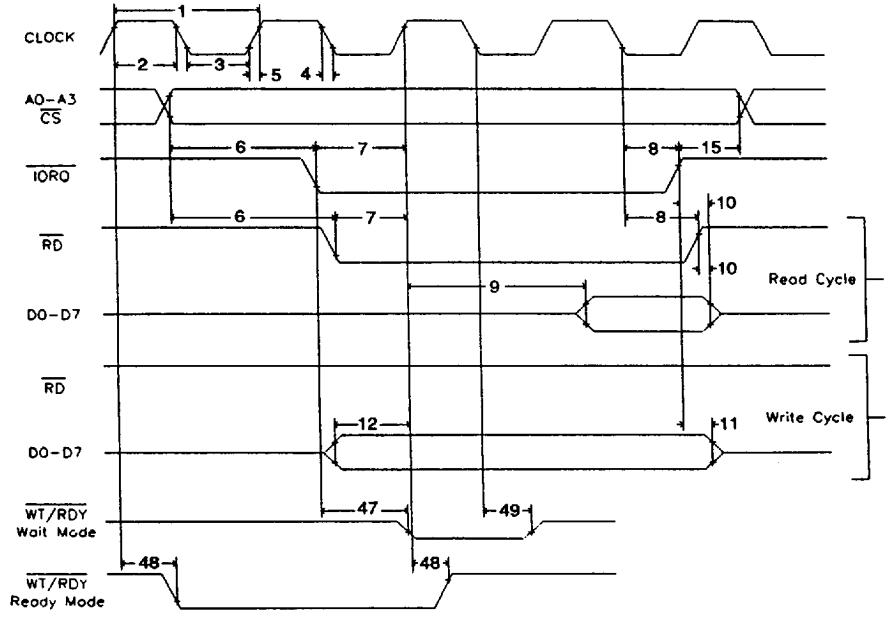


DC CHARACTERISTICS
Z84C90 Z80 KIO

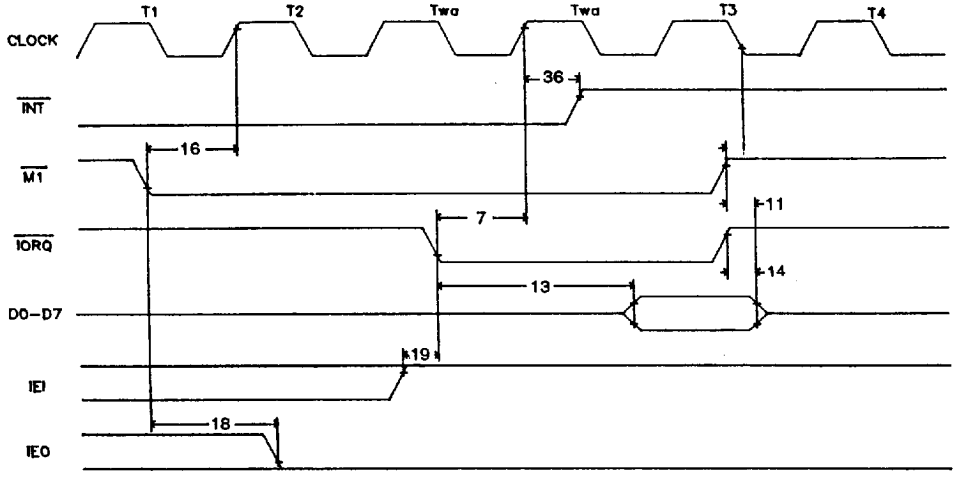
Note: The AC parameters #18, 19, 20, 21, 32, 40, 48 for 8 MHz have been changed.

Symbol	Parameter	Min	Max	Typ	Unit	Condition
V_{ILC}	Clock Input Low Voltage	-0.3	+0.45		V	
V_{IHC}	Clock Input High Voltage	V_{CC}-0.6	V_{CC}+0.3		V	
V_{IL}	Input High Voltage	2.2	V_{CC}		V	
V_{IH}	Input Low Voltage	-0.3	0.8		V	
V_{OL}	Output Low Voltage		0.4		V	I_{LO}=2.0 mA
V_{OH1}	Output High Voltage	2.4			V	IOH=-1.6mA
V_{OH2}	Output High Voltage	V_{CC}-0.8			V	I_{OH}=-250 µA
I_{LI}	Input Leakage Current	-10	10		µA	V_{IN}=0.4V to V_{CC}
I_{LO}	3-state Output Leakage Current in Float	-10	10		µA	V_{OUT}=0.4V to V_{CC}
$I_{L(SY)}$	SYNC Pin Leakage Current	-40	10		µA	V_{OUT}=0.4V to V_{CC}
I_{ODH}	Darlington Drive Current (Port B and ZC/TO0-3)	-1.5				V_{OH}=1.5V REXT = 390 Ohms
I_{CC1}	Power Supply Current - 8 MHz		15 [1]	7	mA	V_{CC}=5V
	- 10 MHz		15 [1]	7	mA	V_{IL}=0.2V
	- 12.5 MHz		15	7	mA	V_{IH}=V_{CC} - 0.2V

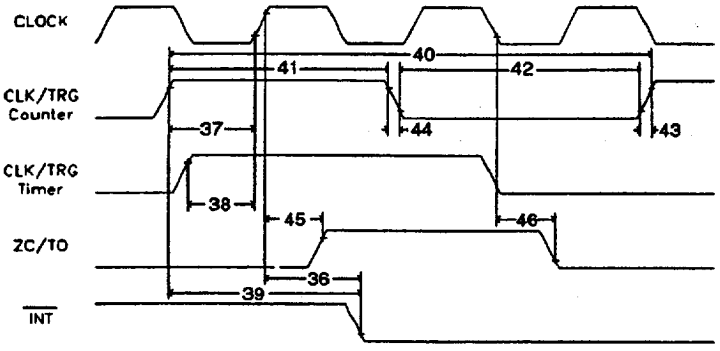
Note:
[1] Measurements made with outputs floating and XTALI at 0V.
V_{CC}=5.0V ± 10%, unless otherwise specified



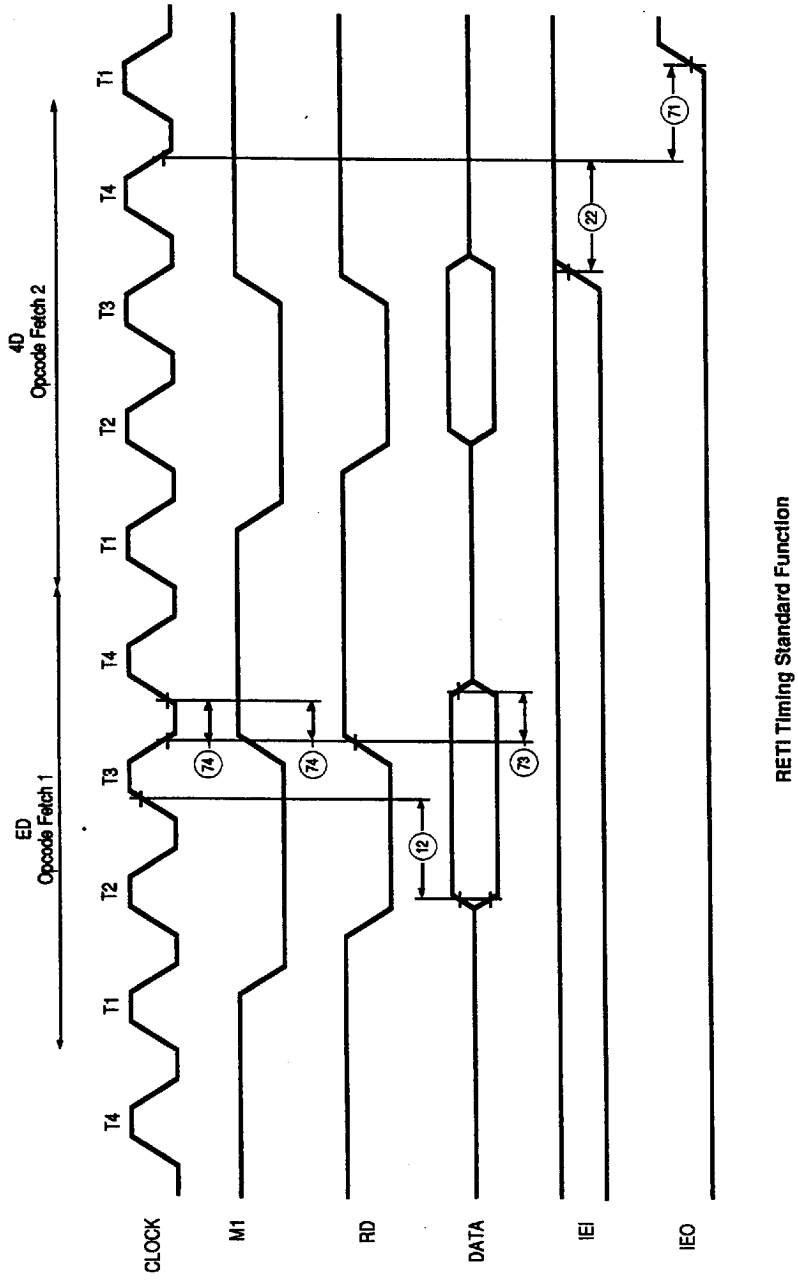
I/O Read/Write Timing ($\overline{M1}$ = 1)



Interrupt Acknowledge Cycle

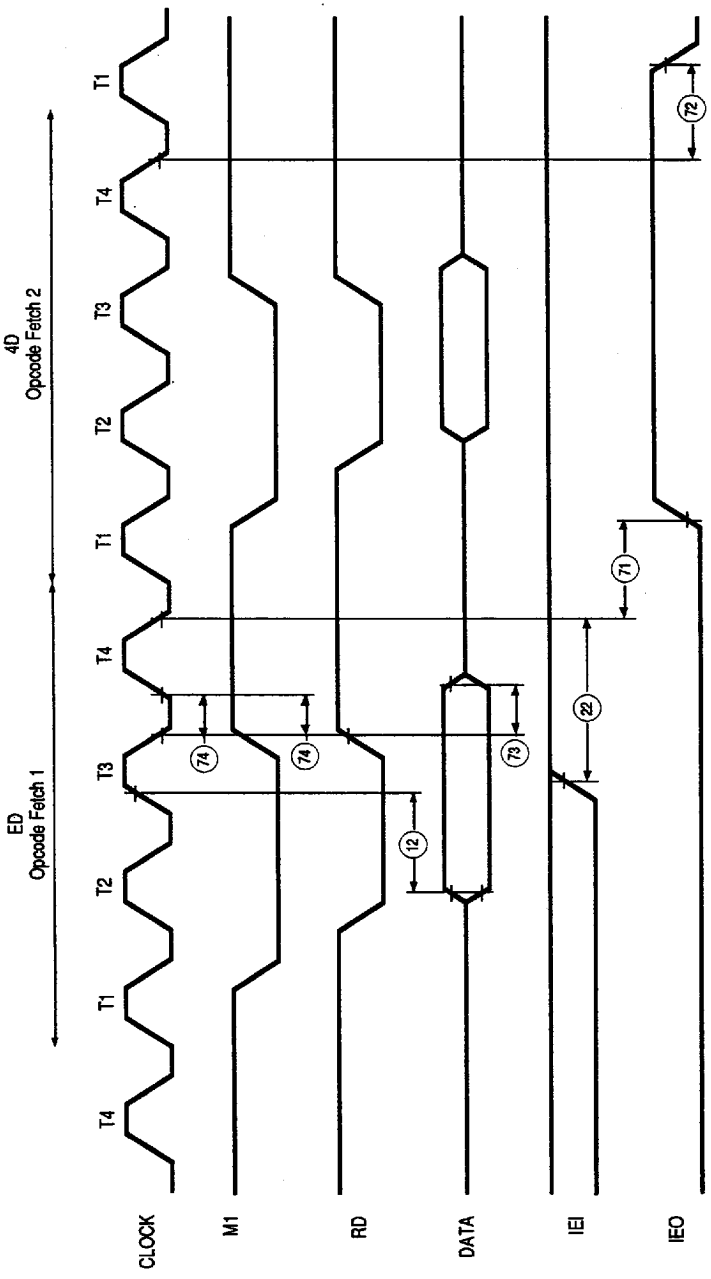


Counter/Timer Timing

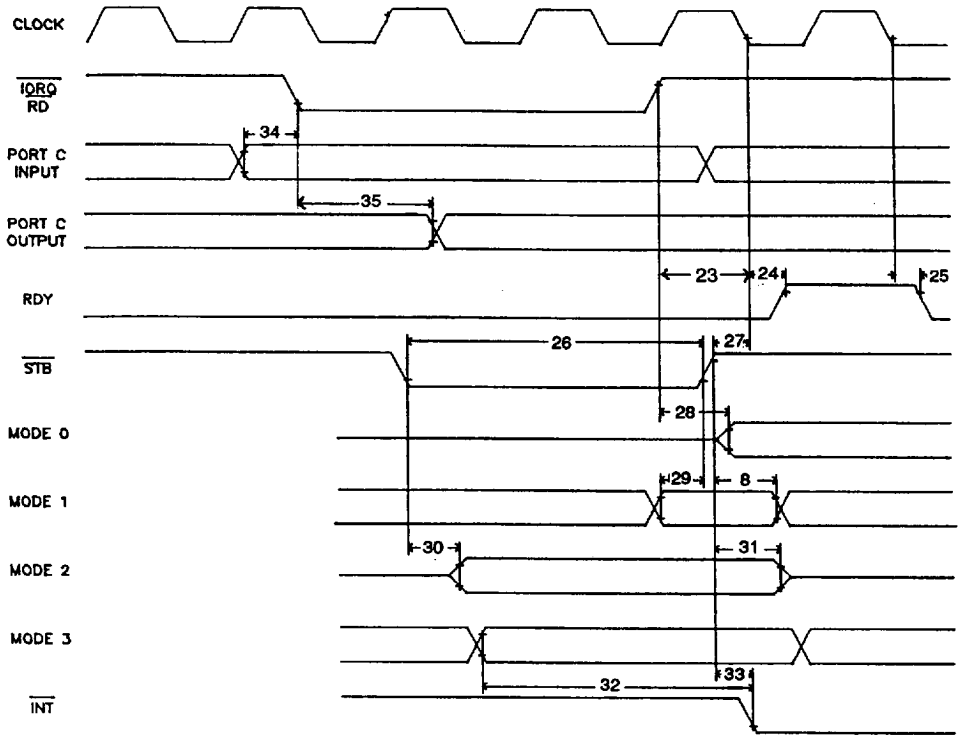


RETI Timing Standard Function

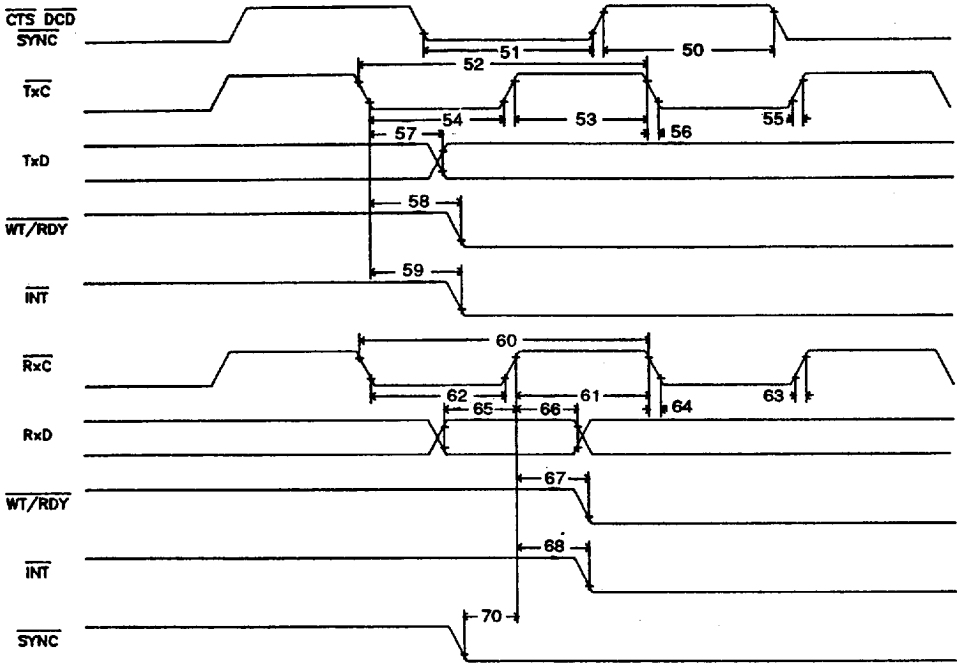
2



RETI Timing Interrupt Pending



Port I/O Read/Write Timing



Serial I/O Timing

CAPACITANCE:

Symbol	Parameter	min	max	unit
C_{CLOCK}	Clock Capactiance		10	pF
C_{IN}	Input Capacitance		10	pF
C_{OUT}	Output Capacitance		15	pF

T_A=25°C, f=1 MHz

Z84C90 AC CHARACTERISTICS
BUS Interface Timing

No	Symbol	Parameter	Z84C9008 Min	Z84C9008 Max	Z84C9010[5] Min	Z84C9010[5] Max	Z84C9012[5][6] Min	Z84C9012[5][6] Max	Note
1	TcC	Clock Cycle Time	125	DC	100	DC	80	DC	
2	TwCh	Clock Pulse Width (High)	55	DC	42	DC	32	DC	
3	TwCl	Clock Pulse Width (Low)	55	DC	42	DC	32	DC	
4	TfC	Clock Fall Time		10		10		10	
5	TrC	Clock Rise Time		10		10		10	
6	TsA(Rlf)	Address, /CS Setup Time to /RD, /IORQ Fall	50		40		30		
7	TsRl(Cr)	/IORQ, /RD to clock rise setup time	60		50		40		
8	Th	Hold Time for Specified Setup	15		15		15		
9	TdCr(DO)	Clock Rising to Data Out Delay		100		80		65	
10	TdRlr(DOz)	/RD, /IORQ Rise to Data Out Float Delay		75		60		55	
11	ThRDr(D)	/M1, /RD, /IORQ Rise to Data **M1 cycle**	15		15		15		
12	TsD(Cr)	Data In to Clock Rise Setup Time	30		25		22		
13	TdIOf(DOI)	/IORQ Fall to Data Out Delay (INTACK Cycle)		95		95	95	[1]	
14	ThIOr(D)	/IORQ Rise to Data **Float**	15		15		15		
15	ThIOr(A)	/IORQ Rise to Address Hold	15		15		15		
16	TsM1f(Cr)	/M1 Fall to Clock Rise Setup Time	40		40		40		
17	TsM1r(Cf)	/M1 Rise to Clock **Fall** Setup Time (M1 Cycle)	-15		-15		-15		
18	TdM1f(IEOf)	/M1 Fall to IEO Fall Delay (Interrupt Immediately Preceding M1 Fall)		*		*		*	[4]
19	TsIEI(IOf)	IEI to /IORQ Fall Setup Time (INTACK Cycle)		*		*		*	[4]
20	TdIEIf(IEOf)	IEI Fall to IEO Fall Delay		160		150		125	[4]
21	TdIEf(IEOr)	IEI Rise to IEO Rise Delay (After ED Decode)		160		150		125	[4]
22	TsIEI(Cf)	IEI to Clock Fall Setup (For 4D Decode)	50		40		30		
23	TsIOr(Cf)	/IORQ Rise to Clock Fall Setup Time (To Activate RDY on Next Clock Cycle)	100		100		100		

AC CHARACTERISTICS:

PIO Timing

No	Symbol	Parameter	Z84C9008 Min	Z84C9008 Max	Z84C9010[5] Min	Z84C9010[5] Max	Z84C9012[5][6] Min	Z84C9012[5][6] Max	Note
24	TdCf(RDYr)	Clock Fall to RDY Rise Delay		100		100		100	
25	TdCf(RDYf)	Clock Fall to RDY Fall Delay		100		100		100	
26	TwSTB	/STB Pulse Width	100		80		60		
27	TsSTBr(Cf)	/STB Rise to Clock Fall Setup Time (To Activate RDY On Next Clock Cycle)	100		100		100		
28	TdIOf(PD)	/IORQ Fall to Port Data Stable Delay (Mode 0)		140		120		110	
29	TsPD(STBr)	Port Data to /STB Rise Setup Time (Mode 1)	140		75		75		
30	TdSTBf(PD)	/STB Fall to Port Data Stable (Mode 2)		150		120		110	
31	TdSTBr(PDz)	/STB Rise to Port Data Float Delay (Mode 2)		140		120		110	
32	TdPD(INTf)	Port Data Match to /INT Fall Delay (Mode 3)		250		200		160	
33	TdSTBr(INTf)	/STB Rise to /INT Fall Delay		290		220		190	
34	TsPD(Rif)	PIA Port Data to /RD, /IORQ Fall Setup	TBD		TBD		TBD		
35	TdIO (PD)	IORQ Fall to PIA Port Data Valid		80		80		80	

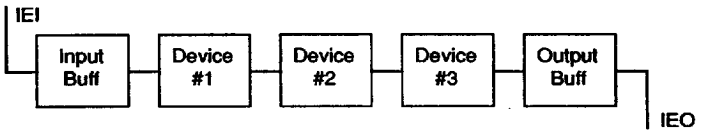
CTC Timing

No	Symbol	Parameter	Z84C9008 Min	Z84C9008 Max	Z84C9010[5] Min	Z84C9010[5] Max	Z84C9012[5] [6] Min	Z84C9012[5] [6] Max	Note
36	TdCr(INTf)	Clock Rise to /INT Fall Delay		(TcC+100)		(TcC+80)		(TcC+75)	
37	TsCTR (Cr)/	CLK/TRG to Clock Rise Setup Time for Immediate Count	90		90		75		
38	TsCTR(Ct)	CLK/TRG to Clock Rise Setup Time for Enabling of Prescaler on Following Clock Rise	90		90		75		
39	TdCTR (INTf)	CLK/TRG to /INT Fall Delay							
		TsCTR(C) Satisfied		(36)+(38)		(36)+(38)		(36)+(38)	
		TsCTR(C) Not Satisfied		(1)+(36)+(38)		(1)+(36)+(38)		(1)+(36)+(38)	
40	TcCTR	CLK/TRG Cycle Time	(2TcC)	DC	(2TcC)	DC	(2TcC)	DC	[2]
41	TwCTRh	CLK/TRG Width (High)	90	DC	90	DC	75	DC	
42	TwCTRl	CLK/TRG Width (Low)	90	DC	90	DC	75	DC	
43	TrCTR	CLK/TRG Rise Time		30		30		30	
44	TfCTR	CLK/TRG Fall Time		30		30		30	
45	TdCr(ZCr)	Clock Rise to ZC/TO Rise Delay		80		80		80	
46	TdCf(ZCf)	Clock Fall to ZC/TO Fall Delay		80		80		80	

No	Symbol	Parameter	Z84C9008 Min	Z84C9008 Max	Z84C9010[5] Min	Z84C9010[5] Max	Z84C9012[5][6] Min	Z84C9012[5][6] Max	Note
47	TdIOf(W/Rf)	/IORQ or /CE Fall to /W//RDY Delay (Wait Mode)		130		110		110	
48	TdCr(W/Rf)	Clock Rise to /W//RDY Delay (Ready Mode)		85		85		85	
49	TdCf(W/Rz)	Clock Fall to /W//RDY Float Delay (Wait Mode)		90+RC		80+RC		75+RC	[7]
50	TwPh	Pulse Width (High)	150		120		100		
51	TwPl	Pulse Width (Low)	150		120		100		
52	TcTxC	/TxC Cycle Time	250		200		160		
53	TwTxCl	/TxC Width (Low)	85		80		70		
54	TwTxCh	/TxC Width (High)	85		80		70		
55	TrTxC	/TxC Rise Time		60		60		60	
56	TfTxC	/TxC Fall Time		60		60		60	
57	TdTxCf(TxD)	/TxC Fall to TxD Delay		160		120		115	
58	TdTxCf(W/RRf)	/TxC Fall to /W//RDY Fall Delay (Ready Mode)	5	9	5	9	5	9	[3]
59	TdTxCf(INTf)	/TxC Fall to /INT Fall Delay	5	9	5	9	5	9	[3]
60	TcRxC	/RxC Cycle Time	250		200		160		
61	TwRxCh	/RxC Width (High)	85		80		70		
62	TwRxCl	/RxC Width (Low)	85		80		70		
63	TrRxC	/RxC Rise Time		60		60		60	
64	TfRxC	/RxC Fall Time		60		60		60	
65	TsRxD(RxCr)	RxD to /RxC Rise Setup Time (X1 Mode)	0		0		0		
66	ThRxCr(RxD)	/RxC Rise to RxD Hold Time (X1 Mode)	80		60		50		
67	TdRxCr(W/RRf)	/RxC Rise to /W//RDY Fall Delay (Ready Mode)	10	13	10	13	10	13	[3]
68	TdRxCr(INTf)	/RxC Rise to /INT Fall Delay	10	13	10	13	10	13	[3]
69	TdRxCr(SYNCf)	/RxC Rise to /SYNC Fall Delay (Output Modes)	4	7	4	7	4	7	[3]
70	TsSYNCf(RxCr)	/SYNC Fall to /RxC Rise Setup (External Sync Modes)	-100		-100		-100		

No	Symbol	Parameter	Z84C9008 Min	Z84C9008 Max	Z84C9010 [5] Min	Z84C9010 [5] Max	Z84C9012 [5,6] Min	Z84C9012 [5,6] Max	Note
71	TdCf(IEOr)	Clock Fall to IEO Rise Delay		90		75		60	
72	TdCf(IEOf)	Clock Fall to IEO Rise Delay		110		90		75	
73	ThDI(M1r,RDr)	Data Hold Time to /M1 Rise or /RD Rise	0		0		0		
74	TsM1/RD(C)	Setup Time For M1 and RD to Clock Rising (with Data Valid)	20		20		20		

Notes:
[1] If the CPU is Z80 and Clock speed is above 8 MHz, one wait state is required to meet this parameter.
[2] Counter Mode only; when using a cycle time less than 3TcC, parameter #37 must be met.
[3] Units equal to System Clock Cycles.
[4] Parameters #18, 19, 20 and 21. These parameters are daisy-chain timing and calculated value and vary depending on the inside daisy-chain configuration which is specified in the KIO command register. Inside the Z80 KIO, the daisy-chain is figured below.
[5] If the CPU is a Z80 CPU; and if it is required to have multiple Z80 peripherals in the system. For this case, only one Z80 peripheral other than Z84C90 is the maximum number of peripherals unless the time period between "/M1 active to /IORQ active" is extended.
[5] * In All Modes, the System Clock rate must be at least five times the maximum data rate.
[6] Timings for 12.5 MHz are preliminary.
[7] Open drain output add register capacitor time constraint (RC) to spec. value.



Internal Daisy Chain Configuration

Z84C90 AC CHARACTERISTICS (Continued)

Table for Note [4] parameters

No	Parameter		8 MHz Min	8 MHz Max	10 MHz Min	10 MHz Max	12.5 MHz Min	12.5 MHz Max
18	TdM1(IEO)	(PIO at #1)		160 ns		150 ns		125 ns
		(CTC at #1)		180 ns		150 ns		125 ns
		(SIO at #1)		230 ns		200 ns		160 ns
19	TsIEI(IO)	(PIO at #3)	170 ns		140 ns		115 ns	
		(CTC at #3)	170 ns		160 ns		135 ns	
		(SIO at #3)	180 ns		160 ns		130 ns	
20	TdIEI(IEOf)			160 ns		150 ns		125 ns
21	TdIEI(IEOr)			160 ns		150 ns		125 ns

To calculate Z80 KIO daisy-chain timing, use the Z80 PIO, CTC and SIO with I/O buffers on the chain. The following are calculation formulas:

Parameter #18
M1 falling to IEO delay TsM1(IEO) = TdM1(IO)#1 + TdIEI(IEO)#2 + TdIEI(IEO)#3 + (Output Buffer Delay)

Parameter #19
IEI to IORQ falling setup time TsIEI(IO) = TdIEI(IEO)#1 + TdIEI(IEO)#2 + TsIEI(IO)#3 + (Input Buffer delay)

Parameter #20
IEI falling to IEO falling delay- TdIEI(IEOf) - TdIEI(IEOf)PIO + TdIEI(IEOf)CTC + TdIEI(IEOf)SIO + (Input Buffer delay) + (output Buffer Delay)

Parameter #21
IEI rising to IEO rising delay (After ED decode)- TdIEI(IEOr) = TdIEI(IEOr)PIO+ TdIEI(IEOr)CTC + TdIEI(IEOr)SIO + (Input Buffer delay) + (output Buffer Delay)

* Where TdIEI(IEO) is the worst number between TdIEI(IEOr) and TdIEI(IEOf).

The following are numbers for the above calculations:

	8 MHz Min	8 MHz Max	10 MHz Min	10 MHz Max	12.5 MHz Min	12.5 MHz Max
Input Buffer delay	10 ns		10 ns		10 ns	
Output Buffer delay	10 ns		10 ns		10 ns	

8 MHz	PIO part Min	PIO part Max	CTC part Min	CTC part Max	SIO part Min	SIO part Max
TdM1(IEO)	60 ns		80 ns		120 ns	
TsIEI(IO)	70 ns		70 ns		70 ns	
TdIEI(IEOf)		50 ns		50 ns		40 ns
TdIEI(IEOr)		50 ns		50 ns		40 ns

10 MHz	PIO part Min	PIO part Max	CTC part Min	CTC part Max	SIO part Min	SIO part Max
TdM1(IEO)	60 ns		60 ns		90 ns	
TsIEI(IO)	50 ns		70 ns		50 ns	
TdIEI(IEOf)		50 ns		50 ns		30 ns
TdIEI(IEOr)		50 ns		50 ns		30 ns

12.5 MHz	PIO part Min	PIO part Max	CTC part Min	CTC part Max	SIO part Min	SIO part Max
TdM1(IEO)	50 ns		50 ns		70 ns	
TsIEI(IO)	40 ns		60 ns		40 ns	
TdIEI(IEOf)		40 ns		40 ns		25 ns
TdIEI(IEOr)		40 ns		40 ns		25 ns

Note [4] (Continued)

When using an interrupt from only a portion of the Z80 KIO, these numbers are smaller than the values shown above.

For more details about the "Z80 daisy-chain structure", please refer to the application note "Z80 Family Interrupt Structure," which is included in the Z80 Data Book.