128 macrocell CPLD | PZ5128

FEATURES

- Industry's first TotalCMOS™ PLD – both CMOS design and process technologies
- Fast Zero Power (FZP™) design technique provides ultra-low power and very high speed
- IEEE 1149.1–compliant, JTAG Testing Capability
  - 4 pin JTAG interface (TCK, TMS, TDI, TDO)
  - IEEE 1149.1 TAP Controller
  - JTAG commands include: Bypass, Sample/Preload, Extest, Usercode, Idcode, HighZ
- 5 Volt, In–System Programmable (ISP) using the JTAG interface
  - On–chip supervoltage generation
  - ISP commands include: Enable, Erase, Program, Verify
  - Supported by multiple ISP programming platforms
- High speed pin-to-pin delays of 7.5ns
- Ultra-low static power of less than 100µA
- Dynamic power that is 70% lower at 50MHz than competing devices
- 100% rcutable with 100% utilization while all pins and all macrocells are fixed
- Deterministic timing model that is extremely simple to use
- 4 clocks with programmable polarity at every macrocell
- Support for asynchronous clocking
- Innovative XPLA™ architecture combines high speed with extreme flexibility
- 1000 erase/program cycles guaranteed
- 20 years data retention guaranteed
- Logic expandable to 37 product terms
- PCI compliant
- Advanced 0.5µ E^2CMOS process
- Security bit prevents unauthorized access
- Design entry and verification using industry standard and Philips CAE tools
- Reprogrammable using industry standard device programmers
- Innovative Control Term structure provides either sum terms or product terms in each logic block for:
  - Programmable 3-State buffer
  - Asynchronous macrocell register preset/reset
- Programmable global 3-State pin facilitates 'bed of nails' testing without using logic resources
- Available in PLCC, TQFP, and PQFP packages
- Available in both Commercial and Industrial grades

Table 1. PZ5128 Features

	PZ5128
Usable gates	4000
Maximum inputs	100
Maximum I/Os	96
Number of macrocells	128
Propagation delay (ns)	7.5
Packages	84-pin PLCC, 100-pin PQFP, 100-pin TQFP 128-pin LQFP, 160-pin PQFP

DESCRIPTION

The PZ5128 CPLD (Complex Programmable Logic Device) is the third in a family of Fast Zero Power (FZP™) CPLDs from Philips Semiconductors. These devices combine high speed and zero power in a 128 macrocell CPLD. With the FZP™ design technique, the PZ5128 offers true pin-to-pin speeds of 7.5ns, while simultaneously delivering power that is less than 100µA at standby without the need for 'turbo bits' or other power down schemes. By replacing conventional sense amplifier methods for implementing product terms (a technique that has been used in PLDs since the bipolar era) with a cascaded chain of pure CMOS gates, the dynamic power is also substantially lower than any competing CPLD – 70% lower at 50MHz. These devices are the first TotalCMOS™ PLDs, as they use both a CMOS process technology **and** the patented full CMOS FZP™ design technique. For 3V applications, Philips also offers the high speed PZ3128 CPLD that offers these features in a full 3V implementation.

The Philips FZP™ CPLDs introduce the new patent-pending XPLA™ (eXtended Programmable Logic Array) architecture. The XPLA™ architecture combines the best features of both PLA and PAL™ type structures to deliver high speed and flexible logic allocation that results in superior ability to make design changes with fixed pinouts. The XPLA™ structure in each logic block provides a fast 10ns PAL™ path with 5 dedicated product terms per output. This PAL™ path is joined by an additional PLA structure that deploys a pool of 32 product terms to a fully programmable OR array that can allocate the PLA product terms to any output in the logic block. This combination allows logic to be allocated efficiently throughout the logic block and supports as many as 37 product terms on an output. The speed with which logic is allocated from the PLA array to an output is only 2ns, regardless of the number of PLA product terms used, which results in worst case t_{PD}'s of only 9.5ns from any pin to any other pin. In addition, logic that is common to multiple outputs can be placed on a single PLA product term and shared across multiple outputs via the OR array, effectively increasing design density.

The PZ5128 CPLDs are supported by industry standard CAE tools (Cadence, Exemplar Logic, Minc, Mentor, Synopsys, Synario, Viewlogic, MINC), using text (Abel, VHDL, Verilog) and/or schematic entry. Design verification uses industry standard simulators for functional and timing simulation. Development is supported on personal computer, Sparc, and HP platforms. Device fitting uses either MINC or Philips Semiconductors-developed tools.

The PZ5128 CPLD is electrically reprogrammable using industry standard device programmers from vendors such as Data I/O, BP Microsystems, SMS, and others. The PZ5128 also includes an industry-standard, IEEE 1149.1, JTAG interface through which in-system programming (ISP) and reprogramming of the device is supported.

PAL is a registered trademark of Advanced Micro Devices, Inc.

ORDERING INFORMATION

ORDER CODE	DESCRIPTION	DESCRIPTION	DRAWING NUMBER
PZ5128–S7A84	84–pin PLCC, 7.5ns t_{PD}	Commercial temp range, 5 volt power supply, ± 5%	SOT189–3
PZ5128-S10A84	84-pin PLCC, 10ns t_{PD}	Commercial temp range, 5 volt power supply, ± 5%	SOT189-3
PZ5128-S12A84	84-pin PLCC, 12ns t_{PD}	Commercial temp range, 5 volt power supply, ± 5%	SOT189-3
PZ528IS10A84	84–pin PLCC, 10ns t_{PD}	Industrial temp range, 5 volt power supply, ± 10%	SOT189–3
PZ5128IS15A84	84-pin PLCC, 15ns t_{PD}	Industrial temp range, 5 volt power supply, ± 10%	SOT189-3
PZ5128–S7BB1	100–pin PQFP, 7.5ns t_{PD}	Commercial temp range, 5 volt power supply, ± 5%	SOT382–1
PZ5128-S10BB1	100-pin PQFP, 10ns t_{PD}	Commercial temp range, 5 volt power supply, ± 5%	SOT382-1
PZ5128-S12BB1	100-pin PQFP, 12ns t_{PD}	Commercial temp range, 5 volt power supply, ± 5%	SOT382-1
PZ5128IS10BB1	100–pin PQFP, 10ns t_{PD}	Industrial temprange, 5 volt power supply, ± 10%	SOT382–1
PZ5128IS15BB1	100-pin PQFP, 15ns t_{PD}	Industrial temp range, 5 volt power supply, ± 10%	SOT382-1
PZ5128–S7BBP	100–pin TQFP, 7.5ns t_{PD}	Commercial temp range, 5 volt power supply, ± 5%	SOT386–1
PZ5128-S10BP	100-pin TQFP, 10ns t_{PD}	Commercial temp range, 5 volt power supply, ± 5%	SOT386-1
PZ5128-S12BP	100-pin TQFP, 12ns t_{PD}	Commercial temp range, 5 volt power supply, ± 5%	SOT386-1
PZ5128IS10BP	100–pin TQFP, 10ns t_{PD}	Industrial temp range, 5 volt power supply, ± 10%	SOT386–1
PZ5128IS15BP	100-pin TQFP, 15ns t_{PD}	Industrial temp range, 5 volt power supply, ± 10%	SOT386-1
PZ5128–S7BE	128–LQFP, 7.5ns t_{PD}	Commercial temp range, 5 volt power supply, ± 5%	SOT425–1
PZ5128-S10BE	128-pin LQFP, 10ns t_{PD}	Commercial temp range, 5 volt power supply, ± 5%	SOT425-1
PZ5128-S12BE	128-pin LQFP, 12ns t_{PD}	Commercial temp range, 5 volt power supply, ± 5%	SOT425-1
PZ5128IS10BE	128–pin LQFP, 10ns t_{PD}	Industrial temp range, 5 volt power supply, ± 10%	SOT425–1
PZ5128IS15BE	128-pin LQFP, 15ns t_{PD}	Industrial temp range, 5 volt power supply, ± 10%	SOT425-1
PZ5128–S7BB2	160–pin PQFP, 7.5ns t_{PD}	Commercial temp range, 5 volt power supply, ± 5%	SOT322–2
PZ5128-S10BB2	160-pin PQFP, 10ns t_{PD}	Commercial temp range, 5 volt power supply, ± 5%	SOT322-2
PZ5128-S12BB2	160-pin PQFP, 12ns t_{PD}	Commercial temp range, 5 volt power supply, ± 5%	SOT322-2
PZ5128IS10BB2	160–pin PQFP, 10ns t_{PD}	Industrial temp range, 5 volt poweer supply, ± 10%	SOT322–2
PZ5128IS15BB2	160-pin PQFP, 15ns t_{PD}	Industrial temp range, 5 volt power supply, ± 10%	SOT322-2

XPLA™ ARCHITECTURE

Figure 1 shows a high level block diagram of a 128 macrocell device implementing the XPLA™ architecture. The XPLA™ architecture consists of logic blocks that are interconnected by a Zero-power Interconnect Array (ZIA). The ZIA is a virtual crosspoint switch. Each logic block is essentially a 36V16 device with 36 inputs from the ZIA and 16 macrocells. Each logic block also provides 32 ZIA feedback paths from the macrocells and I/O pins.

From this point of view, this architecture looks like many other CPLD architectures. What makes the CoolRunner™ family unique is what is inside each logic block and the design technique used to implement these logic blocks. The contents of the logic block will be described next.

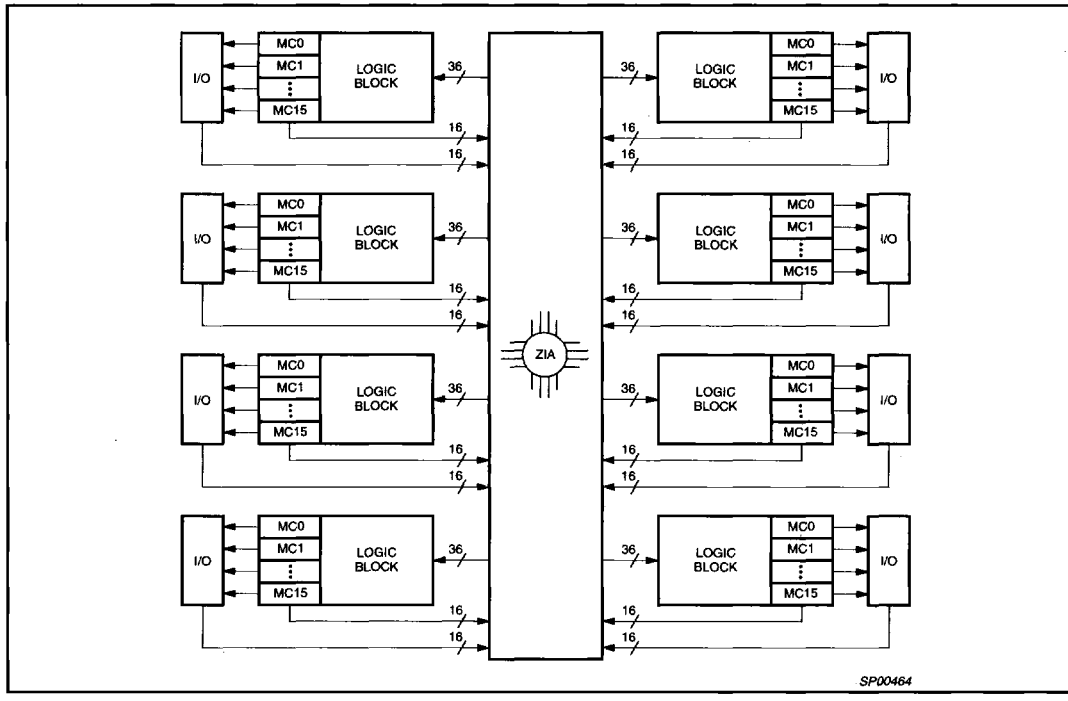


Figure 1. Philips XPLA CPLD Architecture

Logic Block Architecture

Figure 2 illustrates the logic block architecture. Each logic block contains control terms, a PAL array, a PLA array, and 16 macrocells. the 6 control terms can individually be configured as either SUM or PRODUCT terms, and are used to control the preset/reset and output enables of the 16 macrocells' flip-flops. The PAL array consists of a programmable AND array with a fixed OR array, while the PLA array consists of a programmable AND array with a programmable OR array. The PAL array provides a high speed path through the array, while the PLA array provides increased product term density.

Each macrocell has 5 dedicated product terms from the PAL array. The pin-to-pin t_{PD} of the PZ5128 device through the PAL array is 7.5ns. If a macrocell needs more than 5 product terms, it simply gets the additional product terms from the PLA array. The PLA array consists of 32 product terms, which are available for use by all 16 macrocells. The additional propagation delay incurred by a macrocell using 1 or all 32 PLA product terms is just 2ns. So the total pin-to-pin t_{PD} for the PZ5128 using 6 to 37 product terms is 9.5ns (7.5ns for the PAL + 2ns for the PLA).

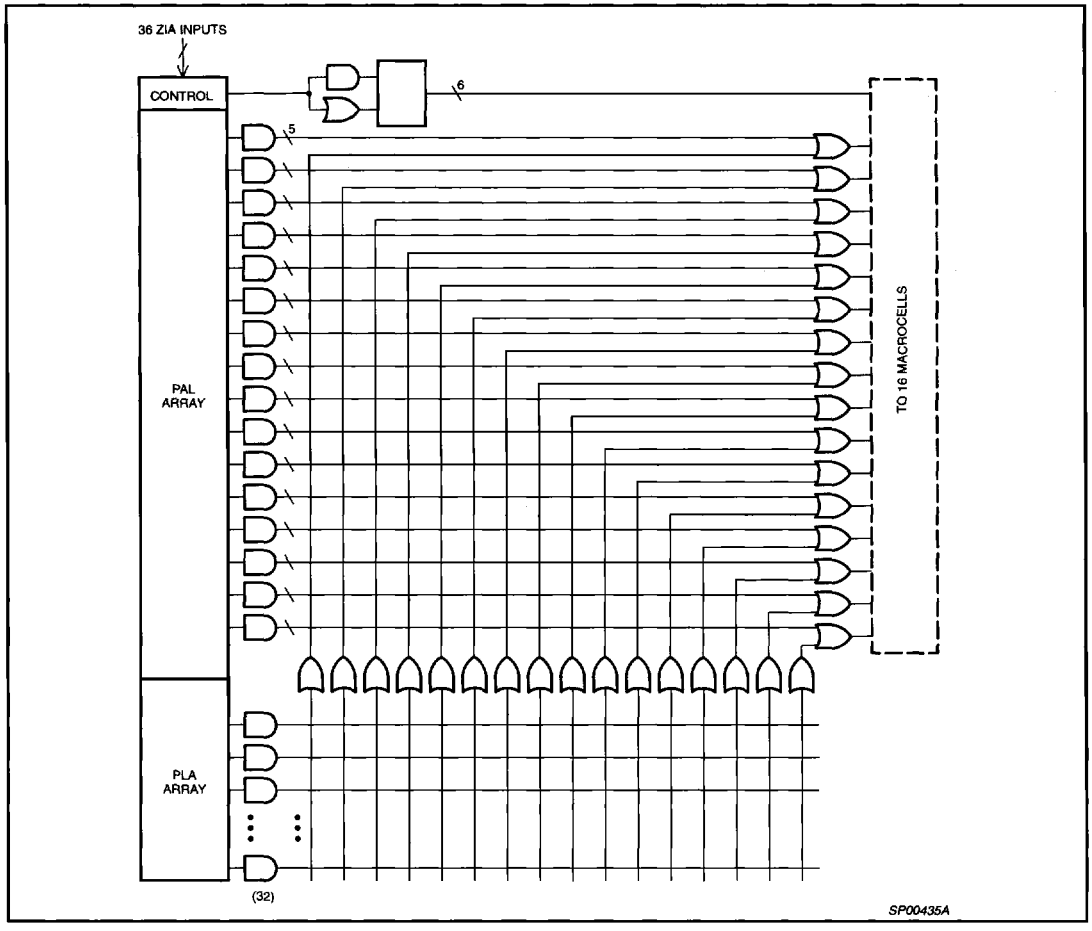


Figure 2. Philips XPLA Logic Block Architecture

Macrocell Architecture

Figure 3 shows the architecture of the macrocell used in the CoolRunner™ family. The macrocell consists of a flip-flop that can be configured as either a D or T type. A D-type flip-flop is generally more useful for implementing state machines and data buffering. A T-type flip-flop is generally more useful in implementing counters. All CoolRunner™ family members provide both synchronous and asynchronous clocking and provide the ability to clock off either the falling or rising edges of these clocks. These devices are designed such that the skew between the rising and falling edges of a clock are minimized for clocking integrity. There are 4 clocks available on the PZ5128 device. Clock 0 (CLK0) is designated as the "synchronous" clock and must be driven by an external source. Clock 1 (CLK1), Clock 2 (CLK2), and Clock 3 (CLK3) can either be used as a synchronous clock (driven by an external source) or as an asynchronous clock (driven by a macrocell equation). The timing for asynchronous clocks is different in that the t_{CO} time is extended by the amount of time that it takes for the signal to propagate through the array and reach the clock network, and the t_{SU} time is reduced. Please see the application note titled "Understanding CoolRunner Clocking Options" for more detail.

Two of the control terms (CT0 and CT1) are used to control the Preset/Reset of the macrocell's flip-flop. The Preset/Reset feature for each macrocell can also be disabled. Note that the Power-on Reset leaves all macrocells in the "zero" state when power is properly applied. The other 4 control terms (CT2–CT5) can be used to control the Output Enable of the macrocell's output buffers. The reason there are as many control terms dedicated for the Output Enable of the macrocell is to insure that all CoolRunner™ devices are PCI compliant. The macrocell's output buffers can also be always enabled or disabled. All CoolRunner™ devices also provide a Global Tri-State ($\overline{GTS}$) pin, which, when enabled and pulled Low, will 3-State all the outputs of the device. This pin is provided to support "In-Circuit Testing" or "Bed-of-Nails Testing".

There are two feedback paths to the ZIA: one from the macrocell, and one from the I/O pin. The ZIA feedback path before the output buffer is the macrocell feedback path, while the ZIA feedback path after the output buffer is the I/O pin ZIA path. When the macrocell is used as an output, the output buffer is enabled, and the macrocell feedback path can be used to feedback the logic implemented in the macrocell. When the I/O pin is used as an input, the output buffer will be 3-Stated and the input signal will be fed into the ZIA via the I/O feedback path, and the logic implemented in the buried macrocell can be fed back to the ZIA via the macrocell feedback path. It should be noted that unused inputs or I/Os should be properly terminated.

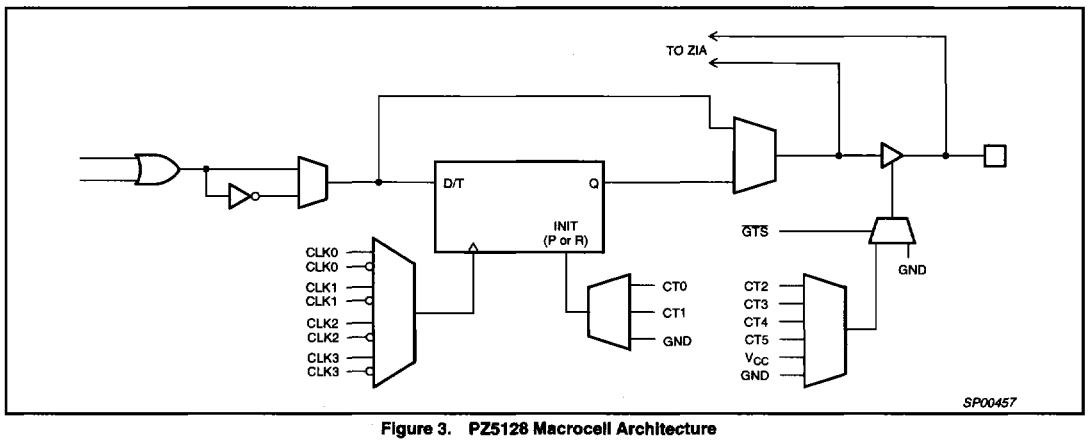


Figure 3. PZ5128 Macrocell Architecture

Simple Timing Model

Figure 4 shows the CoolRunner™ Timing Model. The CoolRunner™ timing model looks very much like a 22V10 timing model in that there are three main timing parameters, including t_{PD}, t_{SU}, and t_{CO}. In other competing architectures, the user may be able to fit the design into the CPLD, but is not sure whether system timing requirements can be met until after the design has been fit into the device. This is because the timing models of competing architectures are very complex and include such things as timing dependencies on the number of parallel expanders borrowed, sharable expanders, varying number of X and Y routing channels used, etc. In the XPLA™ architecture, the user knows up front whether the design will meet system timing requirements. This is due to the simplicity of the timing model.

TotalCMOS™ Design Technique for Fast Zero Power

Philips is the first to offer a TotalCMOS™ CPLD, both in process technology and design technique. Philips employs a cascade of CMOS gates to implement its Sum of Products instead of the traditional sense amp approach. This CMOS gate implementation allows Philips to offer CPLDs which are both high performance and low power, breaking the paradigm that to have low power, you must have low performance. Refer to Figure 5 and Table 2 showing the I_{DD} vs. Frequency of our PZ5128 TotalCMOS™ CPLD (data taken w/eight up/down, loadable 16 bit counters@5V, 25°C.

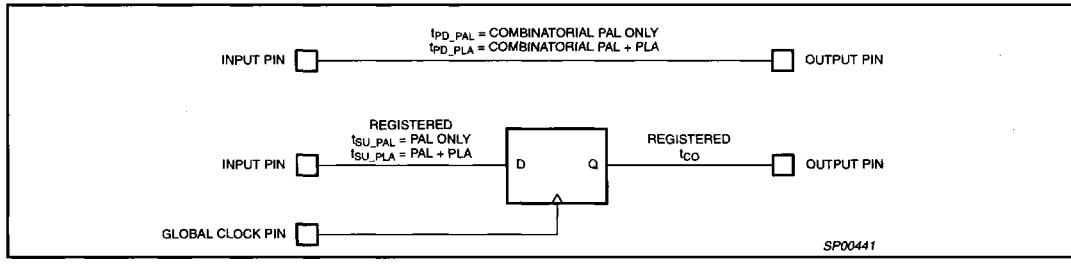


Figure 4. CoolRunner™ Timing Model

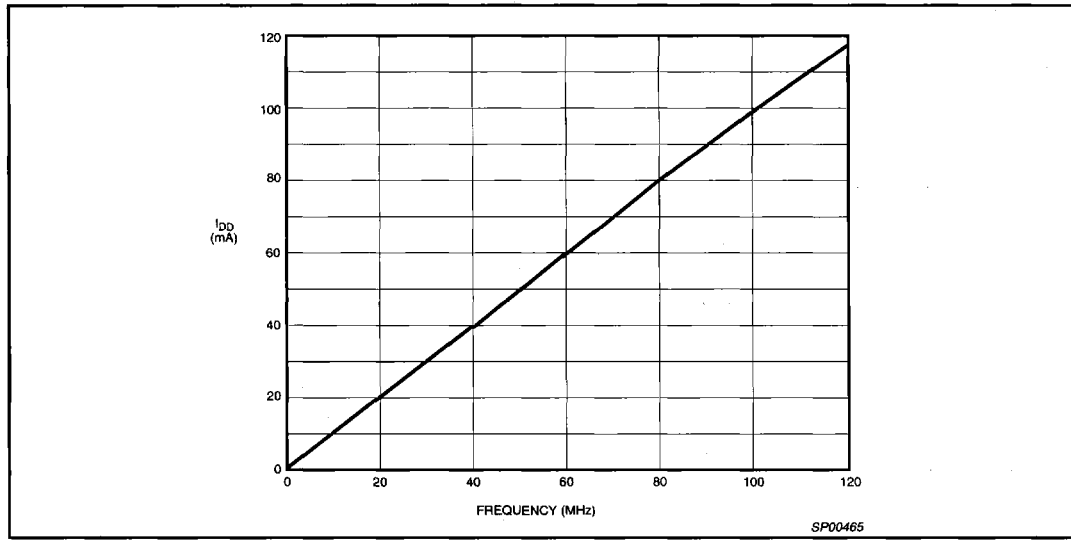


Figure 5. I_{DD} vs. Frequency @ V_{DD} = 5.0V, 25°C

Table 2. I_{DD} vs. Frequency

V_{DD} = 5.00V

FREQUENCY (MHz)	0	1	20	40	60	80	100	120
Typical I_{DD} (mA)	0.5	1	20	40	60	80	99	118

JTAG Testing Capability

JTAG is the commonly-used acronym for the Boundary Scan Test (BST) feature defined for integrated circuits by IEEE Standard 1149.1. This standard defines input/output pins, logic control functions, and commands which facilitate both board and device level testing without the use of specialized test equipment. BST provides the ability to test the external connections of a device, test the internal logic of the device, and capture data from the device during normal operation. BST provides a number of benefits in each of the following areas:

- Testability
  - Allows testing of an unlimited number of interconnects on the printed circuit board
  - Testability is designed in at the component level
  - Enables desired signal levels to be set at specific pins (Preload)
  - Data from pin or core logic signals can be examined during normal operation
- Reliability
  - Eliminates physical contacts common to existing test fixtures (e.g., "bed-of-nails")
  - Degradation of test equipment is no longer a concern
  - Facilitates the handling of smaller, surface-mount components
  - Allows for testing when components exist on both sides of the printed circuit board
- Cost
  - Reduces/eliminates the need for expensive test equipment
  - Reduces test preparation time
  - Reduces spare board inventories

The Philips PZ5128's JTAG interface includes a TAP Port and a TAP Controller, both of which are defined by the IEEE 1149.1 JTAG Specification. As implemented in the Philips PZ5128, the TAP Port includes four of the five pins (refer to Table 3) described in the JTAG specification: TCK, TMS, TDI, and TDO. The fifth signal defined by the JTAG specification is TRST* (Test Reset). TRST* is considered an optional signal, since it is not actually required to perform BST or ISP. The Philips PZ5128 saves an I/O pin for general purpose use by not implementing the optional TRST* signal in the JTAG interface. Instead, the Philips PZ5128 supports the test reset functionality through the use of its power up reset circuit, which is included in all Philips CPLDs. The pins associated with the power up reset circuit should connect to an external pull-up resistor to keep the JTAG signals from floating when they are not being used.

In the Philips PZ5128, the four mandatory JTAG pins each require a unique, dedicated pin on the device. However, if JTAG and ISP are not desired in the end-application, these pins may instead be used as additional general I/O pins. The decision as to whether these pins are used for JTAG/ISP or as general I/O is made when the JEDEC file is generated. If the use of JTAG/ISP is selected, the dedicated pins are not available for general purpose use. However, unlike competing CPLD's, the Philips PZ5128 does allow the macrocell logic associated with these dedicated pins to be used as buried logic even when JTAG/ISP is selected. Table 4 defines the dedicated pins used by the four mandatory JTAG signals for each of the PZ5128 package types.

The JTAG specifications defines two sets of commands to support boundary-scan testing: high-level commands and low-level commands. High-level commands are executed via board test software on an a user test station such as automated test equipment, a PC, or an engineering workstation (EWS). Each high-level command comprises a sequence of low level commands. These low-level commands are executed within the component under test, and therefore must be implemented as part of the TAP Controller design. The set of low-level boundary-scan commands implemented in the Philips PZ5128 is defined in Table 5. By supporting this set of low-level commands, the PZ5128 allows execution of all high-level boundary-scan commands.

Table 3. JTAG Pin Description

PIN	NAME	DESCRIPTION
TCK	Test Clock Output	Clock pin to shift the serial data and instructions in and out of the TDI and TDO pins, respectively. TCK is also used to clock the TAP Controller state machine.
TMS	Test Mode Select	Serial input pin selects the JTAG instruction mode. TMS should be driven high during user mode operation.
TDI	Test Data Input	Serial input pin for instructions and test data. Data is shifted in on the rising edge of TCK.
TDO	Test Data Output	Serial output pin for instructions and test data. Data is shifted out on the falling edge of TCK. The signal is tri-stated if data is not being shifted out of the device.

Table 4. PZ5128 JTAG Pinout by Package Type

DEVICE	(PIN NUMBER / MACROCELL #)			
	TCK	TMS	TDI	TDO
PZ5128				
84-pin PLCC	62 / 96 (F15)	23 / 48 (C15)	14 / 32 (B15)	71 / 112 (G15)
100-pin PQFP	64 / 96 (F15)	17 / 48 (C15)	6 / 32 (B15)	75 / 112 (G15)
100-pin TQFP	62 / 96 (F15)	15 / 48 (C15)	4 / 32 (B15)	73 / 112 (G15)
128-pin LQFP	82 / 96 (F15)	21 / 48 (C15)	8 / 32 (B15)	95 / 112 (G15)
160-pin PQFP	99 / 96 (F15)	22 / 48 (C15)	9 / 32 (B15)	112/ 112 (G15)

Table 5. PZ5128 Low-Level JTAG Boundary-Scan Commands

INSTRUCTION (Instruction Code) *Register Used*	DESCRIPTION
Sample/Preload (0010) *Boundary–Scan Register*	The mandatory SAMPLE/PRELOAD instruction allows a snapshot of the normal operation of the component to be taken and examined. It also allows data values to be loaded onto the latched parallel outputs of the Boundary-Scan Shift-Register prior to selection of the other boundary-scan test instructions.
Extest (0000) *Boundary-Scan Register*	The mandatory EXTEST instruction allows testing of off-chip circuitry and board level interconnections. Data would typically be loaded onto the latched parallel outputs of Boundary-Scan Shift-Register using the Sample/Preload instruction prior to selection of the EXTEST instruction.
Bypass (1111) *Bypass Register*	Places the 1 bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation. The Bypass instruction can be entered by holding TDI at a constant high value and completing an Instruction-Scan cycle.
Idcode (0001) *Boundary-Scan Register*	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO. The IDCODE instruction permits blind interrogation of the components assembled onto a printed circuit board. Thus, in circumstances where the component population may vary, it is possible to determine what components exist in a product.
HighZ (0101) *Bypass Register*	The HIGHZ instruction places the component in a state in which all of its system logic outputs are placed in an inactive drive state (e.g., high impedance). In this state, an in-circuit test system may drive signals onto the connections normally driven by a component output without incurring the risk of damage to the component. The HighZ instruction also forces the Bypass Register between TDI and TDO.

5-Volt, In-System Programming (ISP)

ISP is the ability to reconfigure the logic and functionality of a device, printed circuit board, or complete electronic system before, during, and after its manufacture and shipment to the end customer. ISP provides substantial benefits in each of the following areas:

- Design
  - Faster time-to-market
  - Debug partitioning and simplified prototyping
  - Printed circuit board reconfiguration during debug
  - Better device and board level testing
- Manufacturing
  - Multi-Functional hardware
  - Reconfigurability for Test
  - Eliminates handling of "fine lead-pitch" components for programming
  - Reduced Inventory and manufacturing costs
  - Improved quality and reliability
- Field Support
  - Easy remote upgrades and repair
  - Support for field configuration, re-configuration, and customization

The Philips PZ5128 allows for 5-Volt, in-system programming/reprogramming of its EEPROM cells via its JTAG interface. An on-chip charge pump eliminates the need for externally-provided supervoltages, so that the PZ5128 may be easily programmed on the circuit board using only the 5-volt supply required by the device for normal operation. A set of low-level ISP basic commands implemented in the PZ5128 enable this feature. The ISP commands implemented in the Philips PZ5128 are specified in Table 6. Please note that an ENABLE command must precede all ISP commands **unless** an ENABLE command has already been given for a preceding ISP command **and** the device has not gone through a Test-Logic/Rest TAP Controller State.

Table 6. Low Level ISP Commands

INSTRUCTION *(Register Used)*	INSTRUCTION CODE	DESCRIPTION
Enable *(ISP Shift Register)*	1001	*Enables the Erase, Program, and Verify commands. Using the ENABLE instruction before the* Erase, Program, and Verify instructions allows the user to specify the outputs the device using the JTAG Boundary–Scan SAMPLE/PRELOAD command.
Erase *(ISP Shift Register)*	1010	Erases the entire EEPROM array. The outputs during this operation can be defined by user by using the JTAG SAMPLE/PRELOAD command.
Program *(ISP Shift Register)*	1011	Programs the data in the ISP Shift Register into the addressed EEPROM row. The outputs during this operation can be defined by user by using the JTAG SAMPLE/PRELOAD command.
Verify *(ISP Shift Register)*	1100	Transfers the data from the addressed row to the ISP Shift Register. The data can then be shifted out and compared with the JEDEC file. The outputs during this operation can be defined by user by using the JTAG SAMPLE/PRELOAD command.

JTAG and ISP Interfacing

A number of industry-established methods exist for JTAG/ISP interfacing with CPLD's and other integrated circuits. The Philips PZ5128 supports the following methods:

- PC Parallel Port
- Workstation or PC Serial Port
- Embedded Processor
- Automated Test Equipment
- Third party Programmers
- High-End JTAG and ISP Tools

A Boundary-Scan Description Language (BSDL) description of the PZ5128 is also available from Philips for use in test program development. For more details on JTAG and ISP for the PZ5128, refer to the related application note: *JTAG and ISP in Philips CPLDs.*

Table 7. Programming Specifications

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
DC Parameters				
V_{CCP}	V_{CC} supply program/verify	4.5	5.5	V
I_{CCP}	I_{CC} limit program/verify		200	mA
V_{IH}	Input voltage (High)	2.0		V
V_{IL}	Input voltage (Low)		0.8	V
V_{SOL}	Output voltage (Low)		0.5	V
V_{SOH}	Output voltage (High)	2.4		V
TDO_I_{OL}	Output current (Low)	12		mA
TDO_I_{OH}	Output current (High)	–12		mA
AC Parameters				
f_{MAX}	CLK maximum frequency	10		MHz
PWE	Pulse width erase	100		ms
PWP	Pulse width program	10		ms
PWV	Pulse width verify	10		µs
INIT	Initialization time	100		µs
TMS_SU	TMS setup time before TCK ↑	10		ns
TDI_SU	TDI setup time before TCK ↑	10		ns
TMS_H	TMS hold time after TCK ↑	20		ns
TDI_H	TDI hold time after TCK ↑	20		ns
TDO_CO	TDO valid after TCK ↓		30	ns

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Supply voltage[2]	–0.5	7.0	V
V_I	Input voltage	–1.2	V_{DD}+0.5	V
V_{OUT}	Output voltage	–0.5	V_{DD}+0.5	V
I_{IN}	Input current	–30	30	mA
I_{OUT}	Output current	–100	100	mA
T_J	Maximum junction temperature	–40	150	°C
T_{str}	Storage temperature	–65	150	°C

NOTES:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification is not implied.
2. The chip supply voltage must rise monotonically.

OPERATING RANGE

PRODUCT GRADE	TEMPERATURE	VOLTAGE
Commercial	0 to +70°C	5.0 ±5% V
Industrial	–40 to +85°C	5.0 ±10% V

DC ELECTRICAL CHARACTERISTICS FOR COMMERCIAL GRADE DEVICES

Commercial: 0°C ≤ T_{amb} ≤ +70°C; 4.75V ≤ V_{DD} ≤ 5.25V

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
V_{IL}	Input voltage low	V_{DD} = 4.75V		0.8	V
V_{IH}	Input voltage high	V_{DD} = 5.25V	2.0		V
V_I	Input clamp voltage	V_{DD} = 4.75V, I_{IN} = −18mA		−1.2	V
V_{OL}	Output voltage low	V_{DD} = 4.75V, I_{OL} = 12mA		0.5	V
V_{OH}	Output voltage high	V_{DD} = 4.75V, I_{OH} = −12mA	2.4		V
I_I	Input leakage current	V_{IN} = 0 to V_{DD}	−10	10	µA
I_{OZ}	3-Stated output leakage current	V_{IN} = 0 to V_{DD}	−10	10	µA
I_{DDQ}	Standby current	V_{DD} = 5.25V, T_{amb} = 0°C		100	µA
I_{DDD}[2]	Dynamic current	V_{DD} = 5.25V, T_{amb} = 0°C @ 1MHz		5	mA
		V_{DD} = 5.25V, T_{amb} = 0°C @ 50MHz		75	mA
I_{OS}	Short circuit output current[3]	1 pin at a time for no longer than 1 second	−50	−200	mA
C_{IN}	Input pin capacitance[3]	T_{amb} = 25°C, f = 1MHz		8	pF
C_{CLK}	Clock input capacitance[3]	T_{amb} = 25°C, f = 1MHz	5	12	pF
$C_{I/O}$	I/O pin capacitance[3]	T_{amb} = 25°C, f = 1MHz		10	pF

NOTES:
1. See Table 2 on page 113 for typical values.
2. This parameter measured with a 16-bit, loadable up/down counter loaded into every logic block, with all outputs disabled and unloaded. Inputs are tied to V_{DD} or ground. This parameter guaranteed by design and characterization, not testing.
3. *Typical values, not tested.*

AC ELECTRICAL CHARACTERISTICS[1] FOR COMMERCIAL GRADE DEVICES

Commercial: 0°C ≤ T_{amb} ≤ +70°C; 4.75V ≤ V_{DD} ≤ 5.25V

SYMBOL	PARAMETER	7		10		12		UNIT
		MIN/	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PD_PAL}	Propagation delay time, input (or feedback node) to output through PAL	2	7.5	2	10	2	12	ns
t_{PD_PLA}	Propagation delay time, input (or feedback node) to output through PAL & PLA	3	9.5	3	12	3	14.5	ns
t_{CO}	Clock to out (global synchronous clock from pin)	2	6	2	7	2	8	ns
t_{SU_PAL}	Setup time (from input or feedback node) through PAL	4.5		7		8		ns
t_{SU_PLA}	Setup time (from input or feedback node) through PAL + PLA	6.5		9		10.5		ns
t_H	Hold time		0		0		0	ns
t_{CH}	Clock High time	3		4		4		ns
t_{CL}	Clock Low time	3		4		4		ns
t_R	Input Rise time		20		20		20	ns
t_F	Input Fall time		20		20		20	ns
f_{MAX1}	Maximum FF toggle rate[2] $1/(t_{CH} + t_{CL})$	167		125		125		MHz
f_{MAX2}	Maximum internal frequency[2] $1/(t_{SUPAL} + t_{CF})$	111		80		69		MHz
f_{MAX3}	Maximum external frequency[2] $1/(t_{SUPAL} + t_{CO})$	95		71		63		MHz
t_{BUF}	Output buffer delay time		1.5		1.5		1.5	ns
t_{PDF_PAL}	Input (or feedback node) to internal feedback node delay time through PAL	2	6	2	8.5	2	10.5	ns
t_{PDF_PLA}	Input (or feedback node) to internal feedback node delay time through PAL+PLA	3	8	3	10.5	3	13	ns
t_{CF}	Clock to internal feedback node delay time		4.5		5.5		6.5	ns
t_{INIT}	Delay from valid V_{DD} to valid reset		50		50		50	µs
t_{ER}	Input to output disable[2, 3]		9		12		15	ns
t_{EA}	Input to output valid[2]		9		12		15	ns
t_{RP}	Input to register preset[2]		11		12.5		15	ns
t_{RR}	Input to register reset[2]		11		12.5		15	ns

NOTES:
1. Specifications measured with one output switching. See Figure 6 and Table 8 for derating.
2. This parameter guaranteed by design and characterization, not by test.
3. *Output C_L = 5pF.*

DC ELECTRICAL CHARACTERISTICS FOR INDUSTRIAL GRADE DEVICES

Industrial: $-40°C \le T_{amb} \le +85°C$; $4.5V \le V_{DD} \le 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
V_{IL}	Input voltage low	V_{DD} = 4.5V		0.8	V
V_{IH}	Input voltage high	V_{DD} = 5.5V	2.0		V
V_I	Input clamp voltage	V_{DD} = 4.5V, I_{IN} = −18mA		−1.2	V
V_{OL}	Output voltage low	V_{DD} = 4.5V, I_{OL} = 12mA		0.5	V
V_{OH}	Output voltage high	V_{DD} = 4.5V, I_{OH} = −12mA	2.4		V
I_I	Input leakage current	V_{IN} = 0 to V_{DD}	−10	10	µA
I_{OZ}	3-Stated output leakage current	V_{IN} = 0 to V_{DD}	−10	10	µA
I_{DDQ}[1]	Standby current	V_{DD} = 5.5V, T_{amb} = −40°C		125	µA
I_{DDD}[1, 2]	Dynamic current	V_{DD} = 5.5V, T_{amb} = −40°C @ 1MHz		6	mA
		V_{DD} = 5.5V, T_{amb} = −40°C @ 50MHz		90	mA
I_{OS}	Short circuit output current[3]	1 pin at a time for no longer than 1 second	−50	−230	mA
C_{IN}	Input pin capacitance[3]	T_{amb} = 25°C, f = 1MHz		8	pF
C_{CLK}	Clock input capacitance[3]	T_{amb} = 25°C, f = 1MHz	5	12	pF
$C_{I/O}$	I/O pin capacitance[3]	T_{amb} = 25°C, f = 1MHz		10	pF

NOTES:
1. See Table 2 on page 113 for typical values.
2. This parameter measured with a 16–bit, loadable up/down counter loaded into every logic block, with all outputs disabled and unloaded. Inputs are tied to V_{DD} or ground. This parameter guaranteed by design and characterization, not testing.
3. Typical values, not tested.

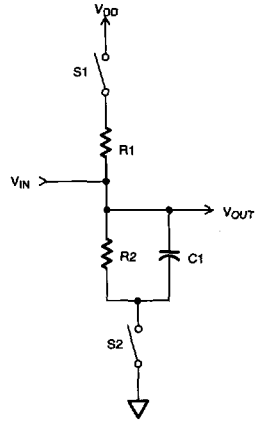
AC ELECTRICAL CHARACTERISTICS FOR INDUSTRIAL GRADE DEVICES

Industrial: $-40°C \le T_{amb} \le +85°C$; $4.5V \le V_{DD} \le 5.5V$

SYMBOL	PARAMETER	10		15		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{PD_PAL}	Propagation delay time, input (or feedback node) to output through PAL	2	10	2	15	ns
t_{PD_PLA}	Propagation delay time, input (or feedback node) to output through PAL & PLA	3	12	3	17.5	ns
t_{CO}	Clock to out (global synchronous clock from pin)	2	7	2	8	ns
t_{SU_PAL}	Setup time (from input or feedback node) through PAL	8		8		ns
t_{SU_PLA}	Setup time (from input or feedback node) through PAL + PLA	10		10.5		ns
t_H	Hold time		0		0	ns
t_{CH}	Clock High time	5		5		ns
t_{CL}	Clock Low time	5		5		ns
t_R	Input Rise time		20		20	ns
t_F	Input Fall time		20		20	ns
f_{MAX1}	Maximum FF toggle rate[2] $1/(t_{CH} + t_{CL})$	100		100		MHz
f_{MAX2}	Maximum internal frequency[2] $1/(t_{SUPAL} + t_{CF})$	71		69		MHz
f_{MAX3}	Maximum external frequency[2] $1/(t_{SUPAL} + t_{CO})$	66		63		MHz
t_{BUF}	Output buffer delay time		1.5		1.5	ns
t_{PDF_PAL}	Input (or feedback node) to internal feedback node delay time through PAL	2	8.5	2	13.5	ns
t_{PDF_PLA}	Input (or feedback node) to internal feedback node delay time through PAL+PLA	3	10.5	3	16	ns
t_{CF}	Clock to internal feedback node delay time		6		6.5	ns
t_{INIT}	Delay from valid V_{DD} to valid reset		50		50	µs
t_{ER}	Input to output disable[2, 3]		15		15	ns
t_{EA}	Input to output valid[2]		15		15	ns
t_{RP}	Input to register preset[2]		15		17	ns
t_{RR}	Input to register reset[2]		15		17	ns

NOTES:
1. Specifications measured with one output switching. See Figure 6 and Table 8 for derating.
2. This parameter guaranteed by design and characterization, not by test.
3. Output C_L = 5pF.

SWITCHING CHARACTERISTICS



COMPONENT	VALUES
R1	470Ω
R2	250Ω
C1	35pF

MEASUREMENT	S1	S2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_P	Closed	Closed

NOTE: For t_{PHZ} and t_{PLZ} C = 5pF

SP00458A

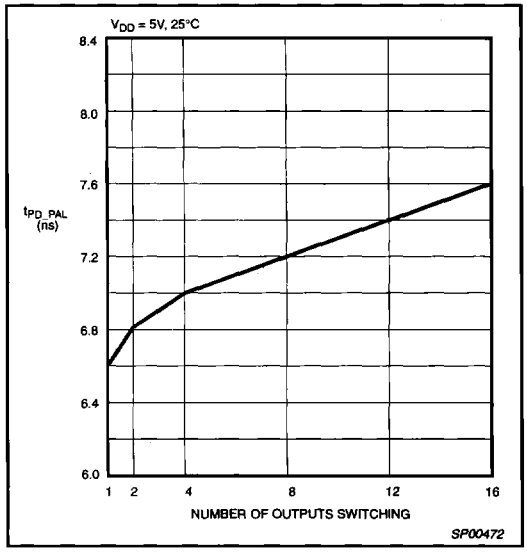


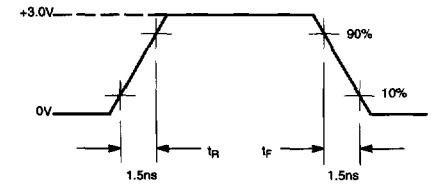
Figure 6. t_{PD_PAL} vs. Outputs Switching

Table 8. t_{PD_PAL} vs. Number of Outputs Switching

V_{DD} = 5.00V

NUMBER OF OUTPUTS	1	2	4	8	12	16
Typical (ns)	6.6	6.8	7.0	7.2	7.4	7.6

VOLTAGE WAVEFORM



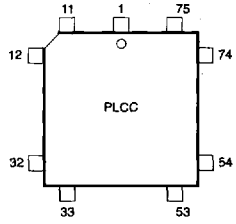
SP00368

MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

PIN DESCRIPTIONS

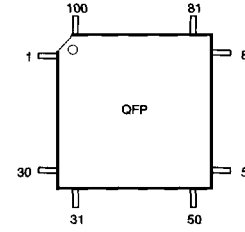
84-Pin Plastic Leaded Chip Carrier



Pin	Function	Pin	Function	Pin	Function
1	IN1	29	I/O-C5	57	I/O-F7
2	IN3	30	I/O-C4	58	I/O-F10
3	V_{DD}	31	I/O-C2	59	GND
4	I/O-A15/CLK3	32	GND	60	I/O-F12
5	I/O-A13	33	I/O-D15	61	I/O-F13
6	I/O-A12	34	I/O-D12	62	I/O-F15 (TCK)
7	GND	35	I/O-D10	63	I/O-G0
8	I/O-A10	36	I/O-D8	64	I/O-G2
9	I/O-A7	37	I/O-D7	65	I/O-G4
10	I/O-A5	38	V_{DD}	66	V_{DD}
11	I/O-A4	39	I/O-D4	67	I/O-G7
12	I/O-A2	40	I/O-D2	68	I/O-G8
13	V_{DD}	41	I/O-D0/CLK2	69	I/O-G10
14	I/O-B15 (TDI)	42	GND	70	I/O-G12
15	I/O-B12	43	V_{DD}	71	I/O-G15 (TDO)
16	I/O-B10	44	I/O-E0/CLK1	72	GND
17	I/O-B8	45	I/O-E2	73	I/O-H2
18	I/O-B7	46	I/O-E4	74	I/O-H4
19	GND	47	GND	75	I/O-H5
20	I/O-B4	48	I/O-E7	76	I/O-H7
21	I/O-B2	49	I/O-E8	77	I/O-H10
22	I/O-B0	50	I/O-E10	78	V_{DD}
23	I/O-C15 (TMS)	51	I/O-E12	79	I/O-H12
24	I/O-C13	52	I/O-E15	80	I/O-H13
25	I/O-C12	53	V_{DD}	81	I/O-H15
26	V_{DD}	54	I/O-F2	82	GND
27	I/O-C10	55	I/O-F4	83	IN0/CLK0
28	I/O-C7	56	I/O-F5	84	IN2-gtsn

SP00467

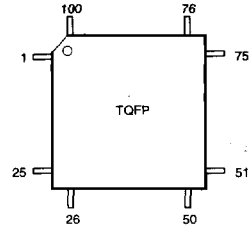
100-Pin Plastic Quad Flat Package



Pin	Function	Pin	Function	Pin	Function
1	I/O-A5	35	I/O-D5	69	I/O-G5
2	I/O-A4	36	V_{DD}	70	I/O-G7
3	I/O-A2	37	I/O-D4	71	I/O-G8
4	I/O-A0	38	I/O-D2	72	I/O-G10
5	V_{DD}	39	I/O-D0/CLK2	73	I/O-G12
6	I/O-B15 (TDI)	40	GND	74	I/O-G13
7	I/O-B13	41	V_{DD}	75	I/O-G15 (TDO)
8	I/O-B12	42	I/O-E0/CLK1	76	GND
9	I/O-B10	43	I/O-E2	77	I/O-H0
10	I/O-B8	44	I/O-E4	78	I/O-H2
11	I/O-B7	45	GND	79	I/O-H4
12	I/O-B5	46	I/O-E5	80	I/O-H5
13	GND	47	I/O-E7	81	I/O-H7
14	I/O-B4	48	I/O-E8	82	I/O-H8
15	I/O-B2	49	I/O-E10	83	I/O-H10
16	I/O-B0	50	I/O-E12	84	V_{DD}
17	I/O-C15 (TMS)	51	I/O-E13	85	I/O-H12
18	I/O-C13	52	I/O-E15	86	I/O-H13
19	I/O-C12	53	V_{DD}	87	I/O-H15
20	V_{DD}	54	I/O-F0	88	GND
21	I/O-C10	55	I/O-F2	89	IN0/CLK0
22	I/O-C8	56	I/O-F4	90	IN2-gtsn
23	I/O-C7	57	I/O-F5	91	IN1
24	I/O-C5	58	I/O-F7	92	IN3
25	I/O-C4	59	I/O-F8	93	V_{DD}
26	I/O-C2	60	I/O-F10	94	I/O-A15/CLK3
27	I/O-C0	61	GND	95	I/O-A13
28	GND	62	I/O-F12	96	I/O-A12
29	I/O-D15	63	I/O-F13	97	GND
30	I/O-D13	64	I/O-F15 (TCK)	98	I/O-A10
31	I/O-D12	65	I/O-G0	99	I/O-A8
32	I/O-D10	66	I/O-G2	100	I/O-A7
33	I/O-D8	67	I/O-G4		
34	I/O-D7	68	V_{DD}		

SP00468

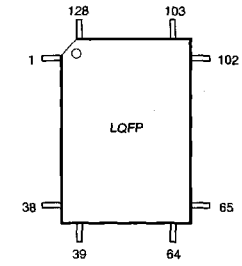
100-Pin Thin Quad Flat Package



Pin	Function	Pin	Function	Pin	Function
1	I/O-A2	35	I/O-D4	69	I/O-G8
2	I/O-A0	36	I/O-D2	70	I/O-G10
3	V_{DD}	37	I/O-D0/CLK2	71	I/O-G12
4	I/O-B15 (TDI)	38	GND	72	I/O-G13
5	I/O-B13	39	V_{DD}	73	I/O-G15 (TDO)
6	I/O-B12	40	I/O-E0/CLK1	74	GND
7	I/O-B10	41	I/O-E2	75	I/O-H0
8	I/O-B8	42	I/O-E4	76	I/O-H2
9	I/O-B7	43	GND	77	I/O-H4
10	I/O-B5	44	I/O-E5	78	I/O-H5
11	GND	45	I/O-E7	79	I/O-H7
12	I/O-B4	46	I/O-E8	80	I/O-H8
13	I/O-B2	47	I/O-E10	81	I/O-H10
14	I/O-B0	48	I/O-E12	82	V_{DD}
15	I/O-C15 (TMS)	49	I/O-E13	83	I/O-H12
16	I/O-C13	50	I/O-E15	84	I/O-H13
17	I/O-C12	51	V_{DD}	85	I/O-H15
18	V_{DD}	52	I/O-F0	86	GND
19	I/O-C10	53	I/O-F2	87	IN0/CLK0
20	I/O-C8	54	I/O-F4	88	IN2-gtsn
21	I/O-C7	55	I/O-F5	89	IN1
22	I/O-C5	56	I/O-F7	90	IN3
23	I/O-C4	57	I/O-F8	91	V_{DD}
24	I/O-C2	58	I/O-F10	92	I/O-A15/CLK3
25	I/O-C0	59	GND	93	I/O-A13
26	GND	60	I/O-F12	94	I/O-A12
27	I/O-D15	61	I/O-F13	95	GND
28	I/O-D13	62	I/O-F15 (TCK)	96	I/O-A10
29	I/O-D12	63	I/O-G0	97	I/O-A8
30	I/O-D10	64	I/O-G2	98	I/O-A7
31	I/O-D8	65	I/O-G4	99	I/O-A5
32	I/O-D7	66	V_{DD}	100	I/O-A4
33	I/O-D5	67	I/O-G5		
34	V_{DD}	68	I/O-G7		

SP00485

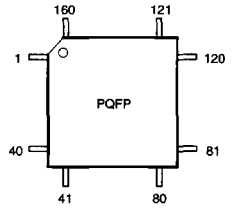
128-Pin Low Profile Quad Flat Package



Pin	Function	Pin	Function	Pin	Function
1	I/O-A3	44	I/O-D7	87	V_{DD}
2	I/O-A2	45	I/O-D5	88	I/O-G5
3	I/O-A0	46	V_{DD}	89	I/O-G7
4	NC	47	I/O-D4	90	I/O-G8
5	NC	48	I/O-D3	91	I/O-G10
6	NC	49	I/O-D2	92	I/O-G11
7	V_{DD}	50	I/O-D0/CLK2	93	I/O-G12
8	I/O-B15 (TDI)	51	GND	94	I/O-G13
9	I/O-B13	52	V_{DD}	95	I/O-G15 (TDO)
10	I/O-B12	53	I/O-E0/CLK1	96	GND
11	I/O-B11	54	I/O-E2	97	NC
12	I/O-B10	55	I/O-E3	98	NC
13	I/O-B8	56	I/O-E4	99	NC
14	I/O-B7	57	GND	100	I/O-H0
15	I/O-B5	58	I/O-E5	101	I/O-H2
16	GND	59	I/O-E7	102	I/O-H3
17	I/O-B4	60	I/O-E8	103	I/O-H4
18	I/O-B3	61	I/O-E10	104	I/O-H5
19	I/O-B2	62	I/O-E11	105	I/O-H7
20	I/O-B0	63	I/O-E12	106	I/O-H8
21	I/O-C15 (TMS)	64	I/O-E13	107	I/O-H10
22	I/O-C13	65	I/O-E15	108	V_{DD}
23	I/O-C12	66	V_{DD}	109	I/O-H11
24	I/O-C11	67	I/O-F0	110	I/O-H12
25	V_{DD}	68	NC	111	I/O-H13
26	I/O-C10	69	NC	112	I/O-H15
27	I/O-C8	70	NC	113	GND
28	I/O-C7	71	I/O-F2	114	IN0/CLK0
29	I/O-C5	72	I/O-F3	115	IN2-gtsn
30	I/O-C4	73	I/O-F4	116	IN1
31	I/O-C3	74	I/O-F5	117	IN3
32	I/O-C2	75	I/O-F7	118	V_{DD}
33	NC	76	I/O-F8	119	I/O-A15/CLK3
34	NC	77	I/O-F10	120	I/O-A13
35	NC	78	GND	121	I/O-A12
36	I/O-C0	79	I/O-F11	122	I/O-A11
37	GND	80	I/O-F12	123	GND
38	I/O-D15	81	I/O-F13	124	I/O-A10
39	I/O-D13	82	I/O-F15(TCK)	125	I/O-A8
40	I/O-D12	83	I/O-G0	126	I/O-A7
41	I/O-D11	84	I/O-G2	127	I/O-A5
42	I/O-D10	85	I/O-G3	128	I/O-A4
43	I/O-D8	86	I/O-G4		

SP00469A

160-Pin Plastic Quad Flat Package



Pin	Function	Pin	Function	Pin	Function
1	NC	54	I/O-D5	107	I/O-G8
2	NC	55	V_{DD}	108	I/O-G10
3	NC	56	I/O-D4	109	I/O-G11
4	NC	57	I/O-D3	110	I/O-G12
5	NC	58	I/O-D2	111	I/O-G13
6	NC	59	I/O-D0/CLK2	112	I/O-G15 (TDO)
7	NC	60	GND	113	GND
8	V_{DD}	61	V_{DD}	114	NC
9	I/O-B15 (TDI)	62	I/O-E0/CLK1	115	NC
10	I/O-B13	63	I/O-E2	116	NC
11	I/O-B12	64	I/O-E3	117	NC
12	I/O-B11	65	I/O-E4	118	NC
13	I/O-B10	66	GND	119	NC
14	I/O-B8	67	I/O-E5	120	NC
15	I/O-B7	68	I/O-E7	121	I/O-H0
16	I/O-B5	69	I/O-E8	122	I/O-H2
17	GND	70	I/O-E10	123	I/O-H3
18	I/O-B4	71	I/O-E11	124	NC
19	I/O-B3	72	I/O-E12	125	NC
20	I/O-B2	73	I/O-E13	126	NC
21	I/O-B0	74	NC	127	NC
22	I/O-C15 (TMS)	75	NC	128	I/O-H4
23	I/O-C13	76	NC	129	I/O-H5
24	I/O-C12	77	NC	130	I/O-H7
25	I/O-C11	78	I/O-E15	131	I/O-H8
26	V_{DD}	79	V_{DD}	132	I/O-H10
27	I/O-C10	80	I/O-F0	133	V_{DD}
28	I/O-C8	81	NC	134	I/O-H11
29	I/O-C7	82	NC	135	I/O-H12
30	I/O-C5	83	NC	136	I/O-H13
31	I/O-C4	84	NC	137	I/O-H15
32	I/O-C3	85	NC	138	GND
33	I/O-C2	86	NC	139	IN0/CLK0
34	NC	87	NC	140	IN2-gtsn
35	NC	88	I/O-F2	141	IN1
36	NC	89	I/O-F3	142	IN3
37	NC	90	I/O-F4	143	V_{DD}
38	NC	91	I/O-F5	144	I/O-A15/CLK3
39	NC	92	I/O-F7	145	I/O-A13
40	NC	93	I/O-F8	146	I/O-A12
41	I/O-C0	94	I/O-F10	147	I/O-A11
42	GND	95	GND	148	GND
43	I/O-D15	96	I/O-F11	149	I/O-A10
44	NC	97	I/O-F12	150	I/O-A8
45	NC	98	I/O-F13	151	I/O-A7
46	NC	99	I/O-F15 (TCK)	152	I/O-A5
47	NC	100	I/O-G0	153	I/O-A4
48	I/O-D13	101	I/O-G2	154	NC
49	I/O-D12	102	I/O-G3	155	NC
50	I/O-D11	103	I/O-G4	156	NC
51	I/O-D10	104	V_{DD}	157	NC
52	I/O-D8	105	I/O-G5	158	I/O-A3
53	I/O-D7	106	I/O-G7	159	I/O-A2
				160	I/O-A0

SP00470A

Package Thermal Characteristics

Philips Semiconductors uses the Temperature Sensitive Parameter (TSP) method to test thermal resistance. This method meets Mil-Std-883C Method 1012.1 and is described in Philips *1995 IC Package Databook*. Thermal resistance varies slightly as a function of input power. As input power increases, thermal resistance changes approximately 5% for a 100% change in power.

Figure 7 is a derating curve for the change in Θ_{JA} with airflow based on wind tunnel measurements. It should be noted that the wind flow dynamics are more complex and turbulent in actual applications than in a wind tunnel. Also, the test boards used in the wind tunnel contribute significantly to forced convection heat transfer, and may not be similar to the actual circuit board, especially in size.

Package	Θ_{JA}
84-pin PLCC	32.8 °C/W
100-pin PQFP	41.2 °C/W
100-pin TQFP	47.4 °C/W
128-pin LQFP	45.0 °C/W
160-pin PQFP	31.4 °C/W

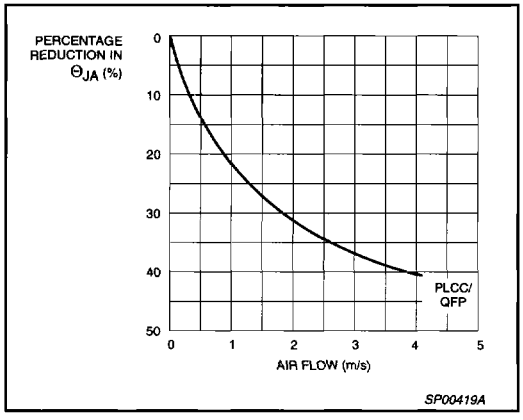


Figure 7. Average Effect of Airflow on Θ_{JA}