SIEMENS

Memories for Graphics Systems

Multibank DRAM
MDRAM

HYB39M93200
HYB39M83200

Version 0.9

Preliminary Information 02.97

HYB39M93200 HYB39M83200 **Revision History:**		**Current Version: 02.97**
Previous Version:		
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)

Edition 02.97

This edition was realized using the software system FrameMaker®.

Published by Siemens AG,
Bereich Halbleiter, Marketing-
Kommunikation, Balanstraße 73,
81541 München

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1 Features

- Ultra-High Performance
  666 MByte/sec single device transfer rate
  24 ns RAS access
  13.1 ns CAS access
  6 ns burst cycle
- Multibank Architecture
  RAS and precharge may overlap CAS READ or WRITE to different banks effectively hiding precharge time.
- Organisations and Speed Sorts

Table 1

Type	Organization	MBytes	No. Banks	Speed Grades [MHz]	Package
HYB39M93200Q	288k × 32	1.125	36	166/150/133/120	P-QFP-128-1
HYB39M93200L	288k × 32	1.125	36	166/150/133/120	P-LCC-68-9
HYB39M83200Q	256k × 32	1.0	32	166/150/133/120	P-QFP-128-1
HYB39M83200L	256k × 32	1.0	32	166/150/133/120	P-LCC-68-9

- Variable Length Burst
  Supports 4 to 128 byte interruptable bursts.
- Byte-level Write Control
- Low Internal and Interface Power
- Small Footprint
  available in two different packages:
  14 mm × 20 mm P-QFP-128-1 for SMD soldering at optimum electrical performance.
  P-LCC-68-9 for economic socketing or SMD soldering at standard electrical performance.
- Compact, Easily Implemented Interface
  26 signal; bus interface employs standard CMOS/Terminated CMOS signaling.
- 3.3 V Power Supply

2 Block Diagram

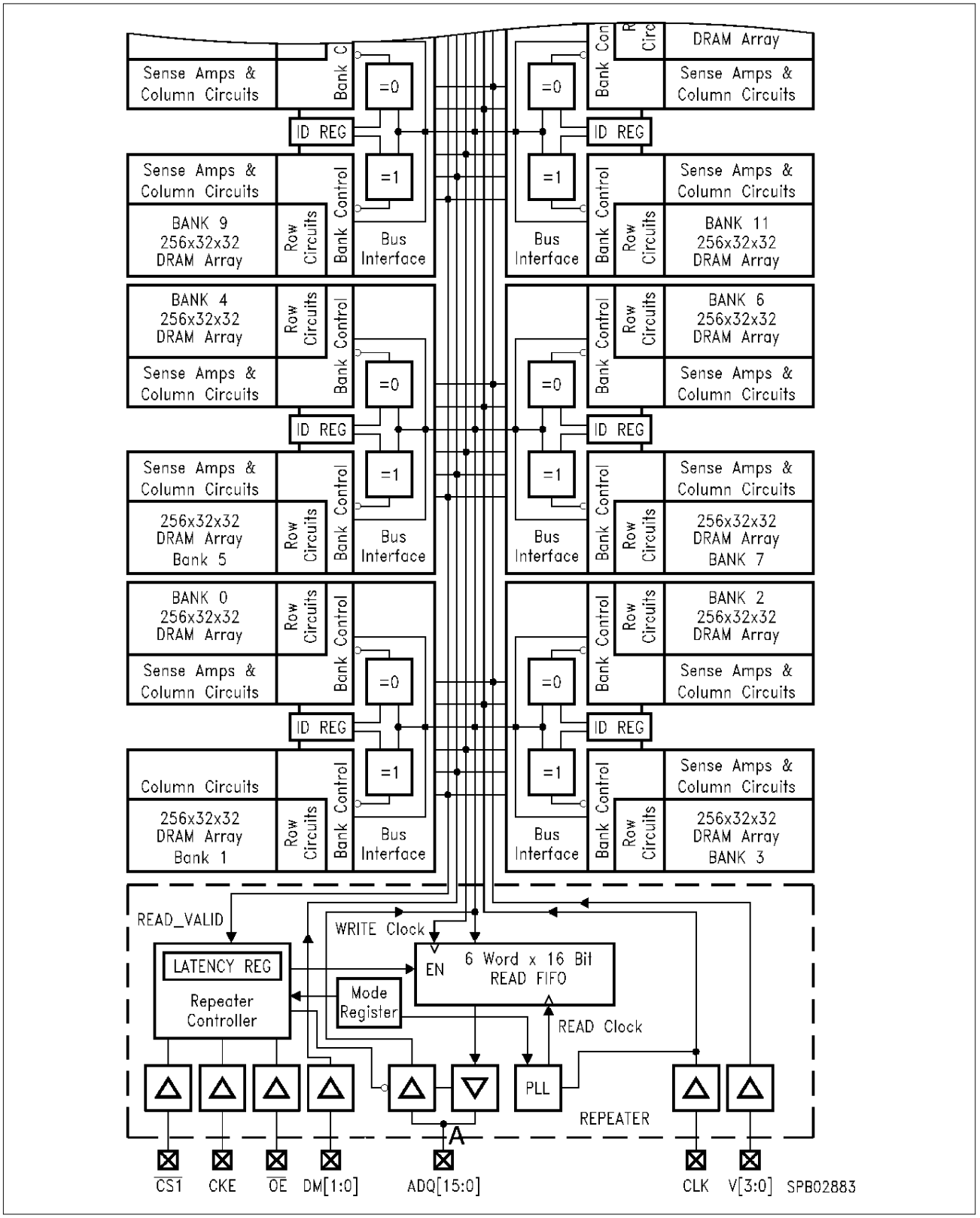


Figure 1
MDRAM Block Diagram

3 Overview

3.1 Description

The SIEMENS Multibank DRAM (MDRAM) is an extended performance synchronous DRAM optimized for ultra-high performance applications where high bandwidth, extremely short access latency and low cost are required. MDRAMs feature fully synchronous I/O at frequencies up to 166 MHz providing 666 MBytes per second of peak bandwidth.

An MDRAM can be viewed as an array of many independent 256 Kbit (32 KByte) DRAMs, – each with a 32-bit interface – connected to a common bus internal to the MDRAM. The external interface is simply a buffered version of the internal bus, seen through a bus repeater. The small bank size and the simplicity of the repeater yield extremely short CAS access latency. The independence of bank facilitates overlapping or hiding the RAS access and precharge penalty so that average access times will approach the CAS access time.

3.2 MDRAM Organization

The block diagram (see **figure 1**) illustrates the internal structure of the MDRAM. The memory is composed of independent and fully functional 32 KByte DRAM banks. The control of each bank is local to each bank rather than centralized.

Address recognition is normally accomplished within the bank so that no external address decoding is required. Programmable bank ID registers are used to map banks to a logical address space. Multiple devices may be cascaded to form larger memory arrays by programming each bank ID register with a unique address. Up to 8 MBytes of memory may be accumulated on a single bus without external address decoding.

Banks are organized in 256 rows by 32 words. Each word is 32 bits wide. All banks are tied to a common internal bus that terminates on a single bus repeater unit at one end of the chip.

Both the internal and external bus consist primarily of a multiplexed address and data bus, a command bus and clock. During data transfer, both clock edges are used for synchronous transfer of 32 bits per clockcycle on only 16 pins. Data mask (DM) facilitate byte level write masking.

The bus repeater buffers the internal bus from the external bus. The repeater also contains a phase lock loop (PLL) and a six half word deep FIFO with programmable latency that guarantees accurate I/O timing.

3.3 MDRAM Operation

A RAS operation (typically called ACTIVATE in SDRAM devices) copies a single row of a single bank into its sense amps. Successive RAS/ACTIVATE commands can activate a single bank or multiple banks.

CAS operations (READ or WRITE) proceed with any activated bank with short latency and high bandwidth. READ or WRITE operations continue in a burst, at ascending column addresses, until terminated by a STOP command. Reading or writing past the end of a row (column address 0x1F) will wrap to the beginning of the row.

A bank is deactivated by the PRECHARGE command. PRECHARGE writes the content of the sense amps back into the memory array – deactivating the bank. Unlike DRAMs, PRECHARGE is optional when changing banks. READ/WRITE operations may proceed at any activated bank. PRECHARGE may be delayed until another row in an already active bank is to be accessed.

Memory is addressed to the 32-bit word. DM bits facilitate byte-level write masking. Banks have a preprogrammed address at power-on which may be overwritten by a command. Each bank can be treated as a single, independent memory module. Large memory arrays are implemented by programming each bank of a multichip memory to a unique address.

4 Signal Description

For both packages, P-LCC and P-QFP, the signals are arranged in the same order. Therefore, the MDRAM can interface with both of them without any modification.
There are 26 active signal pins and 12 power/ground pins. All high speed signals are arranged on one side of the package, in order to equalize and reduce PC board trace length, routing capacitance and inductance.

Table 2
Pin Grouping

Datapath			
ADQ[15:0]	In/Out	16	Multiplexed Address/Data
DM[1:0]	In	2	Write Data Mask
Command V[3:0]			
CRE or V3	In	1	Control Register Enable
$\overline{\text{RAS}}$ or V2	In	1	Row Address Strobe
$\overline{\text{CAS}}$ or V1	In	1	Column Address Strobe
WE or V0	In	1	Write Enable
Control			
CLK	In	1	Clock Input
CKE	In	1	Clock Enable
$\overline{\text{OE}}$	In	1	Output Enable
$\overline{\text{CS1}}$	In	1	Chip Select 1
$\overline{\text{CS2}}$	In	1	Chip Select 2; reserved for future use.

Total signals: 26 (excluding $\overline{\text{CS2}}$)

4.1 ADQ[15:0], Address/Data Bus

These bidirectional pins carry multiplexed address and data. During the command phase of an operation, the ADQ bus carries address information to the MDRAM. The address is sampled on the rising edge of clock.

During the data phase of READ or WRITE the ADQ bus carries 32-bit data words. Data is transferred synchronously, 16 bits at a time, on the rising and falling edge of the clock.

4.2 DM[1:0], Data Mask

These signals are used for data masking during the write operation. They are sampled on the rising and falling edge of the clock. A high on a DM bit prevents the corresponding byte from being written. If data masking is required, the affected DM signals must be high

during the rising and falling edges of the WRITE command phase. If write masking is not required, the DM signals should be tied permanently low.

The following table shows which bit of DM[1:0] refers to which byte of a word.

... of a word	are controlled by ...	on the ... clock edge
bits 7..0	DM[0]	rising
bits 15..8	DM[1]	rising
bits 23..16	DM[0]	falling
bits 31..24	DM[1]	falling

4.3 CRE, $\overline{RAS}$, $\overline{CAS}$, WE, Command Bus V[3:0]

These signals collectively named as V[3:0] form the command bus. They are sampled on the rising edge of the clock. The name V[3:0] and the conventional names (CRE, $\overline{RAS}$, $\overline{CAS}$ and WE) are used interchangeably in this data sheet.

4.4 CLK, Memory Clock

All signals except $\overline{OE}$ and $\overline{CS}$ are synchronously sampled by this clock.

4.5 $\overline{OE}$, Output Enable

This asynchronous control signal can be used to turn around the data bus in systems which operate at relatively low frequencies but requiring short access latency. For most applications $\overline{OE}$ should be tied permanently low.

4.6 CKE, Clock Enable

This control signal enables the memory clock. CKE is sampled on the rising edge of CLK and is effective on the next rising edge. CKE can be used to freeze the data that is clocked out on the falling edge on the memory clock. For most applications CKE should be permanently tied high.

4.7 $\overline{CS1}$, Chip Select 1

This asynchronous control signal enables or disables the MDRAM. It is useful for memory initialization, power management, and for address decoding of arrays larger than 8 MBytes.

4.8 $\overline{CS2}$, Chip Select 2

This signal is reserved for future for larger memories with two dies in the same package.

4.9 VDD/GND (Power)

Memory core power supply.

4.10 IOVDD/IOGND (Power)

I/O driver power supply.

4.11 SH, (Passive), Short

These are no connection (NC) pins shorted together.

4.12 ICS, IC Substrate

These pins are connected to the chip substrate and should remain unconnected.

4.13 Pin Configuration
(top view)

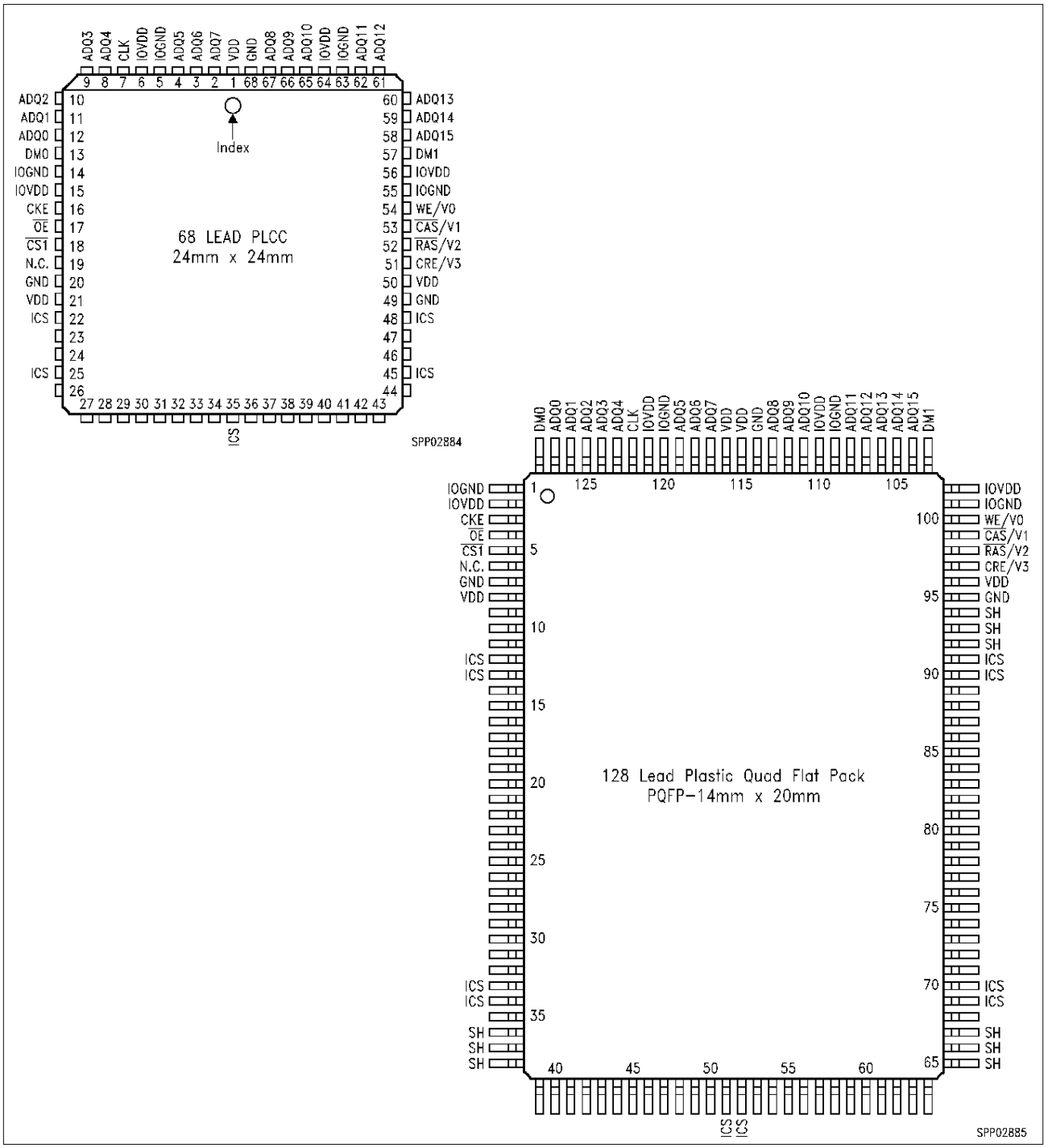


Figure 2

Note: Unlabeled pins are not connected.
Adjacent pins marked SH are shorted together but are not connected to the die.
Pins labeled ICS are connected to the chip substrate. Do not connect externally.
Pin 19 at P-LCC-68 and pin 6 at P-QFP-128 are not connected presently. These pins are reserved for future use as $\overline{CS2}$.

5 Pin Definitions and Functions

Table 3
Pin Definitions and Functions

Pin No. for P-LCC-68	Pin No. for P-QFP-128	Symbol	Input Output	Function
2-4, 8-12, 58-62, 65-67	104-108, 111-113, 117-119, 123-127	ADQ[15:0]	I/O	Multiplexed Address/Data Bus
13, 57	103, 128	DM[1:0]	I	Write Data Mask
51	97	CRE = V[3]	I	Control Register Enable
52	98	$\overline{RAS}$ = V[2]	I	Row Address Strobe
53	99	$\overline{CAS}$ = V[1]	I	Column Address Strobe
54	100	WE = V[0]	I	Write Enable
7	122	CLK	I	Clock Input
16	3	CKE	I	Clock Enable
17	4	$\overline{OE}$	I	Output Enable
18	5	$\overline{CS1}$	I	Chip Select 1
1, 21, 50	8, 96, 115-116	VDD	Power	Memory Core Power Voltage
20, 49, 68	7, 95, 114	GND	Power	Memory Core Ground
6, 15, 56, 64	2, 102, 110, 121	IOVDD	Power	I/O Power Voltage
5, 14, 55, 63	1, 101, 109, 120	IOGND	Power	I/O Ground
	36-38, 65-67, 92-94	SH		Shorted Together
22, 25, 35, 45, 48	12-13, 33-34, 51-52, 69-70, 90-91	ICS		Chip Substrate
19, 23-24, 26-34, 36-44, 46-47	6, 9-11, 14-32, 35, 39-50, 53-64, 68, 71-89	NC		No Connection (NC)

6 MDRAM Command Description

6.1 Command Description

The eight MDRAM commands plus POWERDOWN and MEMORY DISABLE are listed in **table 4** and **5**. The remaining commands are reserved and should never be used. All except four commands are single cycle long. A legal command must be present on the command bus on every clock cycle. A “clock cycle” is from clock rising edge to clock rising edge. All commands are sampled on the rising edge of the clock. All operations begin with a “command/address” phase that is one clock cycle in length.

Table 4
MDRAM Commands (sorted by command code)

Command Name	Command Code on V[3:0]	# of Cycles	Description
Do not use !	0x0		Reserved for future use.
Do not use !	0x1		Reserved for future use.
ACTIVATE	0x2	1	ACTIVATE is similar to RAS in standard DRAM. It loads the contents of the selected row to the sense amplifier latches of that bank. Subsequent READs or WRITEs to the activated bank operate on the sense amplifier latches. Before another row in the same memory bank can be selected, a PRECHARGE command must be used to store the data from the sense amplifiers back to the memory cells. The ACTIVATE command must not be used: • When T_{RP} timing is violated. • When the selected bank is already activated. • Within a READ, WRITE, or IDREGWR operation.
PRECHARGE	0x3	1	PRECHARGE copies the sense amp contents to the memory cells of the addressed bank and prepares the bank for the next ACTIVATE/ RAS operation. A bank may be precharged even if it is in the deactivated or precharged state. During READ operations, this command terminates the current operation and executes a precharge to the bank currently in a read state (STOP&PRE). WRITEs must be terminated with a STOP. If PRECHARGE is used to terminate a READ, then T_{RP} is measured from the falling edge of the PRECHARGE command cycle to the rising edge of the ACTIVATE command cycle. The precharge command can be used at any time except: • To terminate a WRITE • When it violates T_{RAS} (ACTIVATE to PRECHARGE delay).

Table 4
MDRAM Commands (sorted by command code) (cont'd)

Command Name	Command Code on V[3:0]	# of Cycles	Description
READ	0x4	mult.	READ is similar to CAS read in standard DRAM. READ transfers data from the sense amps addressed by the column address to the output. A READ command is followed by a specified nummer of one-half-clock-period latency phases and an even number of data phases. The number of latency phases is programmable and may be even or odd (see "Memory Initialization and Memory Refresh", 6.1.1). After the column access latency, each succeeding clock edge transfers data from ascending column addresses in a burst. A 16-bit value is read each data phase. The READ command must be maintained on the command bus for the duration of the operation. READ terminates with STOP or PRECHARGE. The MDRAM will terminate a READ and will not send data on the ADQ bus if a STOP command is issued immediately after the READ command phase. A burst READ must be terminated with a STOP before another READ command is issued for the same bank but different column. READs past the end of a row (column address 0x1F) will "wrap" to the beginning of the row. The READ command can be used: • Only on activated banks. • At any time except when t_{RCD} is violated.
WRITE	0x5	mult.	WRITE transfers data from the ADQ bus to the selected bank and column address. WRITE employs burst transfers. After the one cycle command/address phase, each succeeding clock edge writes to ascending column addresses. A WRITE command phase must always be followed by an even number of data phases of one half-clock period in length. A 16-bit value is written each data phase. The WRITE command must be maintained on the command bus for the duration of the command phase and data phases. WRITE terminates only with a STOP command. WRITE must be followed by at least two data phases (one 32-bit word) before it can be terminated with a STOP command. At clock frequencies above 120 MHz, a READ following a WRITE to the same bank or the bank that shares the same upper seven address bits must have two STOP commands between the last data phase of WRITE and the command phase of READ. WRITEs past the end of a row (column address 0x1F) will "wrap" to the beginning of the row. The latency setting does not effect WRITE. The WRITE command can be used: • At any time except when t_{RCD} is violated.
MEMRESET	0x6	3	Initializes the mode register and bank ID registers to power up defaults and deactivates (precharges) all banks. *Note:* MEMRESET *is not data-safe. Data may be lost if all banks are not already precharged.*
MODEREGWR	0x7	1	Mode Register Write initializes the mode register. (See "Mode Register" on page 16.)
Do not use !	0x8		Reserved for future use.

Table 4
MDRAM Commands (sorted by command code) (cont'd)

Command Name	Command Code on V[3:0]	# of Cycles	Description
Do not use !	0x9		Reserved for future use.
Do not use !	0xA		Reserved for future use.
Do not use !	0xB		Reserved for future use.
Do not use !	0xC		Reserved for future use.
IDREGWR	0xD	2	ID Register Write loads the bank ID register with a new value. This command is used to map memory banks to logical address space. (See "Bank ID Registers" on page 17.)
Do not use !	0xE		Reserved for future use.
STOP	0xF	1	STOP terminates the current READ or WRITE operation and sets the memory to the idle state without invoking PRECHARGE. Additional READ or WRITE commands to the same bank and row, or to other active banks, can proceed without new ACTIVE commands. Repeated STOP commands are equivalent to no-operation (NOP) commands and hold the memory in an idle state. The stop command can be used at any time except: • Immediately after the WRITE command (before any WRITE data phases).

Table 5
MDRAM Commands (Overview)

Operation	CRE V[3]	RAS V[2]	$\overline{CAS}$ V[1]	WE V[0]	X = DONT'CARE Physical Pins: ADQ [15:0] ADQ[15]----------ADQ[0]	DM[1:0]	CLK	CKE	$\overline{OE}$	$\overline{CS}$	Notes
Single Cycle Commands											
ACTIVATE(2_H)	L	L	H	L	Bank Address, Row Address	X	↑	H	X	L	
PRECHARGE(3_H)	L	L	H	H	Bank Address, X X X X X X X X	X	↑	H	X	L	
STOP&PRE(3_H)	L	L	H	H	X X X X X X X X, X X X X X X X X	X	↑	H	X	L	1)
MODEREGWR(7_H)	L	H	H	H	X X X X P Latency, L L L L L L L L	X	↑	H	X	L	
STOP(F_H)	H	H	H	H	X X X X X X X X, X X X X X X X X	X	↑	H	X	L	
WRITE Command Sequence											
WRITE(5_H)	L	H	L	H	Bank Address, X X X, Column Address	H	↑	H	X	L	2)
WRITE(5_H)	L	H	L	H	D15----------D0	HL	↑	H	X	L	3)
WRITE(5_H)	L	H	L	H	D31----------D16	HL	↓	H	X	L	3)
READ Command Sequence											
READ(4_H)	L	H	L	L	Bank Address, X X X, Column Address	X	↑	H	X	L	
READ(4_H)	L	H	L	L	Hi Impedance/Turn Around	X	↑↓	H	L	L	4),5)
READ(4_H)	L	H	L	L	D15----------D0	X	↑↓	H	L	L	5)
READ(4_H)	L	H	L	L	D31----------D16	X	↑↓	H	L	L	5)
ID Register Write Command Sequence											
IDREGWR(D_H)	H	H	L	H	Current Bank ID, 0 X X X X X X X X	X	↑	H	X	L	
STOP(F_H)	H	H	H	H	New Bank ID, 0 X X X X X X X X	X	↑	H	X	L	
STOP(F_H)	H	H	H	H	X X X X X X X X, X X X X X X X X	X	↓	H	X	L	
Memory Reset Command Sequence											
MEMRESET(6_H)	L	H	H	L	X X X X X X X X X X X X X X H H	X	↑	H	X	L	
STOP(F_H)	H	H	H	H	X X X X X X X X X X X X X X X X	X	↑	H	X	L	
STOP(F_H)	H	H	H	H	X X X X X X X X X X X X X X X X	X	↑	H	X	L	
Powerdown/Memory Disable											
xxxx (x_H)	X	X	X	X	X X X X X X X X X X X X X X X X	X	X	X	X	H	

1) PRECHARGE interrupting a READ is equivalent to STOP followed by PRECHARGE (STOP&PRE) and affects the bank being read. Any address forced on ADQ bus is ignored.

2) If data masking is required affected DM signals must be high during the rising and falling edges of the WRITE command phase. If write masking is not required the DM signals should be tied permanently low.

3) DM[1:0] bits refer to corresponding data bytes. For example, DM[1] high masks D[15:8] on rising clock edges and D[31:24] on falling clock edges.

4) The READ command phase is followed by a specified number of one-half-clock-period latency phases.

5) 'Latency Value' controls which half-word is latched on the rising edge of CLK. The first data half-word latches on rising edges when the 'Latency Value' is even.

6.1.1 Memory Initialization and Memory Refresh

On power up the memory must be initialized with a MEMRESET and MODEREGWR commands.

Memory Refresh is accomplished with an ACTIVATE and PRECHARGE (RAS and precharge) command to every row of every bank within every T_{REF} period.

6.1.2 Mode Register

The mode register definition is shown in **table 6**. On power up, the eight LSBs and PD bit are reset to zero. The 'Latency Value' after power up is undefined. The PD and 'Latency Value' fields must be initialized by MODEREGWR. PD = "0" is the normal, powered up state. PD = "1" places the memory in power down state by turning off the Phase Locked Loop.

Table 6
Mode Register Definition

M[15:12]	M[11]	M[10:8]	M[7:0]
Ignored	PD	Latency Value	Reserved Must be 0 (zero)

MDRAM delivers data on both rising and falling edges of the clock. The latency value can be used to relocate the first 16-bit word of a data burst on a rising or a falling edge of the clock as desired. **Figure 3 on page 22** shows an example at 120 MHz with latency value set to (010). Legal latency settings for each device speed grade versus frequency are given in **table 13 on page 21** 'Legal Latency Values'.

Table 7
Latency Value

M[10]	M[9]	M[8]	t_{CAC} in Clock Edges
0	0	0	3
0	0	1	4
0	1	0	5
0	1	1	6
1	0	0	7
1	0	1	8
1	1	0	9
1	1	1	10

6.1.3 Bank ID Registers

The contents of bank ID registers map each bank to logical address space. On power up, the bank ID registers are preset sequentially starting from bank zero. If multiple devices are tied on the same bus, the bank ID registers of all devices must be initialized in order to remap all memory banks to non-overlapping space.

The contents of the bank ID registers can be changed using the IDREGWR command. To prevent IDREGWR command from effecting all the devices on the bus, the chip select signal $\overline{CS1}$ can be used to enable only one chip at a time. The bank ID register contents are volatile. The default value will be restored each time power is applied or when the MEMRESET command is executed.
Note that the bank ID register contains 7 bits that correspond to the 7 MSB of two banks[1)], meaning that two banks (= a module) are programmed at a time and share the same 7 MSB of their ID. The banks of a module are distingiushed by the LSB.

[1] Two banks are called a *module*.

7 Electrical Characteristics

Table 8
Capacitance
T_A = 25 °C, f = 1 MHz, typical values in pF

Pin Group	Typical Values		Unit
	P-QFP-128	P-LCC-68	
ADQ I/O pin capacitance	2.6	5	pF
DM input pin capacitance	1.6	3	pF
Clock input capacitance	1.8	3.8	pF
Input capacitance (all other)	1.8	3.8	pF

Table 9
Absolute Maximum Ratings

Parameter	Limit Values			Unit
	min.	typ.	max.	
Voltage on V_{DD} pin relative to V_{SS}	– 1.0	–	4.6	V
Voltage on I/O pin relative to V_{SSQ} (during normal operation)	– 1.0	–	4.6	V
Voltage on input pin relative to V_{SS} (no V_{DD} applied)	– 1.0	–	4.6	V
Short-circuit output current, I_{OS}	–	20	–	mA
Operating temperature, T_{OPR}	0	–	+ 70	°C
Storage temperature, T_{STG}	– 55	–	+ 125	°C

Note: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under 'Recommended Operating Conditions', 'DC Current Requirements' and 'AC Characteristics'.

Table 10
Recommended Operating Condition

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Supply Voltage	V_{DD}	3.14	3.3	3.47	V	1)
Input Voltage High	V_{IH}	$0.5 \times (V_{DD} + 1)$	–	V_{DD}	V	
Input Voltage Low	V_{IL}	0	–	$0.5 \times (V_{DD} - 1)$	V	
Output Voltage High	V_{OH}	–	$0.8 \times V_{DDQ}$	–	V	1)
Output Voltage Low	V_{OL}	–	$0.2 \times V_{DDQ}$	–	V	1)
Ambient Temperature	T_A	0	–	70	°C	

1) Output load is 110 Ω to V_{DDQ}/2 (or 220 Ω to V_{DDQ} plus 220 Ω to V_{SSQ}).

Table 11
DC Current Requirements

Parameter	Symbol	Typ.		Unit	Test Condition: (V_{DD} = 3.6 V, T_A = 0 °C, f = 120 MHz, I_Q = 0 mA)
		PD = 0	PD = 1		
Operating Current	I_{DD}	80	–	mA	35% read, 35% write, 30% idle. Read, write and idle conditions are defined next in this table. (No I/O loading)
Idle Current	I_{DDIDLE}	45	40	mA	$\overline{CS1}$ = 0, CKE = 1, V[3:0] = 1111 (STOP). I_{DDIDLE}(f) = TBD.
Refresh only Current	$I_{DDREFRESH}$	15	5	mA	ACTIVATE and PRECHARGE every (2 microseconds, on all remaining cycles $\overline{CS1}$ = 1.
Chip Suspend Current	$I_{DDSUSPEND}$	15	5	mA	CKE = 1, $\overline{CS1}$ = 1, V[3:0] = XXXX on all cycles.
Clock Suspend Current	I_{DDLP}	10	1	mA	CKE = 0, $\overline{CS1}$ = 0, V[3:0] = XXXX on all cycles.

Table 12
AC Characteristics (at recommended operating condition)

Parameter	Symbol	Speed Grade								Unit	Notes
		– 166		– 150		– 133		– 120			
		Limit Values									
		min.	max.	min.	max.	min.	max.	min.	max.		
READ to data valid	t_{CAC}		13.1		14.5		16.1		17.9	ns	5), 6)
ACTIVATE to READ/WRITE delay	t_{RCD}	16.2		17.0		18.0		19.2		ns	1), 6)
ACTIVATE to PRECHARGE delay	t_{RAS}	24.0		26.0		27.0		28.0		ns	1), 6)
PRECHARGE to ACTIVATE delay	t_{RP}	24		26.0		27.0		28.0		ns	1, 6)
Burst mode READ/WRITE cycle	t_{PC}	6.0		6.7		7.5		8.3		ns	
CLK frequency	f_{CLK}		166.7		150		133.3		120	MHz	
CLK duty cycle		– 10	+10	– 10	+ 10	– 10	+ 10	– 10	+ 10	%	2)
CLK high level width	t_{CLKH}	2.7	3.3	3.0	3.7	3.4	4.1	3.8	4.6	ns	2)
CLK low level width	t_{CLKL}	2.7	3.3	3.0	3.7	3.4	4.1	3.8	4.6	ns	2)
Command setup time	t_{CSU}	1.5		1.7		1.9		2.1		ns	3)
Command hold time	t_{CH}	1.1		1.3		1.4		1.6		ns	3)
CKE setup time	t_{ESU}	1.9		2.1		2.3		2.6		ns	
CKE hold time	t_{EH}	1.1		1.3		1.4		1.6		ns	
Address setup time	t_{ASU}	1.5		1.7		1.9		2.1		ns	
Address hold time	t_{AH}	1.1		1.3		1.4		1.6		ns	
Data setup time	t_{DSU}	1.1		1.3		1.4		1.6		ns	
Data hold time	t_{DH}	1.1		1.3		1.4		1.6		ns	
Data Mask setup time	t_{DMSU}	0.8		0.8		0.9		1.0		ns	
Data Mask hold time	t_{DMH}	1.5		1.7		1.9		2.1		ns	
Refresh period	t_{REF}		16		16		16		16	ms	
Clock to data output	t_{CO}	0.8	1.9	0.8	2.1	1.0	2.3	1.0	2.6	ns	7)
Read command to ADQ Lo-Z	t_{CLZ}	3.0		3.0		3.0		3.0		ns	
Burst STOP/PRECHARGE to ADQ Hi-Z	t_{OFF}		4.1		4.6		5.2		5.7	ns	
OE high to ADQ Hi-Z	t_{OEHZ}	3.0		3.0		3.0		3.0		ns	
OE low to ADQ Lo-Z	t_{OELZ}	3.0		3.0		3.0		3.0		ns	
Chip select high to clock	t_{CSD}	2.3		2.5		2.8		3.1		ns	
Chip select low to clock	t_{CSA}	3.0		3.5		3.5		3.8		ns	
Chip select high to ADQ Hi-Z	t_{CSO}		4.0		4.0		4.0		4.0	ns	
Minimum PLL lock frequency	f_{LOCK}	50		50		50		50		MHz	
Power-up/power-on time	t_{PU}		1.0		1.0		1.0		1.0	ms	4)
ACTIVATE to READ/WRITE delay	t_{RCD}	3		3		3		3		cycles	1, 2)
ACTIVATE to PRECHARGE delay	t_{RAS}	4		4		4		4		cycles	1, 2)
PRECHARGE to ACTIVATE delay	t_{RP}	4		4		4		4		cycles	1, 2)

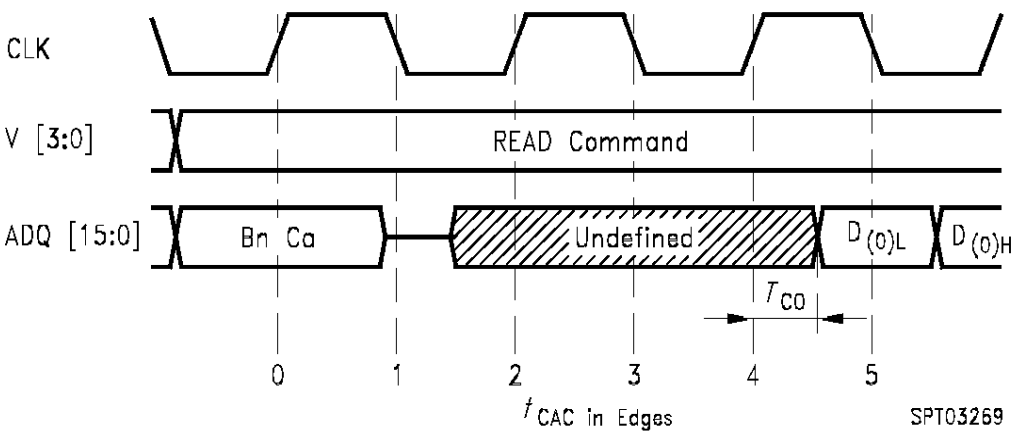
1) To same bank.
2) f_{clk} = max.
3) "Command bus" is CRE, $\overline{RAS}$, $\overline{CAS}$ and WE.
4) Power on or PD = "1" -> "0", delay to full function.
5) To any activated bank.
6) Characterized but not tested.
7) Tested with half of ADQ pins switching to V_{DDQ} and the other half switching to V_{SSQ}. Load is 25 pF to V_{SSQ} and 110 Ω to 0.5 × V_{DDQ}.

Table 13
Legal Latency Values

Latency Value				Speed Grade								Units
				-166		-150		-133		-120		
				Frequency Range								
↓	↑	↓	↑	min.	max.	min.	max.	min.	max.	min.	max.	
000	001			50	100	50	100	50	100	50	100	MHz
	001	010		100	135	90	133	90	133	70	120	MHz
		010		100	166	100	150					MHz
		010	011	145	166							MHz

Note: The latency value must be selected based on frequency of operation and whether the first read data is to be latched on the falling (↓) or rising (↑) edge of the clock. For example: The MDRAM operating at 125 MHz with the first read data latched on the falling edge of the clock must have the latency set to (010).

8 Timing Specification



Bn = bank number Ca = column address

Figure 3
READ with Latency Set to 010

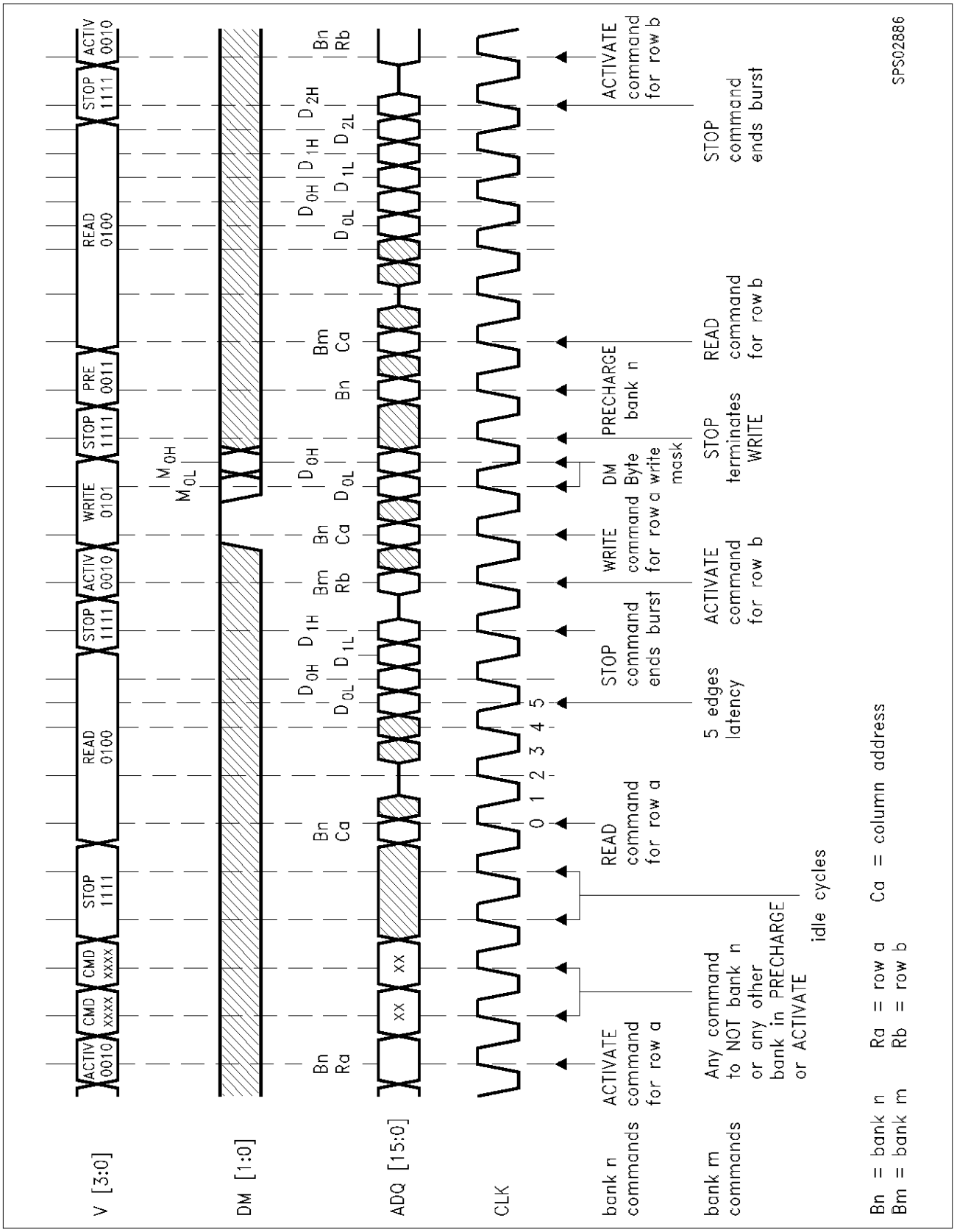


Figure 4
Command Sequence Example

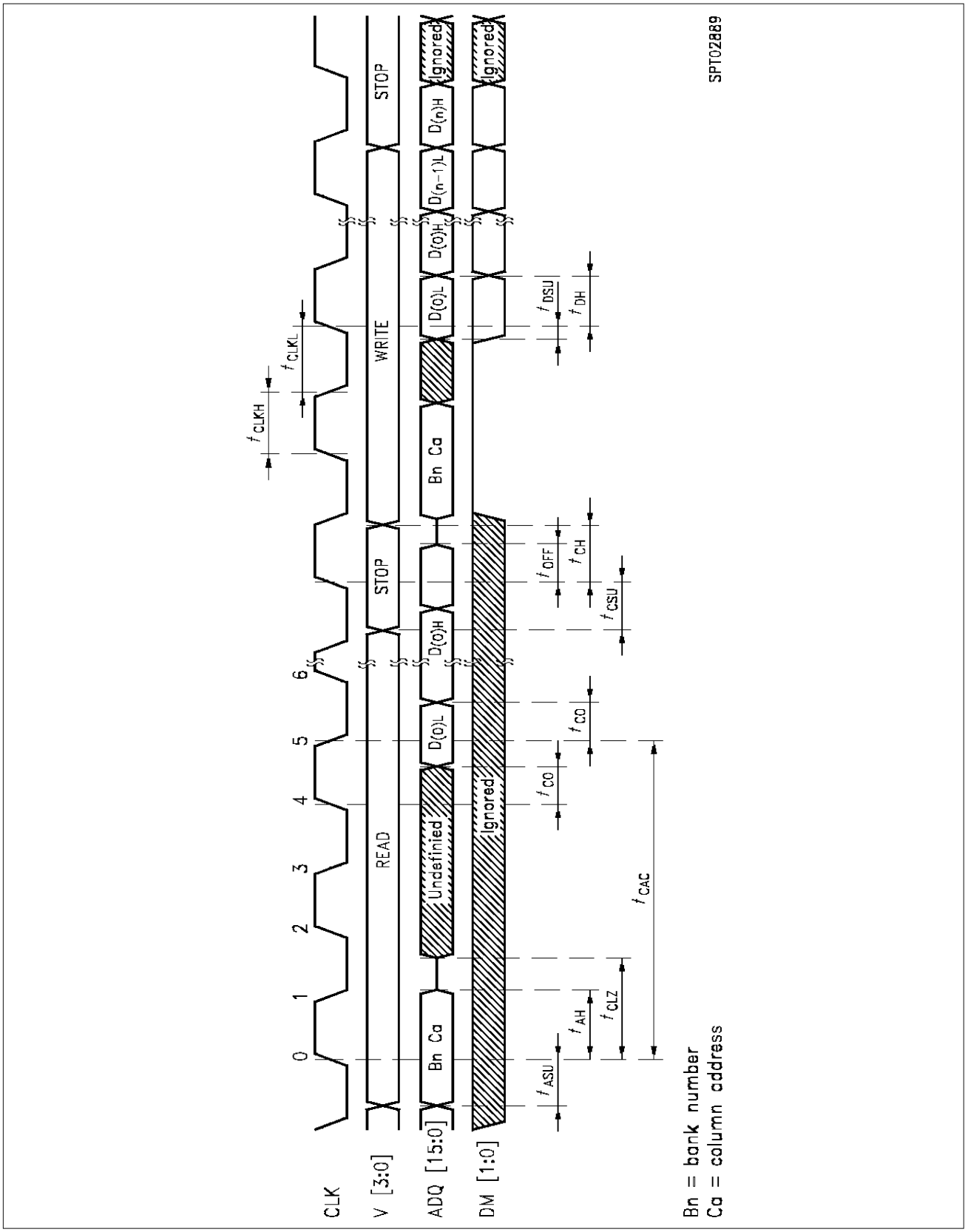


Figure 5
READ and WRITE Timing

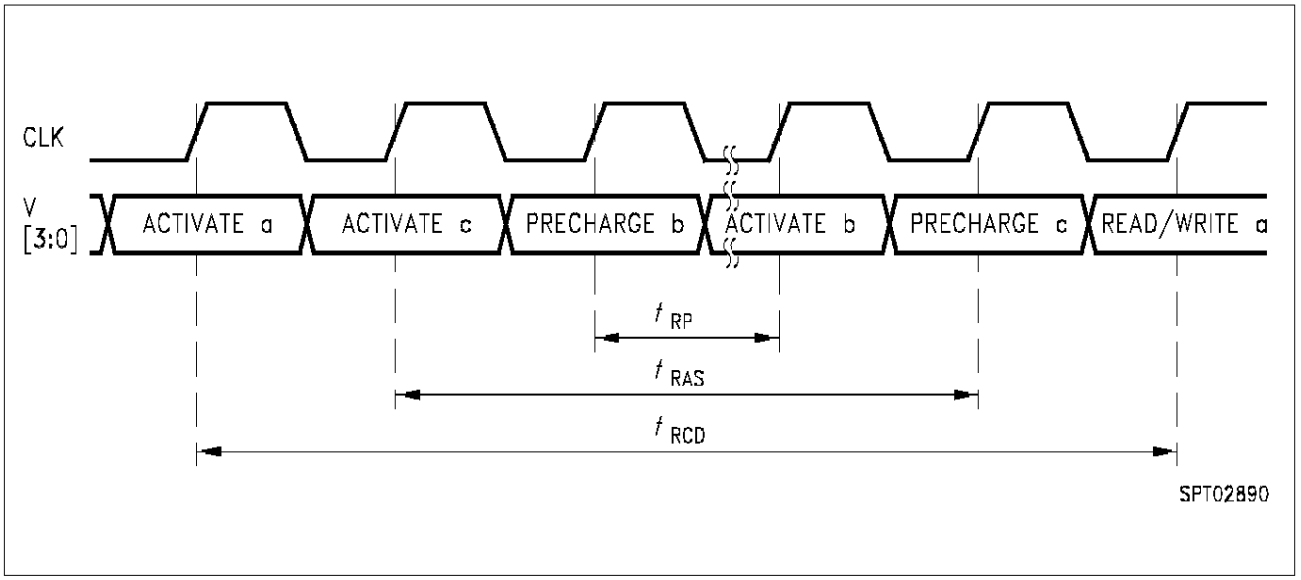


Figure 6
ACTIVATE and PRECHARGE Timing

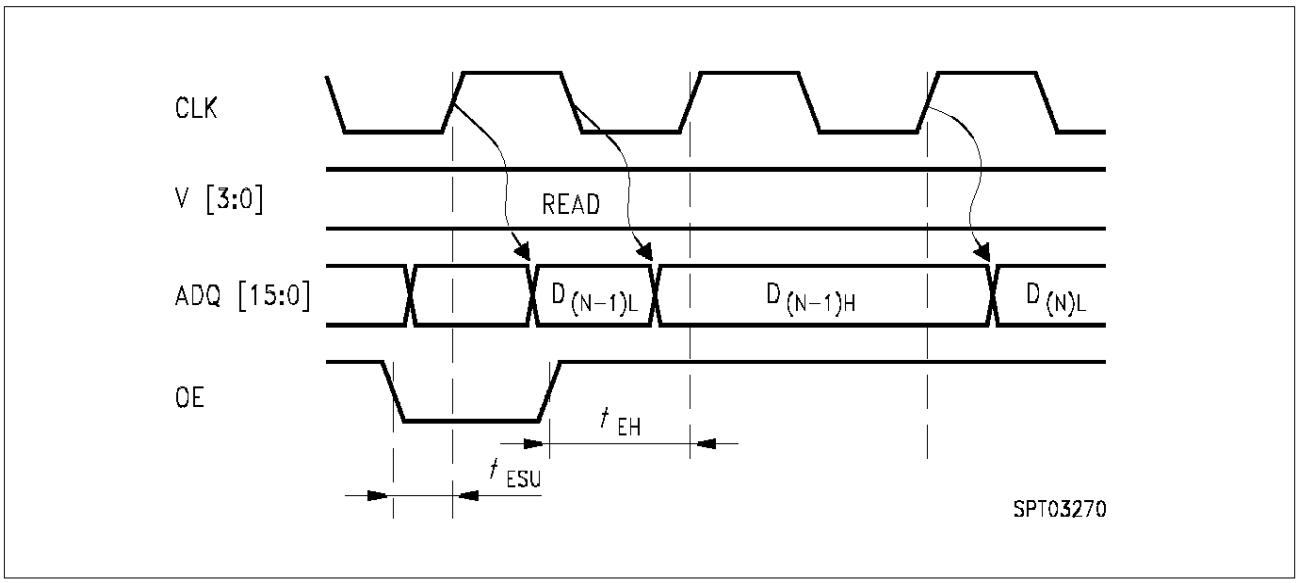


Figure 7
Clock Enable Timing

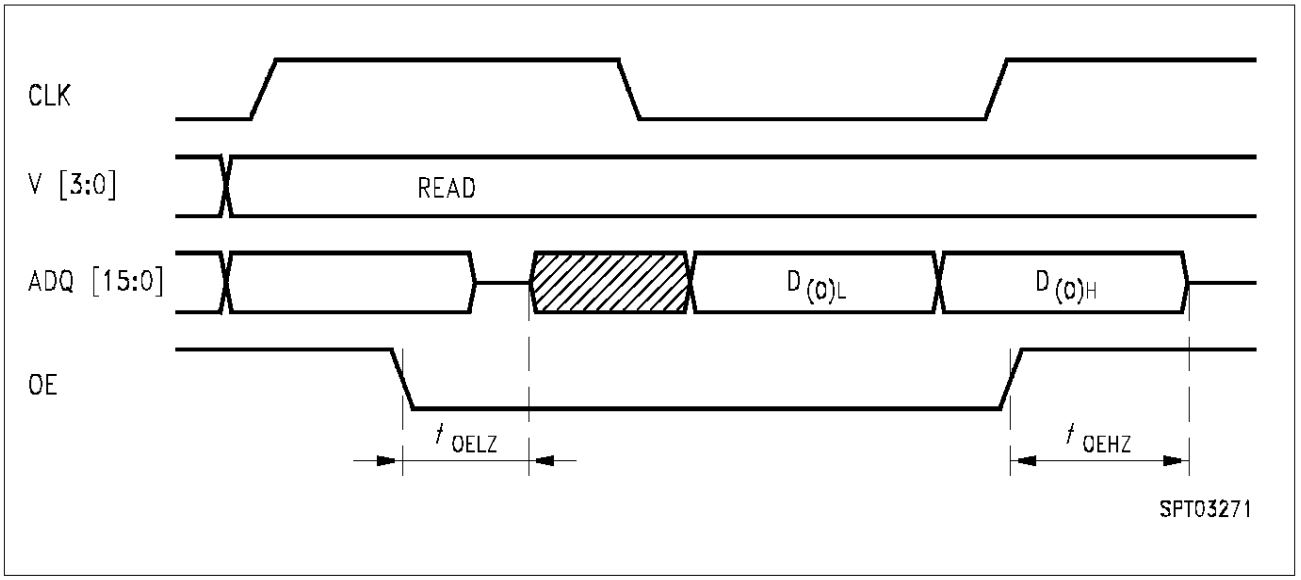


Figure 8
Output Enable Timing

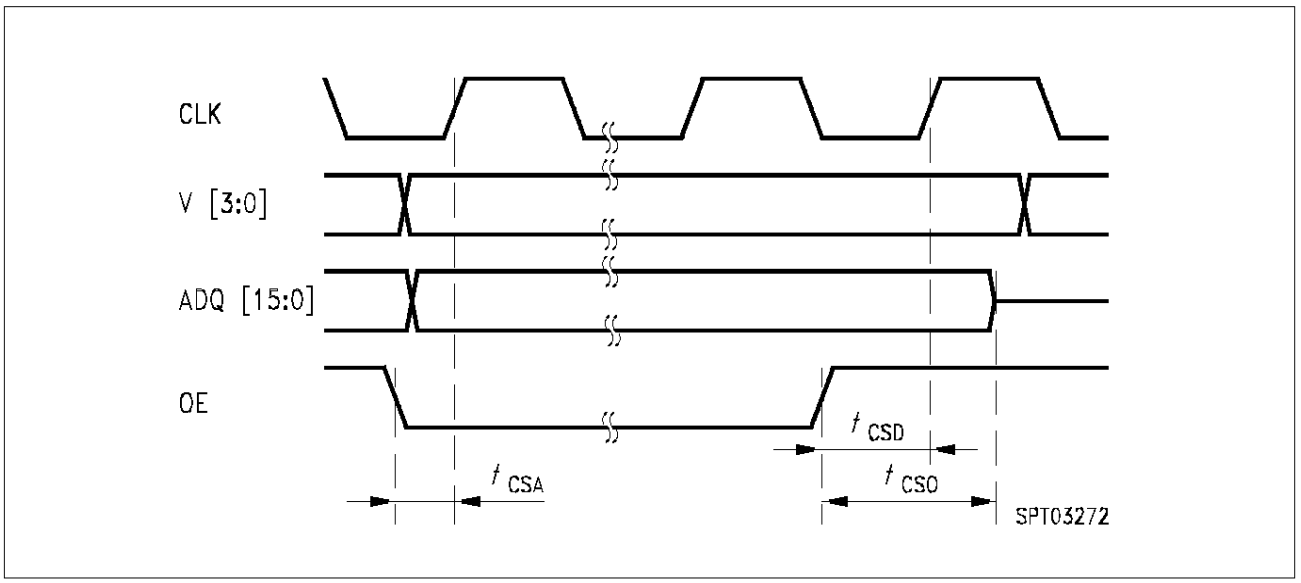
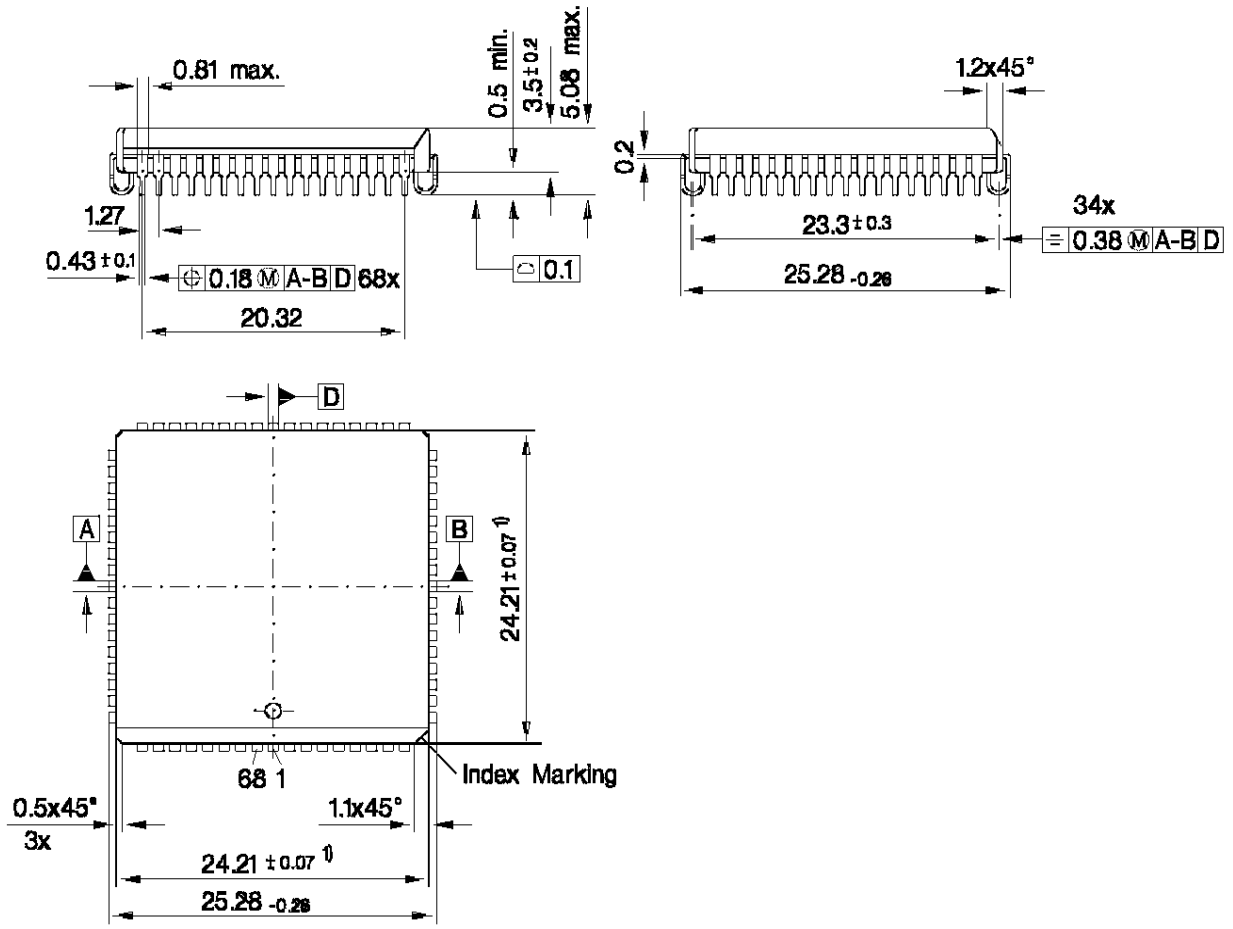


Figure 9
Chip Select Timing

9 Mechanical Specification

Package Outlines

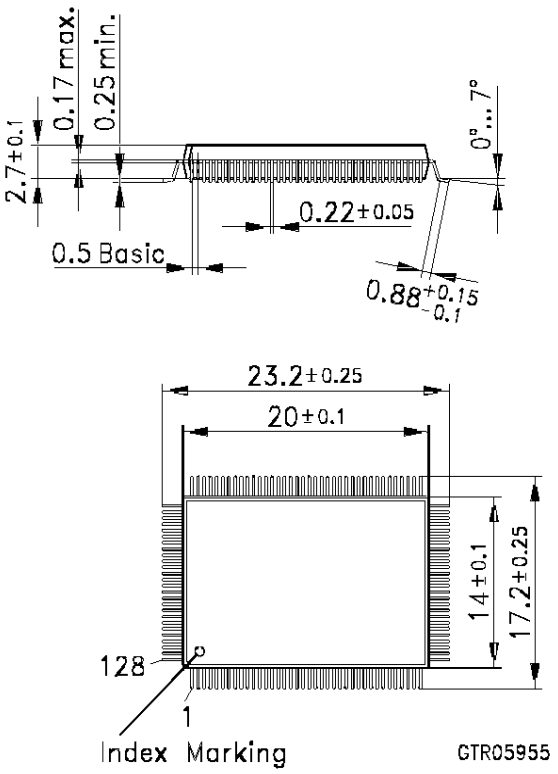
Plastic Package, P-LCC-68-9 (SMD)
(Plastic Leaded Chip Carrier)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our
Data Book “Package Information”
SMD = Surface Mounted Device

Dimensions in mm

Plastic Package, P-QFP-128-1 (SMD)
(Ceramic/Plastic Quad Flat Package)



GTR05955

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information"
SMD = Surface Mounted Device

Dimensions in mm

10 Ordering Options

Memory Components (Multibank DRAMS)

HYB 39 M xxxxx Q -166