DENSE-PAC MICROSYSTEMS

4 Megabit (5V) CMOS Flash EEPROM

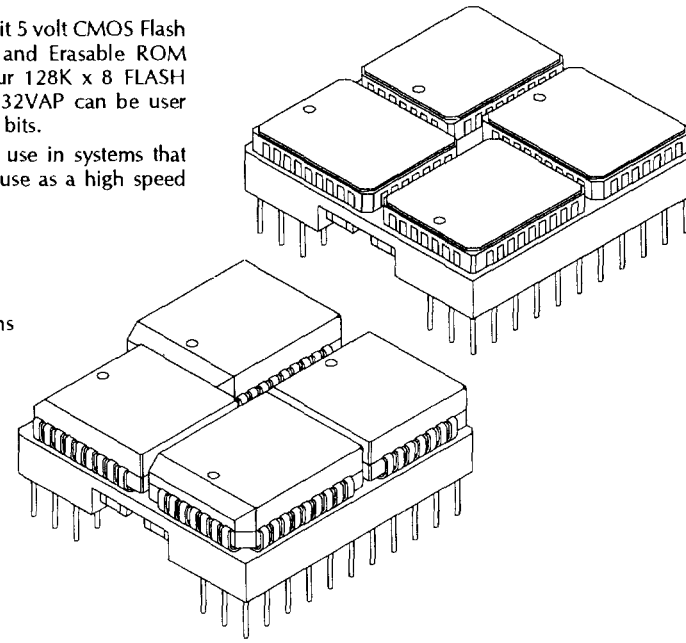
DP5Z12832VA/DP5Z12832VAP

PRELIMINARY

DESCRIPTION:

The DP5Z12832VA/DP5Z12832VAP is a 4 megabit 5 volt CMOS Flash EEPROM (Electrically In-System Programmable and Erasable ROM Memory) module. The module is built with four 128K x 8 FLASH memory devices. The DP5Z12832VA/DP5Z12832VAP can be user configurable as 512K x 8, 256K x 16 or 128K x 32 bits.

The DP5Z12832VA/DP5Z12832VAP is ideal for use in systems that require In System periodic code updates, or for use as a high speed nonvolatile storage medium.

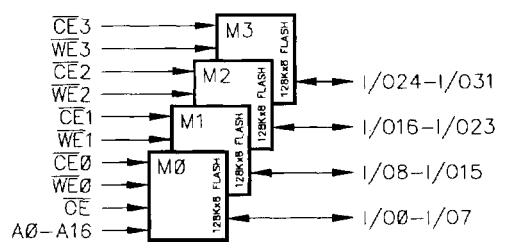


FEATURES:

- User Defined Configuration:
  512K x 8, 256K x 16 or 128K x 32
- Fast Read Access Times: 45*, 55, 70, 90, 120ns
- Low Power:
  120mA Maximum Active
  200µA Maximum Standby (CMOS)
- 10,000 Erase/Program Cycles Minimum
- 5 Volt Only In-System Programming
- TTL-Compatible Inputs and Outputs
- Military Version Available with all Devices used to construct the Module Compliant to MIL-STD-883; Class B
- 66-Pin Ceramic PGA

* Commercial Only.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES	
A0 - A16	Address Inputs
I/O0 - I/O31	Data Input/Output
$\overline{CE0}$ - $\overline{CE3}$	Chip Enables
$\overline{WE0}$ - $\overline{WE3}$	Write Enables
$\overline{OE}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground
N.C.	No Connect

PIN-OUT DIAGRAM

1	I/O8	12	$\overline{WE1}$	23	I/O15	34	I/O24	45	VDD	56	I/O31
2	I/O9	13	$\overline{CE1}$	24	I/O14	35	I/O25	46	$\overline{CE3}$	57	I/O30
3	I/O10	14	VSS	25	I/O13	36	I/O26	47	$\overline{WE3}$	58	I/O29
4	A13	15	I/O11	26	I/O12	37	A6	48	I/O27	59	I/O28
5	A14	16	A10	27	$\overline{OE}$	38	A7	49	A3	60	A0
6	A15	17	A11	28	N.C.	39	N.C.	50	A4	61	A1
7	A16	18	A12	29	$\overline{WE0}$	40	A8	51	A5	62	A2
8	N.C.	19	VDD	30	I/O7	41	A9	52	$\overline{WE2}$	63	I/O23
9	I/O0	20	$\overline{CE0}$	31	I/O6	42	I/O16	53	$\overline{CE2}$	64	I/O22
10	I/O1	21	N.C.	32	I/O5	43	I/O17	54	VSS	65	I/O21
11	I/O2	22	I/O3	33	I/O4	44	I/O18	55	I/O19	66	I/O20

(TOP VIEW)

DEVICE OPERATION:

The FLASH devices are electrically erasable and programmable memories that function similarly to an EPROM device, but can be erased without being removed from the system and exposed to ultraviolet light. Each 128K x 8 device or sector on any device can be programmed and erased individually elimination the need to re-program the entire module when partial code changes are required.

READ/RESET:

The Module is accessed like a Static Ram. When $\overline{CE}$ and $\overline{OE}$ are Low and $\overline{WE}$ is High, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

The read or reset operation is initiated by writing read/reset command into the command register (see the Command Definition Table). The device remains in the read mode until another valid command is written into the command register. The device will automatically be set to the read/reset mode upon power-up.

BYTE PROGRAMMING:

The module is programmed one byte at a time. The program operation is four cycles long. There are two "unlock" write cycles. The "unlock" cycles are followed by the program set-up command and data write cycles.

Addresses are latched on the falling edge of $\overline{WE}$, while the data is latched on the rising edge of $\overline{WE}$. The program cycle will begin on the rising edge of $\overline{WE}$. The program algorithm is internally generated providing all the necessary timing, pulse widths, and margins to reliably complete the program cycle. The program operation is completed when the I/O7 bit (or I/O15, I/O23, I/O31) on the device(s) programmed is equivalent to the data written to that bit. The device programmed returns to the read/reset mode upon completion of the program operation.

Programming is allowed in any sequence and across sector boundaries.

CHIP ERASE:

The chip erase operation is six cycles long. There are two "unlock" write cycles followed by writing the set-up chip erase command followed by two more "unlock" write cycles.

It is not required to program all of the memory locations to "0" prior to the chip erase operation. At the start of the chip erase operation the device will internally program and verify the entire memory to an all "0" data pattern prior to electrical erase.

The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence. When the chip erase operation is completed the data on the I/O7 bit (or I/O15, I/O23, I/O31) of the device being erased will equal "1" at which time the device will return to the read/reset mode.

SECTOR ERASE:

The sector erase operation is six cycles long. There are two "unlock" write cycles followed by writing the set-up sector erase command followed by two more "unlock" write cycles. The sector address (any address within the sector) is latched on the falling edge of $\overline{WE}$, while the command (data) is latched on the rising edge of $\overline{WE}$. A time-out of 100µs from the rising edge of the last $\overline{WE}$ will initiate the sector erase command(s).

Multiple sectors may be erased concurrently by writing the six bus cycle operations as described above. This sequence is followed with writes of the sector erase command 30H to addresses in other sectors desired to be concurrently erased. A time-out of 100µs from the rising edge of the last $\overline{WE}$ will initiate the sector erase command(s). If another falling edge of the $\overline{WE}$ occurs within the 100µs time-out window the timer is reset. Any command other than sector erase within the time-out window will reset the device to the read mode, ignoring the previous command string. Loading the sector erase buffer may be done in any sequence and with any number of sectors (1 to 8).

It is not required to program all of the memory locations to "0" prior to the sector erase operation. During the sector erase operation, any sectors not selected will not be affected.

The sector erase operation is completed when the I/O7 bit (or I/O15, I/O23, I/O31) on the devices being erased is "1". The device erased returns to the read/reset mode upon completion of the sector erase operation.

$\overline{DATA}$ POLLING:

The module features $\overline{Data}$ Polling as a method to indicate the end of a program or erase operation.

During a program operation, an attempt to read the device(s) being programmed will produce the compliment data of the last data written to the I/O7 bit (or I/O15, I/O23, I/O31) of the device or devices the operation is being performed on. $\overline{Data}$ Polling is valid after the rising edge of the fourth $\overline{WE}$ pulse in the four write pulse sequence.

During the erase operation, the I/O7 bit of the device(s) being erased will be "0" until the erase operation is completed. Upon completion the data on the I/O7 bit will be "1". For chip erase, the $\overline{Data}$ Polling is valid after the rising edge of the sixth $\overline{WE}$ pulse in the six write pulse sequence. For sector erase, the $\overline{Data}$ Polling is valid after the last rising edge of the sector erase $\overline{WE}$ pulse.

TOGGLE BIT:

The module also features the Toggle Bit function for determining the completion of a program or erase operation.

During a program or erase operation, successive attempts to read data from the device(s) will result in the I/O6 (or I/O14, I/O22, I/O30) bit toggling between "1" and "0". Once the program or erase operation has completed, the I/O pin will stop toggling and valid data can be read. During the program operation, the Toggle Bit is valid after the rising edge of the fourth $\overline{WE}$ pulse in the four write pulse sequence. For chip erase, the Toggle Bit is valid after the rising edge of the sixth $\overline{WE}$ pulse in the six write pulse sequence. For sector erase, the Toggle Bit is valid after the last rising edge of the sector erase $\overline{WE}$ pulse. The Toggle Bit is active during the sector time out.

PRODUCT I.D. COMMAND:

The product I.D. command operation outputs the manufacturer code (01H) and the device code (20H). This allows programming equipment to match the device with the proper erase and programming algorithms.

To activate this mode, the programming equipment must force V_{ID} (11.5V to 13.0V) on address pin A9. With $\overline{CE}$ and $\overline{OE}$ = V_{IL} and $\overline{WE}$ = V_{IH}, the two I.D. bytes may then be read from the device outputs by toggling address A0 from V_{IL} to V_{IH}. All addresses are don't cares except A0 and A1.

The I.D. codes can also be accessed via the command register. There are two "unlock" write cycles followed by a write of the read product I.D. command. Following the read product I.D. command, a read from address XXX0H will return 01H and a read from address XXX1H will return 20H. The sector protect status can also be read while in this mode. If the sector is protected, performing a read operation at address location XXX2H with A16, A15, and A14 set for the proper sector address will return a "1" on the I/O0 (or I/O8, I/O16, I/O24) bit of the device the operation is being performed on.

SECTOR PROTECT:

The module also features hardware sector protection. This feature will disable both program and erase operations in any number of sectors (1 through 8). The sector protect feature is enabled using programming equipment at the user's site. The module is shipped with all sectors unprotected.

To activate this mode, the programming equipment must force V_{ID} on A9 and $\overline{OE}$. The sector addresses (A16, A15, and A14) should be set to the sector to be protected. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of $\overline{WE}$. Sector addresses must remain stable during the $\overline{WE}$ pulse.

To verify programming of the protection circuitry, the programming equipment must force V_{ID} on address pin A9 with $\overline{CE}$ and $\overline{OE}$ = V_{IL} and $\overline{WE}$ = V_{IH}. Selecting the sector with A16, A15, and A14 set for the proper sector address will return a "1" on the I/O0 (or I/O8, I/O16, I/O24) bit of the device the operation is being performed on. In this mode, the lower order addresses, except for A0 and A1, are don't care. Address location 00H and 01H are reserved for product ID codes. If a sector protect verify is performed at one of these locations in sector 0, the device would return the manufacturer and device codes respectively (A0 = V_{IL}, A0 = V_{IH}).

It is also possible to determine if a sector is protected in the system by writing the product I.D. command sequence. Performing a read operation at address location XXX2H with the higher order addresses (A16, A15, and A14) set to the proper sector address will return a "1" on the I/O0 (or I/O8, I/O16, I/O24) bit of the device the operation is being performed on.

TIMING LIMIT FLAG:

The I/O5 (or I/O13, I/O21, I/O29) bit will indicate if the program or erase time has exceeded the specified limits. Under these conditions these I/O's will produce a "1" if the program or erase function was not successfully completed. $\overline{Data}$ Polling is the only operating function of the device under this condition. The $\overline{CE}$ circuit will partially power down the device under these conditions. The $\overline{OE}$ and $\overline{WE}$ pins will control the output disable function. To reset the device, write the Reset command sequence to the device. This allows the system to continue to use the other active sectors in the device.

HARDWARE SEQUENCE FLAG:

If the device has exceeded the specified erase or program time and the I/O5 bit is "1", then the I/O4 (or I/O12, I/O20, I/O28) bit will indicate which step in the algorithm the device exceeded the limits. A "0" indicates in programming, a "1" indicates an erase.

SECTOR ERASE TIMER:

After the completion of the initial sector erase command sequence the sector erase time-out will begin. The I/O3 (or I/O11, I/O19, I/O27) bit will remain low until the time-out is complete. $\overline{Data}$ Polling and Toggle Bit are also valid after the initial sector erase command sequence.

If $\overline{Data}$ Polling or the Toggle Bit indicates the device has been written a valid erase command, the I/O3 bit may be used to determine if the sector erase timer window is still open. If the I/O3 bit is high ("1"), the internally controlled erase cycle has begun suspending access to the command register until the erase operation is completed as indicated by $\overline{Data}$ Polling or Toggle Bit. If the I/O3 bit is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the software should check the status of the I/O3 bit prior to and following each sector erase command. If the I/O3 bit was high on the second status check, the command may not have been accepted.

DATA PROTECTION:

The devices used in the construction of the module are designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. The devices power up in the read state only. Also, with a control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from V_{DD} power-up and power-down transitions or system noise.

LOW V_{DD} WRITE INHIBIT;

To avoid initiation of a write cycle during V_{DD} power-up or power-down, a write cycle is locked out for V_{DD} less than 3.2V (typically 3.7V). If V_{DD} V_{LKO}, the command register is disabled and all internal program/erase circuits are disabled. The device will reset to the read mode. Subsequent writes will be ignored until the V_{DD} level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{DD} is above 3.2V.

WRITE PULSE "GLITCH" PROTECTION:

Noise pulses of less than 5ns (typical) on $\overline{OE}$, $\overline{CE}$, and $\overline{WE}$ will not initiate a write cycle.

LOGICAL INHIBIT:

Writing is inhibited by holding any one of $\overline{OE}$ = V_{IL}, $\overline{CE}$ = V_{IH}, or $\overline{WE}$ = V_{IH}. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be = V_{IL} while $\overline{OE}$ = V_{IH}.

POWER-UP WRITE INHIBIT:

If power-up is performed with $\overline{WE}$ = $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IH}, the command register will not latch a command on the rising edge of $\overline{WE}$. The command register is automatically reset to the read mode on power-up.

PRELIMINARY

TRUTH TABLE

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A9	I/O Pin
Product I.D. Manufacturer Code [1]	L	L	H	L	L	V_{ID}	CODE
Product I.D. Device Code [1]	L	L	H	H	L	V_{ID}	CODE
Read	L	L	X	A0	A1	A9	D_{OUT}
Standby	H	X	X	X	X	X	HIGH-Z
Output Disable	L	H	H	X	X	X	HIGH-Z
Write	L	H	L	A0	A1	A9	D_{IN} [2]
Enable Sector Protect	L	V_{ID}	L	X	X	V_{ID}	X
Verify Sector Protect [3]	L	L	H	L	H	V_{ID}	CODE

LEGEND: L = V_{IL}, H = V_{IH}, X = Don't Care

COMMAND DEFINITIONS TABLE [4, 5, 6, 7]

COMMAND SEQUENCE	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
Read / Reset	4	5555H	AAH	2AAAH	55H	5555H	F0H	RA	RD	-	-	-	-
Auto Select	4	5555H	AAH	2AAAH	55H	5555H	90H	00H/01H	01H/20H	-	-	-	-
Byte Program	4	5555H	AAH	2AAAH	55H	5555H	A0H	PA	PD	-	-	-	-
Chip Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Selector Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H

WRITE OPERATION STATUS FLAGS

Status		I/O7[8]	I/O6[8]	I/O5[8]	I/O4[8]	I/O3[8]	I/O2 - I/O0[8]
In Progress	Auto - Programming	I/O7	Toggle	0	0	0	Reserved for Future Use
	Programming in Auto - Erase	0	Toggle	0	0	0	
	Erase in Auto - Erase	0	Toggle	0	1	1	
Exceeded Time Limits	Auto - Programming	I/O7	Toggle	1	0	1	Reserved for Future Use
	Programming in Auto - Erase	0	Toggle	1	0	1	
	Erase in Auto - Erase	0	Toggle	1	1	1	

PRODUCT I.D. CODES

Type	A16	A15	A14	A1	A0	Code (HEX)	I/O7 [8]	I/O6 [8]	I/O5 [8]	I/O4 [8]	I/O3 [8]	I/O2 [8]	I/O1 [8]	I/O0 [8]
Manufacturer Code	X	X	X	V_{IL}	V_{IL}	01H	0	0	0	0	0	0	0	1
Device Code	X	X	X	V_{IL}	V_{IH}	20H	0	0	1	0	0	0	0	0
Sector Protection	Sector Address			V_{IH}	V_{IL}	01H[9]	0	0	0	0	0	0	0	1

NOTES:

[1] Manufacturer and device codes may also be accessed via a command register write sequence.

[2] Refer to Command Definition Table for valid D_{IN} during write operations.

[3] Refer to the section on Sector Address.

[4] Address bit A16 = X = Don't Care for all address commands except for Programming Address (PA) and Sector Address (SA).

[5] Bus Operations are defined in Truth Table.

[6] RA = Address of the memory located on read;
PA = Address of the memory located to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ pulse;
SA = Address of the sector to be erased. The combination of A16, A15, A14 will uniquely select any sector.

[7] RD = Data read from location RA during read operations;
DP = Data to be programmed at location PA. Data is latched on the Falling edge of $\overline{WE}$.

[8] I/O7 = I/O7 and/or I/O15, I/O23, I/O31
I/O6 = I/O6 and/or I/O14, I/O22, I/O30
I/O5 = I/O5 and/or I/O13, I/O21, I/O29
I/O4 = I/O4 and/or I/O12, I/O20, I/O28
I/O3 = I/O3 and/or I/O11, I/O19, I/O27
I/O2 = I/O2 and/or I/O10, I/O18, I/O26
I/O1 = I/O1 and/or I/O9, I/O17, I/O25
I/O0 = I/O0 and/or I/O8, I/O16, I/O24

[9] Outputs 01H at protected sector address.

PRELIMINARY

ERASE AND PROGRAMMING PERFORMANCE					
Parameter	Limits			Units	Comments
	Min.	Typ.	Max.		
Chip/Sector Erase Time	-	1	30 [1]	S	Excluding 00H programming prior to erasure
Sector Programming Time	-	0.25	-	ms	
Chip Programming Time	-	2	24 [2]	S	Excludes system - level overhead
Erase/Program Cycles	100,000	-	-	Cycles	

NOTES:
[1] The Embedded Algorithm allows for 60 second erase time for military temperature range operation.
[2] The Embedded Algorithm allows for a longer chip algorithm program time. However, the actual time will considerably less since most bytes program significantly faster than the worst case.

ABSOLUTE MAXIMUM RATING [3]			
Symbol	Parameter	Value	Unit
T_{STC}	Storage Temperature	-65 to + 150	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
V_{ID}	Voltage on A9 [2]	-0.5 to +13.5	V
I_{OUT}	Output Short Circuit Current	100	mA
$V_{I/O}$	Input/Output Voltage [2]	-0.5 to V_{DD}+0.5	V
V_{DD}	Supply Voltage [2]	-0.5 to + 7.0	V

RECOMMENDED OPERATING RANGE						
Symbol	Characteristic		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
V_{IL}	Input LOW Voltage		-0.5[2]		0.8	V
V_{IH}	Input HIGH Voltage		2.0		V_{DD}+0.5	V
T_A	Operating Temperature	C	0	+25	+70	°C
		I	-40	+25	+85	
		M/B	-55	+25	+125	
V_{ID}	A9 I.D. Voltage		11.5		13.0	V

CAPACITANCE [4]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{CE}	Chip Enable	30	pF	V_{IN} = 0V
C_{ADR}	Address Input	70		
C_{WE}	Write Enable	70		
C_{OE}	Output Enable	70		
$C_{I/O}$	Data Input/Output	30		

DO OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OH}	HIGH Voltage	I_{OH}=-2.5mA	2.4	-	V
V_{OL}	LOW Voltage	I_{OL} = 12mA	-	0.45	V

DC OPERATING CHARACTERISTICS: Over the operating ranges.					
Symbol	Characteristics	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Load Current	V_{DD} = V_{DD} Max., V_{IN} = V_{SS} to V_{DD}		±4.0	µA
I_{LO}	Output Leakage Current	V_{DD} = V_{DD} Max., V_{OUT} = V_{SS} to V_{DD}		±4.0	µA
I_{CC1}	V_{DD} Active Current for Read	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		120	mA
I_{CC2}	V_{DD} Active Current for Program Erase	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		200	mA
I_{SB1}	Standby Current (TTL)	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}		4.0	mA
I_{SB2}	Full Standby Current (CMOS)	$\overline{CE}$ ≥ V_{DD} -0.2V		200	µA
V_{IL}	Input Voltage LOW		-5.0	0.8	V
V_{IH}	Input Voltage HIGH		2.0	V_{DD} + 0.5	V
V_{ID}	A9 Voltage for Auto Select	V_{DD} +5.0V	11.5	13.0	V
V_{OL}	Output Voltage LOW	I_{OUT} = 12mA, V_{DD} = V_{DD} Min.		0.45	V
V_{OH}	Output Voltage HIGH	I_{OUT} = -2.5mA, V_{DD} = V_{DD} Min.	2.4		V
V_{LKO}	LOW V_{DD} Lock-Out Voltage		3.2		V

AC TEST CONDITIONS	
Input Pulse Level	0V to 3.0V
Input Pulse Rise and Fall Times	5ns*
Input and Output Timing Reference Levels	1.5 V

* Transition between 0.8 and 2.2V.

OUTPUT LOAD		
Float	**C_L**	**Parameters Measured**
1	100pF	except t_{DF}
2	5pF	t_{DF}

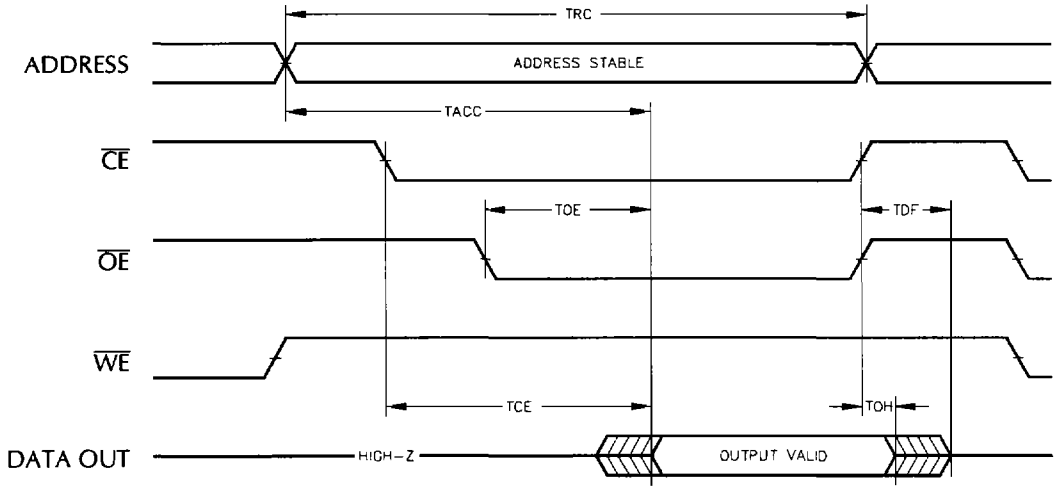
AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges

No.	Symbol	Parameter	45ns		55ns		70ns		90ns		120ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	45		55		70		90		120		ns
2	t_{ACC}	Address to Output Delay		45		55		70		90		120	ns
3	t_{CE}	Chip Enable to Output Valid		45		55		70		90		120	ns
4	t_{OE}	Output Enable to Output Valid		15		18		25		30		50	ns
5	t_{DF}	Chip Enable to Output in LOW-Z [4]	0	15	0	18	0	25	0	30	0	30	ns
6	t_{DF}	Output Enable to Output in HIGH-Z [4]	0	15	0	18	0	25	0	30	0	30	ns
7	t_{OH}	Output Hold from Address, Chip Enable or Output Enable, Whichever Occurs First	0		0		0		0		0		ns

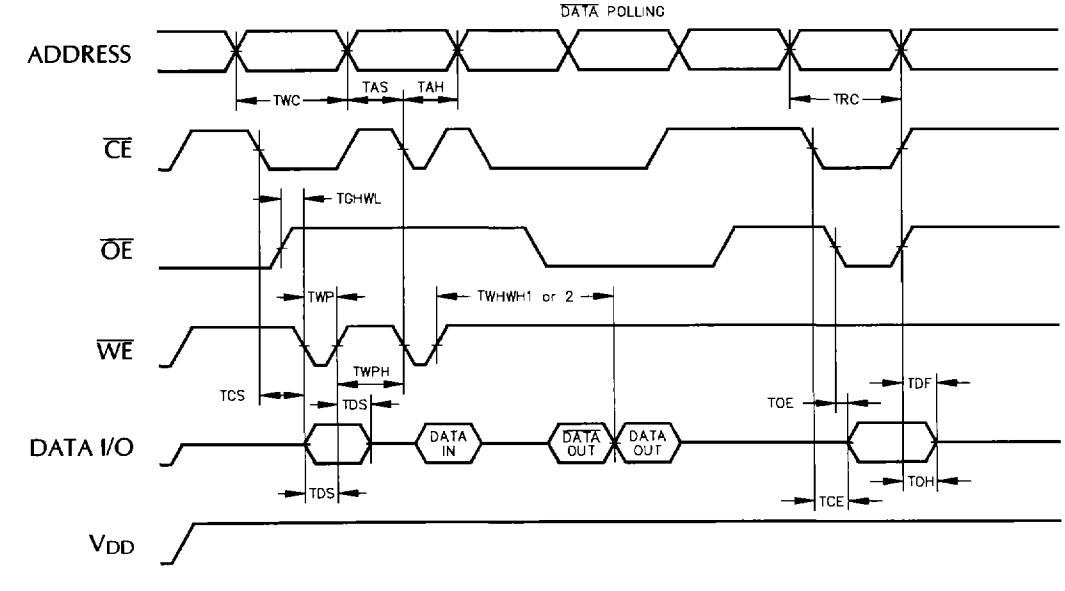
AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges

No.	Symbol	Parameter		45ns		55ns		70ns		90ns		120ns		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
8	t_{WC}	Write Cycle Time		45		55		70		90		120		ns
9	t_{AS}	Address Setup Time		0		0		0		0		0		ns
10	t_{AH}	Address Hold Time		35		45		45		45		50		ns
11	t_{DS}	Data Setup Time		20		20		30		40		50		ns
12	t_{DH}	Data Hold Time		0		0		0		0		0		ns
13	t_{OES}	Output Enable Setup Time		0		0		0		0		0		ns
14	t_{OEH}	Output Enable Hold Time	Read	0		0		0		0		0		ns
			Toggle and $\overline{DATA}$ Polling	10		10		10		10		10		
15	t_{GHWL}	Read Recovery Time before Write		0		0		0		0		0		ns
16	t_{CS}	Chip Enable Setup Time		0		0		0		0		0		ns
17	t_{CH}	Chip Enable Hold Time		0		0		0		0		0		ns
18	t_{WP}	Write Pulse Width		25		30		35		40		50		ns
19	t_{WPH}	Write Pulse Width HIGH		15		20		20		20		20		ns
20	t_{WHWH1}	Programming Operation (Min.)		16		16		16		16		16		µs
21	t_{WHWH2}	Erase Operation (Min.)		1		1		1		1		1		S
22	t_{VCS}	V_{PP} Setup Time		2		2		2		2		2		µs

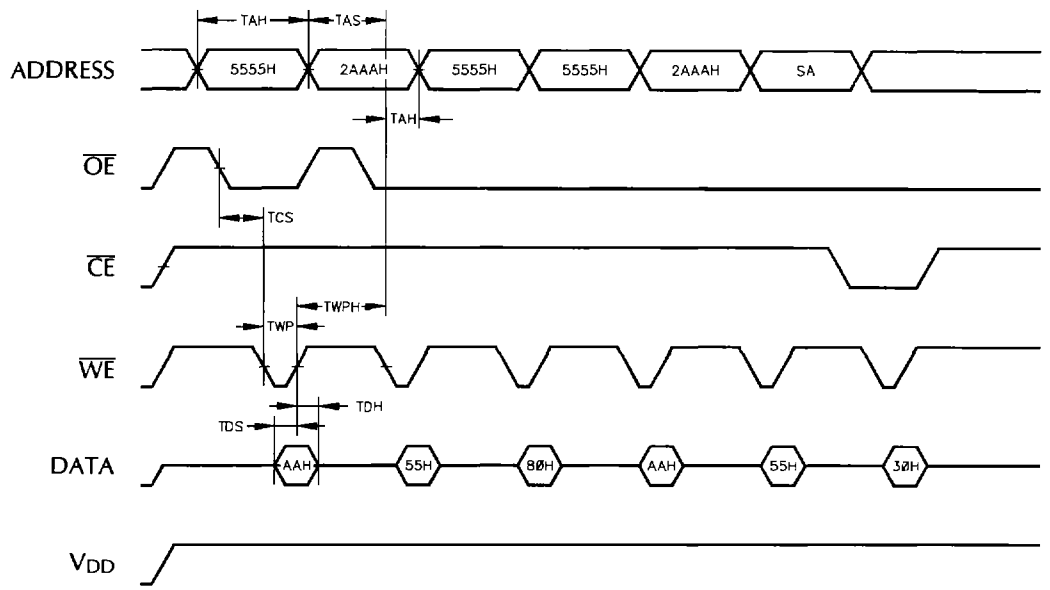
AC WAVEFORMS: READ CYCLE



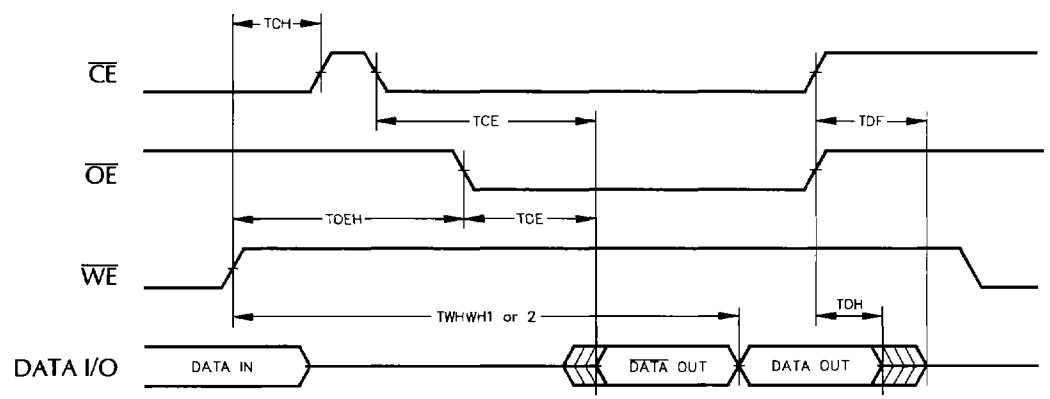
AC WAVEFORMS: WRITE CYCLE



AC WAVEFORMS: SECTOR ERASE OPERATION

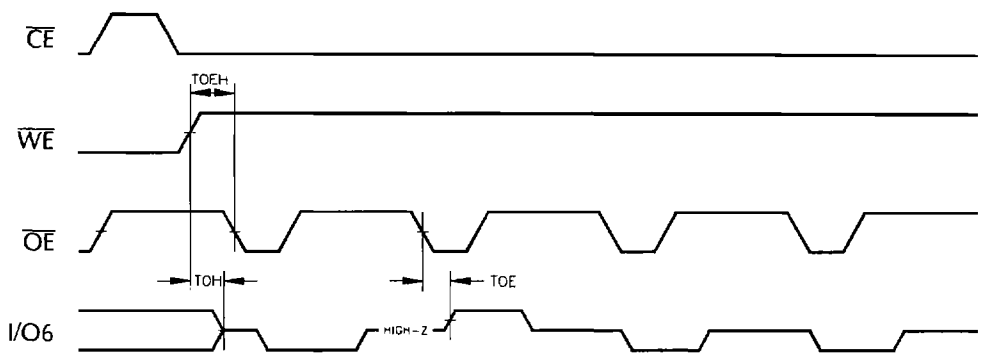


AC WAVEFORMS: DATA POLLING



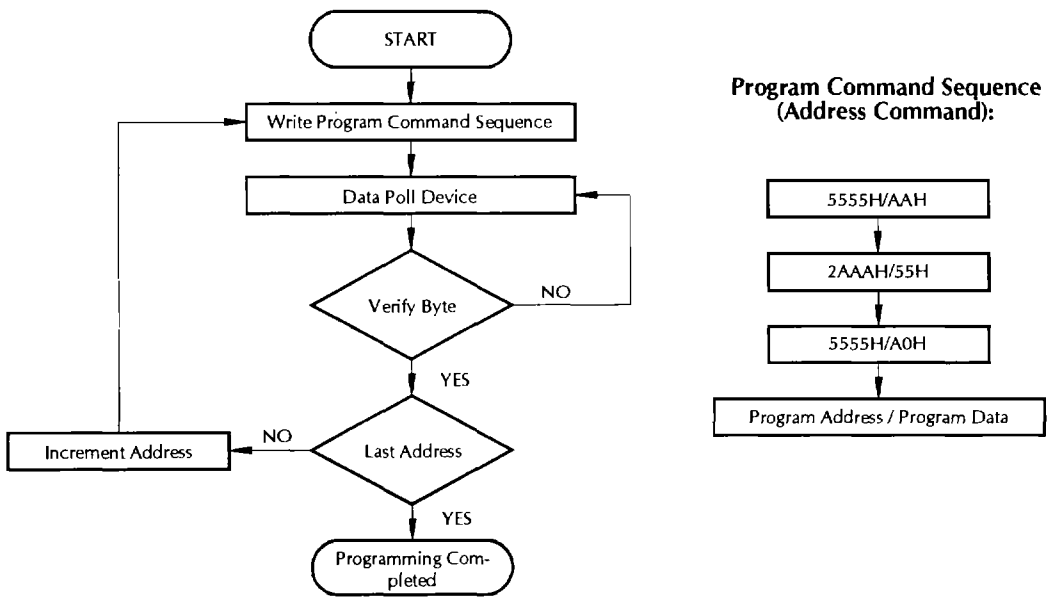
PRELIMINARY

AC WAVEFORMS: TOGGLE BIT



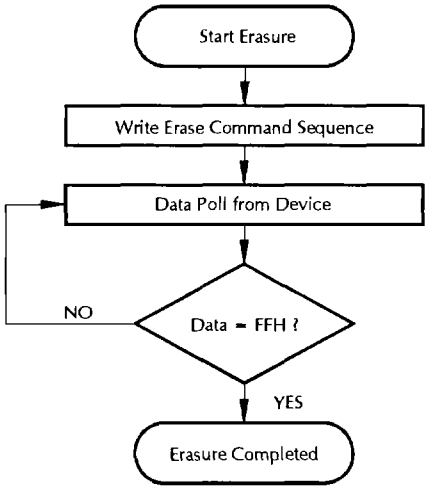
WAVEFORM KEY

PROGRAMMING ALGORITHM

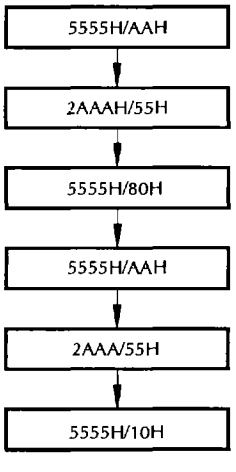


ERASE ALGORITHM

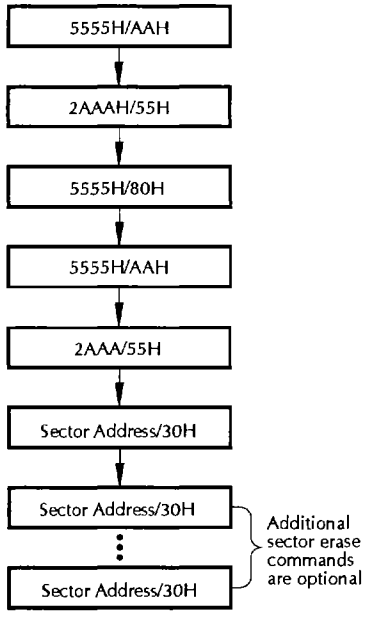
Embedded Erase Algorithm



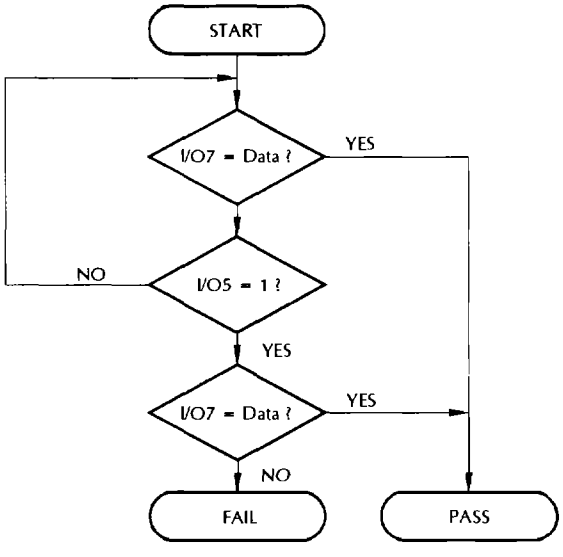
Chip Erase Command Sequence (Address Command):



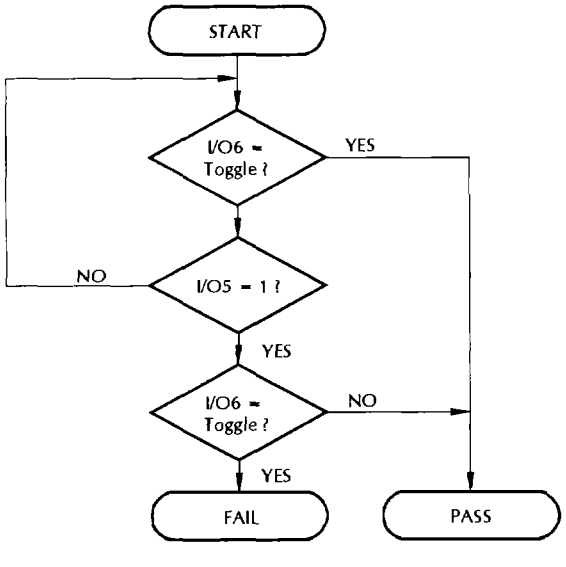
Sector Erase Command Sequence (Address Command):



DATA POLLING ALGORITHM

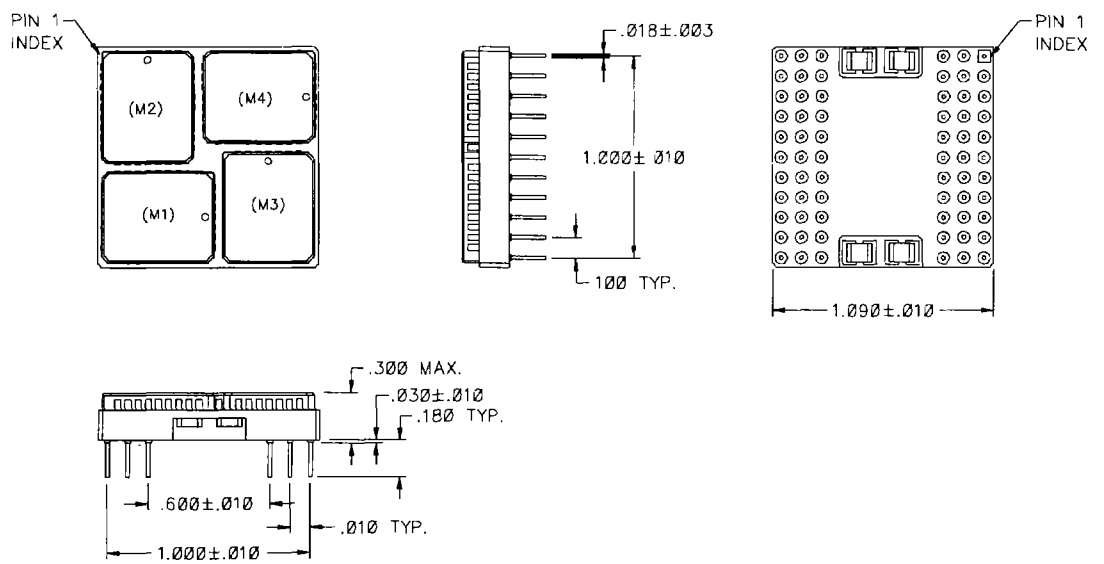


TOGGLE BIT ALGORITHM

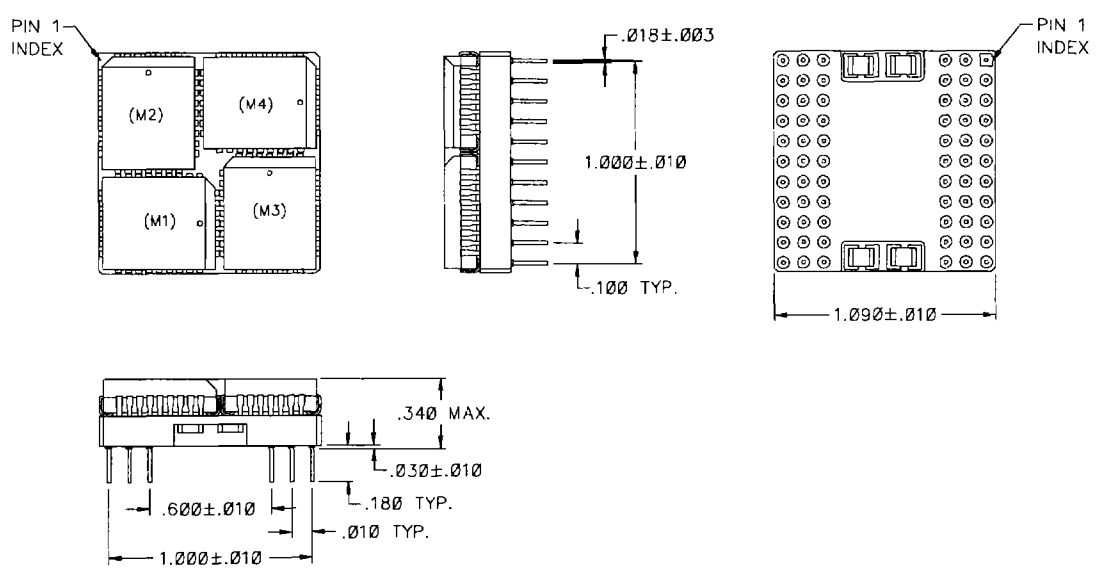


PRELIMINARY

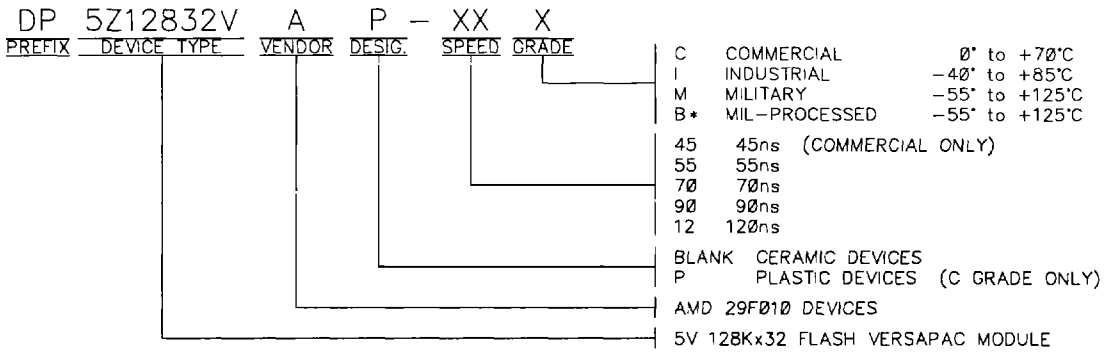
DP5Z12832VA - MECHANICAL DRAWING



DP5Z12832VAP - MECHANICAL DRAWING



ORDERING INFORMATION



* Built with 883 devices.

NOTES:

1. All voltages are with respect to V_{SS}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. A7 through A16 specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.

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