CY2308

3.3V Zero Delay Buffer

Features

- **Zero input-output propagation delay, adjustable by capacitive load on FBK input**
- **Multiple configurations, see "Available CY2308 Configurations" table**
- **Multiple low skew outputs**
  - **Output-output skew less than 250 ps**
  - **Device-device skew less than 700 ps**
  - **Two banks of four outputs, three-stateable by two select inputs**
- **10 MHz to 130 MHz operating range**
- **Low jitter, less than 200 ps cycle-cycle (-1, -1H, -4)**
- **Advanced 0.65μ CMOS technology**
- **Space-saving 16-pin 150-mil SOIC package**
- **3.3V operation**

Functional Description

The CY2308 is a 3.3V zero delay buffer designed to distribute high-speed clocks in PC, workstation, datacom, telecom, and other high-performance applications.

The part has an on-chip PLL which locks to an input clock presented on the REF pin. The PLL feedback is required to be driven into the FBK pin, and can be obtained from one of the outputs. The input to output propagation delay is guaranteed to be less than 350 ps, and output to output skew is guaranteed to be less than 250 ps.

The CY2308 has two banks of four outputs each, which can be controlled by the Select inputs as shown in the table below. If all output clocks are not required, Bank B can be three-stated. The select inputs also allow the input clock to be directly applied to the output for chip and system testing purposes.

The CY2308 PLL enters a Power-Down state when there are no rising edges on the REF input. In this mode, all outputs are three-stated and the PLL is turned off, resulting in less than 50 μA of current draw. The PLL shuts down in two additional cases as shown in the "Select Input Decoding" table below.

Multiple CY2308 devices can accept the same input clock and distribute it in a system. In this case, the skew between the outputs of two devices is guaranteed to be less than 700 ps.

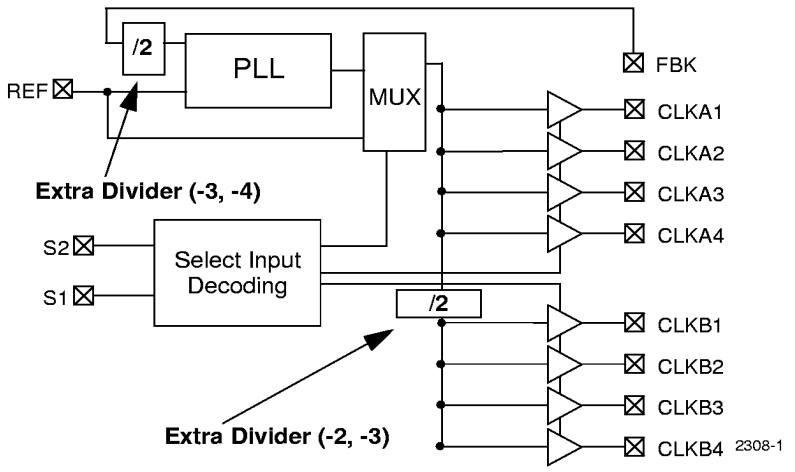
The CY2308 is available in four different configurations, as shown in the "Available CY2308 Configurations" table below. The CY2308-1 is the base part, where the output frequencies equal the reference if there is no counter in the feedback path. The CY2308-1H is the high drive version of the -1, and rise and fall times on this device are much faster.

The CY2308-2 allows the user to obtain 2X and 1X frequencies on each output bank. The exact configuration and output frequencies depends on which output drives the feedback pin. The CY2308-3 allows the user to obtain 4X and 2X frequencies on the outputs.

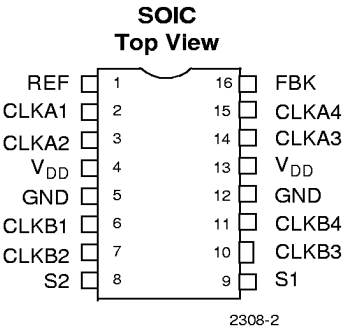
Finally, the CY2308-4 enables the user to obtain 2X clocks on all outputs. Thus, the part is extremely versatile, and can be used in a variety of applications.

The CY2308 operates off a 3.3V supply and is available in a 16-pin 150-mil SOIC package.

Block Diagram



Pin Configuration



Select Input Decoding

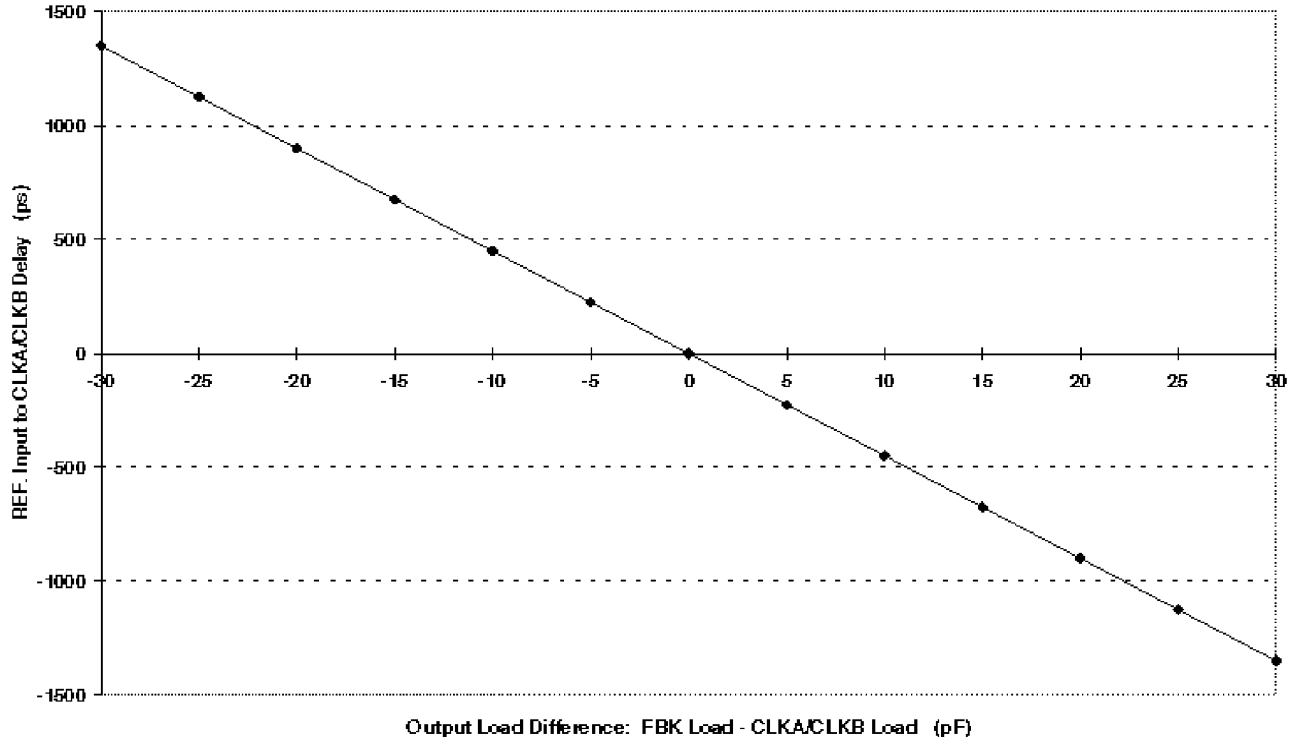
S2	S1	CLOCK A1–A4	CLOCK B1–B4	Output Source	PLL Shutdown
0	0	Three-State	Three-State	PLL	Y
0	1	Driven	Three-State	PLL	N
1	0	Driven	Driven	Reference	Y
1	1	Driven	Driven	PLL	N

Available CY2308 Configurations

Device	Feedback From	Bank A Frequency	Bank B Frequency
CY2308-1	Bank A or Bank B	Reference	Reference
CY2308-1H	Bank A or Bank B	Reference	Reference
CY2308-2	Bank A	Reference	Reference/2
CY2308-2	Bank B	2X Reference	Reference
CY2308-3	Bank A	2X Reference	Reference
CY2308-3	Bank B	4X Reference	2X Reference
CY2308-4	Bank A or Bank B	2X Reference	2X Reference

Zero Delay and Skew Control

REF. Input to CLKA/CLKB Delay v/s Difference in Loading between FBK pin and CLKA/CLKB pins



To close the feedback loop of the CY2308, the FBK pin can be driven from any of the 8 available output pins. The output driving the FBK pin will be driving a total load of 7 pF plus any additional load that it drives. The relative loading of this output (with respect to the remaining outputs) can adjust the input-output delay. This is shown in the graph above.

For applications requiring zero input-output delay, all outputs including the one providing feedback should be equally loaded. If input-output delay adjustments are required, use the above graph to calculate loading differences between the feedback output and remaining outputs.

For zero output-output skew, be sure to load outputs equally. For further information on using CY2308, refer to the application note “CY2308: Zero Delay Buffer”

Pin Description

Pin	Signal	Description
1	REF[1]	Input reference frequency, 5V tolerant input
2	CLKA1[2]	Clock output, Bank A
3	CLKA2[2]	Clock output, Bank A
4	V_{DD}	3.3V supply
5	GND	Ground
6	CLKB1[2]	Clock output, Bank B
7	CLKB2[2]	Clock output, Bank B
8	S2[3]	Select input, bit 2
9	S1[3]	Select input, bit 1
10	CLKB3[2]	Clock output, Bank B
11	CLKB4[2]	Clock output, Bank B
12	GND	Ground
13	V_{DD}	3.3V supply
14	CLKA3[2]	Clock output, Bank A
15	CLKA4[2]	Clock output, Bank A
16	FBK	PLL feedback input

Maximum Ratings

Supply Voltage to Ground Potential ..... –0.5V to +7.0V

DC Input Voltage (Except Ref).....–0.5V to V_{DD} + 0.5V

DC Input Voltage REF ..... –0.5 to 7V

Storage Temperature .....–65°C to +150°C

Max. Soldering Temperature (10 sec.) ..... 260°C

Junction Temperature ..... 150°C

Static Discharge Voltage
(per MIL-STD-883, Method 3015) ..... >2000V

Operating Conditions

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	0	70	°C
C_L	Load Capacitance		30	pF
C_{IN}	Input Capacitance		7	pF

Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage[4]			0.8	V
V_{IH}	Input HIGH Voltage[4]		2.0		V
I_{IL}	Input LOW Current	V_{IN} = 0V		50.0	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}		100.0	µA
V_{OL}	Output LOW Voltage[5]	I_{OL} = 8 mA (-1, -2, -3, -4) I_{OL} = 12 mA (-1H)		0.4	V
V_{OH}	Output HIGH Voltage[5]	I_{OH} = –8 mA (-1, -2, -3, -4) I_{OH} = –12mA (-1H)	2.4		V
I_{DD} (PD mode)	Power Down Supply Current	REF = 0 MHz		50.0	µA
I_{DD}	Supply Current	Unloaded outputs, 66.66 MHz, Select inputs at V_{DD} or GND		40.0	mA

Notes:

1. Weak pull-down.
2. Weak pull-down on all outputs.
3. Weak pull-ups on these inputs.
4. REF and FBK inputs have a threshold voltage of $V_{DD}/2$.
5. Parameter is guaranteed by design and characterization. Not 100% tested in production.

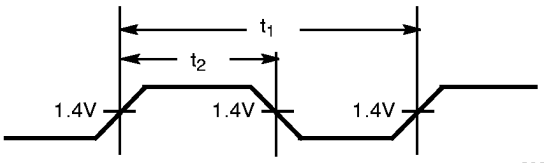
Switching Characteristics [6]

Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
t_1	Output Frequency	30 pF load, All devices	10		100	MHz
t_1	Output Frequency	20 pF load, -1H device	10		130	MHz
t_1	Output Frequency	15 pF load, -1, -2, -3, -4 devices	10		130	MHz
	Duty Cycle[5] = $t_2 \div t_1$ (-1, -2, -3, -4)	Measured at 1.4V	40.0	50.0	60.0	%
	Duty Cycle[5] = $t_2 \div t_1$ (-1H)	Measured at $V_{DD}/2$, $F_{OUT} < 66.66$ MHz	45.0	50.0	55.0	%
	Duty Cycle[5] = $t_2 \div t_1$ (-1H)	Measured at 1.4V, $F_{OUT} \leq 45$ MHz	45.0	50.0	55.0	%
t_3	Rise Time[5] (-1, -2, -3, -4 @ 30 pF)	Measured between 0.8V and 2.0V			2.50	ns
t_3	Rise Time[5] (-1, -2, -3, -4 @ 15 pF)	Measured between 0.8V and 2.0V			1.50	ns
t_3	Rise Time[5] (-1H)	Measured between 0.8V and 2.0V			1.50	ns
t_4	Fall Time[5] (-1, -2, -3, -4 @ 30 pF)	Measured between 0.8V and 2.0V			2.50	ns
t_4	Fall Time[5] (-1, -2, -3, -4 @ 15 pF)	Measured between 0.8V and 2.0V			1.50	ns
t_4	Fall Time[5] (-1H)	Measured between 0.8V and 2.0V			1.50	ns
t_5	Output to Output Skew[5]	All outputs equally loaded			250	ps
t_6	Delay, REF Rising Edge to FBK Rising Edge[5]	Measured at $V_{DD}/2$		0	±350	ps
t_7	Device to Device Skew[5]	Measured at $V_{DD}/2$ on the FBK pins of devices		0	700	ps
t_8	Output Slew Rate[5]	Measured between 0.8V and 2.0V on -1H device using Test Circuit # 2.	1			V/ns
t_J	Cycle to Cycle Jitter[5] (-1, -1H, -4)	Measured at 66.67 MHz, loaded outputs			200	ps
t_J	Cycle to Cycle Jitter[5] (-2, -3)	Measured at 66.67 MHz, loaded outputs			500	ps
t_{LOCK}	PLL Lock Time[5]	Stable power supply, valid clocks presented on REF and FBK pins			1.0	ms

Note:
6. All parameters specified with loaded outputs.

Switching Waveforms

Duty Cycle Timing



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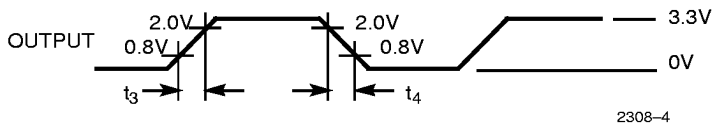
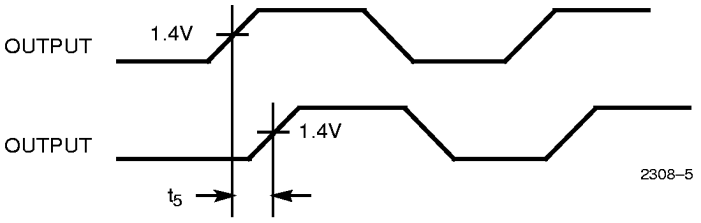
Switching Waveforms (continued)

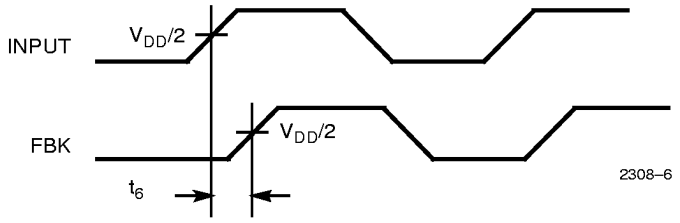
All Outputs Rise/Fall Time



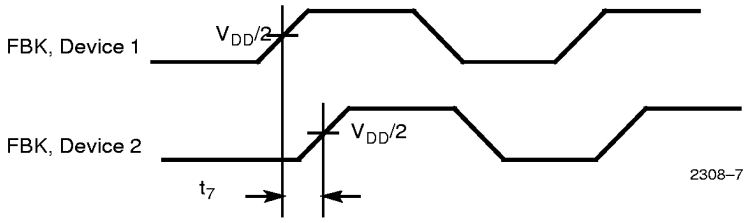
Output-Output Skew



Input-Output Propagation Delay

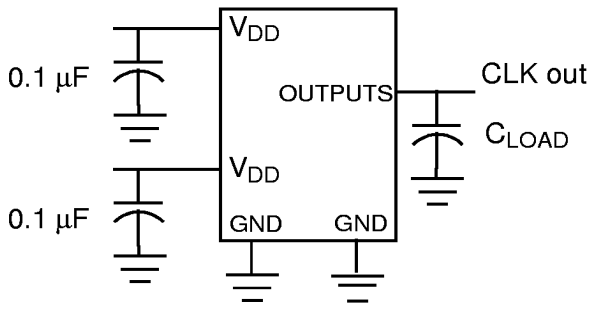


Device-Device Skew



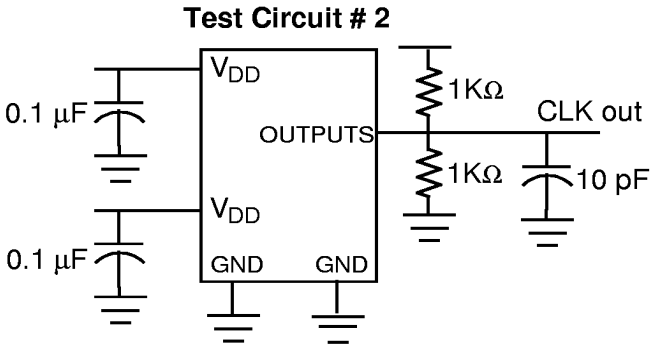
Switching Waveforms (continued)

Test Circuit # 1



Test Circuit for all parameters except t_8

Test Circuit # 2



Test Circuit for t_8, Output slew rate on -1H device

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2308SC–1	S16	16-pin 150-mil SOIC	Commercial
CY2308SC–1H	S16	16-pin 150-mil SOIC	Commercial
CY2308ZC–1H	Z16	16-pin 150-mil TSSOP	Commercial
CY2308SC–2	S16	16-pin 150-mil SOIC	Commercial
CY2308SC–3	S16	16-pin 150-mil SOIC	Commercial
CY2308SC–4	S16	16-pin 150-mil SOIC	Commercial

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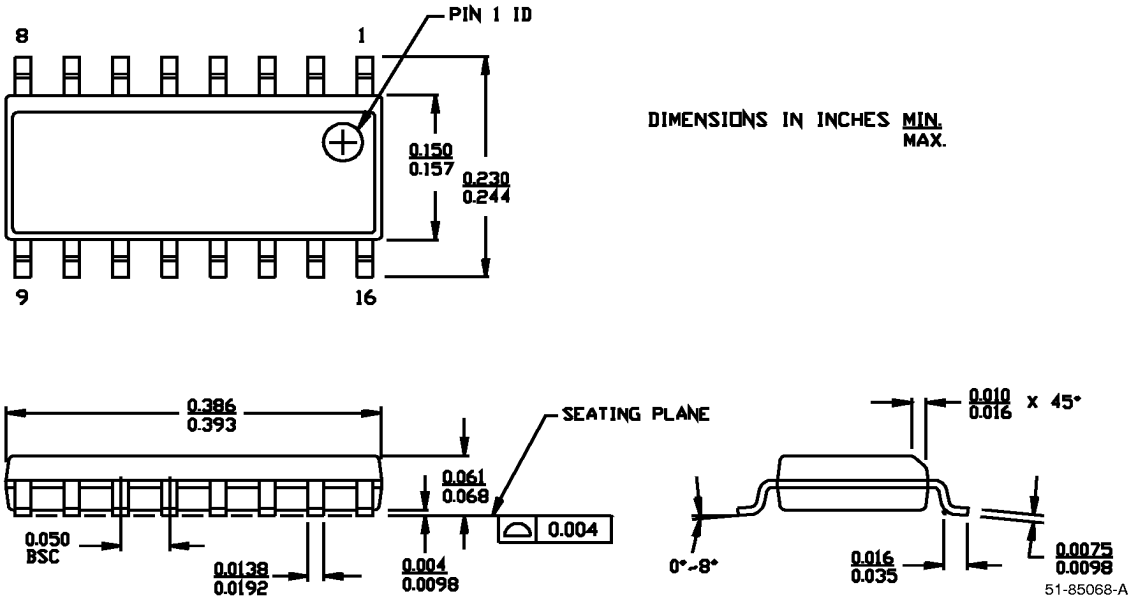
Package Diagrams

16-Lead (150-Mil) Molded SOIC S16



Package Diagrams (continued)

16-Lead Thin Shrunk Small Outline Package (4.40 MM Body) Z16