# 18-Bit 250/670 kSPS PulSAR® Bipolar Programmable Inputs ADC

Preliminary Technical Data

# AD7631/AD7634

## FEATURES

**Multiple pins/software programmable input ranges:**
**±10V, ±5V, 10V, 5V**
***i*CMOS™ process technology**
**Pins or serial SPI input ranges/mode selection**
**Throughput:**
**670kSPS (AD7634)**
**250kSPS (AD7631)**
**INL: ± 1.75 LSB (7± ppm of full scale)**
**DNL: +2/-1 LSB**
**18-bit resolution with no missing codes**
**Dynamic range: 102.5 dB typical**
**SNR: 101 dB typical**
**THD: -122 dB typical**
**5V internal reference: typical drift 7ppm/°C; TEMP output**
**No pipeline delay (SAR architecture)**
**Parallel (18, 16- or 8-bit bus) and serial 5 V/3.3 V interface**
**SPI®-/QSPI™-/MICROWIRE™-/DSP-compatible**
**Power dissipation:**
**190 mW @ 670kSPS**
**75 mW @ 250kSPS**
**Pb-free 48-lead LQFP and LFCSP (7x7mm) packages**
**Pin compatible with other PulSAR ADCs**

## APPLICATIONS

**Process control**
**High speed data acquisition**
**Digital signal processing**
**Spectrum analysis**
**Instrumentation**
**Communications**

## GENERAL DESCRIPTION

The AD7631/AD7634 is an18-bit, charge redistribution successive approximation register (SAR) architecture analog-to-digital converter (ADC) with programmable input ranges and mode selection via a dedicated write only serial interface (or by hardware pin-strapping). The device is fabricated on ADI's patented *i*CMOS high voltage process. The device contains a high speed 18-bit sampling ADC, an internal conversion clock, an internal reference (and buffer), and both serial and parallel system interface ports. Power consumption is automatically scaled with throughput (AD7634 in Impulse mode), making it ideal for battery-powered applications. It is available in Pb-free, 48-lead packages with operation specified from −40°C to +85°C.

## FUNCTIONAL BLOCK DIAGRAM

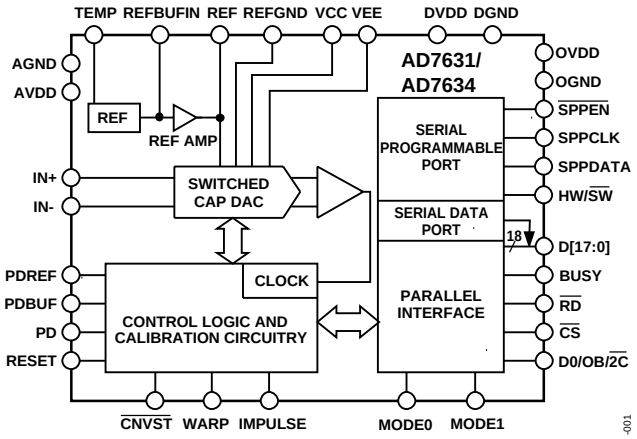


*Figure 1.*

**Table 1. PulSAR® Selection**

| Type/kSPS | 100 to 250 | 500 to 570 | 650 to 1000 | >1000 |
|---|---|---|---|---|
| Pseudo Differential | AD7651, AD7660 AD7661 | AD7650 AD7652 AD7664 AD7666 | AD7653 AD7667 | |
| True Bipolar | AD7610, AD7663 | AD7665 | AD7612, AD7671 | |
| True Differential | AD7675 | AD7676 | AD7677 | AD7621 AD7622 AD7623 |
| 18-Bit Multichannel/ Simultaneous | AD7631 AD7678 | AD7679 AD7654 AD7655 | AD7634 AD7674 | AD7641 AD7643 |

## PRODUCT HIGHLIGHTS

1. Programmable input range and mode selection.
   Dedicated write only serial port used for selecting input range and mode select (mode select AD7634 only).
2. Fast throughput
   The AD7634 is 670kSPS and the AD7631 is 250kSPS.
3. Superior Linearity.
   No missing 18-bit code. +/- 1.75 LSB typical INL
4. Internal Reference.
   5 V internal reference with a typical drift of ±7 ppm/°C and on-chip TEMP sensor.
5. Serial or Parallel Interface.
   Versatile parallel (18, 16- or 8-bit bus) or 2-wire serial interface arrangement compatible with 3.3 V, or 5 V logic.

**Rev. PrC**


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## REVISION HISTORY

# SPECIFICATIONS

AVDD = DVDD = 5 V; OVDD = 2.7 V to 5.5 V; VCC = 15V; VEE = -15V; $V_{REF}$ = 5 V; all specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 2.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RESOLUTION | | 18 | | | Bits |
| ANALOG INPUT[1] | | | | | |
| Differential Voltage Range | | | | | |
| 0 to 5V | $V_{IN+}$ - $V_{IN-}$ | $-V_{REF}$ | | $V_{REF}$ | |
| 0 to 10V | $V_{IN+}$ - $V_{IN-}$ | $-2V_{REF}$ | | $2V_{REF}$ | |
| ±5V | $V_{IN+}$ - $V_{IN-}$ | $-2V_{REF}$ | | $2V_{REF}$ | |
| ±10V | $V_{IN+}$ - $V_{IN-}$ | $-4V_{REF}$ | | $4V_{REF}$ | |
| Operating Input Voltage Range | | | | | |
| 0 to 5V | ($V_{IN+}$, $V_{IN-}$) to AGND | -0.1V | | $V_{REF}$ + 0.1V | |
| 0 to 10V | ($V_{IN+}$, $V_{IN-}$) to AGND | -0.1V | | $2V_{REF}$ + 0.1V | |
| ±5V | ($V_{IN+}$, $V_{IN-}$) to AGND | $-V_{REF}$ – 0.1V | | $V_{REF}$ + 0.1V | |
| ±10V | ($V_{IN+}$, $V_{IN-}$) to AGND | $-2V_{REF}$ – 0.1V | | $2V_{REF}$ + 0.1V | |
| Common Mode Voltage range | | | | | |
| 0 to 5V | $V_{IN+}$, $V_{IN-}$ | $V_{REF}$/2 – 0.1V | $V_{REF}$/2 | $V_{REF}$/2 + 0.1V | |
| 0 to 10V | $V_{IN+}$, $V_{IN-}$ | $V_{REF}$ – 0.2V | $V_{REF}$ | $V_{REF}$ + 0.2V | |
| Bipolar ranges | $V_{IN+}$, $V_{IN-}$ | –0.1V | 0 | 0.1V | |
| Analog Input CMRR | $f_{IN}$ = 100 kHz | | TBD | | dB |
| Input Current | @ 670 kSPS throughput | | TBD | | µA |
| Input Current | @ 250 kSPS throughput | | TBD | | µA |
| Input Impedance | | | | | |
| THROUGHPUT SPEED | | | | | |
| Complete Cycle | AD7634 in Warp mode | | | 1.49 | µs |
| Throughput Rate | AD7634 in Warp mode | 1 | | 670 | kSPS |
| Time between Conversions | AD7634 in Warp mode | | | 1 | ms |
| Complete Cycle | AD7634 in Normal mode | | | 1.75 | µs |
| Throughput Rate | AD7634 in Normal mode | 0 | | 570 | kSPS |
| Complete Cycle | AD7634 in Impulse | | | 2.22 | µs |
| Throughput Rate | AD7634 in Impulse mode | 0 | | 450 | kSPS |
| Complete Cycle | AD7631 | | | 4 | µs |
| Throughput Rate | AD7631 | 0 | | 250 | kSPS |
| DC ACCURACY | | | | | |
| Integral Linearity Error[2] | $V_{REF}$ = 5V, PDREF = PDBUF = High | | ±1.75 | | LSB[3] |
| No Missing Codes | | 18 | | | Bits |
| Differential Linearity Error | | –1 | | +2 | LSB |
| Transition Noise | | | 0.75 | | LSB |
| Bipolar Offset Error | | | 10 | | LSB |
| Bipolar Offset Error Temperature Drift | | | TBD | | ppm/°C |
| Bipolar Full-Scale Error | | | ±60 | | LSB |
| Bipolar Full-Scale Error Temperature Drift | | | TBD | | ppm/°C |
| Power Supply Sensitivity | AVDD = 5 V ± 5% | | TBD | | LSB |

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| AC ACCURACY | | | | | |
| Dynamic Range | $V_{IN}$ = ±5V, $f_{IN}$ = 2 kHz, -60dB | | 102.5 | | dB[4] |
| Signal-to-Noise | $V_{IN}$ = ±5V, $f_{IN}$ = 2 kHz | | 101 | | dB |
| Spurious-Free Dynamic Range | $V_{IN}$ = ±5V, $f_{IN}$ = 2 kHz | | 122 | | dB |
| Total Harmonic Distortion | $V_{IN}$ = ±5V, $f_{IN}$ = 2 kHz | | -106 | | dB |
| Signal-to-(Noise + Distortion) | $V_{IN}$ = ±5V, $f_{IN}$ = 2 kHz | | 100 | | dB |
| –3 dB Input Bandwidth | | | 12 | | MHz |
| SAMPLING DYNAMICS | | | | | |
| Aperture Delay | | | 1 | | ns |
| Aperture Jitter | | | 5 | | ps rms |
| Transient Response | Full-scale step | | | 115 | ns |
| INTERNAL REFERENCE | PDREF = PDBUF = low | | | | |
| Output Voltage | REF @ 25°C | 4.985 | 5.000 | 5.015 | V |
| Temperature Drift | –40°C to +85°C | | ±7 | | ppm/°C |
| Line Regulation | AVDD = 5 V ± 5% | | ±15 | | ppm/V |
| Turn-On Settling Time | $C_{REF}$ = 10 µF | | 5 | | ms |
| REFERENCE BUFFER | PDREF = high | | | | |
| REFBUFIN Input Voltage Range | | | 2.5 | | V |
| EXTERNAL REFERENCE | PDREF = PDBUF = high | | | | |
| Voltage Range | REF | | 5 | AVDD+0.1 | V |
| Current Drain | AD7634 @ 670 kSPS throughput | | TBD | | µA |
| Current Drain | AD7631 @ 250 kSPS throughput | | TBD | | µA |
| TEMPERATURE PIN | | | | | |
| Voltage Output | TEMP @ 25°C | | TBD | | mV |
| Temperature Sensitivity | | | 1 | | mV/°C |
| Output Resistance | | | 4 | | kΩ |
| DIGITAL INPUTS | | | | | |
| Logic Levels | | | | | |
| $V_{IL}$ | | –0.3 | | +0.6 | V |
| $V_{IH}$ | | 2.1 | | OVDD+0.3 | V |
| $I_{IL}$ | | –1 | | +1 | µA |
| $I_{IH}$ | | –1 | | +1 | µA |
| DIGITAL OUTPUTS | | | | | |
| Data Format[5] | | | | | |
| Pipeline Delay[6] | | | | | |
| $V_{OL}$ | $I_{SINK}$ = 500 µA | | | 0.4 | V |
| $V_{OH}$ | $I_{SOURCE}$ = –500 µA | OVDD – 0.6 | | | V |
| POWER SUPPLIES | | | | | |
| Specified Performance | | | | | |
| AVDD | | 4.75 | 5 | 5.25 | V |
| DVDD | | 4.75 | 5 | 5.25 | V |
| OVDD | | 2.7 | | 5.25 | V |
| VCC | | | 15 | | V |
| VEE | | | -15 | | V |

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Operating Current[7] | PDREF = PDBUF = low | | | | |
| AVDD[8] | AD7631 @ 250kSPS throughput | | 8.5 | | mA |
| | AD7634 @ 670kSPS throughput | | 21 | | mA |
| DVDD | AD7631 @ 250kSPS throughput | | 3.5 | | mA |
| | AD7634 @ 670kSPS throughput | | 7 | | mA |
| OVDD | AD7631 @ 250kSPS throughput | | 0.1 | | mA |
| | AD7634 @ 670kSPS throughput | | 0.2 | | mA |
| VCC | AD7631 @ 250kSPS throughput | | 1 | | mA |
| VEE | AD7631 @ 250kSPS throughput | | 0.6 | | mA |
| VCC | AD7634 @ 670kSPS throughput | | 2.8 | | mA |
| VEE | AD7634 @ 670kSPS throughput | | 2 | | mA |
| Power Dissipation | | | | | |
| With Internal Reference[7] | AD7631 @ 250kSPS throughput | | 75 | | mW |
| With Internal Reference[7] | AD7634 @ 670kSPS throughput | | 190 | | |
| Without Internal Reference | AD7631 @ 250kSPS throughput | | 62 | | mW |
| Without Internal Reference[7] | AD7634 @ 670kSPS throughput | | 160 | | mW |
| In Power-Down Mode[9] | PD = high | | 2 | | µW |
| TEMPERATURE RANGE[10] | | | | | |
| Specified Performance | $T_{MIN}$ to $T_{MAX}$ | –40 | | +85 | °C |

[1] The inputs are differential anti-phase. Refer to the **Error! Reference source not found.** section.
[2] Linearity is tested using endnotes, not best fit.
[3] LSB means least significant bit. With the 0 to 5V input range, 1 LSB 38.15µV.
[4] All specifications in dB are referred to a full-scale input FSR. Tested with an input signal at 0.5 dB below full-scale, unless otherwise specified.
[5] Parallel or serial 18-bit.
[6] Conversion results are available immediately after completed conversion.
[7] Tested in parallel reading mode.
[8] With internal reference, PDREF and PDBUF are low; without internal reference, PDREF and PDBUF are high.
[9] With all digital inputs forced to OVDD.
[10] Consult sales for extended temperature range.

# TIMING SPECIFICATIONS

AVDD = DVDD = 5 V; OVDD = 2.7 V to 5.5 V; VCC = 15V; VEE = -15V; $V_{REF}$ = 5 V; all specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 3.**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| CONVERSION AND RESET | | | | | |
| Convert Pulse Width | $t_1$ | 10 | | | ns |
| Time Between Conversions (Warp Mode/Normal Mode[1]) | $t_2$ | | | | ns |
| AD7631 | | 4 | | | µs |
| AD7634 (Warp Mode/Normal Mode/Impulse Mode)[2] | | 1.49/1.75/2.22 | | | µs |
| $\overline{CNVST}$ Low to BUSY High Delay | $t_3$ | | | 35 | ns |
| BUSY High All Modes (Except Master Serial Read After Convert) | $t_4$ | | | | |
| AD7631 | | | | TBD | µs |
| AD7634 (Warp Mode/Normal Mode/Impulse Mode) | | | | TBD | µs |
| Aperture Delay | $t_5$ | | 2 | | ns |
| End of Conversion to BUSY Low Delay | $t_6$ | 10 | | | ns |
| Conversion Time | $t_7$ | | | | |
| AD7631 | | | | TBD | µs |
| AD7634 (Warp Mode/Normal Mode/Impulse Mode) | | | | TBD | µs |
| Acquisition Time | $t_8$ | | | | |
| AD7631 | | 250 | | | ns |
| AD7634 (Warp Mode/Normal Mode/Impulse Mode) | | 250 | | | ns |
| RESET Pulse Width | $t_9$ | 10 | | | ns |
| PARALLEL INTERFACE MODES | | | | | |
| $\overline{CNVST}$ Low to DATA Valid Delay | $t_{10}$ | | | | |
| AD7631 | | | | 1.5 | µs |
| AD7634 (Warp Mode/Normal Mode/Impulse Mode) | | | | 1/1.25/1.5 | µs |
| DATA Valid to BUSY Low Delay | $t_{11}$ | 12 | | | ns |
| Bus Access Request to DATA Valid | $t_{12}$ | | | 45 | ns |
| Bus Relinquish Time | $t_{13}$ | 5 | | 15 | ns |
| MASTER SERIAL INTERFACE MODES[3] | | | | | |
| $\overline{CS}$ Low to SYNC Valid Delay | $t_{14}$ | | | 10 | ns |
| $\overline{CS}$ Low to Internal SCLK Valid Delay | $t_{15}$ | | | 10 | ns |
| $\overline{CS}$ Low to SDOUT Delay | $t_{16}$ | | | 10 | ns |
| $\overline{CNVST}$ Low to SYNC Delay | $t_{17}$ | | | | |
| AD7631 | | | 525 | | ns |
| AD7634 (Warp Mode/Normal Mode/Impulse Mode) | | | 25/275/525 | | ns |
| SYNC Asserted to SCLK First Edge Delay | $t_{18}$ | 3 | | | ns |
| Internal SCLK Period[4] | $t_{19}$ | 25 | | 40 | ns |
| Internal SCLK High[4] | $t_{20}$ | 12 | | | ns |
| Internal SCLK Low[4] | $t_{21}$ | 7 | | | ns |
| SDOUT Valid Setup Time[4] | $t_{22}$ | 4 | | | ns |
| SDOUT Valid Hold Time[4] | $t_{23}$ | 2 | | | ns |
| SCLK Last Edge to SYNC Delay[4] | $t_{24}$ | 3 | | | ns |
| $\overline{CS}$ High to SYNC HI-Z | $t_{25}$ | | | 10 | ns |
| $\overline{CS}$ High to Internal SCLK HI-Z | $t_{26}$ | | | 10 | ns |
| $\overline{CS}$ High to SDOUT HI-Z | $t_{27}$ | | | 10 | ns |

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| | | | See | | |
| BUSY High in Master Serial Read after Convert[4] | $t_{28}$ | | Table 4 | | |
| $\overline{\text{CNVST}}$ Low to SYNC Asserted Delay (all Modes) | $t_{29}$ | | | | ns |
| AD7631 | | | TBD | | ns |
| AD7634 (Warp Mode/Normal Mode/Impulse Mode) | | | TBD | | ns |
| SYNC Deasserted to BUSY Low Delay | $t_{30}$ | | 25 | | ns |
| SLAVE SERIAL INTERFACE MODES | | | | | |
| External SCLK Setup Time | $t_{31}$ | 5 | | | ns |
| External SCLK Active Edge to SDOUT Delay | $t_{32}$ | 1 | | 8 | ns |
| SDIN Setup Time | $t_{33}$ | 5 | | | ns |
| SDIN Hold Time | $t_{34}$ | 5 | | | ns |
| External SCLK Period | $t_{35}$ | 12.5 | | | ns |
| External SCLK High | $t_{36}$ | 5 | | | ns |
| External SCLK Low | $t_{37}$ | 5 | | | ns |

[1] In warp mode only, the maximum time between conversions is 1 ms; otherwise, there is no required maximum time.
[2] In warp mode only, the time between conversions is 1 ms; otherwise, there is no required maximum time.
[3] In serial interface modes, the SYNC, SCLK, and SDOUT timings are defined with a maximum load $C_L$ of 10 pF; otherwise, the load is 60 pF maximum.
[4] In serial master read during convert mode. See **Error! Reference source not found.** for serial master read after convert mode timing specifications.

**Table 4. Serial Clock Timings in Master Read After Convert Mode**

| **DIVSCLK[1]** | | **0** | **0** | **1** | **1** | |
|---|---|---|---|---|---|---|
| **DIVSCLK[0]** | **Symbol** | **0** | **1** | **0** | **1** | **Unit** |
| SYNC to SCLK First Edge Delay Minimum | $t_{18}$ | 3 | 17 | 17 | 17 | ns |
| Internal SCLK Period Minimum | $t_{19}$ | 25 | 60 | 120 | 240 | ns |
| Internal SCLK Period Maximum | $t_{19}$ | 40 | 80 | 160 | 320 | ns |
| Internal SCLK High Minimum | $t_{20}$ | 12 | 22 | 50 | 100 | ns |
| Internal SCLK Low Minimum | $t_{21}$ | 7 | 21 | 49 | 99 | ns |
| SDOUT Valid Setup Time Minimum | $t_{22}$ | 4 | 18 | 18 | 18 | ns |
| SDOUT Valid Hold Time Minimum | $t_{23}$ | 2 | 4 | 30 | 89 | ns |
| SCLK Last Edge to SYNC Delay Minimum | $t_{24}$ | 3 | 60 | 140 | 300 | ns |
| BUSY High Width Maximum (Warp mode) | $t_{28}$ | 1.75 | 2.5 | 4 | 7 | µs |
| BUSY High Width Maximum (Normal mode) | $t_{28}$ | 2 | 2.75 | 4.25 | 7.25 | µs |
| BUSY High Width Maximum (Impulse mode) | $t_{28}$ | 2.25 | 3 | 4.5 | 7.5 | µs |

# ABSOLUTE MAXIMUM RATINGS

**Table 5.**

| Parameter | Rating |
|---|---|
| Analog Inputs/Outputs | |
| IN+, IN−, REF, REFBUFIN, TEMP, INGND, REFGND to AGND | AVDD + 0.3 V to AGND − 0.3 V |
| Ground Voltage Differences | |
| AGND, DGND, OGND | ±0.3 V |
| Supply Voltages | |
| AVDD, DVDD | −0.3 V to +2.7 V |
| OVDD | −0.3 V to +3.8 V |
| AVDD to DVDD | ±2.8 V |
| AVDD, DVDD to OVDD | −3.8 V to +2.8 V |
| Digital Inputs | −0.3 V to +5.5 V |
| PDREF, PDBUF | ±20 mA |
| Internal Power Dissipation[1] | 700 mW |
| Internal Power Dissipation[2] | 2.5 W |
| Junction Temperature | 125°C |
| Storage Temperature Range | −65°C to +125°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. Specification is for the device in free air:
   48-Lead LQFP; $\theta_{JA}$ = 91°C/W, $\theta_{JC}$ = 30°C/W.
2. Specification is for the device in free air:
   48-Lead LFCSP; $\theta_{JA}$ = 26°C/W.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

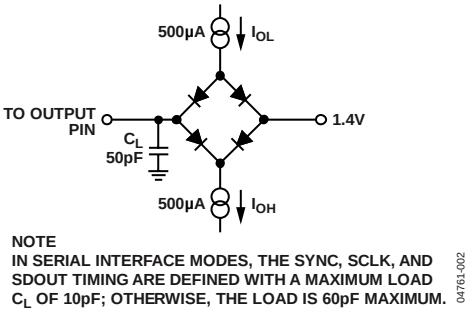




*Figure 2. Load Circuit for Digital Interface Timing, SDOUT, SYNC, and SCLK Outputs, $C_L$ = 10 pF*

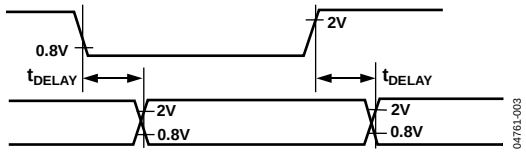



*Figure 3. Voltage Reference Levels for Timing*

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

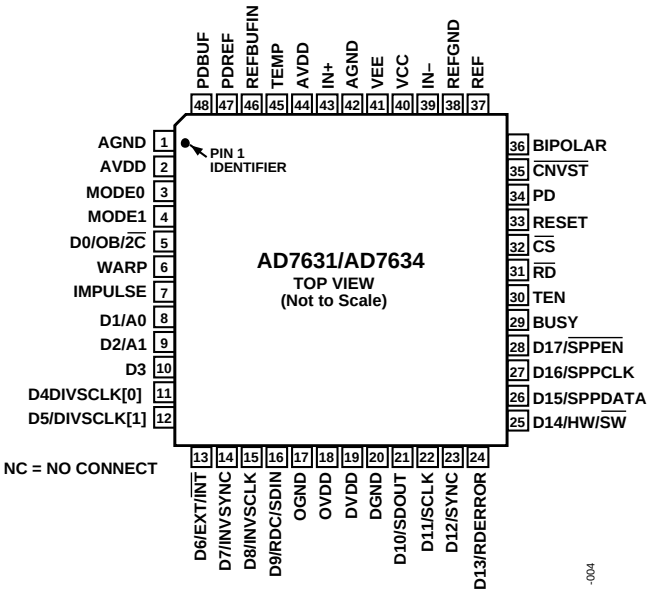



*Figure 4. Pin Configuration*

**Table 6. Pin Function Descriptions**

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| 1, 42 | AGND | P | Analog Power Ground Pin. |
| 2, 44 | AVDD | P | Input Analog Power Pins. Nominally 5 V. |
| 3, 4 | MODE[0:1] | DI | Data Output Interface Mode Selection. |

| Interface MODE# | MODE1 | MODE0 | Description |
|---|---|---|---|
| 0 | 0 | 0 | 18-bit interface |
| 1 | 0 | 1 | 16-bit interface |
| 2 | 1 | 0 | 8-bit (byte) interface |
| 3 | 1 | 1 | Serial interface |

| | | | |
|---|---|---|---|
| 5 | D0/OB/$\overline{2C}$ | DI/O | When MODE[1:0] = 0 (18-bit interface mode), this pin is Bit 0 of the parallel port data output bus and the data coding is straight binary. In all other modes, this pin allows the choice of straight binary/twos complement. When OB/$\overline{2C}$ is high, the digital output is straight binary; when low, the MSB is inverted resulting in a twos complement output from its internal shift register. |
| 6 | WARP | DI | AD7634: Conversion Mode Selection. When WARP = high and IMPULSE = low, this selects warp mode. In this mode, the maximum throughput is achievable, and a minimum conversion rate must be applied to guarantee full specified accuracy.<br>When WARP = low and IMPULSE = low, this selects normal mode where full accuracy is maintained independent of the minimum conversion rate.<br>AD7631: Connect to DGND. |
| 7 | IMPULSE | DI | AD7634: Conversion Mode Selection. When IMPULSE = high and WARP = low, this input selects impulse mode, a reduced power mode. In this mode, the power dissipation is approximately scaled proportional to the sampling rate.<br>AD7631: Connect to DGND. |
| 8 | D1/A0 | DI/O | When MODE[1:0] = 0, this pin is Bit 1 of the parallel port data output bus. In all other modes, this input pin controls the form in which data is output as shown in Table 7. |
| 9 | D2/A1 | DI/O | When MODE[1:0] = 0, this pin is Bit 2 of the parallel port data output bus.<br>When MODE[1:0] = 1 or 2, this input pin controls the form in which data is output as shown in Table 7. |
| 10 | D3 | D0 | When MODE[1:0] = 0, 1, or 2, this output is used as Bit 3 of the parallel port data output bus. This pin is always an output, regardless of the interface mode. |

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| 11, 12 | D[4:5] | DI/O | When MODE[1:0] = 0, 1, or 2, these pins are Bit 4 and Bit 5 of the parallel port data output bus. |
| | or DIVSCLK[0:1] | | When MODE[1:0] = 3 (serial mode), serial clock division selection. When using serial master read after convert mode (EXT/$\overline{INT}$ = low, RDC/SDIN = low), these inputs can be used to slow down the internally generated serial clock that clocks the data output. In other serial modes, these pins are high impedance outputs. |
| 13 | D6 | DI/O | When MODE[1:0] = 0, 1, or 2, this output is used as Bit 6 of the parallel port data output bus. |
| | or EXT/$\overline{INT}$ | | When MODE[1:0] = 3 (serial mode), serial clock source select. This input is used to select the internally generated (master) or external (slave) serial data clock. |
| | | | When EXT/$\overline{INT}$ = low, master mode. The internal serial clock is selected on SCLK output. |
| | | | When EXT/$\overline{INT}$ = high, slave mode. The output data is synchronized to an external clock signal, gated by $\overline{CS}$, connected to the SCLK input. |
| 14 | D7 | DI/O | When MODE[1:0] = 0, 1, or 2, this output is used as Bit 7 of the parallel port data output bus. |
| | or INVSYNC | | When MODE[1:0] = 3 (serial mode), invert sync select. In serial master mode (EXT/$\overline{INT}$ = low), this input is used to select the active state of the SYNC signal. |
| | | | When INVSYNC = low, SYNC is active high. |
| | | | When INVSYNC = high, SYNC is active low. |
| 15 | D8 | DI/O | When MODE[1:0] = 0, 1, or 2, this output is used as Bit 8 of the parallel port data output bus. |
| | or INVSCLK | | When MODE[1:0] = 3, invert SCLK select. In all serial modes, this input is used to invert the SCLK signal. |
| 16 | D9 | DI/O | When MODE[1:0] = 0, 1, or 2, this output is used as bit 9 of the parallel port data output bus. |
| | or RDC | | When MODE[1:0] = 3 (serial mode), read during convert. When using serial master mode (EXT/$\overline{INT}$ = low), RDC is used to select the read mode. |
| | | | When RDC = high, the previous conversion result is output on SDOUT during conversion and the period of SCLK changes. |
| | | | When RDC = low (read after convert), the current result can be output on SDOUT only when the conversion is complete. |
| | or SDIN | | When MODE[1:0] = 3 (serial mode), serial data in. When using serial slave mode, (EXT/$\overline{INT}$ = high), SDIN could be used as a data input to daisy-chain the conversion results from two or more ADCs onto a single SDOUT line. The digital data level on SDIN is output on SDOUT with a delay of 18 SCLK periods after the initiation of the read sequence. |
| 17 | OGND | P | Input/Output Interface Digital Power Ground. |
| 18 | OVDD | P | Input/Output Interface Digital Power. Nominally at the same supply as the supply of the host interface (2.7 V to 5V). |
| 19 | DVDD | P | Digital Power. Nominally at 5 V. |
| 20 | DGND | P | Digital Power Ground. |
| 21 | D10 | DO | When MODE[1:0] = 0, 1, or 2, this output is used as Bit 10 of the parallel port data output bus. |
| | or SDOUT | | When MODE[1:0] = 3 (serial mode), serial data output. In serial mode, this pin is used as the serial data output synchronized to SCLK. Conversion results are stored in an on-chip register. The ADC provides the conversion result, MSB first, from its internal shift register. The data format is determined by the logic level of OB/$\overline{2C}$. |
| | | | In master mode, EXT/$\overline{INT}$ = low. SDOUT is valid on both edges of SCLK. |
| | | | In slave mode, EXT/$\overline{INT}$ = high: |
| | | | When INVSCLK = low, SDOUT is updated on SCLK rising edge and valid on the next falling edge. |
| | | | When INVSCLK = high, SDOUT is updated on SCLK falling edge and valid on the next rising edge. |
| 22 | D11 | DI/O | When MODE[1:0] = 0, 1, or 2, this output is used as Bit 11 of the parallel port data output bus. |
| | or SCLK | | When MODE[1:0] = 3 (serial mode), serial clock. In all serial modes, this pin is used as the serial data clock input or output, depending upon the logic state of the EXT/$\overline{INT}$ pin. The active edge where the data SDOUT is updated depends on the logic state of the INVSCLK pin. |
| 23 | D12 | DO | When MODE[1:0] = 0, 1, or 2, this output is used as Bit 12 of the parallel port data output bus. |
| | or SYNC | | When MODE[1:0] = 3 (serial mode), frame synchronization. In serial master mode (EXT/$\overline{INT}$= low), this output is used as a digital output frame synchronization for use with the internal data clock. |

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| | | | When a read sequence is initiated and INVSYNC = low, SYNC is driven high and remains high while SDOUT output is valid.<br>When a read sequence is initiated and INVSYNC = high, SYNC is driven low and remains low while SDOUT output is valid. |
| 24 | D13<br>or RDERROR | DO | When MODE[1:0] = 0, 1, or 2, this output is used as Bit 13 of the parallel port data output bus.<br>When MODE[1:0] = 3 (serial mode), read error. In serial slave mode (EXT/$\overline{INT}$ = high), this output is used as an incomplete read error flag. If a data read is started and not completed when the current conversion is complete, the current data is lost and RDERROR is pulsed high. |
| 25 | D14<br>or HW/$\overline{SW}$ | DI/O | When MODE[1:0] = 0, 1, or 2, this output is used as Bit 14 of the parallel port data output bus.<br>When MODE[1:0] = 3 (serial mode) hardware/software select. This input, part of the serial programmable port, is used to select hardware or software input ranges and mode selection. |
| 26 | D15<br>or SPPDATA | DI/O | When MODE[1:0] = 0, 1, or 2, this output is used as Bit 15 of the parallel port data output bus.<br>When MODE[1:0] = 3 (serial mode), serial programmable port data. This input is used to write in the serial programmable port data when HW/$\overline{SW}$ = low. |
| 27 | D16<br>or SPPCLK | DI/O | When MODE[1:0] = 0, 1, or 2, this output is used as Bit 16 of the parallel port data output bus.<br>When MODE[1:0] = 3 (serial mode), serial programmable port clock. This input is used to clock in the data on SPPDATA. The active edge where the data SPPDATA is updated depends on the logic state of the INVSCLK pin. |
| 28 | D17<br>or $\overline{SPPEN}$ | DI/O | When MODE[1:0] = 0, 1, or 2, this output is used as Bit 17 of the parallel port data output bus.<br>When MODE[1:0] = 3 (serial mode), serial programmable port enable. Asserting this input enables the serial programmable port. |
| 29 | BUSY | DO | Busy Output. Transitions high when a conversion is started and remains high until the conversion is complete and the data is latched into the on-chip shift register. The falling edge of BUSY can be used as a data-ready clock signal. |
| 30 | TEN | DI | 10 Volt Input Range. Refer to Table 8.<br>When MODE[1:0] = 0, 1, or 2, this input is used to select the 10V input range.<br>When MODE[1:0] = 3 (serial mode), and<br>HW/$\overline{SW}$ = high, driving TEN high selects the 10 Volt input range.<br>HW/$\overline{SW}$ = low, the input range is programmed with the serial programmable port and this pin is a don't care. |
| 31 | $\overline{RD}$ | DI | Read Data. When $\overline{CS}$ and $\overline{RD}$ are both low, the interface parallel or serial output bus is enabled. |
| 32 | $\overline{CS}$ | DI | Chip Select. When $\overline{CS}$ and $\overline{RD}$ are both low, the interface parallel or serial output bus is enabled. $\overline{CS}$ is also used to gate the external clock in slave serial mode. |
| 33 | RESET | DI | Reset Input. When high, resets the ADC. Current conversion, if any, is aborted. Falling edge of RESET enables the calibration mode indicated by pulsing BUSY high. If not used, this pin can be tied to DGND. |
| 34 | PD | DI | Power-Down Input. When high, power downs the ADC. Power consumption is reduced and conversions are inhibited after the current one is completed. |
| 35 | $\overline{CNVST}$ | DI | Conversion Start. A falling edge on $\overline{CNVST}$ puts the internal sample-and-hold into the hold state and initiates a conversion. |
| 36 | BIP | DI | Bipolar Input Range. Refer to Table 8.<br>When MODE[1:0] = 0, 1, or 2, this input is used to select the bipolar input range.<br>When MODE[1:0] = 3 (serial mode), and<br>HW/$\overline{SW}$ = high, driving BIP high selects the bipolar input range.<br>HW/$\overline{SW}$ = low, the input range is programmed with the serial programmable port and this pin is a don't care. |
| 37 | REF | AI/O | Reference Output/Input.<br>When PDREF/PDBUF = low, the internal reference and buffer are enabled producing 5 V on this pin.<br>When PDREF/PDBUF = high, the internal reference and buffer are disabled allowing an externally supplied voltage reference up to AVDD volts. Decoupling is required with or without the internal reference and buffer. |

| Pin No. | Mnemonic | Type[1] | Description |
|---|---|---|---|
| 38 | REFGND | AI | Reference Input Analog Ground. |
| 39 | IN– | AI | Differential Negative Analog Input; referenced to IN+. |
| 40 | $V_{CC}$ | P | High Voltage Positive Supply. |
| 41 | $V_{EE}$ | P | High Voltage Negative Supply. |
| 43 | IN+ | AI | Differential Positive Analog Input; referenced to IN-. |
| 45 | TEMP | AO | Temperature Sensor Analog Output. |
| 46 | REFBUFIN | AI/O | Reference Buffer Input.<br>When using an external reference with the internal buffer (PDBUF = low, PDREF = high), applying 2.5V on this pin produces 5V on the REF pin.<br>When using the internal reference (PDBUF = PDREF = low), this pin should not be connected. |
| 47 | PDREF | DI | Internal Reference Power-Down Input.<br>When low, the internal reference is enabled (PDBUF also needs to be low).<br>When high, the internal reference is powered down and an external reference must been used. |
| 48 | PDBUF | DI | Internal Reference Buffer Power-Down Input.<br>When low, the buffer is enabled (PDREF also needs to be low).<br>When high, the buffer is powered-down and an external reference must be used. |

[1] AI = analog input; AI/O = bidirectional analog; AO = analog output; DI = digital input; DI/O = bidirectional digital; DO = digital output; P = power.

**Table 7. Data Bus Interface Definition**

| MODE | MODE1 | MODE0 | D0/OB/$\overline{2C}$ | D1/A0 | D2/A1 | D[3] | D[4:9] | D[10:11] | D[12:15] | D[16:17] | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | R[0] | R[1] | R[2] | R[3] | R[4:9] | R[10:11] | R[12:15] | R[16:17] | 18-Bit Parallel |
| 1 | 0 | 1 | OB/$\overline{2C}$ | A0 = 0 | R[2] | R[3] | R[4:9] | R[10:11] | R[12:15] | R[16:17] | 16-Bit High Word |
| 1 | 0 | 1 | OB/$\overline{2C}$ | A0 = 1 | R[0] | R[1] | All Zeros | | | | 16-Bit Low Word |
| 2 | 1 | 0 | OB/$\overline{2C}$ | A0 = 0 | A1 = 0 | All Hi-Z | | R[10:11] | R[12:15] | R[16:17] | 8-Bit High Byte |
| 2 | 1 | 0 | OB/$\overline{2C}$ | A0 = 0 | A1 = 1 | All Hi-Z | | R[2:3] | R[4:7] | R[8:9] | 8-Bit Mid Byte |
| 2 | 1 | 0 | OB/$\overline{2C}$ | A0 = 1 | A1 = 0 | All Hi-Z | | R[0:1] | All Zeros | | 8-Bit Low Byte |
| 2 | 1 | 0 | OB/$\overline{2C}$ | A0 = 1 | A1 = 1 | All Hi-Z | | All Zeros | | R[0:1] | 8-Bit Low Byte |
| 3 | 1 | 1 | OB/$\overline{2C}$ | All Hi-Z | | Serial Interface | | | | | Serial Interface |

**Table 8. Input Range Selection. Parallel Mode and Serial Hardware Mode**

| Range | BIP | TEN | HW/$\overline{SW}$ (serial mode) |
|---|---|---|---|
| 0 - 5V | Low | Low | High |
| 0 - 10V | Low | High | High |
| ±5V | High | Low | High |
| ±10V | High | High | High |
| All Ranges[1] | X | X | Low |

[1] In serial mode (MODE[1:0] = 3) when HW/$\overline{SW}$ = low, the input ranges are defined by registers.

# TERMINOLOGY

**Integral Nonlinearity Error (INL)**
Linearity error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

**Differential Nonlinearity Error (DNL)**
In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

**Gain Error**
The first transition (from 000…00 to 000…01) should occur for an analog voltage ½ LSB above the nominal negative full scale (19.073486 V for the 0 to 5V range). The last transition (from 111…10 to 111…11) should occur for an analog voltage 1½ LSB below the nominal full scale (+4.999943 V for the 0 to 5V V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

**Zero Error**
The zero error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

**Dynamic Range**
It is the ratio of the rms value of the full scale to the rms noise measured with the inputs shorted together. The value for dynamic range is expressed in decibels.

**Signal-to-Noise Ratio (SNR)**
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

**Total Harmonic Distortion (THD)**
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

**Signal to (Noise + Distortion) Ratio (SINAD)**
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

**Spurious-Free Dynamic Range (SFDR)**
The difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

**Effective Number of Bits (ENOB)**

ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD and is expressed in bits by

$$ENOB = [(SINAD_{dB} - 1.76)/6.02]$$

**Aperture Delay**
Aperture delay is a measure of the acquisition performance and is measured from the falling edge of the $\overline{\text{CNVST}}$ input to when the input signal is held for a conversion.

**Transient Response**
The time required for the AD7641 to achieve its rated accuracy after a full-scale step function is applied to its input.

**Reference Voltage Temperature Coefficient**

It is derived from the typical shift of output voltage at 25°C on a sample of parts maximum and minimum reference output voltage ($V_{REF}$) measured at $T_{MIN}$, T(25°C), and $T_{MAX}$. It is expressed in ppm/°C using

$$TCV_{REF}(\text{ppm/°C}) = \frac{V_{REF}(Max) - V_{REF}(Min)}{V_{REF}(25°\text{C}) \times (T_{MAX} - T_{MIN})} \times 10^6$$

where:

$V_{REF}$ (*Max*) = Maximum $V_{REF}$ at $T_{MIN}$, T(25°C), or $T_{MAX}$

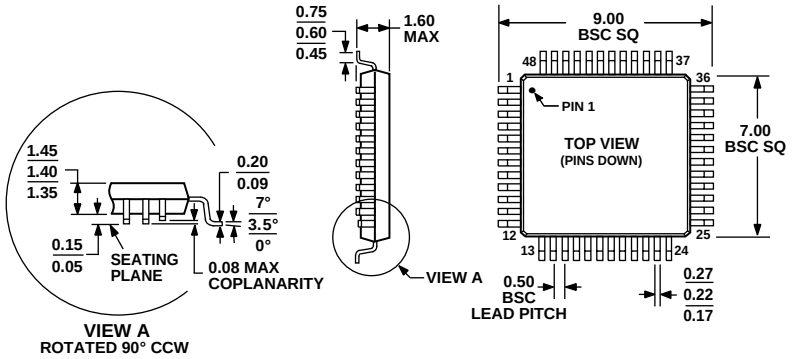
$V_{REF}$ (*Min*) = Minimum $V_{REF}$ at $T_{MIN}$, T(25°C), or $T_{MAX}$

$V_{REF}$ (25°*C*) = $V_{REF}$ at 25°C

$T_{MAX}$ = +85°C

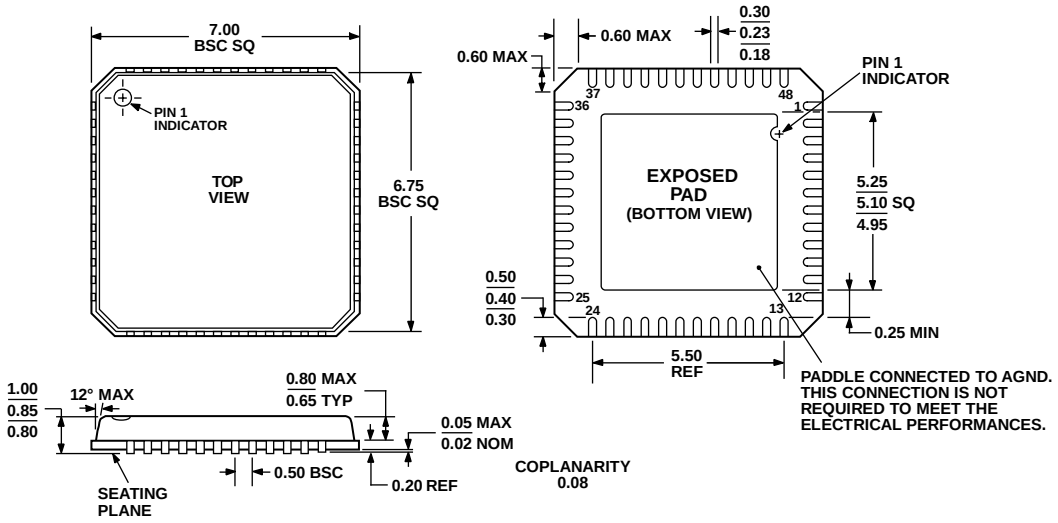
$T_{MIN}$ = –40°C

# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MS-026-BBC

*Figure 5. 48-Lead Low Profile Quad Flat Package [LQFP]*
*(ST-48)*
*Dimensions shown in millimeters*




COMPLIANT TO JEDEC STANDARDS MO-220-VKKD-2

*Figure 6. 48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]*
*7 mm × 7 mm Body, Very Thin Quad (CP-48-1)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD7641BCPZ[1] | –40°C to +85°C | 48-Lead Lead Frame Chip Scale Package (LFCSP_VQ) | CP-48-1 |
| AD7641BCPZRL[1] | –40°C to +85°C | 48-Lead Lead Frame Chip Scale Package (LFCSP_VQ) | CP-48-1 |
| AD7641BSTZ[1] | –40°C to +85°C | 48-Lead Low Profile Quad Flat Package (LQFP) | ST-48 |
| AD7641BSTZRL[1] | –40°C to +85°C | 48-Lead Low Profile Quad Flat Package (LQFP) | ST-48 |
| EVAL-AD7641CB[2] | | Evaluation Board | |
| EVAL-CONTROLBRD3[3] | | Controller Board | |

[1] Z = Pb-free part.
[2] This board can be used as a standalone evaluation board or in conjunction with the EVAL-CONTROL BRD3 for evaluation/demonstration purposes.
[3] This board allows a PC to control and communicate with all Analog Devices, Inc. evaluation boards ending in the CB designators.



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