

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT597**

8-bit shift register with input  
flip-flops

Product specification  
File under Integrated Circuits, IC06

December 1990

## 8-bit shift register with input flip-flops

## 74HC/HCT597

## FEATURES

- 8-bit parallel storage register inputs
- Shift register has direct overriding load and clear
- Output capability: standard
- $I_{CC}$  category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT597 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT597 consist each of an 8-bit storage register feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and the shift register have positive edge-triggered clocks. The shift register also has direct load (from storage) and clear inputs.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f = 6\text{ ns}$

| SYMBOL            | PARAMETER                                  | CONDITIONS                                   | TYPICAL |     | UNIT |
|-------------------|--------------------------------------------|----------------------------------------------|---------|-----|------|
|                   |                                            |                                              | HC      | HCT |      |
| $t_{PHL}/t_{PLH}$ | propagation delay<br>SH <sub>CP</sub> to Q | $C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$ | 17      | 20  | ns   |
|                   | ST <sub>CP</sub> to Q                      |                                              | 25      | 29  | ns   |
|                   | $\overline{PL}$ to Q                       |                                              | 21      | 26  | ns   |
| $f_{max}$         | maximum clock frequency SH <sub>CP</sub>   |                                              | 96      | 83  | MHz  |
| $C_I$             | input capacitance                          |                                              | 3.5     | 3.5 | pF   |
| $C_{PD}$          | power dissipation capacitance per package  | notes 1 and 2                                | 29      | 32  | pF   |

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz

$f_o$  = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in V

2. For HC the condition is  $V_I = \text{GND to } V_{CC}$   
For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

## ORDERING INFORMATION

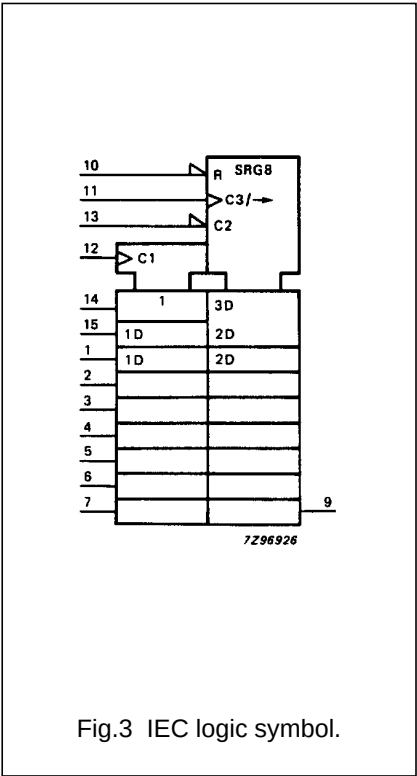
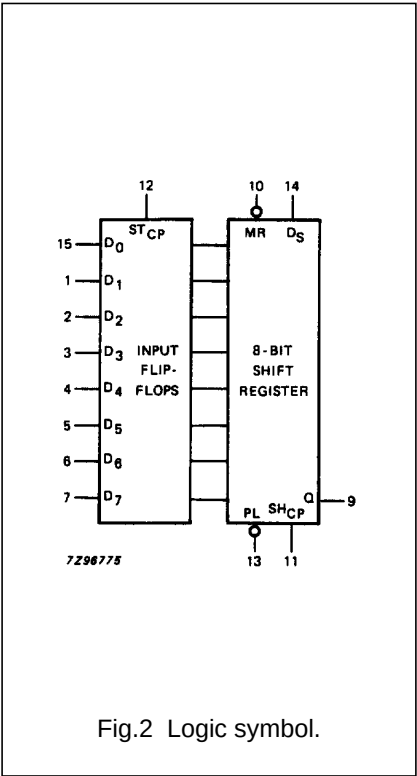
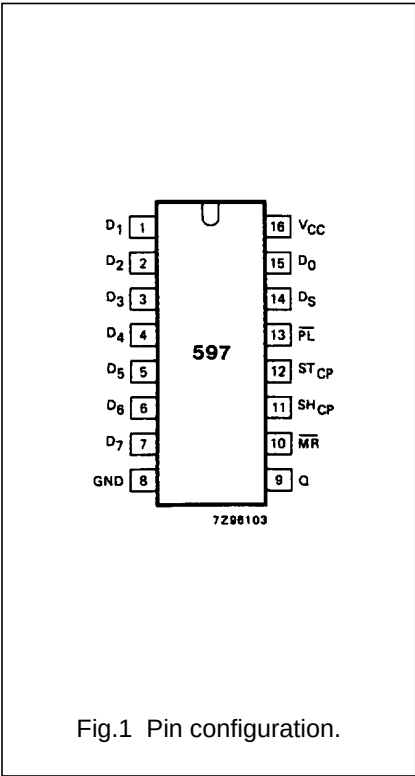
See "74HC/HCT/HCU/HCMOS Logic Package Information".

8-bit shift register with input flip-flops

74HC/HCT597

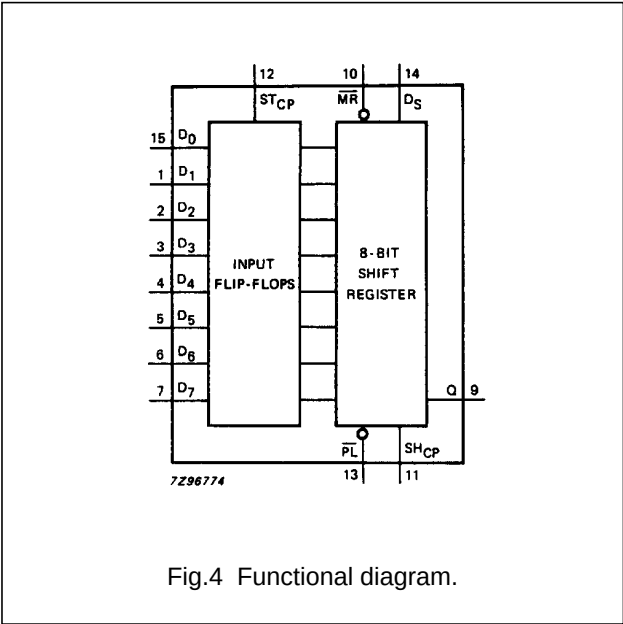
PIN DESCRIPTION

| PIN NO.                 | SYMBOL                       | NAME AND FUNCTION                                 |
|-------------------------|------------------------------|---------------------------------------------------|
| 8                       | GND                          | ground (0 V)                                      |
| 9                       | Q                            | serial data output                                |
| 10                      | $\overline{\text{MR}}$       | asynchronous reset input (active LOW)             |
| 11                      | $\text{SH}_{\text{CP}}$      | shift clock input (LOW-to-HIGH, edge-triggered)   |
| 12                      | $\text{ST}_{\text{CP}}$      | storage clock input (LOW-to-HIGH, edge-triggered) |
| 13                      | $\overline{\text{PL}}$       | parallel load input (active LOW)                  |
| 14                      | $\text{D}_{\text{S}}$        | serial data input                                 |
| 15, 1, 2, 3, 4, 5, 6, 7 | $\text{D}_0$ to $\text{D}_7$ | parallel data inputs                              |
| 16                      | $\text{V}_{\text{CC}}$       | positive supply voltage                           |



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74HC/HCT597



FUNCTION TABLE

| ST <sub>CP</sub> | SH <sub>CP</sub> | $\overline{\text{PL}}$ | $\overline{\text{MR}}$ | FUNCTION                                                                  |
|------------------|------------------|------------------------|------------------------|---------------------------------------------------------------------------|
| ↑                | X                | X                      | X                      | data loaded to input latches                                              |
| ↑                | X                | L                      | H                      | data loaded from inputs to shift register                                 |
| no clock edge    | X                | L                      | H                      | data transferred from input flip-flops to shift register                  |
| X                | X                | L                      | L                      | invalid logic, state of shift register indeterminate when signals removed |
| X                | X                | H                      | L                      | shift register cleared                                                    |
| X                | ↑                | H                      | H                      | shift register clocked $Q_n = Q_{n-1}$ , $Q_0 = D_S$                      |

Notes

- 1. H = HIGH voltage level
- L = LOW voltage level
- X = don't care
- ↑ = LOW-to-HIGH CP transition

## 8-bit shift register with input flip-flops

74HC/HCT597

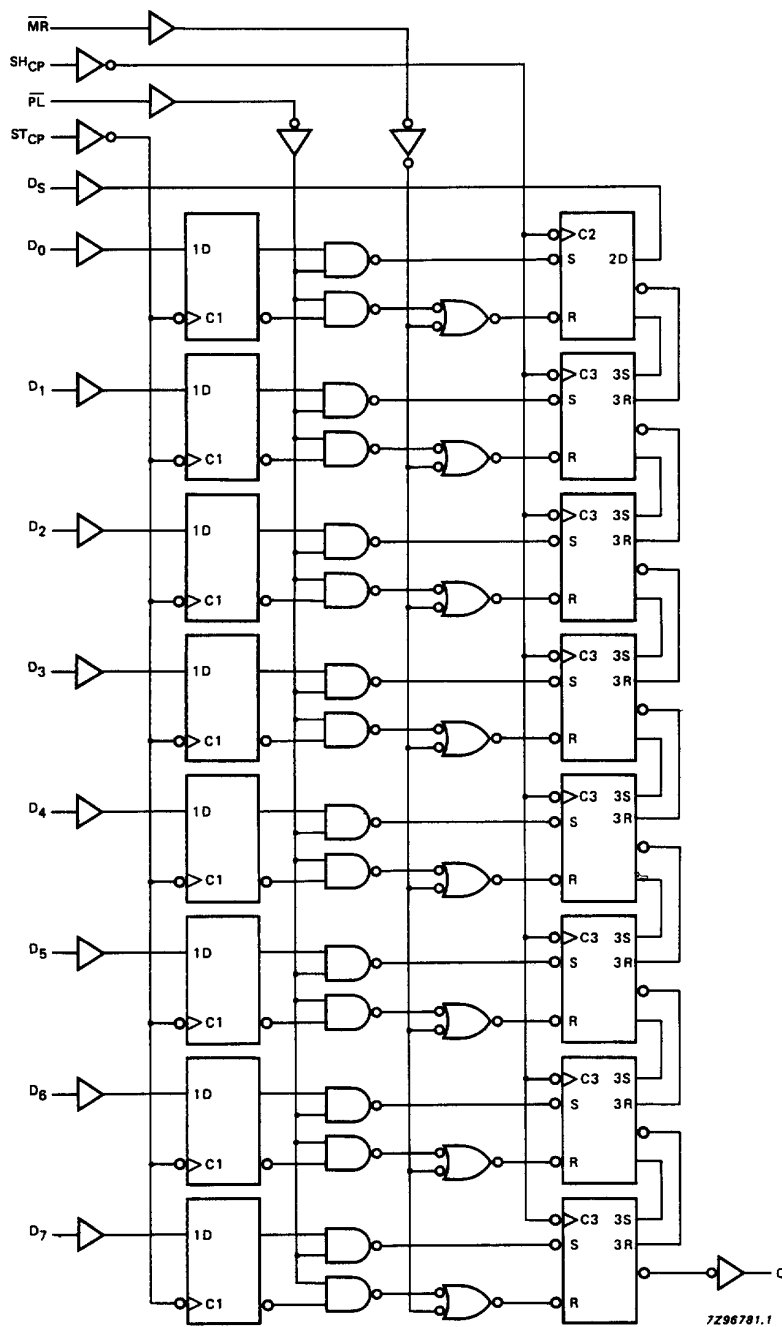


Fig.5 Logic diagram.

## 8-bit shift register with input flip-flops

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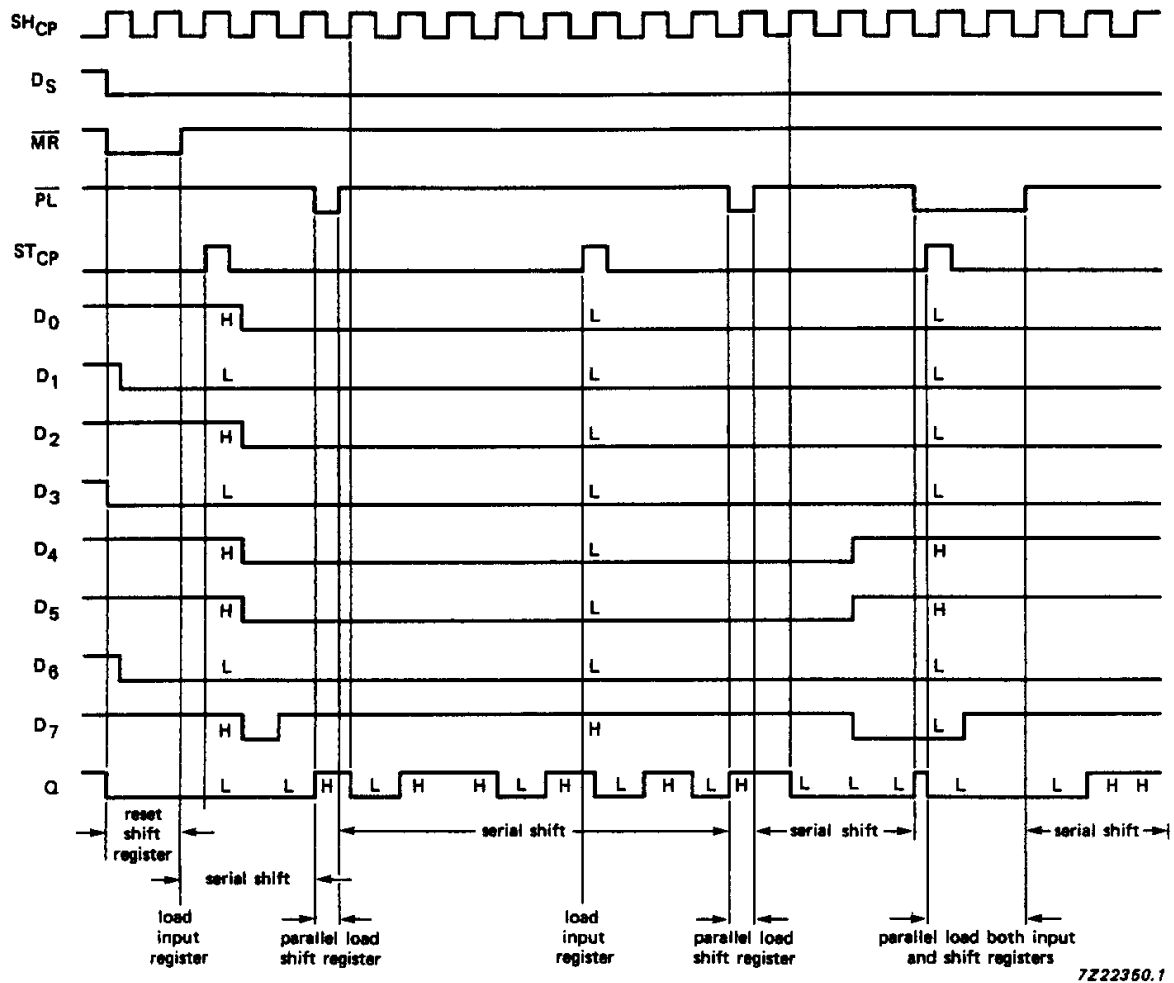


Fig.6 Timing diagram.

## 8-bit shift register with input flip-flops

## 74HC/HCT597

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

| SYMBOL                              | PARAMETER                                         | T <sub>amb</sub> (°C) |                |                 |                 |                 |                 |                 | UNIT | TEST CONDITIONS        |           |
|-------------------------------------|---------------------------------------------------|-----------------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------|------------------------|-----------|
|                                     |                                                   | 74HC                  |                |                 |                 |                 |                 |                 |      | V <sub>CC</sub><br>(V) | WAVEFORMS |
|                                     |                                                   | +25                   |                |                 | −40 to +85      |                 | −40 to +125     |                 |      |                        |           |
|                                     |                                                   | min.                  | typ.           | max.            | min.            | max.            | min.            | max.            |      |                        |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>SH <sub>CP</sub> to Q        |                       | 55<br>20<br>16 | 175<br>35<br>30 |                 | 220<br>44<br>37 |                 | 265<br>53<br>45 | ns   | 2.0<br>4.5<br>6.0      | Fig.7     |
| t <sub>PHL</sub>                    | propagation delay<br>MR to Q                      |                       | 58<br>21<br>17 | 175<br>35<br>30 |                 | 220<br>44<br>37 |                 | 265<br>53<br>45 | ns   | 2.0<br>4.5<br>6.0      | Fig.8     |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>ST <sub>CP</sub> to Q        |                       | 80<br>29<br>23 | 250<br>50<br>43 |                 | 315<br>63<br>54 |                 | 375<br>75<br>64 | ns   | 2.0<br>4.5<br>6.0      | Fig.7     |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>PL to Q                      |                       | 69<br>25<br>20 | 215<br>43<br>37 |                 | 270<br>54<br>46 |                 | 325<br>65<br>55 | ns   | 2.0<br>4.5<br>6.0      | Fig.9     |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time                            |                       | 19<br>7<br>6   | 75<br>15<br>13  |                 | 95<br>19<br>16  |                 | 110<br>22<br>19 | ns   | 2.0<br>4.5<br>6.0      | Fig.9     |
| t <sub>w</sub>                      | ST <sub>CP</sub> pulse width<br>HIGH or LOW       | 80<br>16<br>14        | 11<br>4<br>3   |                 | 100<br>20<br>17 |                 | 120<br>24<br>20 |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.7     |
| t <sub>w</sub>                      | SH <sub>CP</sub> pulse width<br>HIGH or LOW       | 80<br>16<br>14        | 14<br>5<br>4   |                 | 100<br>20<br>17 |                 | 120<br>24<br>20 |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.7     |
| t <sub>w</sub>                      | MR pulse width<br>LOW                             | 80<br>16<br>14        | 22<br>8<br>6   |                 | 100<br>20<br>17 |                 | 120<br>24<br>20 |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.8     |
| t <sub>w</sub>                      | PL pulse width<br>LOW                             | 80<br>16<br>14        | 22<br>8<br>6   |                 | 100<br>20<br>17 |                 | 120<br>24<br>20 |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.9     |
| t <sub>rem</sub>                    | removal time<br>MR to SH <sub>CP</sub>            | 60<br>12<br>10        | −3<br>−1<br>−1 |                 | 75<br>15<br>13  |                 | 90<br>18<br>15  |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.10    |
| t <sub>su</sub>                     | set-up time<br>D <sub>n</sub> to ST <sub>CP</sub> | 60<br>12<br>10        | 8<br>3<br>2    |                 | 75<br>15<br>13  |                 | 90<br>18<br>15  |                 | ns   | 2.0<br>4.5<br>6.0      | Fig.11    |

## 8-bit shift register with input flip-flops

## 74HC/HCT597

| SYMBOL           | PARAMETER                                            | T <sub>amb</sub> (°C) |                 |      |                 |      |                 |      | UNIT | TEST CONDITIONS        |           |
|------------------|------------------------------------------------------|-----------------------|-----------------|------|-----------------|------|-----------------|------|------|------------------------|-----------|
|                  |                                                      | 74HC                  |                 |      |                 |      |                 |      |      | V <sub>CC</sub><br>(V) | WAVEFORMS |
|                  |                                                      | +25                   |                 |      | −40 to +85      |      | −40 to +125     |      |      |                        |           |
|                  |                                                      | min.                  | typ.            | max. | min.            | max. | min.            | max. |      |                        |           |
| t <sub>su</sub>  | set-up time<br>D <sub>S</sub> to SH <sub>CP</sub>    | 60<br>12<br>10        | 11<br>4<br>3    |      | 75<br>15<br>13  |      | 90<br>18<br>15  |      | ns   | 2.0<br>4.5<br>6.0      | Fig.11    |
| t <sub>su</sub>  | set-up time<br>PL to SH <sub>CP</sub>                | 60<br>12<br>10        | 11<br>4<br>3    |      | 75<br>15<br>13  |      | 90<br>18<br>15  |      | ns   | 2.0<br>4.5<br>6.0      | Fig.12    |
| t <sub>h</sub>   | hold time<br>D <sub>n</sub> to ST <sub>CP</sub>      | 5<br>5<br>5           | −3<br>−1<br>−1  |      | 5<br>5<br>5     |      | 5<br>5<br>5     |      | ns   | 2.0<br>4.5<br>6.0      | Fig.11    |
| t <sub>h</sub>   | hold time<br>PL̄, D <sub>S</sub> to SH <sub>CP</sub> | 5<br>5<br>5           | −6<br>−2<br>−2  |      | 5<br>5<br>5     |      | 5<br>5<br>5     |      | ns   | 2.0<br>4.5<br>6.0      | Fig.11    |
| f <sub>max</sub> | maximum pulse frequency<br>SH <sub>CP</sub>          | 6.0<br>30<br>35       | 29<br>87<br>104 |      | 4.8<br>24<br>28 |      | 4.0<br>20<br>24 |      | MHz  | 2.0<br>4.5<br>6.0      | Fig.7     |



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8-bit shift register with input flip-flops74HC/HCT597

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**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT                               | UNIT LOAD COEFFICIENT |
|-------------------------------------|-----------------------|
| D <sub>S</sub>                      | 0.25                  |
| D <sub>n</sub>                      | 0.30                  |
| PL, MR                              | 1.50                  |
| ST <sub>CP</sub> , SH <sub>CP</sub> | 1.50                  |

## 8-bit shift register with input flip-flops

## 74HC/HCT597

## AC WAVEFORMS FOR 74HCT

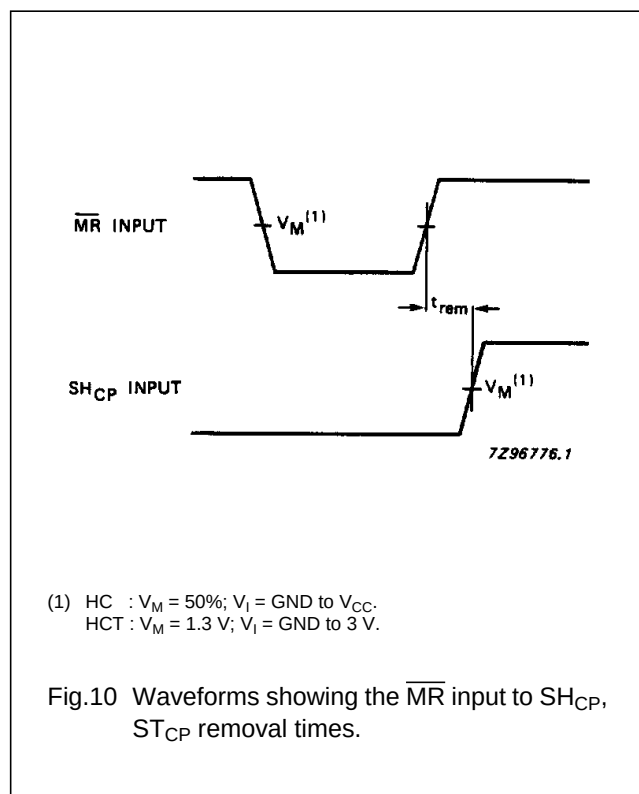
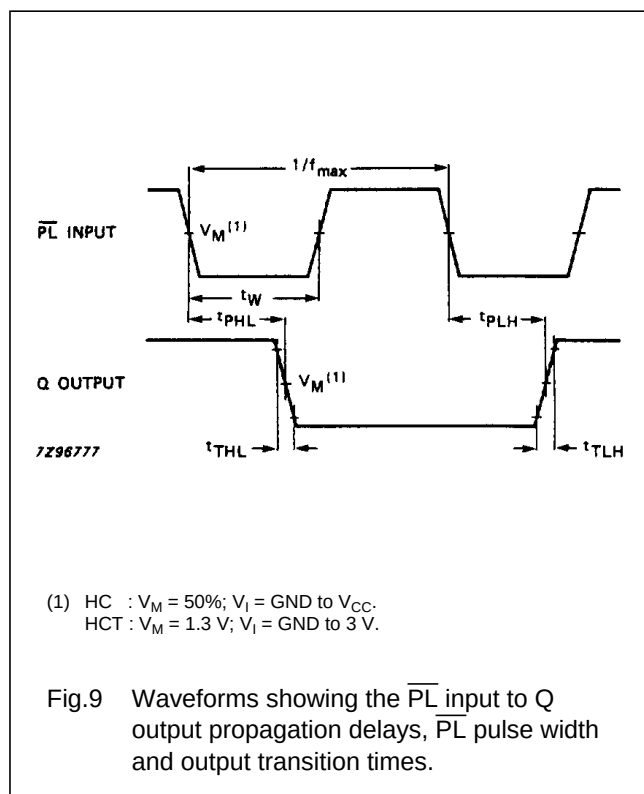
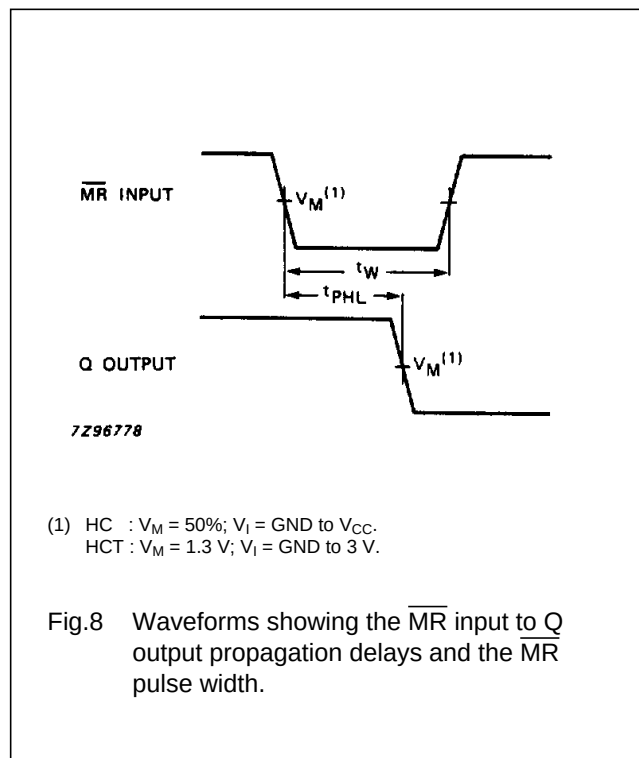
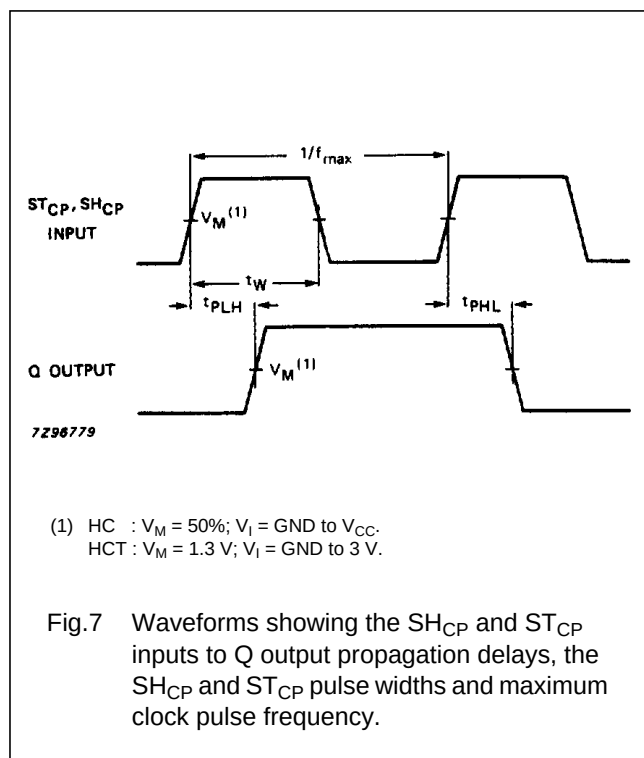
GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

| SYMBOL                              | PARAMETER                                           | T <sub>amb</sub> (°C) |      |      |            |      |             |      |     | UNIT | TEST CONDITIONS        |           |
|-------------------------------------|-----------------------------------------------------|-----------------------|------|------|------------|------|-------------|------|-----|------|------------------------|-----------|
|                                     |                                                     | 74HCT                 |      |      |            |      |             |      |     |      | V <sub>CC</sub><br>(V) | WAVEFORMS |
|                                     |                                                     | +25                   |      |      | −40 to +85 |      | −40 to +125 |      |     |      |                        |           |
|                                     |                                                     | min.                  | typ. | max. | min.       | max. | min.        | max. |     |      |                        |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>SH <sub>CP</sub> to Q          |                       | 23   | 40   |            | 50   |             | 60   | ns  | 4.5  | Fig.7                  |           |
| t <sub>PHL</sub>                    | propagation delay<br>MR to Q                        |                       | 28   | 49   |            | 61   |             | 74   | ns  | 4.5  | Fig.8                  |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>ST <sub>CP</sub> to Q          |                       | 33   | 57   |            | 71   |             | 86   | ns  | 4.5  | Fig.7                  |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>PL to Q                        |                       | 30   | 52   |            | 65   |             | 78   | ns  | 4.5  | Fig.9                  |           |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time                              |                       | 7    | 15   |            | 19   |             | 22   | ns  | 4.5  | Fig.9                  |           |
| t <sub>W</sub>                      | SH <sub>CP</sub> pulse width<br>HIGH or LOW         | 16                    | 7    |      | 20         |      | 24          |      | ns  | 4.5  | Fig.7                  |           |
| t <sub>W</sub>                      | ST <sub>CP</sub> pulse width<br>HIGH or LOW         | 16                    | 6    |      | 20         |      | 24          |      | ns  | 4.5  | Fig.7                  |           |
| t <sub>W</sub>                      | MR pulse width<br>LOW                               | 25                    | 14   |      | 31         |      | 38          |      | ns  | 4.5  | Fig.8                  |           |
| t <sub>W</sub>                      | PL pulse width<br>LOW                               | 20                    | 10   |      | 25         |      | 30          |      | ns  | 4.5  | Fig.9                  |           |
| t <sub>rem</sub>                    | removal time<br>MR to SH <sub>CP</sub>              | 12                    | −2   |      | 15         |      | 18          |      | ns  | 4.5  | Fig.10                 |           |
| t <sub>su</sub>                     | set-up time<br>D <sub>n</sub> to ST <sub>CP</sub>   | 12                    | 5    |      | 15         |      | 18          |      | ns  | 4.5  | Fig.11                 |           |
| t <sub>su</sub>                     | set-up time<br>D <sub>S</sub> to SH <sub>CP</sub>   | 12                    | 2    |      | 15         |      | 18          |      | ns  | 4.5  | Fig.11                 |           |
| t <sub>su</sub>                     | set-up time<br>PL to SH <sub>CP</sub>               | 12                    | 4    |      | 15         |      | 18          |      | ns  | 4.5  | Fig.12                 |           |
| t <sub>h</sub>                      | hold time<br>D <sub>n</sub> to ST <sub>CP</sub>     | 5                     | −1   |      | 5          |      | 5           |      | ns  | 4.5  | Fig.11                 |           |
| t <sub>h</sub>                      | hold time<br>PL, D <sub>S</sub> to SH <sub>CP</sub> | 5                     | −2   |      | 5          |      | 5           |      | ns  | 4.5  | Fig.11                 |           |
| f <sub>max</sub>                    | maximum pulse frequency<br>SH <sub>CP</sub>         | 30                    | 75   |      | 24         |      | 20          |      | MHz | 4.5  | Fig.7                  |           |

## 8-bit shift register with input flip-flops

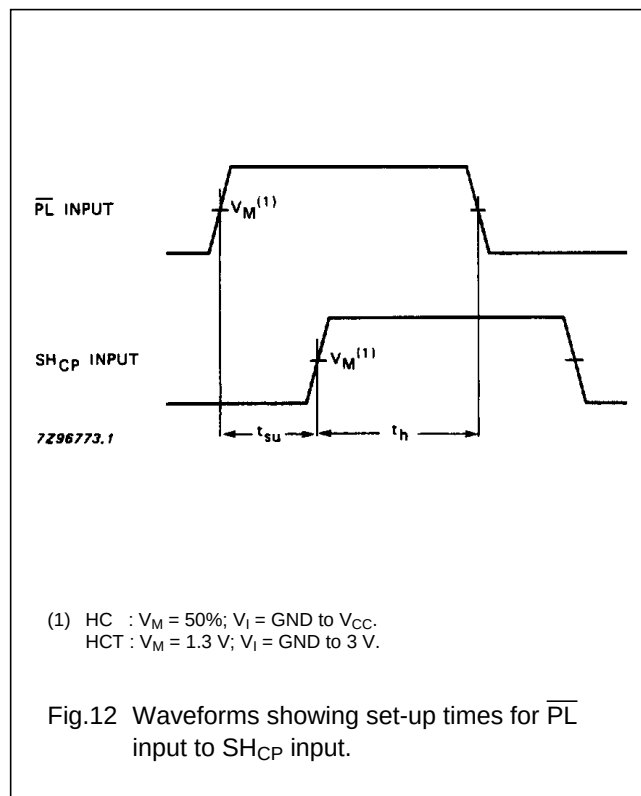
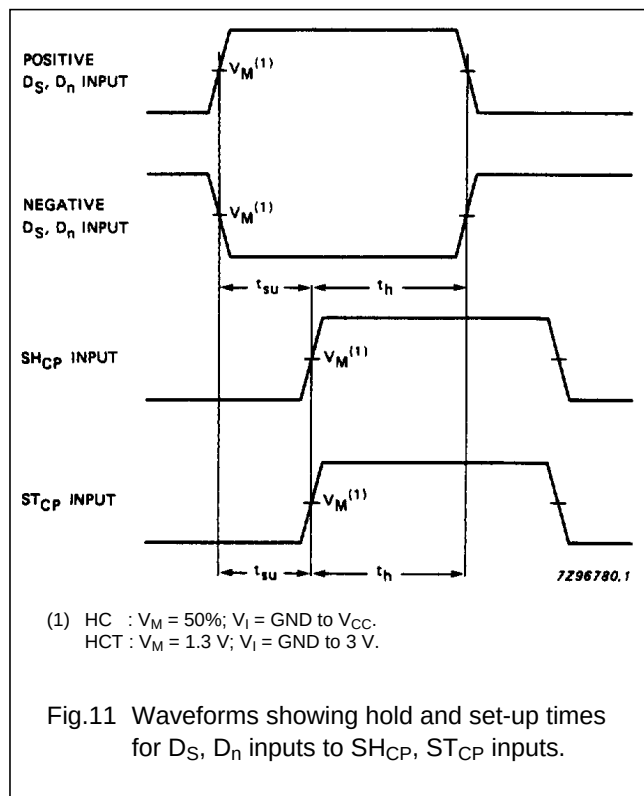
## 74HC/HCT597

## AC WAVEFORMS



## 8-bit shift register with input flip-flops

## 74HC/HCT597



## PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".