

N-Channel Enhancement-Mode MOS Transistor

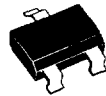
PRODUCT SUMMARY

| | | |
|----------------------|------------------------------|--------------|
| $V_{(BR)DSS}$ (V) | $r_{DS(ON)}$ (Ω) | I_D (A) |
| 60 | 7.5 | 0.115 |

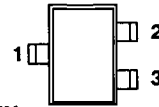
Performance Curves: VNDS06

| PRODUCT MARKING | |
|-----------------|-----|
| 2N7002 | 702 |

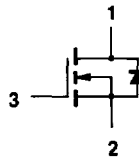
SOT-23



TOP VIEW



1 DRAIN
2 SOURCE
3 GATE



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

| PARAMETERS/TEST CONDITIONS | | SYMBOL | LIMITS | UNITS |
|--|---------------------------|-----------|-------------|-------|
| Drain-Source Voltage | | V_{DS} | 60 | V |
| Gate-Source Voltage | | V_{GS} | ± 40 | |
| Continuous Drain Current | $T_A = 25^\circ\text{C}$ | I_D | ± 0.115 | A |
| | $T_A = 100^\circ\text{C}$ | | ± 0.073 | |
| Pulsed Drain Current ¹ | | I_{DM} | 0.8 | |
| Power Dissipation | $T_A = 25^\circ\text{C}$ | P_D | 200 | mW |
| | $T_A = 100^\circ\text{C}$ | | 80 | |
| Operating Junction Temperature Range | | T_J | -55 to 150 | °C |
| Storage Temperature Range | | T_{stg} | -55 to 150 | |
| Lead Temperature ($1/16''$ from case for 10 sec.) | | T_L | 300 | |

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THERMAL RESISTANCE RATINGS

| THERMAL RESISTANCE | SYMBOL | LIMITS | UNITS |
|---------------------|------------|--------|-------|
| Junction-to-Ambient | R_{thJA} | 625 | K/W |

¹Pulse width limited by maximum junction temperature

| SPECIFICATIONS* | | | LIMITS | | | |
|--|---------------|---|------------------|-----|-----------|----------|
| PARAMETER | SYMBOL | TEST CONDITIONS | TYP ^b | MIN | MAX | UNIT |
| STATIC | | | | | | |
| Drain-Source Breakdown Voltage | $V_{(BR)DSS}$ | $I_D = 10 \mu A, V_{GS} = 0 V$ | 70 | 60 | | V |
| Gate-Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 0.25 mA$ | 2.15 | 1 | 2.5 | |
| Gate-Body Leakage | I_{GSS} | $V_{GS} = \pm 20 V, V_{DS} = 0 V$ | | | ± 100 | nA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 60 V, V_{GS} = 0 V$ $T_C = 125^\circ C$ | | | 1 500 | μA |
| On-State Drain Current ^c | $I_{D(ON)}$ | $V_{DS} \geq 2 V_{DS(ON)}, V_{GS} = 10 V$ | 1000 | 500 | | mA |
| Drain-Source On-Resistance ^c | $r_{DS(ON)}$ | $V_{GS} = 5 V, I_D = 50 mA$ $T_C = 125^\circ C$ | 5 | | 7.5 | Ω |
| | | $V_{GS} = 10 V, I_D = 0.5 A$ $T_C = 125^\circ C$ | 2.5 | | 7.5 | |
| | | $V_{GS} = 10 V, I_D = 0.5 A$ $T_C = 125^\circ C$ | 4.4 | | 13.5 | |
| Drain-Source On-Voltage ^c | $V_{DS(ON)}$ | $V_{GS} = 5 V, I_D = 50 mA$ | 0.25 | | 0.375 | V |
| | | $V_{GS} = 10 V, I_D = 0.5 A$ | 1.25 | | 3.75 | |
| | | $V_{GS} = 10 V, I_D = 0.5 A$ $T_C = 125^\circ C^d$ | 2.2 | | 6.75 | |
| Forward Transconductance ^c | g_{fs} | $V_{DS} = 10 V, I_D = 0.2 A$ | 170 | 80 | | mS |
| Common Source Output Conductance ^{c, d} | g_{os} | $V_{DS} = 5 V, I_D = 50 mA$ | 500 | | | μS |
| DYNAMIC | | | | | | |
| Input Capacitance | C_{iss} | $V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz$ | 16 | | 50 | pF |
| Output Capacitance ^d | C_{oss} | | 11 | | 25 | |
| Reverse Transfer Capacitance | C_{rss} | | 2 | | 5 | |
| SWITCHING | | | | | | |
| Turn-On Time | t_{ON} | $V_{DD} = 30 V, R_L = 150 \Omega, I_D = 0.2 A$ $V_{GEN} = 10 V, R_G = 25 \Omega$ | 7 | | 20 | nS |
| Turn-Off Time | t_{OFF} | (Switching time is essentially independent of operating temperature) | 7 | | 20 | |

NOTES:

- a. $T_C = 25^\circ C$ unless otherwise noted.
- b. For design aid only, not subject to production testing.
- c. Pulse test; $PW = \leq 80 \mu S$, duty cycle $\leq 1\%$.
- d. This parameter not registered with JEDEC.