TEMIC
Semiconductors

U4082B

Low-Voltage Voice-Switched IC for Hands-Free Operation

Description

The low-voltage voice-switched speakerphone circuit, U4082B, incorporates the wide range of functions listed below. Versatility of the device is further enhanced by giving access to internal circuit points. The block diagram (figure 1) shows amplifiers, level detectors, transmit and receive attenuators operating in complementary functions, background noise monitors, chip disable, dial tone detector and mute function. Due to low-voltage operation, it can be operated either by a low supply or via a telephone line requiring 5.5 mA typically. Also featured is stand-alone operation through a coupling transformer (Tip and Ring) or in conjunction with a handset speech network, as shown in figure 2.

Features

- Low-voltage operation: 3 to 6.5 V

- Attenuator gain range between transmit and receive: 52 dB

- Four point signal sensing for improved sensitivity

- Monitoring system for background-noise level

- Microphone amplifier gain adjustable

- Mute function

- Chip disable for active/standby operation

- On-board filter

- Dial tone detector

- Compatible with U4083B speaker amplifier

Benefits

- Fast channel switching allows quasi duplex operation
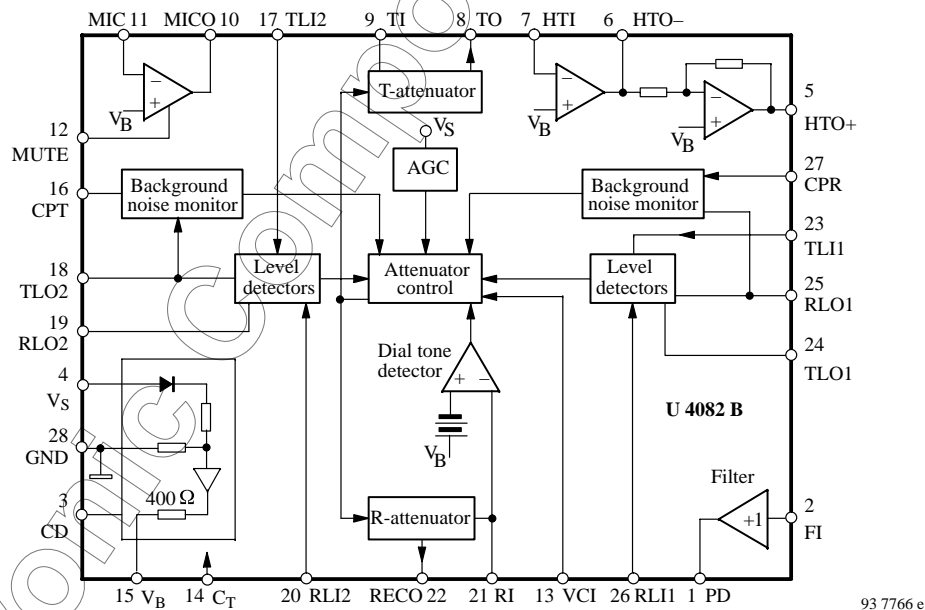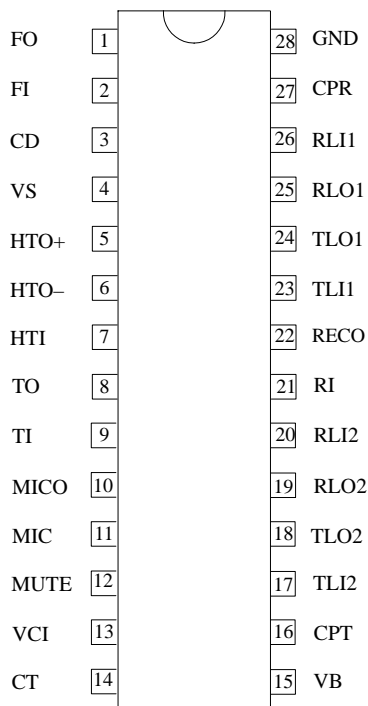
- Proper operation in noisy surrounding

Figure 1. Block diagram

Ordering Information

Extended Type Number	Package	Remarks
U4082B–A	DIP28	
U4082B–AFL	SO28	

U4082B

Figure 2. Block diagram with external circuit

Pin Description

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         ┌──────────┐
   FO  1 │          │ 28  GND
   FI  2 │          │ 27  CPR
   CD  3 │          │ 26  RLI1
   VS  4 │          │ 25  RLO1
  HTO+ 5 │          │ 24  TLO1
  HTO− 6 │          │ 23  TLI1
   HTI 7 │          │ 22  RECO
   TO  8 │          │ 21  RI
   TI  9 │          │ 20  RLI2
  MICO 10│          │ 19  RLO2
   MIC 11│          │ 18  TLO2
  MUTE 12│          │ 17  TLI2
   VCI 13│          │ 16  CPT
   CT  14│          │ 15  VB
         └──────────┘
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Pin	Symbol	Function
1	FO	Filter output. Output impedance is less than 50 Ω.
2	FI	Filter input. Input impedance is greater than 1 MΩ.
3	CD	Chip disable. A logic low (< 0.8 V) sets normal operation. A logic high (> 2 V) disables the IC to conserve power. Input impedance is nominally 90 kΩ.
4	V_S	Supply voltage 2.8 to 6.5 V, approximately 5 mA. AGC circuit reduces the receive attenuator gain @ 25 dB − Receive mode at 2.8 V.
5	HTO+	Output of the second hybrid amplifier. − Hybrid output. Gain is internally set at −1 to provide a differential output, (in conjunction with HTO−) to the hybrid transformer.
6	HTO−	Output of the first hybrid amplifier. Hybrid output. Gain is set by external resistors.
7	HTI	Input and summing node for the first hybrid amplifier. DC level is approximately V_B.
8	TO	Transmit attenuator output. DC level is approximately V_B.

Pin	Symbol	Function
9	TI	Transmit attenuator input. Maximum signal level is 350 mVrms. Input impedance is approximately 10 kΩ
10	MICO	Microphone amplifier output. Gain is set by external resistors.
11	MIC	Microphone amplifier input. Bias voltage is approximately V_B.
12	MUTE	Mute input. A logic low (< 0.8 V) sets normal operation. A logic high (> 2 V) mutes the microphone amplifier without affecting the rest of the circuit. Input impedance is nominally 90 kΩ.
13	VCI	Volume control input. When VCI = V_B, the receive attenuator is at maximum gain when in receive mode. When VCI = 0.3 V_B, the receive gain is down 35 dB. It does not affect the transmit mode.
14	C_T	Response time. An RC at this pin sets the response time for the circuit to switch modes.
15	V_B	Output voltage $\approx V_{S/2}$. It is a system ac ground and biases the volume control. A filter cap is required.
16	CPT	An RC at this pin sets the time constant for the transmit background monitor.
17	TLI2	Transmit level detector input on the microphone/speaker side.
18	TLO2	Transmit level detector output on the microphone/speaker side, and input to the transmit background monitor.
19	RLO2	Receive level detector output on the microphone/speaker side.
20	RLI2	Receive level detector input on the microphone/speaker side.
21	RI	Input receive attenuator and dial tone detector. Maximum input level is 350 mVrms. Input impedance is approximately 10 kΩ.
22	RECO	Receive attenuator output. DC level is approximately V_B.
23	TLI1	Transmit level detector input on the line side.
24	TLO1	Transmit level detector output on the line side.
25	RLO1	Receive level detector output on the line side and input to the receive background monitor.
26	RLI1	Receive level detector input on the line side.
27	CPR	An RC at this pin sets the time constant for the receive background monitor.
28	GND	Ground

Introduction

General

The fundamental difference between the operation of a speakerphone and a handset is that of half-duplex versus full duplex. The handset is full duplex since conversation can occur in both directions (transmit and receive) simultaneously. A speakerphone has higher gain levels in both paths, and attempting to converse full duplex results in oscillatory problems due to the loop that exists within the system. The loop is formed by the receive and transmit paths, the hybrid and the acoustic coupling (speaker to microphone).

The only practical and economical solution used to date is to design the speakerphone to function in a half duplex mode. That is, only one person speaks at a time, while the other listens. To achieve this, a circuit is required which can detect who is talking, switch on the appropriate path (transmit or receive), and switch off (attenuate) the other path. In this way, the loop gain is maintained less than unity. When the talkers exchange function, the circuit must quickly detect this, and switch the circuit appropriately. By providing speech level detectors, the circuit operates in a "hands-free" mode, eliminating the need for a "push-to-talk" switch.

The handset has the same loop as the speakerphone. Oscillations don't occur because the gains are considerably lower and the coupling from the earpiece to the mouthpiece is almost nonexistent (the receiver is normally held against a person's ear).

The U4082B provides the necessary level detectors, attenuators, and switching control for a properly operating speakerphone. The detection sensitivity and timing are externally controllable. Additionally, the U4082B provides background noise monitors (which make the circuit insensitive to room and line noise), hybrid amplifiers for interfacing to tip and ring, the microphone amplifier, and other associated functions.

For further explanation which is given below, please refer to figure 1

Transmit and Receive Attenuators TI, TO and RI, RECO

The attenuators are complementary in function, i.e., when one is at maximum gain (+6.0 dB), the other is at maximum attenuation (–46 dB), and vice versa. Neither

is ever fully on or off. The sum of their gains remains constant (within a nominal error band of ±0.1 dB) at a typical value of –40 dB (see figure 11). Their purpose is to control the transmit and receive paths to provide the half-duplex operation required in a speakerphone.

The attenuators are non-inverting, and have a –3.0 dB (from max. gain) frequency of approximately 100 kHz. The input impedance of each attenuator (TI and RI) is nominally 10 kΩ (see figure 3), and to prevent distortion, the input signal should be limited to 350 mVrms. Maximum recommended input signal is independent of the volume control setting. The diode clamp on the inputs limits the input swing, and therefore the maximum negative output swing. This is the reason V_{RECO} and V_{TOL} specification are defined as they are in the electrical characteristics. The output impedance is less than 10 Ω until the output current limit (typically 2.5 mA) is reached.
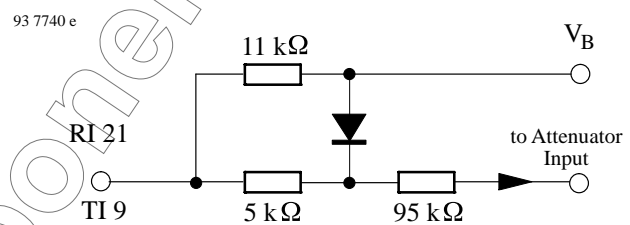
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Figure 3. Attenuator input stage

The attenuators are controlled by the single output of the control block, which is measurable at the C_T pin (Pin 14). When the C_T pin is at +240 mV w. r. t. V_B, the circuit is in the receive mode (receive attenuator is at +6.0 dB). When the C_T pin is at –240 mV w.r.t. V_B, the circuit is in the transmit mode (transmit attenuator is at +6.0 dB). The circuit is in an idle mode when the C_T voltage is equal to V_B causing the attenuators' gain to be halfway between their fully on and fully off positions (–20 dB each). Monitoring the C_T voltage (w.r.t. V_B) is the most direct method of monitoring the circuit's mode.

The attenuator control has seven inputs: two from the comparators operated by the level detectors, two from the background noise monitors, volume control, dial-tone detector, and AGC. They are described as follows:

Level Detectors

There are four level detectors, two on the receive side and two on the transmit side. As shown in figure 4, the terms in parentheses form one system, and the other terms form the second system. Each level detector is a high-gain amplifier with back-to-back diodes in the feedback path, resulting in nonlinear gain, which permits operation over a wide dynamic range of speech levels. Refer to the graphs of figures 12, 13 and 14 for their DC and ac transfer characteristics. The sensitivity of each level detector is determined by the external resistor and capacitor at each input (TLI1, TLI2, RLI1, and RLI2). Each output charges an external capacitor through a diode and limiting resistor, thus providing a DC representation of the input ac signal level. The outputs have a quick rise time (determined by the capacitor and an internal 350-Ω resistor) and a slow decay time set by an internal current source and the capacitor. The capacitors on the four outputs should have the same value ($\pm 10\%$) to prevent timing problems.

Referring to figure 2, on the receive side, one level detector (RLI1) is at the receive input receiving the same signal as at tip and ring, and the other (RLI2) is at the output of the speaker amplifier. On the transmit side, one level detector (TLI2) is at the output of the microphone amplifier, while the other (TLI1) is at the hybrid output. Outputs RLO1 and TLO1 feed a comparator. The output of the comparator goes to the attenuator control block.

Likewise, outputs RLO2 and TLO2 feed a second comparator which also goes to the attenuator control block. The truth table for the effects of the level detectors is given below in the attenuator control block section.

Background Noise Monitors

This circuit distinguishes speech (which consists of bursts) from background noise (a relatively constant signal level). There are two background noise monitors – one for the receive path and the other for the transmit path. The receive background noise monitor is operated on by the RLI1-RLO1 level detector, while the transmit background noise monitor is operated on by the TLI2-TLO2 level detector (see figure 4).

They monitor the background noise by storing a DC voltage representative of the respective noise levels in capacitors at CPR and CPT. The voltages at these pins have slow rise times (determined by the external RC), but fast decay times. If the signal at RLI1 (or TLI2) changes slowly, the voltage at CPR (or CPT) will remain more positive than the voltage at the non-inverting input of the monitor's output comparator. When speech is present, the voltage on the non-inverting input of the comparator will rise quicker than the voltage at the inverting input (due to the burst characteristic of speech), causing its output to change. This output is sensed by the attenuator control block.
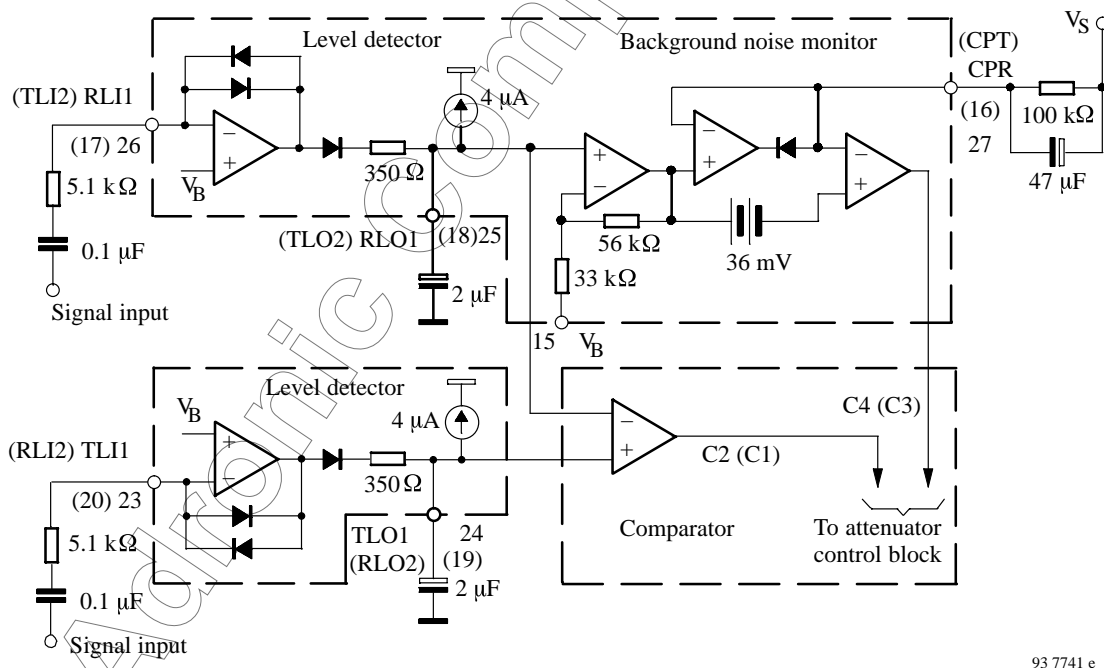

Figure 4. Level detectors

The 36-mV offset at the comparator's input keeps the comparator from changing state unless the speech level exceeds the background noise by approximately 4.0 dB. The time constant of the external RC (approximately 4.7 seconds) determines the response time to background noise variations.

Volume Control

The volume control input at VCI (Pin 13) is sensed as a voltage w. r. t. V_B. It affects the attenuators only in receive mode and has no effect in idle or transmit modes.

In receive mode, the attenuator receive gain, G_R, is +6.0 dB, and attenuator transmit gain G_T is – 46 dB under the condition that VCI = V_B. When VCI < V_B, the attenuator receive gain is reduced (figure 15), whereas the attenuator transmit gain is increased, their sum, however, remains constant. Voltage deviation at VCI changes the voltage at C_T, which in turn controls the attenuators (see attenuator control block).

The volume control setting does not affect the maximum attenuator input signal at which noticeable distortion occurs.

The bias current at VCI is typically – 60 nA. It does not vary significantly with the VCI voltage or supply voltage V_S.

Dial Tone Detector

The dial tone detector is a comparator with one side connected to the receive input (RI) and the other to V_B with a 15 mV offset (see figure 5). If the circuit is in idle mode, and the incoming signal is greater than 15 mV (10 mV$_{rms}$), the comparator's output will change, disabling the receive idle mode. The receive attenuator will then be at a setting determined mainly by the volume control.

This circuit prevents the dial tone (which would be considered as continuous noise) from fading away as the circuit would have the tendency to switch to idle mode. By disabling receive idle mode, the dial tone remains at the normally expected full level.
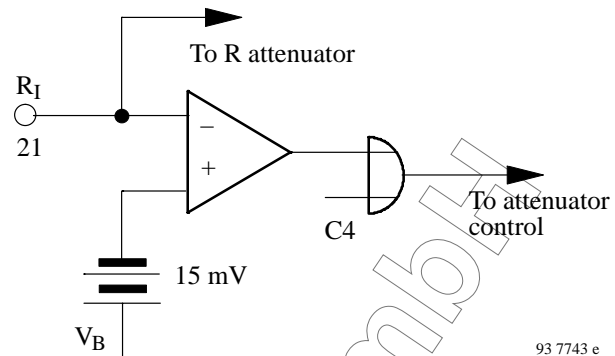

Figure 5. Dial tone detector

AGC

The AGC circuit affects the circuit only in receive mode, and only when the supply voltage is less than 3.5 V. As V_S < 3.5 V, the gain of the receive attenuator is reduced according to figure 16. The transmit path attenuation changes such that the sum of the transmit and receive gains remains constant.

The purpose of this feature is to reduce the power (and current) used by the speaker when a line-powered speakerphone is connected to a long line where the available power is limited. By reducing the speaker power, the voltage sag at V_S is controlled, preventing possible erratic operation.

Attenuator Control Block

The attenuator control block has seven inputs:

● The output of the comparator operated by RLO2 and TLO2 (microphone/speaker side) – designated C1.

● The output of the comparator operated by RLO1 and TLO1 (Tip/Ring side) – designated C2.

● The output of the transmit background noise monitor – designated C3.

● The output of the receive background noise monitor – designated C4.

● The volume control.

● The dial tone detector.

● The AGC circuit.

The single output of the control block controls the two attenuators. The effect of C1-C4 is as follows:

Inputs				Output
C1	C2	C3	C4	Mode
T	T	1	X	Transmit
T	R	Y	Y	Fast Idle
R	T	Y	Y	Fast Idle
R	R	X	1	Receive
T	T	0	X	Slow Idle
T	R	0	0	Slow Idle
R	T	0	0	Slow Idle
R	R	X	0	Slow Idle

X = Don't Care; Y = C3 and C4 are not both 0.

Term definitions

1. "Transmit" means the transmit attenuator is fully on ($+6.0$ dB), and the receive attenuator is at maximum attenuation (-46 dB).

2. "Receive" means both attenuators are controlled by the volume control. At maximum volume, the receive attenuator is fully on ($+6.0$ dB), and the transmit attenuator is at maximum attenuation (-46 dB).

3. "Fast Idle" means both transmit and receive speech are present in approximately equal levels. The attenuators are quickly switched (30 ms) to idle until one speech level dominates the other.

4. "Slow Idle" means speech has ceased in both transmit and receive paths. The attenuators are then slowly switched (1 second) to idle mode.

5. Switching to full transmit or receive modes from any other mode is at the fast rate (≈ 30 ms).

Summary of the truth table

1. The circuit will switch to transmit if

a) both transmit level detectors sense higher signal levels relative to the respective receive level detectors (TLI1 versus RLI1, TLI2 versus RLI2), and

b) the transmit background noise monitor indicates the presence of speech.

2. The circuit will switch to receive if

a) both receive level detectors sense higher signal levels relative to the respective transmit level detectors, and

b) the receive background noise monitor indicates the presence of speech.

3. The circuit will switch to fast idle mode if the level detectors disagree on the relative strengths of the signal levels, and at least one of the background noise monitors indicates speech. For example, referring to the block diagram (figure 2), if there is a sufficient signal at the microphone amp output (TLI2) to override the speaker signal (RLI2) and there is sufficient signal at the receive input (RLI1) to override the signal at the hybrid output (TLI1), and either or both background monitors indicate speech, then the circuit will be in fast idle mode.

Two conditions which can cause fast idle mode:

a) when both talkers are attempting to gain control of the system by talking at the same time, and

b) when one talker is in a very noisy environment, forcing the other talker to continually override that noise level. In general, fast idle mode will occur infrequently.

4. The circuit will switch to slow idle mode when

a) both talkers are quiet (no speech present), or

b) when one talker's speech level is continuously overridden by noise at the other speaker's location.

The time required to switch the circuit between transmit, receive, fast idle and slow idle is determined in part by the components at Pin 14. (See the section on switching times for a more complete explanation of the switching time components.) A diagram of the C_T circuitry is shown in figure 6, and operates as follows:
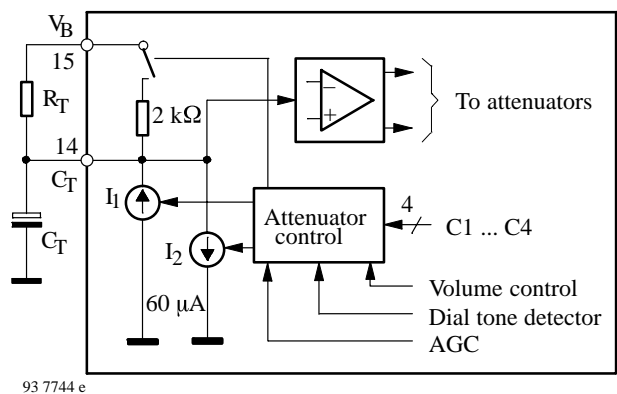

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Figure 6. C_T Attenuator control block circuit

– R_T is typically 120 kΩ, and C_T is typically 5.0 μF.

– To switch to receive mode, I_1 is turned on (I_2 is off), charging the external capacitor to $+240$ mV above V_B. (An internal clamp prevents further charging of the capacitor.)

– To switch to transmit mode, I_2 is turned on (I_1 is off) bringing down the voltage on the capacitor to -240 mV with respect to V_B.

– To switch to idle quickly (fast idle), the current sources are turned off, and the internal 2-kΩ resistor is switched on, discharging the capacitor to V_B with a time constant of 2 k$\Omega \times C_T$.

– To switch to idle slowly (slow idle), the current sources are turned off, the switch at the 2-kΩ resistor is open, and the capacitor discharges to V_B through the external resistor, R_T, with a time constant of $= R_T \times C_T$.

Microphone Amplifier

The microphone amplifier (Pins 10, 11) has the non-inverting input internally connected to V_B, while the inverting input and the output are pinned out.

Unlike most op amps, the amplifier has an all-NPN output stage which maximizes phase margin and gain bandwidth. This feature ensures stability at gains less than unity, as well with a wide range of reactive loads.

The open loop gain is typically 80 dB (f < 100 Hz), and the gain-bandwidth is typically 1.0 MHz (see figure 17). The maximum p-p output swing is typ. ($V_S - 1$ V) with an output impedance of < 10 Ω until current limiting is reached (typically 1.5 mA). Input bias current at MIC is typically -40 nA.
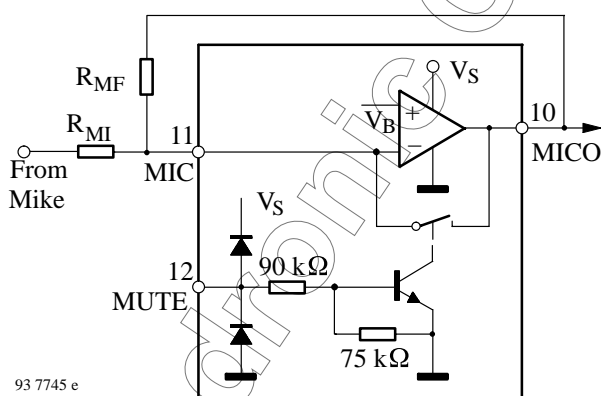

Figure 7. Microphone amplifier and mute

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The muting function (Pin 12), when activated, will reduce the gain of the amplifier to approximately -39dB (with RMI = 5.1 kΩ) by shorting the output to the inverting input (see figure 7). The mute input has a threshold of approximately 1.5 V, and the voltage at this pin must be kept within the range of ground and V_S (see figure 17). If the mute function is not used, the pin should be grounded.

Hybrid Amplifiers

The two hybrid amplifiers (at HTO+, HTO−, and HTI), in conjunction with an external transformer, provide the two-to-four-wire converter for interfacing to the telephone line. The gain of the first amplifier (HTI to HTO−) is set by external resistors (gain = $-R_{HF}/R_{HI}$ in figure 2), and its output drives the second amplifier, the gain of which is internally set at -1.0. Unlike most op amps, the amplifiers have an all-NPN output stage, which maximizes phase margin and gain bandwidth. This feature ensures stability at gains less than unity, as well as with a wide range of reactive loads. The open-loop gain of the first amplifier is typically 80 dB, and the gain bandwidth of each amplifier is approximately 1.0 MHz (see figure 17). The maximum output swing (p-p) of each amplifier is typically 1.2 V less than V_S with an output impedance of < 10 Ω until current limiting is reached (typically 8.0 mA). The output current capability is guaranteed to be a minimum of 5.0 mA. The bias current at HTI is typically -30 nA.

The connections to the coupling transformer are shown in figure 1. Balancing network is necessary to match the line impedance.

Filter

The operation of the filter circuit is determined by the external components. The circuit within the U4082B from pins FI to FO is a buffer with a high input impedance (> 1 MΩ) and a low output impedance (< 50 Ω). The configuration of the external components determines whether the circuit is a high-pass filter (as shown in figure 2), a low-pass filter, or a band-pass filter.

As a high-pass filter, with the components shown in figure 8, the filter will keep out the 60-Hz (and 120-Hz) hum which can be picked up by the external telephone lines.

As a low-pass filter (figure 9), it can be used to roll off the high-end frequencies in the receive circuit, which aids in protecting against acoustic feedback problems.

With an appropriate choice of an input coupling capacitor to the low-pass filter, a band-pass filter is formed.
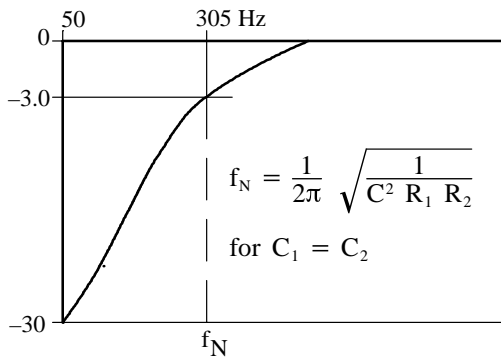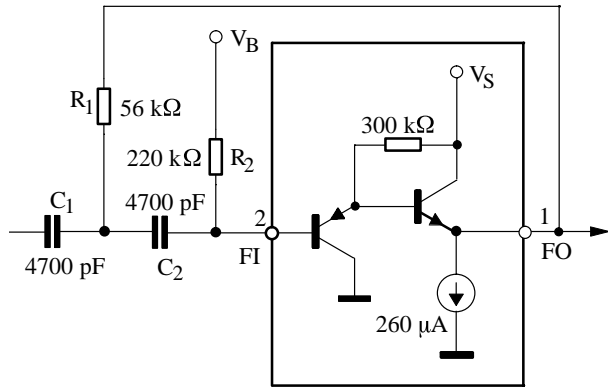
$$f_N = \frac{1}{2\pi} \sqrt{\frac{1}{C^2 \, R_1 \, R_2}}$$

for $C_1 = C_2$

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Figure 8. High-pass filter

$$f_N = \frac{1}{2\pi} \sqrt{\frac{1}{C_1 \, C_2 \, R^2}}$$
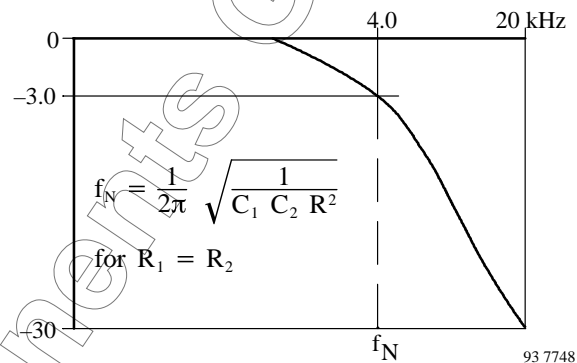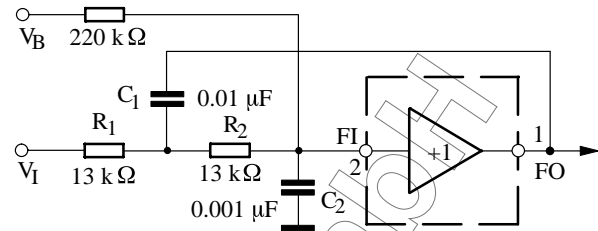
for $R_1 = R_2$

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Figure 9. Low-pass filter

Power Supply, V_B, and Chip Disable

The power supply voltage at Pin 4 (V_S) is between 3.5 and 6.5 V for normal operation, but reduced operation is possible down to 2.8 V (see figure 16 and the AGC section). The power supply current is shown in figure 19 for both power-up and power-down mode.

The output voltage at V_B (Pin 15) is approx. ($V_S - 0.7$)/2, and provides the ac ground for the system. The output impedance at V_B is approximately 400 Ω (see figure 20), and in conjunction with the external capacitor at V_B, forms a low-pass filter for power supply rejection. Figure 21 gives an indication of the amount of rejection with different capacitors. The capacitor value depends on whether the circuit is powered by the telephone line or a power supply.

Since V_B biases the microphone and hybrid amplifiers, the amount of supply rejection at their outputs is directly related to the rejection at V_B, as well as their respective gains. Figure 22 depicts this graphically.

The chip disable (Pin 3) permits powering down the IC to conserve power and/or for muting purposes. With CD < 0.8 volts, normal operation is in effect.

With CD > 2.0 volts and < V_S, the IC is powered down. In powered-down mode, the microphone and the hybrid amplifiers are disabled, and their outputs reach high-impedance state. Additionally, the bias is removed from the level detectors.

The bias is not removed from the filter (Pins 1 and 2), the attenuators (Pins 8, 9, 21 and 22), or from Pins 13, 14, and 15 (the attenuators are disabled, however, and will not pass a signal). The input impedance at CD is typically 90 kΩ, has a threshold of approximately 1.5 V, and the voltage at this pin must be kept within the range of ground and V_S (see figure 18). If CD is not used, the pin should be grounded.

U4082B

Absolute Maximum Ratings

Reference point Pin 28, $T_{amb} = 25°C$, unless otherwise specified.

Parameters		Symbol	Value	Unit
Supply voltage	Pin 4	V_S	-1.0 to $+7.0$	V
Voltages	Pin 3, 12		-1.0 to $(V_S + 1.0)$	
	Pin 13		-1.0 to $(V_S + 0.5)$	V
	Pin 2, 9, 21		-0.5 to $(V_S + 0.5)$	
Storage temperature range		T_{stg}	-55 to $+150$	°C
Junction temperature		T_j	125	°C
Ambient temperature range		T_{amb}	-20 to $+60$	°C
Power dissipation $T_{amb} = 60°C$	DIP28	P_{tot}	1.3	W
	SO28	P_{tot}	520	mW
Maximum thermal resistance Junction ambient	DIP28	R_{thJA}	50	K/W
	SO28	R_{thJA}	120	K/W

Operation Recommendation

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Pin 4	V_S	3.5	–	6.5	V
CD input MUTE input	Pin 3 Pin 12		0	–	V_S	V
Output current	Pin 15	I_B	–	–	500	μA
Volume control input	Pin 13	VCI	$0.3 \times V_B$	–	V_B	V
Attenuator input signal voltage	Pins 9, 21		0	–	350	mV_{rms}
Microphone amplifier, hybrid amplifier gain			0	–	40	dB
Load current	@ RECO, TO		0	–	± 2.0	
	Pins 8, 22		0	–	± 1.0	mA
	@ MICO Pin 10		0	–	± 5.0	
	@ HTO$-$, HTO$+$ Pins 6, 5					
Ambient temperature range		T_{amb}	-20	–	$+60$	°C

Electrical Characteristics

$T_{amb} = +25°C$, $V_S = 5.0$ V, CD ≤ 0.8 V, unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Power supply						
Supply current	$V_S = 6.5$ V, CD = 0.8 V	I_S		5.5	8.0	mA
	$V_S = 6.5$ V, CD = 2.0 V			600.0	800.0	μA
CD input resistance	$V_S = V_{CD} = 6.5$ V	R_{CD}	50.0	90.0		kΩ
CD input voltage	– High	V_{CDH}	2.0		V_S	V
	– Low	V_{CDL}	0.0		0.8	
Output voltage	$V_S = 3.5$ V	V_B		1.3		V
	$V_S = 5.0$ V		1.8	2.1	2.4	
Output resistance	$I_{VB} = 1$ mA	R_{OVB}		400.0		Ω
Power supply rejection ratio	$C_{VB} = 220$ μF, f = 1 kHz	PSRR		54.0		dB
Attenuators						
Receive attenuator gain	f = 1.0 kHz, $V_{CI} = V_B$ R mode, RI = 150 mVrms ($V_S = 5.0$ V) ($V_S = 3.5$ V)	G_R	+4.0	+6.0	+8.0	dB
Gain change	$V_S = 3.5$ V versus $V_S = 5.0$ V	ΔG_{R1}	–0.5	0.0	+0.5	
AGC gain change	$-V_S = 2.8$ V versus $V_S = 5.0$ V	ΔG_{R2}		–25.0	–15.0	
Idle mode	RI = 150 mVrms	G_{RI}	–22.0	–20.0	–17.0	dB
Range R to T mode		ΔG_{R3}	49.0	52.0	54.0	
Volume control range	R Mode, $0.3 V_B < V_{CI} < V_B$	V_{CR}	27.0	35.0		dB
RECO DC voltage	R mode	V_{RECO}		V_B		V
RECO DC voltage	R to T mode	ΔV_{RECO}		±10	±150.0	mV
RECO high voltage	$I_O = -1$ mA $RI = V_B + 1.5$ V	V_{RECOH}	3.7			V
RECO low voltage	$I_O = 1$ mA, $RI = V_B -1$ V, output measured w. r. t. V_B	V_{RECOL}		–1.5	–1.0	V
RI input resistance	RI < 350 mVrms	R_{RI}	7.0	10.0	14.0	kΩ
Transmit attenuator gain	f = 1 kHz T mode, TI = 150 mVrms Idle mode, TI = 150 mVrms Range T to R mode	G_T G_{TI} G_{TI}	+4.0 –22.0 49.0	+6.0 –20.0 52.0	+8.0 –17.0 54.0	dB
TO DC voltage	T Mode	V_{TO}		V_B		V
TO DC voltage	T to R Mode	V_{TO}		±100	±150.0	mV
TO high voltage	$I_O = -1.0$ mA $TI = V_B + 1.5$ V	V_{TOH}	3.7			V
TO low voltage	$I_O = +1.0$ mA $TI = V_B - 1.0$ V, output measured w. r. t. V_B	V_{TOL}		–1.5	–1.0	V
TI input resistance	TI < 350 mVrms	R_{TI}	7.0	10.0	14.0	kΩ
Gain tracking	$G_R + G_T$, @ T, Idle, R	G_{TR}		±0.1		dB

Electrical Characteristics (continued)

$T_{amb} = +25°C$, $V_S = 5.0$ V, CD $\leq$ 0.8 V, unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Attenuator control						
C_T voltage	Pin 14 – V_B R mode, $V_{CI} = V_B$ Idle mode T mode	V_{CT}		+240.0 0.0 −240.0		mV
C_T source current	R mode	I_{CTR}	−85.0	−60.0	−40.0	µA
C_T sink current	T mode	I_{CTT}	+40.0	+60.0	+85.0	µA
C_T slow idle current		I_{CTS}		0.0		µA
C_T fast idle internal resistance		R_{FI}	1.5	2.0	3.6	kΩ
VCI input current		I_{VCI}		−60.0		nA
Dial tone detector threshold		V_{DT}	10.0	15.0	20.0	mV
Microphone amplifier $V_{MUTE} < 0.8$ V, $G_{VCL} = 31$dB						
Output offset	$V_{MICO} - V_B$, Feedback R = 180 kΩ	MICO V_{OS}	−50.0	0.0	+50.0	mV
Open loop gain	f < 100 Hz	G_{VOLM}	70.0	80.0		dB
Gain bandwidth		GBW_M		1.0		MHz
Output high voltage	$I_O = -1.0$ mA, $V_S = 5.0$ V	V_{MICOH}	3.7			V
Output low voltage	$I_O = +1.0$ mA	V_{MICOL}			200.0	mV
Input bias current (MIC)		I_{BM}		−40.0		nA
Muting (Δ gain)	f = 1 kHz, $V_{MUTE} = 2.0$ V 300 Hz < f < 10 kHz	G G	−55.0	−68.0		dB dB
MUTE input resistance	$V_S = V_{MUTE} = 6.5$ V	R_{MUTE}	50.0	90.0		kΩ
MUTE input high		V_{MUTEH}	2.0		V_S	V
MUTE input low		V_{MUTEL}	0.0		0.8	V
Distortion	300 Hz < f < 10 kHz	THD_M		0.15		%
Hybrid amplifiers						
HTO-Offset	$V_{HTO} - V_B$, Feedback R = 51 kΩ	H_{VOS}	−20.0	0.0	+20.0	mV
HTO to HTO+ Offset	Feedback R = 51 kΩ	HB_{VOS}	−30.0	0.0	+30.0	mV
Open loop gain	HTI to HTO−, f < 100 Hz	G_{VOLH}	60.0	80.0		dB
Gain bandwidth		GB		1.0		MHz
Closed loop gain	HTO− to HTO+	G_{VCLH}	−0.35	0.0	+0.35	dB
Input bias current	@ HTI	I_{BH}		−30.0		nA
HTO high voltage	$I_O = -5.0$ mA	$V_{HT}H$	3.7			V
HTO low voltage	$I_O = +5.0$ mA	$V_{HT}L$			250.0	mV
HTO+ high voltage	$I_O = -5.0$ mA	$V_{HT}H$	3.7			V
HTO+ low voltage	$I_O = +5.0$ mA	$V_{HT}L$			450.0	mV
Distortion	300 Hz < f < 10 kHz, (see figure 10)	d		0.3		%

Electrical Characteristics (continued)

$T_{amb} = +25°C$, $V_S = 5.0$ V, CD ≤ 0.8 V, unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Level detectors and background noise monitors						
Transmit receive switching threshold	Current ratio from T to R at RLI1 + RLI2 to 20 µA at TLI1 + TLI2 to switch	I_{TH}	0.8	1.0	1.2	
Source current	RLO1, RLO2, TLO1, TLO2	I_{LSO}		−2.0		mA
Sink current	RLO1, RLO2, TLO1, TLO2	I_{LSK}		4.0		µA
CPR, CPT output resistance	$I_O = 1.2$ mA	R_{CP}		35		Ω
CPR, CPT leakage current		I_{CPLK}		−0.2		µA
Filter						
Voltage offset at FO	$V_{FO} − V_B$, 220 kΩ from V_B to FI	FO_{VOS}	−200.0	−90	0.0	mV
FO sink current		I_{FO}	150.0	260	400.0	µA
FI bias current		I_{FI}		−50.0		nA
System distortion						
R Mode	from FI to RECO, FO connected to RI	d_R		0.5	3.0	%
T Mode	from MIC to HTO−/HTO+, includes T attenuator	d_T		0.8	3.0	%
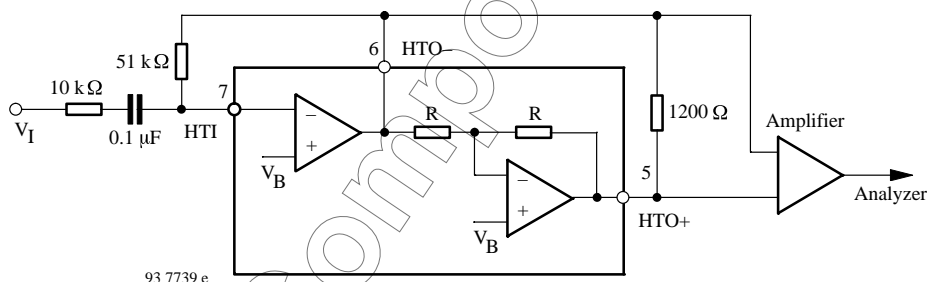
Figure 10. Hybrid amplifier distortion test

Temperature Characteristics

| Parameter	Typical Value @ 25°C	Typical Change −20 to +60°C
Supply current, CD = 0.8 V I_S	5.0 mA	−0.3 %/°C
Supply current, CD = 2.0 V I_S	400.0 µA	−0.4 %/°C
V_B output voltage, $V_S = 5.0$ V V_O	2.1 V	+0.8 %/°C
Attenuator gain (max. gain)	+6.0 dB	0.0008 dB/°C
Attenuator gain (max. attenuation)	−46.0 dB	0.004 dB/°C
Attenuator input resistance (@ TI, RI)	10.0 kΩ	+0.6 %/°C
Dial tone detector threshold	15.0 mV	+20.0 µV/°C
CT source, sink current	±60.0 µA	−0.15 %/°C
Microphone, hybrid amplifier offset	0.0 mV	±4.0 µV/°C
Transmit receive switching threshold	1.0	±0.02 %/°C
Sink current at RLO1, RLO2, TLO1, TLO2	4.0 µA	−10.0 nA/°C
Closed loop gain (HTO− to HTO+)	0.0 dB	0.001 %/°C
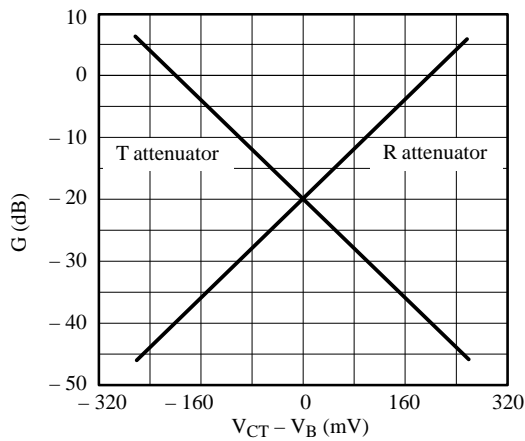
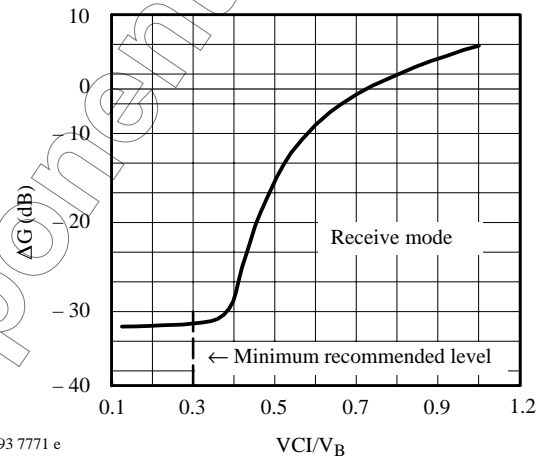Figure 11. Attenuator gain versus VCT (Pin 14)
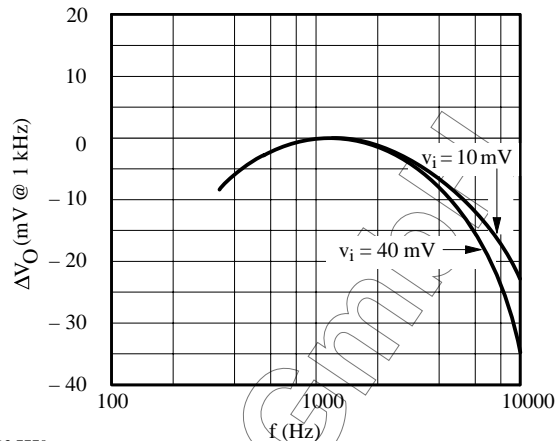
93 7767 e

Figure 14. Level detector AC transfer characteristics versus frequency
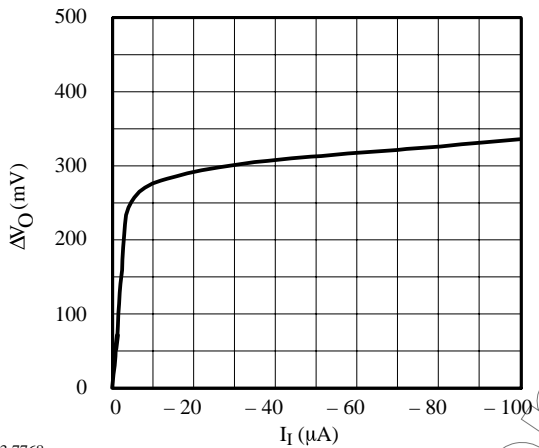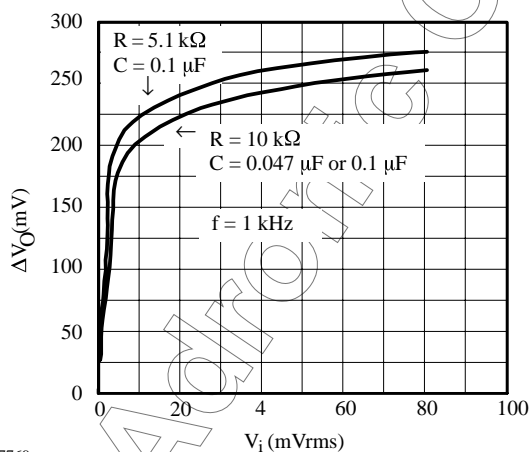
93 7770 e
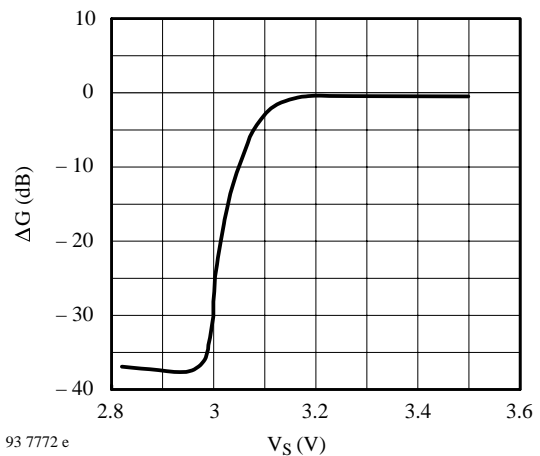
Figure 12. Level detector DC transfer characteristics

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Figure 15. Receive attenuator versus volume control

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Figure 13. Level detector AC transfer characteristics

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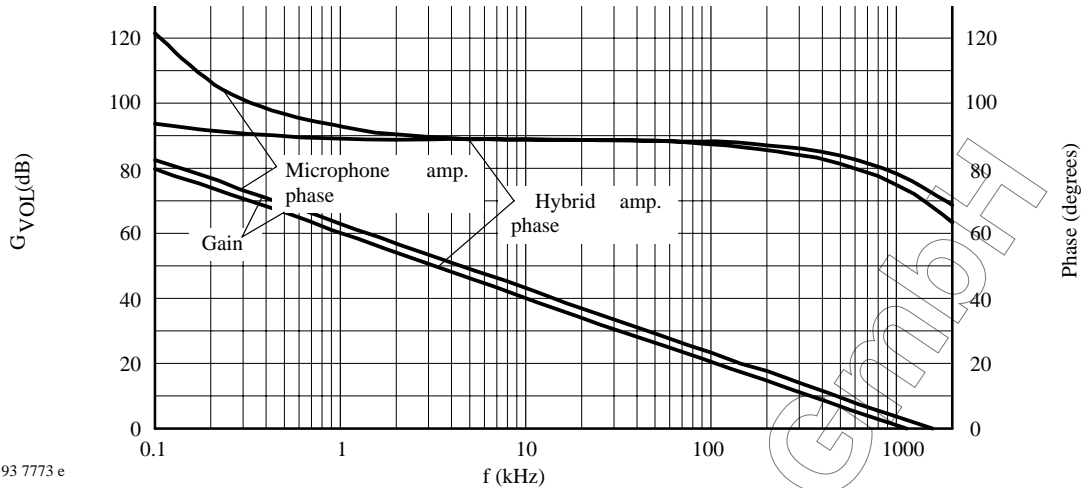Figure 16. Receive attenuation gain versus V_S

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Figure 17. Microphone–and 1st hybrid amplifier open-loop gain and phase versus frequency

93 7774 e
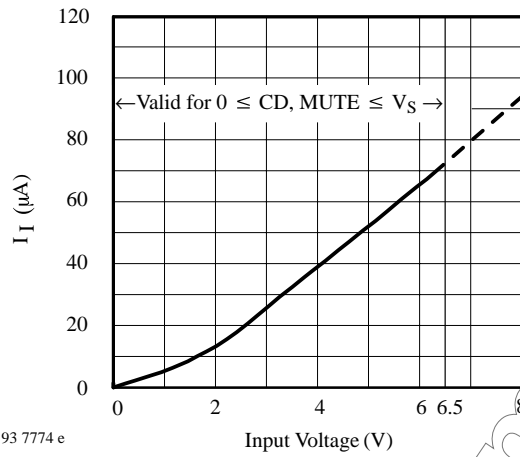
Figure 18. Input characteristics @ CD, MUTE

93 7776 e
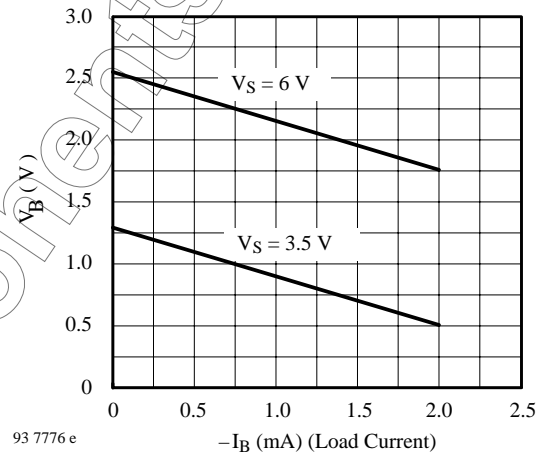
Figure 20. V$_B$ output characteristics

93 7775 e
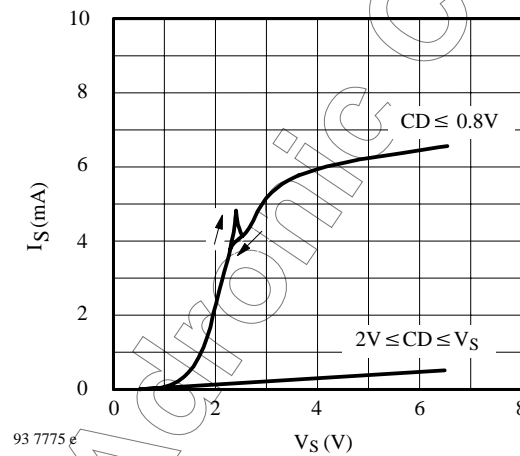
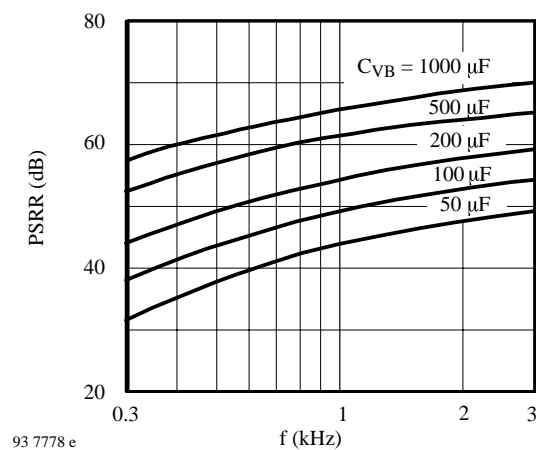Figure 19. Supply current versus supply voltage

93 7778 e

Figure 21. V$_B$ power supply rejection versus frequency characteristics and V$_B$ capacitor

Design Guidelines

Switching Time

The switching time of the U4082B circuit is determined by C_T (Pin 14, refer to figure 5), and secondarily by the capacitors at the level detector outputs (RLO1, RLO2, TLO1, TLO2). See figure 2.

The time to switch from idle to receive or transmit mode is determined by the capacitor at C_T, together with the internal current sources. The switching time is:

$$\Delta T = \frac{\Delta V \times C_T}{I}$$

$$= \frac{240 \times 5}{60} = 20.0 \ \text{ms}$$

where

$$\Delta V = 240 \ \text{mV}$$
$$C_T = 5 \ \mu\text{F}$$
$$I = 60 \ \mu\text{A}$$

If the circuit switches directly from receive to transmit mode (or vice versa), the total switching time would be 40 ms.

The switching time depends upon the mode selection. If the circuit is going to "fast idle", the time constant is determined by the C_T capacitor, and the internal 2-kΩ resistor. With $C_T = 5 \ \mu$F, the time constant is approximately 10 ms, giving a switching time to idle of approximately 30 ms (for 95 % change). Fast idle is an infrequent mode, however, occurring when both speakers are talking and competing for control of the circuit. The switching time from idle back to either transmit or receive mode is described above.

By switching to "slow idle," the time constant is determined by the C_T capacitor and R_T, the external resistor (see figure 6). With $C_T = 5.0 \ \mu$F and $R_T = 120 \ k\Omega$, the time constant is approximately 600 ms, giving a switching time of approximately 1.8 seconds (for 95% change). The switching period to slow idle begins when both speakers have stopped talking. The switching time back to the original mode will depend on how soon that speaker begins speaking again. The sooner the speaking starts during the 1.8-s period, the quicker the switching time since a smaller voltage excursion is required.

Switching time is determined by the internal current source as described above.

The above switching times occur, however, after the level detectors have detected the appropriate signal levels, since their outputs operate the attenuator control block. Referring to figure 4, the rise time of the level detectors' outputs to new speech is quick by comparison (approximately 1 ms), determined by the internal 350-Ω resistor and the external capacitor (typically 2 μF). The output's decay time is determined by the external capacitor and an internal 4-μA current source, giving a decay rate of 60 ms for a 120-mV excursion at RLO or TLO. Total response time of the circuit is not constant since it depends on the relative strength of the signals at the different level detectors and the timing of the signals with respect to each other. The capacitors at the four outputs (RLO1, RLO2, TLO1, TLO2) must be equal of value (± 10 %) to prevent problems in timing and level response.

The rise time of the level detector's outputs is not significant since it is so short. The decay time, however, provides a significant part of the "hold time" necessary to hold the circuit during the normal pauses in speech.

The components at the inputs of the level detectors (RLI1, RLI2, TLI1, TLI2) do not affect the switching time but rather affect the relative signal levels required to switch the circuit and the frequency response of the detectors.

Design Equations

The following definitions are used at 1 kHz with reference to figure 2 and figure 24 where coupling capacitors are omitted for the sake of simplicity:

– G_{MA} is the gain of the microphone amplifier measured from the microphone output to TI (typically 35 V/V, or 31 dB);

– G_T is the gain of the transmit attenuator, measured from TI to TO;

– G_{HA} is the gain of hybrid amplifiers, measured from TO to the HTO–/HTO+ differential output (typically 10.2 V/V, or 20.1 dB);

– G_{HT} is the gain from HTO–/HTO+ to Tip/Ring for transmit signals, and includes the balance network (measured at 0.4 V/V, or –8 dB);
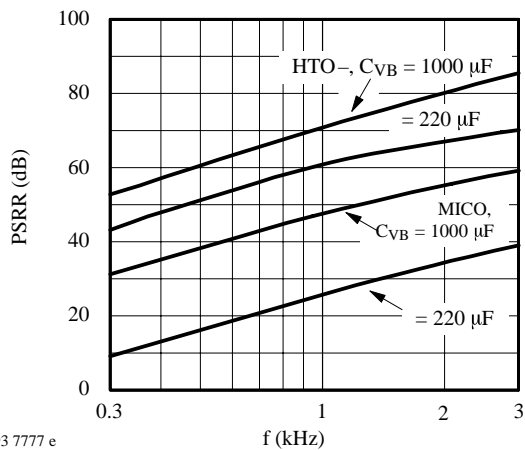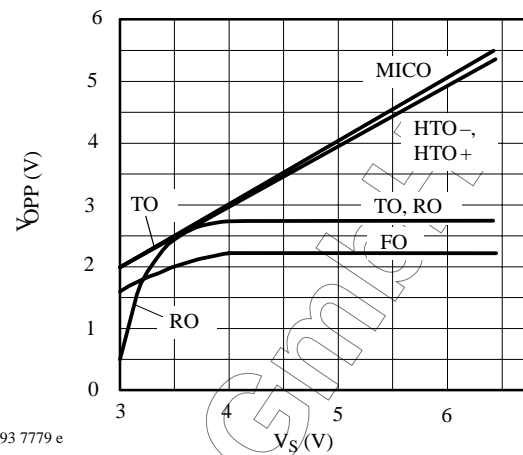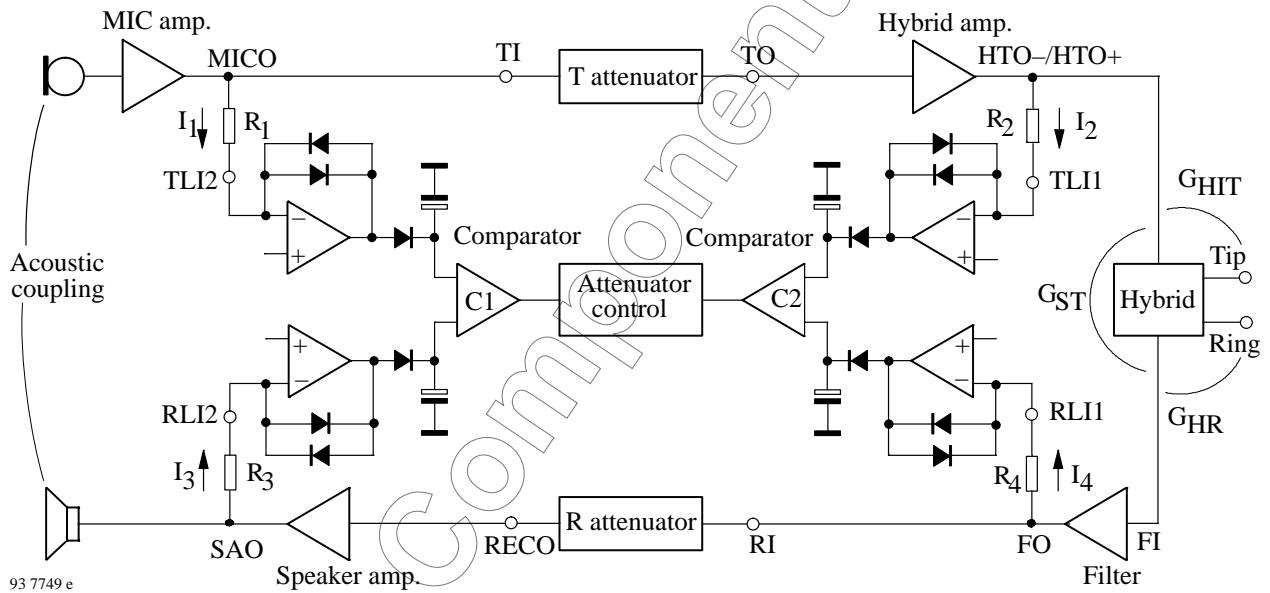
Figure 22. V_B power supply rejection of the microphone and hybrid amplifiers

Figure 23. Typical output swing versus V_S

Figure 24. Basic block diagram for design purposes

– G_{ST} is the sidetone gain, measured from HTO–/HTO+ to the filter input (measured at 0.18 V/V, or –15 dB);

– G_{HR} is the gain from Tip/Ring to the filter input for receive signals (measured at 0.833 V/V or –1.6 dB);

– G_{FO} is the gain of the filter stage, measured from the input of the filter to RI, typically 0 dB;

– G_R is the gain of the receive attenuator measured from RI to RECO;

– G_{SA} is the gain of the speaker amplifier, measured from RECO to the differential output of the U4083B (typically 22 V/V or 26.8 dB);

– G_{AC} is the acoustic coupling, measured from the speaker differential voltage to the microphone output voltage.

I) Transmit gain

The transmit gain, from the microphone output (V_M) to Tip and Ring, is determined by the output characteristics of the microphone, and the desired transmit level. For example, a typical electret microphone will produce approximately 0.35 mVrms under normal speech conditions. To achieve 100 mVrms at Tip/Ring, an overall gain of 285 V/V is necessary. The gain of the transmit attenuator is fixed at 2.0 (+ 6.0 dB), and the gain through the hybrid of figure 2 (G_{HT}) is nominally 0.4 (– 8.0 dB). Therefore, a gain of 357 V/V is required of the microphone and hybrid amplifiers. It is desirable to have the majority of that gain in the microphone amplifier for three reasons:

1. the low-level signals from the microphone should be amplified as soon as possible to minimize signal/noise problems;

2. to provide a reasonable signal level to the TLI2 level detector; and

3. to minimize any gain applied to broadband noise generated within the attenuator. However, to cover the normal voiceband, the microphone amplifier's gain should not exceed 48 dB (see figure 17). For the circuit in figure 24, the gain of the microphone amplifier was set at 35 V/V (31 dB), and the differential gain of the hybrid amplifiers was set at 10.2 V/V (20.1 dB).

II) Receive gain

The overall receive gain depends on the incoming signal level and the desired output power at the speaker. Nominal receive levels (independent of the peaks) at Tip/Ring can be 35 mVrms (– 27 dBm), although on long lines that level can be down to 8.0 mVrms (– 40 dBm). The speaker power is:

$$P_{SPK} = \frac{10^{dBm/10} \times 0.6}{R_S} \qquad (1)$$

where R_S is the speaker impedance, and the dBm term is the incoming signal level increased by the gain of the receive path. Experience has shown that approximately 30 dB gain is a satisfactory amount for the majority of applications. Using the above numbers and equation 1, it would appear that the resulting power to the speaker is extremely low. However, equation 1 does not consider the peaks in normal speech which can be 10 to 15 times the rms value. Considering the peaks, the overall average power approaches 20 to 30 mW on long lines, and much more on short lines.

Referring to figure 2, the gain from Tip/Ring to the filter input was measured at 0.833 V/V (– 1.6 dB), the filter's gain is unity, and the receive attenuator's gain is 2.0 V/V (+ 6.0 dB) at maximum volume. The speaker amplifier's gain is set at 22 V/V (26.8 dB) which puts the overall gain at approximately 31.2 dB.

III) Loop gain

The total loop gain (of figure 24) must add up to less than 0 dB to obtain a stable circuit. This can be expressed as:

$$G_{MA} + G_T + G_{HA} + G_{ST} + G_{FO} + G_R + G_{SA} + G_{AC} < 0 \qquad (2)$$

Using the typical numbers mentioned above, and knowing that $G_T + G_R = – 40$ dB, the required acoustic coupling can be determined:

$$G_{AC} < –[31 + 20.1 + (– 15) + 0 + (– 40) + 26.8] = – 22.9 \text{ dB}. \qquad (3)$$

An acoustic loss of at least 23 dB is necessary to prevent instability and oscillations, commonly referred to as "singing". However, the following equations show that greater acoustic loss is necessary to obtain proper level detection and switching.

IV) Switching thresholds

To switch comparator C1, currents I_1 and I_3 need to be determined. Referring to figure 24, with a receive signal V_L applied to Tip/Ring, a current I_3 will flow through R3 into RLI2 according to the following equation:

$$I_3 = \frac{V_L}{R_3} \times \left[G_{HR} \times G_{FO} \times G_R \times \frac{G_{SA}}{2} \right] \qquad (4)$$

where the terms in the brackets are the V/V gain terms. The speaker amplifier gain is divided by two since G_{SA} is the differential gain of the amplifier, and V_3 is obtained from one side of that output. The current I_1, coming from the microphone circuit, is defined by:

$$I_1 = \frac{V_M \times G_{MA}}{R_1} \qquad (5)$$

where V_M is the microphone voltage. Since the switching threshold occurs when $I_1 = I_3$, combining the above two equations yields:

$$V_M = V_L \times \frac{R_1}{R_3} \times \frac{[G_{HR} \times G_{FO} \times G_R \times G_{SA}]}{G_{MA} \times 2} \qquad (6)$$

This is the general equation defining the microphone voltage necessary to switch comparator C1 when a receive signal V_L is present. The highest V_M occurs when the receive attenuator is at maximum gain (+ 6.0 dB). Using the typical numbers for equation 6 yields:

$$V_M = 0.52 \ V_L \qquad (7)$$

To switch comparator C2, currents I_2 and I_4 need to be determined. With sound applied to the microphone, a voltage V_M is created by the microphone, resulting in a current I_2 into TLI1:

$$I_2 = \frac{V_M}{R_2} \left[G_{MA} \times G_T \times \frac{G_{HA}}{2} \right] \qquad (8)$$

Since G_{HA} is the differential gain of the hybrid amplifiers, it is divided by two to obtain the voltage V_2 applied to R_2. Comparator C2 switches when $I_4 = I_2$. I_4 is defined by:

$$I_4 = \frac{V_L}{R_4} \left[G_{HR} \times G_{FO} \right] \qquad (9)$$

Setting $I_4 = I_2$, and combining the above equations results in:

$$V_L = V_M \times \frac{R_4}{R_2} \times \frac{[G_{MA} \times G_T \times G_{HA}]}{[G_{HR} \times G_{FO} \times 2]} \qquad (10)$$

This equation defines the line voltage at Tip/Ring necessary to switch comparator C2 in the presence of a microphone voltage. The highest V_L occurs when the circuit is in transmit mode ($G_T = +6.0$ dB). Using the typical numbers for equation 10 yields:

$$V_L = 840 \, V_M \; (\text{or} \; V_M = 0.0019 \, V_L) \qquad (11)$$

At idle, where the gain of the two attenuators is –20 dB (0.1 V/V), equations 6 and 10 yield the same result:

$$V_M = 0.024 \, V_L \qquad (12)$$

Equations 7, 11, and 12 define the thresholds for switching, and are represented in figure 25

The "M" terms are the slopes of the lines (0.52, 0.024, and 0.0019) which are the coefficients of the three equations. The M_R line represents the receive to transmit threshold, in that it defines the microphone signal level necessary to switch to transmit in the presence of a given receive signal level. The M_T line represents the transmit to receive threshold. The M_I line represents the idle condition, and defines the threshold level on one side (transmit or receive) necessary to overcome noise on the other.
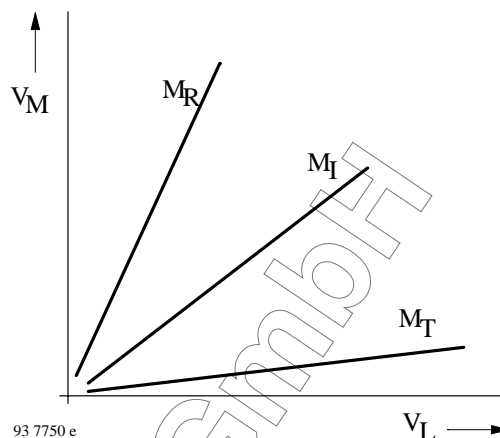

Figure 25. Switching thresholds

Some comments on the graph (figure 25):

- Acoustic coupling and sidetone coupling were not included in equations 7 and 12. Those couplings will affect the actual performance of the final speakerphone due to their interaction with speech at the microphone and the receive signal coming in at Tip/Ring. The effects of those couplings are difficult to predict due to their associated phase shifts and frequency response. In some cases the coupling signal will add, and other times subtract from the incoming signal. The physical design of the speakerphone enclosure, as well as the specific phone line to which it is connected, will affect the acoustic and sidetone couplings, respectively.

- The M_R line helps define the maximum acoustic coupling allowed in a system, which can be found from the following equation:

$$G_{AC(MAX)} = \frac{R_1}{2 \times R_3 \times G_{MA}} \qquad (13)$$

Equation 13 is independent of the volume control setting. Conversely, the acoustic coupling of a designed system helps determine the minimum slope of that line. Using the component values of figure 2 in equation 13 yields a $G_{AC(MAX)}$ of – 37 dB. Experience has shown, however, that an acoustic coupling loss of 40 dB is desirable.

- The M_T line helps define the maximum sidetone coupling (G_{ST}) allowed in the system. G_{ST} can be found using the following equation:

$$G_{ST} = \frac{R_4}{2 \times R_2 \times G_{FO}} \qquad (14)$$

Using the component values of figure 2 in equation 14 yields a maximum sidetone of 0 dB. Experience has shown, however, that a minimum of 6.0 dB loss is preferable.

The above equations can be used to determine the resistor values for the level detector inputs. Equation 6 can be

used to determine the R_1, R_3 ratio, and equation 10 can be used to determine the R_1-R_2 ratio. In figure 24, R_1–R_4 each represent the combined impedance of the resistor and coupling capacitor at each level detector input. The magnitude of each RC's impedance should be kept within the range of 2.0 kΩ to 15 kΩ in the voiceband (due to the typical signal levels present) to obtain the best performance from the level detectors. The specific R and C at each location will determine the frequency response of that level detector.

Application Information

Dial Tone Detector

The threshold for the dial tone detector is internally set at 15 mV (10 mVrms) below V_B (see figure 5). That threshold can be reduced by connecting a resistor from RI to ground. The resistor value is calculated from:

$$R = 10 \text{ k} \left[\frac{V_B}{\Delta V} - 1 \right]$$

where V_B is the voltage at Pin 15, and ΔV is the amount of threshold reduction. By connecting a resistor from V_S to RI, the threshold can be increased. The resistor value is calculated from:

$$R = 10 \text{ k} \left[\frac{V_S - V_B}{\Delta V} - 1 \right]$$

where ΔV is the amount of the threshold increase.

Background Noise Monitors

For testing or circuit analysis purposes, the transmit or receive attenuators can be set to "on" position by disabling the background noise monitors and applying a signal so as to activate the level detectors. Grounding the CPR pin will disable the receive background noise

monitor, thereby indicating the "presence of speech" to the attenuator control block. Grounding CPT does the same for the transmit path.

Additionally, the receive background noise monitor is automatically disabled by the dial tone detector whenever the receive signal exceeds the detector's threshold.

Transmit/Receive Detection Priority

Although the U4082B was designed to have idle mode such that the attenuators are halfway between their full on and full off positions, idle mode can be biased towards the transmit or the receive side. With this done, gaining control of the circuit from idle will be easier for that side towards which it is biased since that path will have less attenuation at idle.

By connecting a resistor from C_T (Pin 14) to ground, the circuit will be biased towards the transmit side. The resistor value is calculated from:

$$R = R_T \left[\frac{V_B}{\Delta V} - 1 \right]$$

where

$R_T = 120$ kΩ (typ.) connected between Pin 14 and 15. $\Delta V = V_B - V14$ (see figure 11).

By connecting a resistor from C_T (Pin 14) to V_S, the circuit will be biased towards the receive side. The resistor value is calculated from:
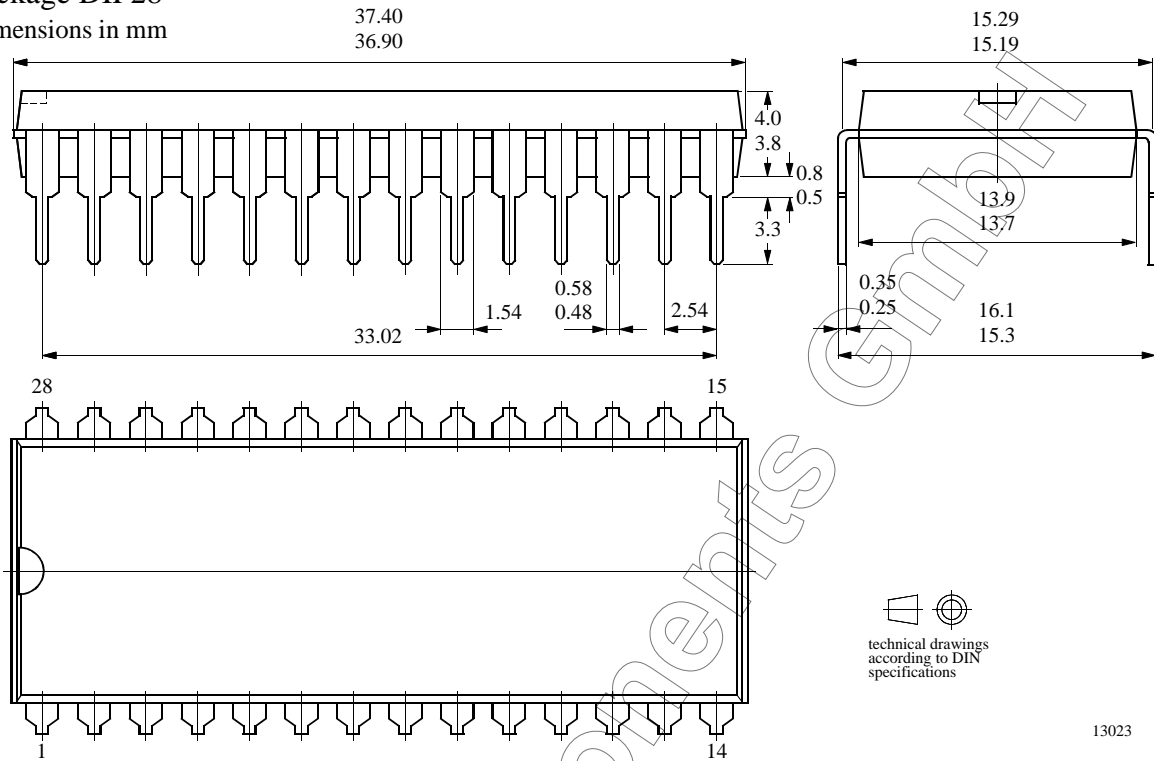
$$R = R_T \left[\frac{V_S - V_B}{\Delta V} - 1 \right]$$

Switching time will be somewhat affected in each case due to the different voltage excursions required to get to transmit and receive from idle. For practical considerations, the ΔV shift should not exceed 100 mV.
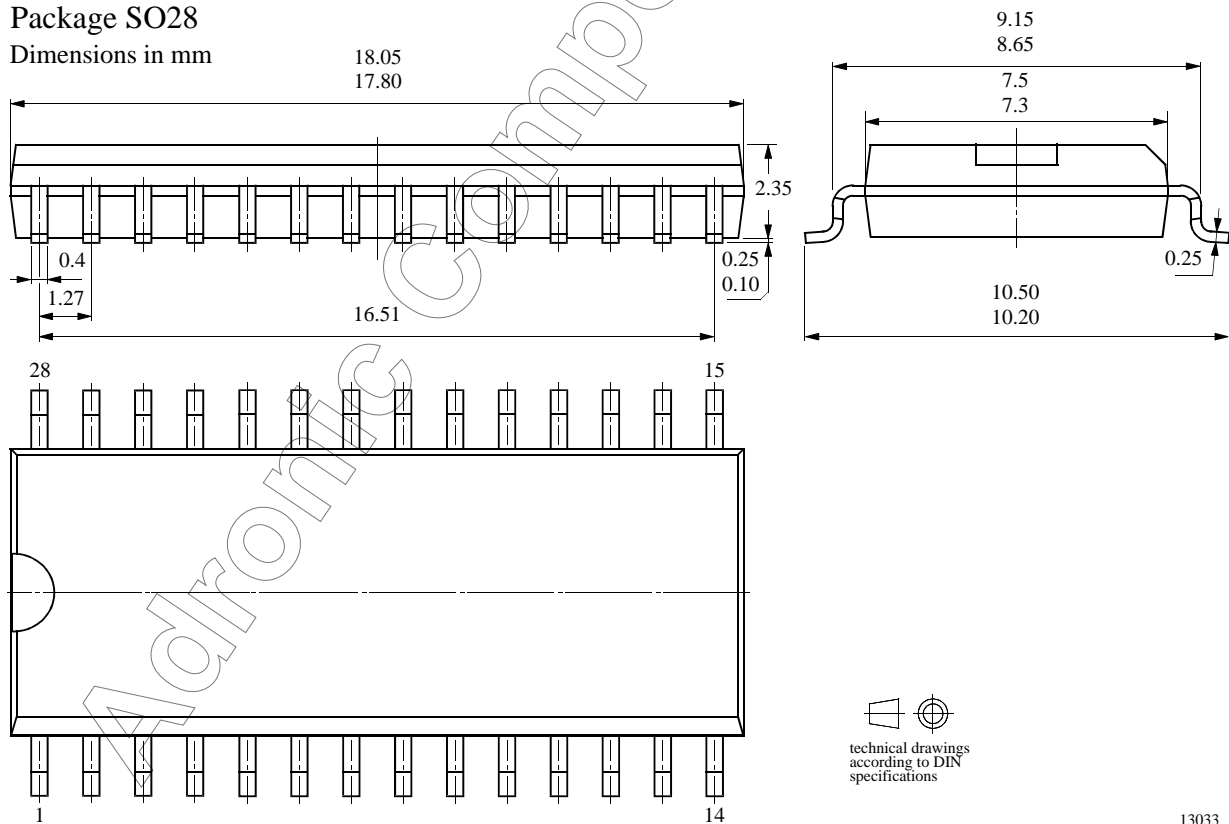
Package Information

Package DIP28
Dimensions in mm

technical drawings
according to DIN
specifications

13023

Package SO28
Dimensions in mm

technical drawings
according to DIN
specifications

13033

Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.