16-bit Proprietary Microcontroller

CMOS

F²MC-16FX MB96340 Series

■ DESCRIPTION

MB96340 series is based on Fujitsu's advanced 16FX architecture (16-bit with instruction pipeline for RISC-like performance). The CPU uses the same instruction set as the established 16LX series - thus allowing for easy migration of 16LX Software to the new 16FX products. 16FX improvements compared to the previous generation include significantly improved performance - even at the same operation frequency, reduced power consumption and faster start-up time.

For highest processing speed at optimized power consumption an internal PLL can be selected to supply the CPU with up to 56MHz operation frequency from an external 4MHz resonator. The result is a minimum instruction cycle time of 17.8ns going together with excellent EMI behavior. An on-chip clock modulation circuit significantly reduces emission peaks in the frequency spectrum. The emitted power is minimised by the on-chip voltage regulator that reduces the internal CPU voltage. A flexible clock tree allows to select suitable operation frequencies for peripheral resources independent of the CPU speed.

FUJITSU

■ FEATURES

Feature	Description
Technology	• 0.18µm CMOS
CPU	• F2MC-16FX CPU • Up to 56 MHz internal, 17.8 ns instruction cycle time • Optimized instruction set for controller applications (bit, byte, word and long-word data types; 23 different addressing modes; barrel shift; variety of pointers) • 8-byte instruction execution queue • Signed multiply (16-bit × 16-bit) and divide (32-bit/16-bit) instructions available
System clock	• On-chip PLL clock multiplier (x1..25, x1 when PLL stop) • 3-16 MHz external quartz clock, up to 4MHz external clock • 32-100 kHz subsystem quartz clock • 100kHz/2MHz internal RC clock for quick and save startup, oscillator stop detection, watchdog • Clock source selectable from main- and subclock oscillator (partnumber suffix “W”) on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals. • Low Power Consumption - 13 operating modes : (different Run, Sleep, Timer modes, Stop mode) • Clock modulator
On-chip voltage regulator	• Internal voltage regulator supports reduced internal MCU voltage, offering low EMI and low power consumption figures
Low voltage reset	• Reset is generated when supply voltage is below minimum.
Code Security	• Protects ROM content from unintended read-out
Memory Patch Function	• Replaces ROM content • Can also be used to implement embedded debug support
DMA	• Automatic transfer function independent of CPU, can be assigned freely to resources
Interrupts	• Fast Interrupt processing • 8 programmable priority levels • Non-Maskable Interrupt (NMI)
Timers	• Two independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer) • Watchdog Timer

Feature	Description
CAN	• Supports CAN protocol version 2.0 part A and B • ISO16845 certified • Bit rates up to 1 Mbit/s • 32 message objects • Each message object has its own identifier mask • Programmable FIFO mode (concatenation of message objects) • Maskable interrupt • Disabled Automatic Retransmission mode for Time Triggered CAN applications • Programmable loop-back mode for self-test operation
USART	• Full duplex USARTs (SCI/LIN) • Wide range of baud rate settings using a dedicated reload timer • Special synchronous options for adapting to different synchronous serial protocols • LIN functionality working either as master or slave LIN device
I2C	• Up to 400 kbit/s • Master and Slave functionality, 8-bit and 10-bit addressing
A/D converter	• SAR-type • 10bit resolution • Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger or reload timer
A/D Converter Reference Voltage switch	• 2 independant positive A/D converter reference voltages available
Reload Timers	• 16-bit wide • Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency • Event count function
Free Running Timers	• Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4), Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$,$1/2^8$ of peripheral clock frequency
Input Capture Units	• 16-bit wide • Signals an interrupt upon external event • Rising edge, falling edge or rising & falling edge sensitive
Output Compare Units	• 16-bit wide • Signals an interrupt when a match with 16-bit I/O Timer occurs • A pair of compare registers can be used to generate an output signal.

Feature	Description
Programmable Pulse Generator	• 16-bit down counter, cycle and duty setting registers • Interrupt at trigger, counter borrow and/or duty match • PWM operation and one-shot operation • Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock and Reload timer overflow as clock input • Can be triggered by software or reload timer
Real Time Clock	• Can be clocked either from sub oscillator (devices with partnumber suffix “W”),main oscillator or from the RC oscillator • Facility to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration) • Read/write accessible second/minute/hour registers • Can signal interrupts every halfsecond/second/minute/hour/day • Internal clock divider and prescaler provide exact 1s clock based on a 4 MHz or a 32 kHz clock input (devices with partnumber suffix “W”) clock input
External Interrupts	• Edge sensitive or level sensitive • Interrupt mask and pending bit per channel • Each available CAN channel RX has an external interrupt for wake-up • Selected USART channels SIN have an external interrupt for wake-up
Non Maskable Interrupt	• Disabled after reset • Once enabled, can not be disabled other than by reset. • Level high or level low sensitive • Pin shared with external interrupt 0.
External bus interface	• 8-bit or 16-bit bidirectional data • Up to 24-bit addresses • 6 chip select signals • Multiplexed address/data lines • Wait state request • External bus master possible • Timing programmable
Alarm comparators	• Monitors an external voltage and generates an interrupt in case of a voltage lower or higher than the defined thresholds • Threshold voltages defined externally or generated internally • Status is readable, interrupts can be masked separately

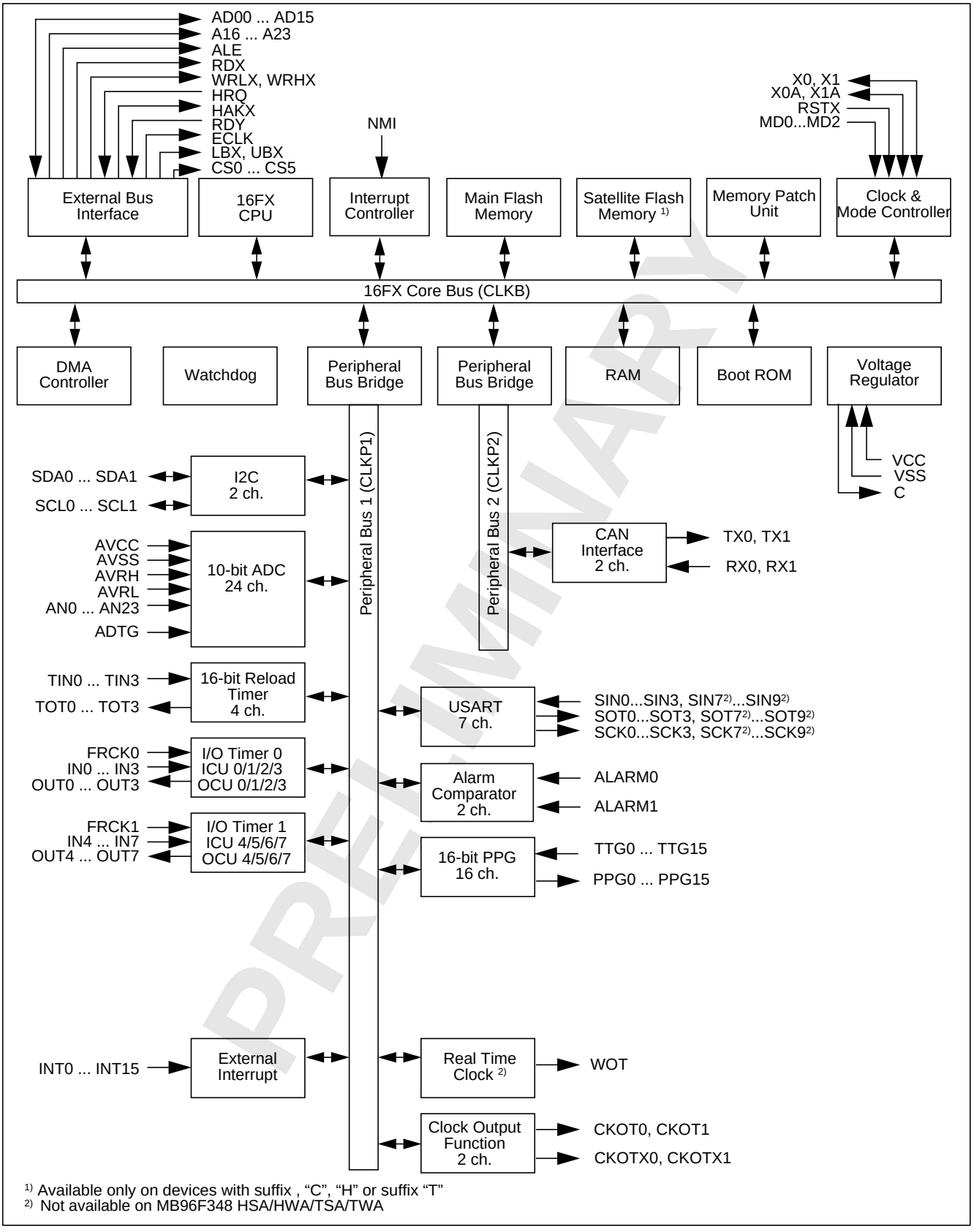
Feature	Description
I/O Ports	• Virtually all external pins can be used as general purpose I/O • All push-pull outputs (except when used as I2C SDA/SCL line) • Bit-wise programmable as input/output or peripheral signal • Bit-wise programmable input enable • Bit-wise programmable input levels (Automotive / CMOS-Schmitt trigger / TTL) • Bit-wise programmable pull-up resistor • Bit-wise programmable output driving strength for EMI optimization
Package	• 100-pin plastic QFP and LQFP
Flash Memory	• Supports automatic programming, Embedded Algorithm™*1 • Write/Erase/Erase-Suspend/Resume commands • A flag indicating completion of the algorithm • Number of erase cycles : 10,000 times • Data retention time : 20 years • Erase can be performed on each sector individually • Sector protection • Flash Security feature to protect the content of the Flash • Low voltage detection during Flash erase
*1 : Embedded Algorithm is a trade mark of Advanced Micro Devices Inc.	

■ PRODUCT LINEUP

Features		MB96V300	MB9634x
Product type		Evaluation sample	Flash product: MB96F34x Mask ROM product: MB9634x
Product options			
YS		NA	LVD persistently on / Single clock devices
RS			LVD can be disabled / Single clock devices
YW			LVD persistently on / Dual clock devices
RW			LVD can be disabled / Dual clock devices
TS			Satellite Flash / LVD persistently on / Single clock devices
HS			Satellite Flash / LVD can be disabled / Single clock devices
TW			Satellite Flash / LVD persistently on / Dual clock devices
HW			Satellite Flash / LVD can be disabled / Dual clock devices
AS			No CAN / No Satellite Flash / LVD persistently on / Single clock devices
CS			No CAN / /Satellite Flash / LVD can be disabled / Single clock devices
AW			No CAN / No Satellite Flash / LVD persistently on / Dual clock devices
CW			No CAN / Satellite Flash / LVD can be disabled / Dual clock devices
Flash/ ROM	RAM		
128kB	6kB	ROM/Flash memory emulation by external RAM, 92kB internal RAM	MB96344R, MB96344Y
288kB	16kB		MB96F346R, MB96346R, MB96F346Y, MB96346Y, MB96F346A
416kB	16kB		MB96F347R, MB96347R, MB96F347Y, MB96347Y, MB96F347A
544kB	24kB		MB96F348R, MB96F348Y, MB96F348A
Main: 544kB, Sat.: 32kB	24kB		MB96F348C, MB96F348H, MB96F348T
Package		BGA416	FPT-100P-M20 FPT-100P-M22
DMA		16 channels	6 channels
USART		10 channels	7 channels MB96F348 TSA/HSA/TWA/HWA: 4 channels
I2C		2 channels	2 channel
A/D Converter		40 channels	24 channels

Features	MB96V300	MB9634x
A/D Converter Reference Voltage switch	yes	yes
16-bit Reload Timer	6 channels	4 channels
16-bit Free-Running Timer	4 channels	2 channels
16-bit Output Compare	12 channels	8 channels
16-bit Input Capture	12 channels	8 channels
16-bit Programmable Pulse Generator	20 channels	16 channels
CAN Interface (not available on MB963xxA, MB963xxC)	5 channels	2 channels
External Interrupts	16 channels	
Non-Maskable Interrupt	1 channel	
Real Time Clock	1 MB96F348TSA/HSA/TWA/HWA: not available	
I/O Ports	136	80 for part number with suffix "W", 82 for part number with suffix "S"
Alarm comparator	2 channels	
External bus interface	Yes	Multiplexed
Chip select	6 signal	
Clock output function	2 channels	
Low voltage reset	Reset is generated when supply voltage is below minimum.	
On-chip RC-oscillator	Yes	

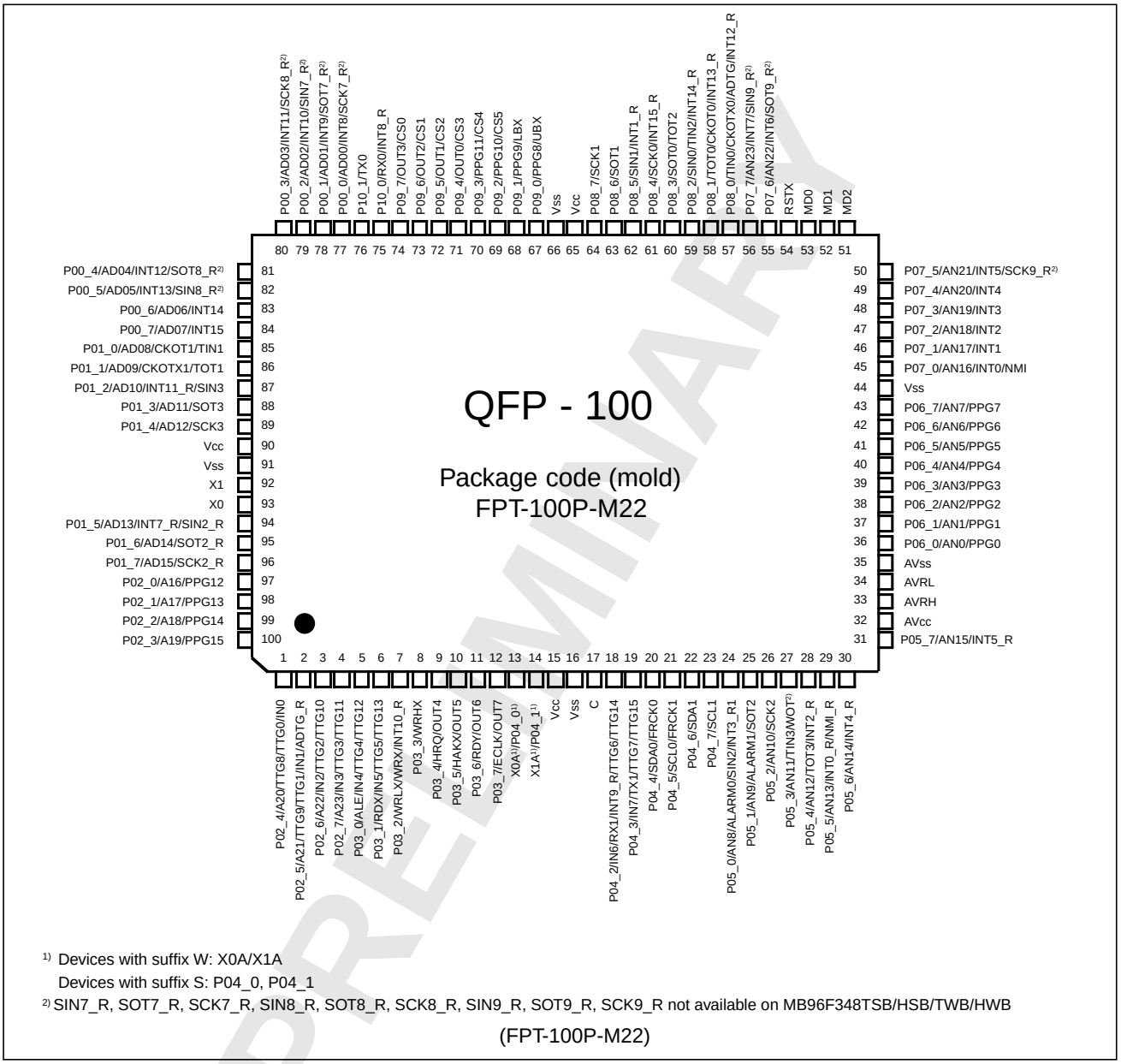
■ BLOCK DIAGRAM



1) Available only on devices with suffix , “C”, “H” or suffix “T”
2) Not available on MB96F348 HSA/HWA/TSA/TWA

■ PIN ASSIGNMENTS

Pin assignment (FPT-100P-M22)



1) Devices with suffix W: X0A/X1A
Devices with suffix S: P04_0, P04_1

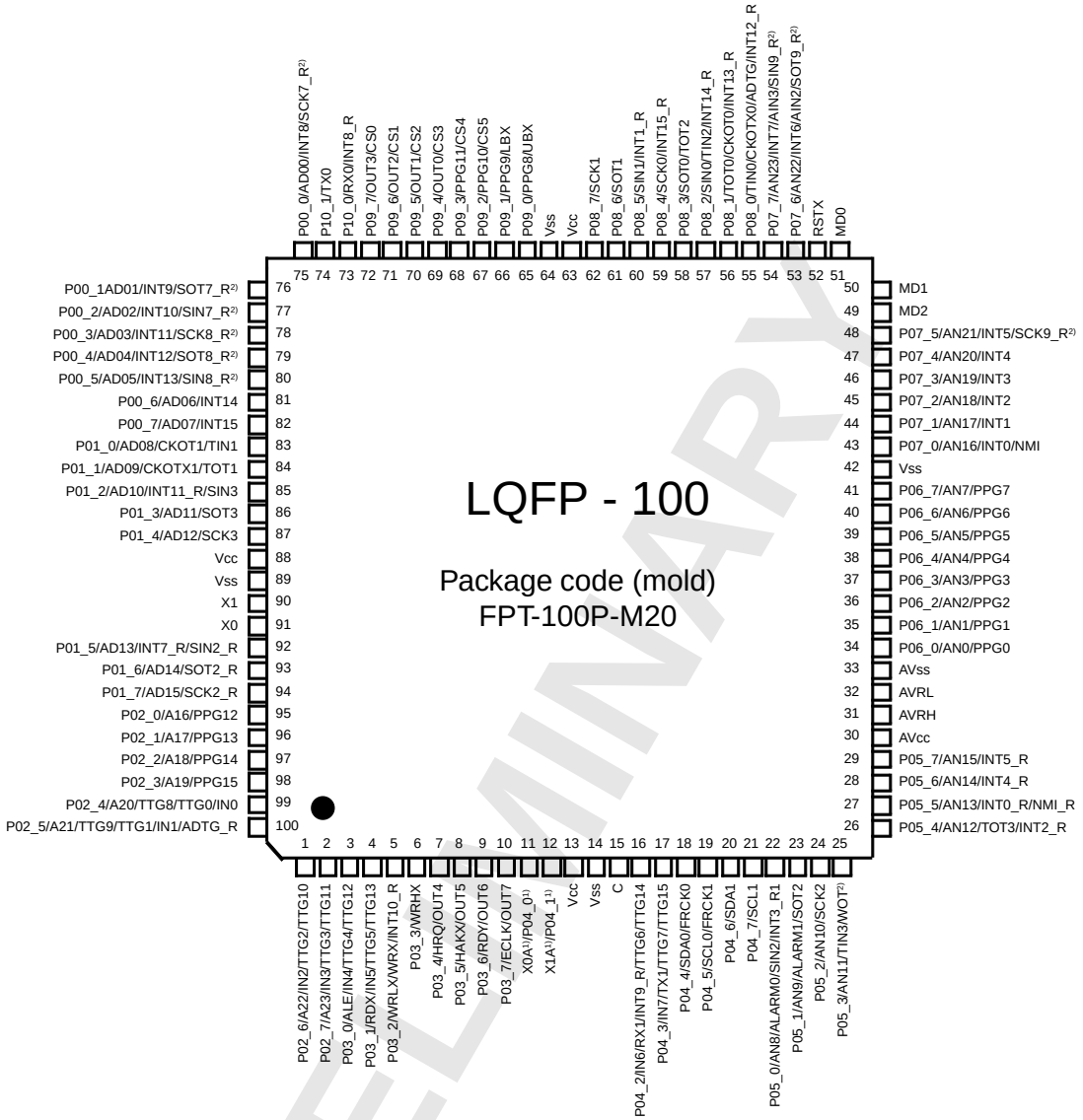
2) SIN7_R, SOT7_R, SCK7_R, SIN8_R, SOT8_R, SCK8_R, SIN9_R, SOT9_R, SCK9_R not available on MB96F348TSB/HSB/TWB/HWB

(FPT-100P-M22)

Remark:

MB96(F)34x products are pin-compatible to F²MC-16LX family MB90340 series.

Pin assignment (FPT-100P-M20)



1) Devices with suffix W: X0A/X1A
Devices with suffix S: P04_0, P04_1

2) SIN7_R, SOT7_R, SCK7_R, SIN8_R, SOT8_R, SCK8_R, SIN9_R, SOT9_R, SCK9_R not available on MB96F348TSB/HSB/TWB/HWB

(FPT-100P-M20)

Remark:

MB96(F)34x products are pin-compatible to F²MC-16LX family MB90340 series.

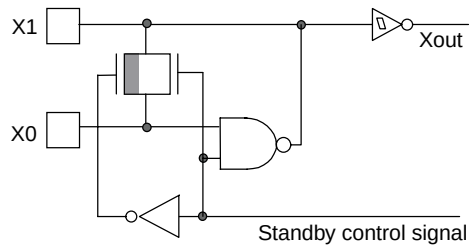
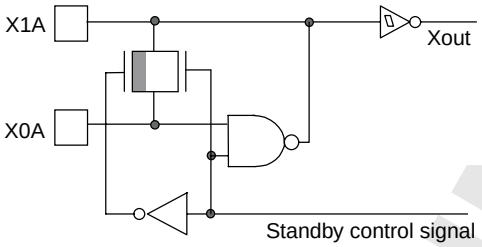
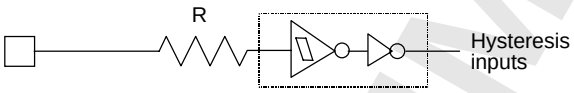
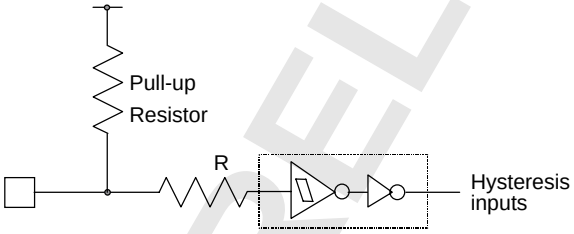
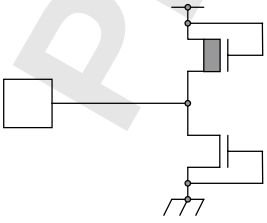
■ PIN CIRCUIT TYPE

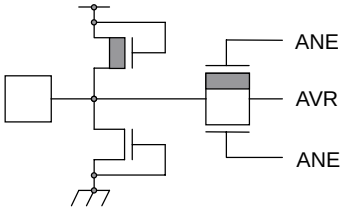
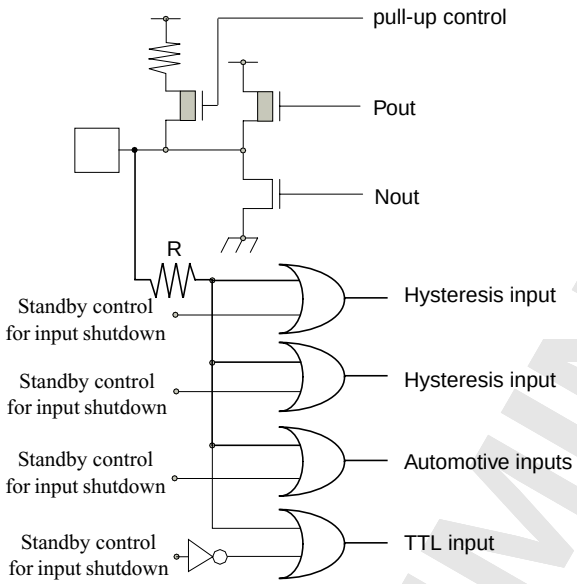
FPT-100P-M20	
Pin no.	Circuit type
1-10	H
11,12	B[1)]
11,12	H[2)]
13,14	Supply
15	C-Pin
16,17	H
18-21	N
22-29	I
30	F
31	G
32-33	F
34 to 41	I
42	Supply
43 to 48	I
49 to 51	C
52	E
53 to 54	I
55 to 62	H
63, 64	Supply
65 to 87	H
88,89	Supply
90, 91	A
92-100	H

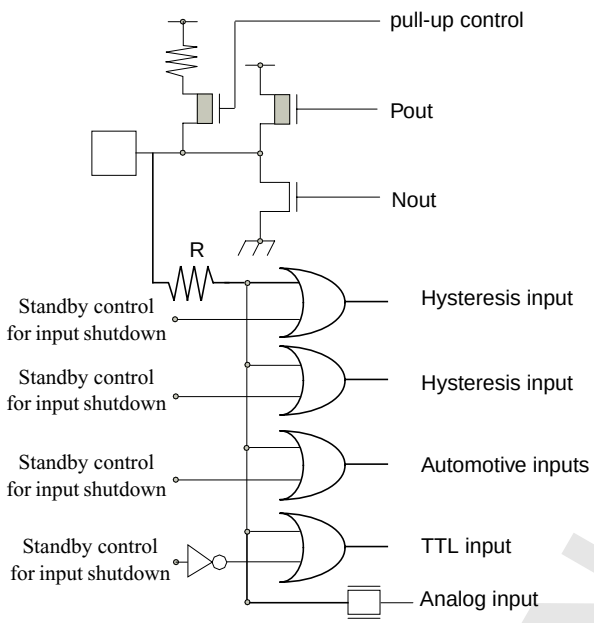
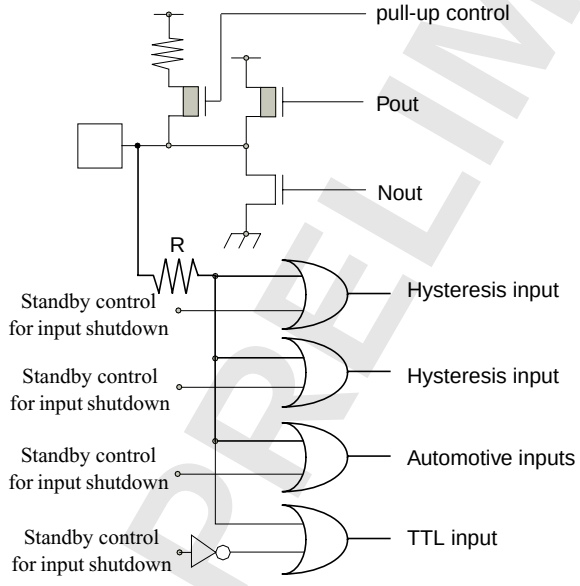
FPT-100P-M22	
Pin no.	Circuit type
1-12	H
13, 14	B[1)]
13, 14	H[2)]
15,16	Supply
17	C-Pin
18,19	H
20-23	N
24-31	I
32	F
33	G
34-35	F
36 to 43	I
44	Supply
45 to 50	I
51 to 53	C
54	E
55 to 56	I
57 to 64	H
65, 66	Supply
67 to 89	H
90, 91	Supply
92, 93	A
94 to 100	H

[1)] Devices with suffix ”W”
[2)] Devices without suffix ”W”

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		Oscillation circuit High-speed oscillation feedback resistor = approx. 1 MΩ
B		Oscillation circuit Low-speed oscillation feedback resistor = approx. 10 MΩ
C		Mask ROM and EVA device: CMOS Hysteresis input pin Flash device: CMOS input pin
E		CMOS Hysteresis input pin Pull-up resistor value: approx. 50 kΩ
F		Power supply input protection circuit

Type	Circuit	Remarks
G		A/D converter ref+ (AVRH) power supply input pin, With the protection circuit Flash devices do not have a protection circuit against VCC for pin AVRH
H		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up registor:50kΩ approx.

Type	Circuit	Remarks
I		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function) TTL input with input shutdown function Programmable pull-up registor: 50kΩ approx. Analogue input
N		CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up registor:50kΩ approx.

■ PIN FUNCTION DESCRIPTION

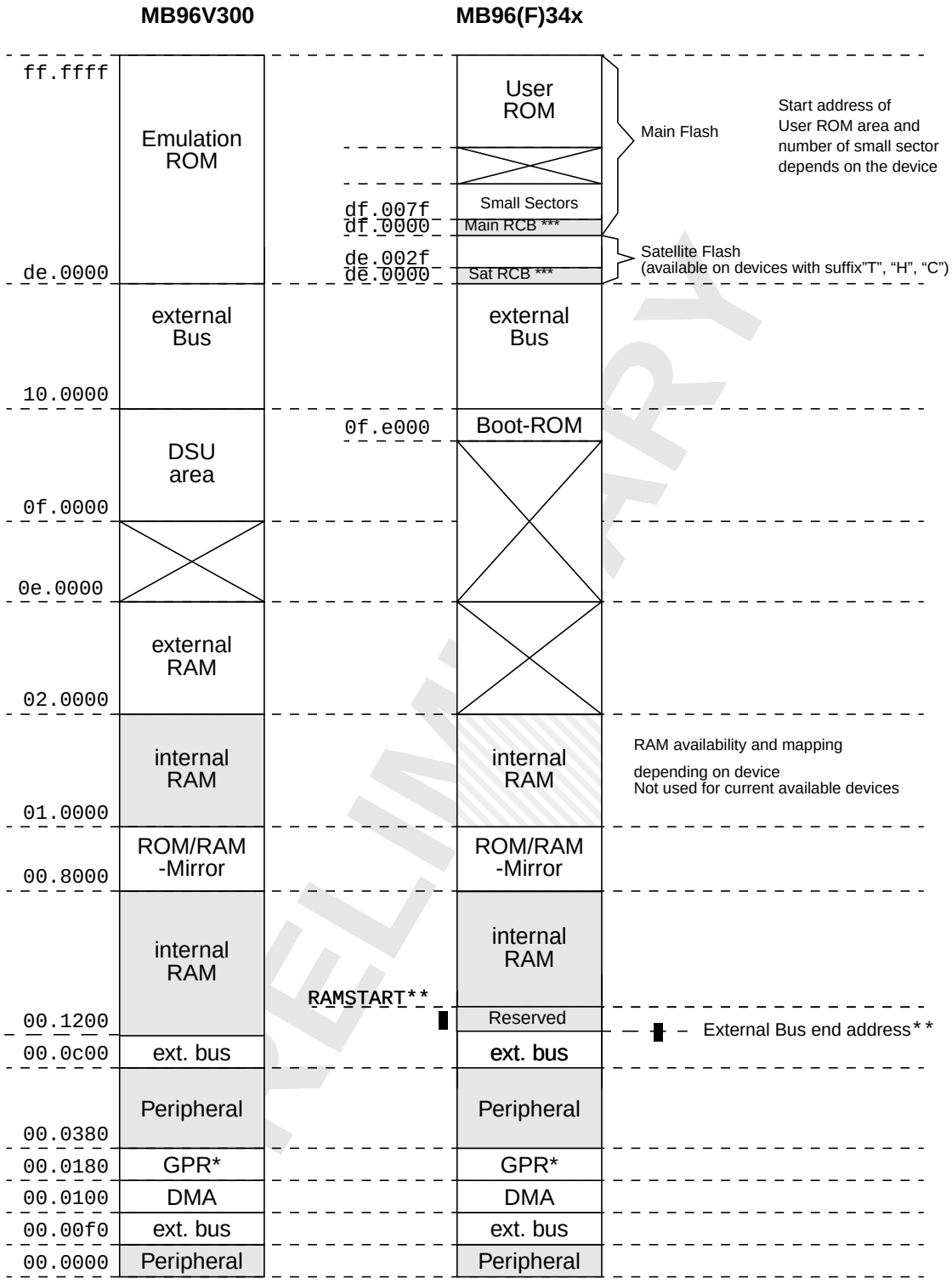
Pin Function description (1 / 2)

Pin name	Feature	Description
ADn	External bus	External bus interface (multiplexed mode) address/data input/ output
ADTG	ADC	A/D converter trigger input
ADTG_R	ADC	Relocated A/D converter trigger input
ALARMn	Alarm comparator	Alarm Comparator n input
ALE	External bus	External bus Address Latch Enable output
ANn	ADC	A/D converter channel n input
AVCC	Supply	Analogue circuits power supply
AVRH	ADC	A/D converter high reference voltage input
AVRL	ADC	A/D converter low reference voltage input
AVSS	Supply	Analogue circuits power supply
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin.
CKOTn	Clock output function	Clock Output function n output
CKOTXn	Clock output function	Clock Output Function n inverted output
ECLK	External bus	External bus clock output
CSn	External bus	External bus chip select n output
FRCKn	Free Running Timer	Free Running Timer n input
HAKX	External bus	External bus Hold Acknowlegde
HRQ	External bus	External bus Hold Request
INn	ICU	Input Capture Unit n input
INTn	External Interrupt	External Interrupt n input
INTn_R	External Interrupt	Relocated External Interrupt n input
LBX	External bus	External Bus Interface Lower Byte select strobe output
MDn	Core	Input pins for specifying the operating mode.
NMI	External Interrupt	Non-Maskable Interrupt input
NMI_R	External Interrupt	Relocated Non-Maskable Interrupt input
OUTn	OCU	Output Compare Unit n waveform output
PPGn	PPG	Programmable Pulse Generator n output
PPGn_R	PPG	Relocated Programmable Pulse Generator n output

Pin Function description (2 / 2)

Pin name	Feature	Description
RDX	External bus	External bus interface read strobe output
RDY	External bus	External bus interface external wait state request input
RSTX	Core	Reset input
RXn	CAN	CAN interface n RX input
SCKn	USART	USART n serial clock input/output
SCKn_R	USART	Relocated USART n serial clock input/output
SCLn	I2C	I2C interface n clock I/O input/output
SDAn	I2C	I2C interface n serial data I/O input/output
SINn	USART	USART n serial data input
SINn_R	USART	Relocated USART n serial data input
SOTn	USART	USART n serial data output
SOTn_R	USART	Relocated USART n serial data output
TINn	Reload Timer	Reload Timer n event input
TOTn	Reload Timer	Reload Timer n output
TTGn	PPG	Programmable Pulse Generator n trigger input
TTGn_R	PPG	Relocated Programmable Pulse Generator n trigger input
TXn	CAN	CAN interface n TX output
UBX	External bus	External Bus Interface Upper Byte select strobe output
VCC	Supply	Power supply
VSS	Supply	Power supply
WOT	RTC	Real Timer clock output
WRHX	External bus	External bus High byte Write strobe output
WRLX	External bus	External bus Low byte Write strobe output
X0	Clock	Oscillator input
X0A	Clock	"Subclock Oscillator input (only for devices with suffix ""W"")"
X1	Clock	Oscillator output
X1A	Clock	"Subclock Oscillator output (only for devices with suffix ""W"")"

■ MEMORY MAP

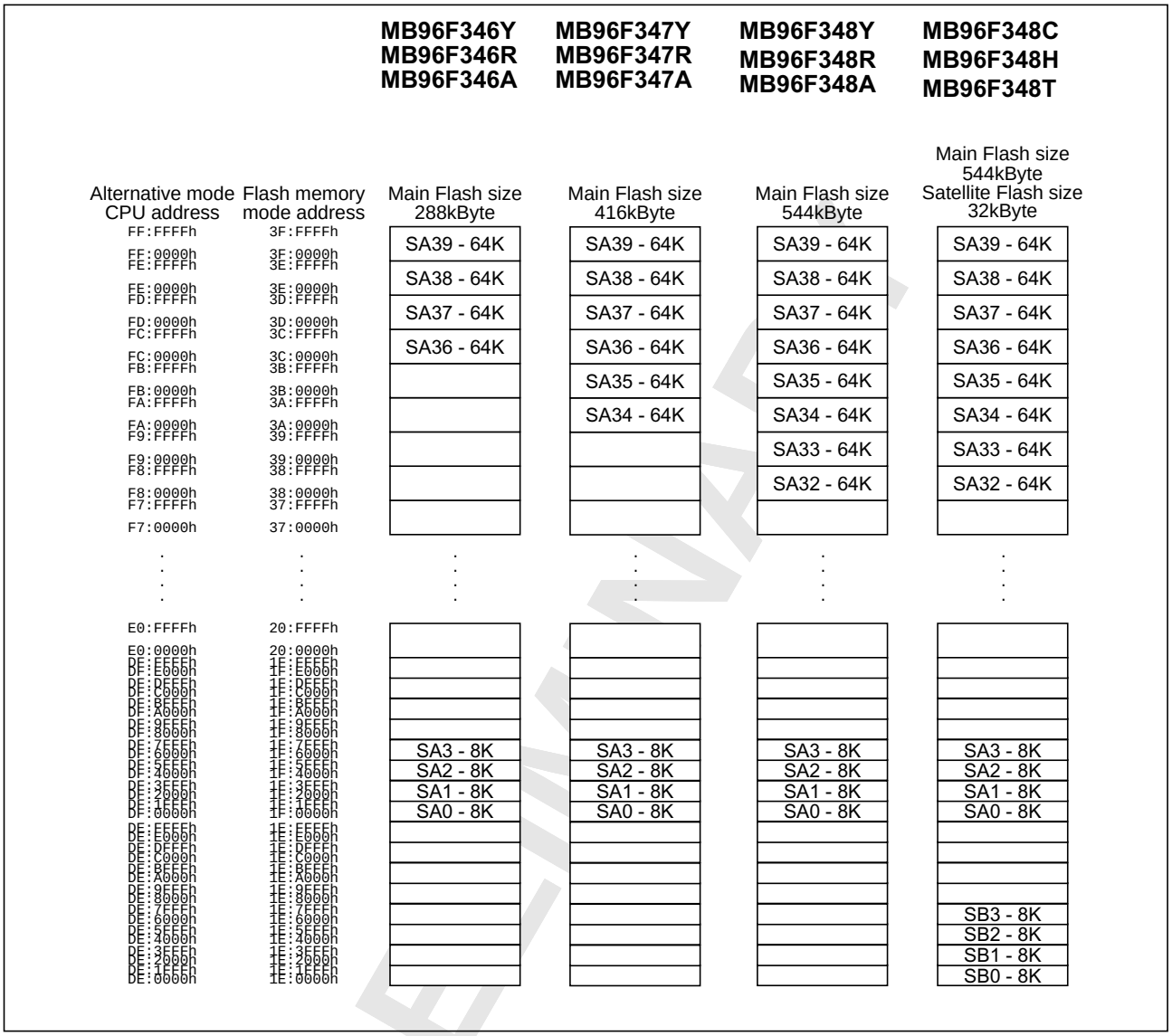


* Unused GPR banks can be used as RAM area.
** Please refer to the table "RAMSTART for different RAM sizes" on the next page
*** ROM Configuration Block (RCB) must not be used for other purposes than described in the manual
The external Bus area DMA area are only available if the device contains the corresponding resource.
The available RAM and ROM area depends on the device configuration.

■ RAMSTART AND EXTERNAL BUS END ADDRESS FOR DIFFERENT RAM SIZES

Devices	RAM size	RAMSTART	End address of external bus area
MB96344	6 kB	6A40	69FF
MB96(F)346, MB96(F)347	16 kB	4240	41FF
MB96F348	24 kB	2240	21FF

■ FLASH SECTOR CONFIGURATION



■ PARALLEL PROGRAMMING FLASH MEMORY CONTROL SIGNALS

Flash memory control signals (MD[2:0] = 111)

MB96F34X				MBM29LV200
Pin number		Normal function	Flash memory mode	
LQFP	QFP			
3	5	P03_0	AQ16	A15
4	6	P03_1	$\overline{CE}$	$\overline{CE}$
5	7	P03_2	$\overline{OE}$	$\overline{OE}$
6	8	P03_3	$\overline{WE}$	$\overline{WE}$
7	9	P03_4	AQ17	A16
8	10	P03_5	AQ18	
9	11	P03_6	$\overline{BYTE}$	$\overline{BYTE}$
10	12	P03_7	RY/$\overline{BY}$	RY/$\overline{BY}$
16 to 19	18 to 21	P04_2 to P04_5	AQ8 to AQ11	A7 to A10
20 to 21	22 to 23	P04_6 to P04_7	AQ12 to AQ13	A11 to A12
22 to 23	24 to 25	P05_0 to P05_1	AQ14 to AQ15	A13 to A14
27 to 29	29 to 31	P05_5 to P05_7	AQ19 to AQ21	
49	51	MD2	MD2	OE
50	52	MD1	MD1	$\overline{RESET}$
51	53	MD0	MDO	A9
52	54	$\overline{RST}$	$\overline{RESET}$	$\overline{RESET}$
75 to 82	77 to 84	P00_0 to P00_7	DQ0 to DQ7	DQ0 to DQ7
83 to 86	85 to 88	P01_0 to P01_3	DQ8 to DQ11	DQ8 to DQ11
87, 92 to 94	89, 94 to 96	P01_4 to P01_7	DQ12 to DQ15	DQ12 to DQ15
99 to 2, 95 to 98	1 to 4, 97 to 100	P02_0 to P02_7	AQ0 to AQ7	A-1, A0 to A6

■ SERIAL PROGRAMMING COMMUNICATION INTERFACE

USART pins for Flash serial programming (MD[2:0] = 010)

MB96F34x			
Pin number	Pin number	USART Number	Normal function
LQFP-100	QFP-100		
57	59	USART0	SIN0
58	60		SOT0
59	61		SCK0
60	62	USART1	SIN1
61	63		SOT1
62	64		SCK1
22	24	USART2	SIN2
23	25		SOT2
24	26		SCK2
92	94	USART2	SIN2_R
93	95		SOT2_R
94	96		SCK2_R
85	87	USART3	SIN3
86	88		SOT3
87	89		SCK3
77	79	USART7	SIN7_R
76	78		SOT7_R
75	77		SCK7_R
80	82	USART8	SIN8_R
79	81		SOT8_R
78	80		SCK8_R
54	56	USART9	SIN9_R
53	55		SOT9_R
48	50		SCK9_R

Note: For handshaking pin, please use for this device the default pin P00_1. If any other pin is required, please contact the Flash programmer device vendor.

■ I/O MAP

I/O map (1 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
000000H	P00 - I/O Port Port Data Register	PDR00			RW
000001H	P01 - I/O Port Port Data Register	PDR01			RW
000002H	P02 - I/O Port Port Data Register	PDR02			RW
000003H	P03 - I/O Port Port Data Register	PDR03			RW
000004H	P04 - I/O Port Port Data Register	PDR04			RW
000005H	P05 - I/O Port Port Data Register	PDR05			RW
000006H	P06 - I/O Port Port Data Register	PDR06			RW
000007H	P07 - I/O Port Port Data Register	PDR07			RW
000008H	P08 - I/O Port Port Data Register	PDR08			RW
000009H	P09 - I/O Port Port Data Register	PDR09			RW
00000AH	P10 - I/O Port Port Data Register	PDR10			RW
00000BH - 000017H	Reserved				
000018H	ADC - Control Status register 0 Low	ADCSL	ADCS		RW
000019H	ADC - Control Status register 0 High	ADCSH			RW
00001AH	ADC - Data Register 0 Low	ADCRL	ADCR		R
00001BH	ADC - Data Register 0 High	ADCRH			R
00001CH	ADC - Setting Register Low 0		ADSR		RW
00001DH	ADC - Setting Register High 0				
00001EH	ADC - Extended Configuration Register	ADECR			RW
000020H	FRT0 - Data register of free-running timer		TCDT0		RW
000021H	FRT0 - Data register of free-running timer				RW
000022H	FRT0 - Control status register of free-running timer	TCCSL0	TCCS0		RW
000023H	FRT0 - Control status register of free-running timer	TCCSH0			RW
000024H	FRT1 - Data register of free-running timer		TCDT1		RW

I/O map (2 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
000025H	FRT1 - Data register of free-running timer				RW
000026H	FRT1 - Control status register of free-running timer	TCCSL1	TCCS1		RW
000027H	FRT1 - Control status register of free-running timer	TCCSH1			RW
000028H	OCU0 - Output Compare Control Status	OCS0			RW
000029H	OCU1 - Output Compare Control Status	OCS1			RW
00002AH	OCU0 - Compare Register		OCCP0		RW
00002BH	OCU0 - Compare Register				RW
00002CH	OCU1 - Compare Register		OCCP1		RW
00002DH	OCU1 - Compare Register				RW
00002EH	OCU2 - Output Compare Control Status	OCS2			RW
00002FH	OCU3 - Output Compare Control Status	OCS3			RW
000030H	OCU2 - Compare Register		OCCP2		RW
000031H	OCU2 - Compare Register				RW
000032H	OCU3 - Compare Register		OCCP3		RW
000033H	OCU3 - Compare Register				RW
000034H	OCU4 - Output Compare Control Status	OCS4			RW
000035H	OCU5 - Output Compare Control Status	OCS5			RW
000036H	OCU4 - Compare Register		OCCP4		RW
000037H	OCU4 - Compare Register				RW
000038H	OCU5 - Compare Register		OCCP5		RW
000039H	OCU5 - Compare Register				RW
00003AH	OCU6 - Output Compare Control Status	OCS6			RW
00003BH	OCU7 - Output Compare Control Status	OCS7			RW

I/O map (3 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
00003CH	OCU6 - Compare Register		OCCP6		RW
00003DH	OCU6 - Compare Register				RW
00003EH	OCU7 - Compare Register		OCCP7		RW
00003FH	OCU7 - Compare Register				RW
000040H	ICU0/ICU1 - Control Status Register	ICS01			RW
000041H	ICU0/ICU1 - Edge register	ICE01			RW
000042H	ICU0 - Capture Register	IPCPL0	IPCP0		R
000043H	ICU0 - Capture Register	IPCPH0			R
000044H	ICU1 - Capture Register	IPCPL1	IPCP1		R
000045H	ICU1 - Capture Register	IPCPH1			R
000046H	ICU2/ICU3 - Control Status Register	ICS23			RW
000047H	ICU2/3 - Edge register	ICE23			RW
000048H	ICU2 - Capture Register	IPCPL2	IPCP2		R
000049H	ICU2 - Capture Register	IPCPH2			R
00004AH	ICU3 - Capture Register	IPCPL3	IPCP3		R
00004BH	ICU3 - Capture Register	IPCPH3			R
00004CH	ICU4/ICU5 - Control Status Register	ICS45			RW
00004DH	ICU4/ICU5 - Edge register	ICE45			RW
00004EH	ICU4 - Capture Register	IPCPL4	IPCP4		R
00004FH	ICU4 - Capture Register	IPCPH4			R
000050H	ICU5 - Capture Register	IPCPL5	IPCP5		R
000051H	ICU5 - Capture Register	IPCPH5			R
000052H	ICU6/ICU7 - Control Status Register	ICS67			RW
000053H	ICU6/ICU7 - Edge register	ICE67			RW
000054H	ICU6 - Capture Register	IPCPL6	IPCP6		R
000055H	ICU6 - Capture Register	IPCPH6			R
000056H	ICU7 - Capture Register	IPCPL7	IPCP7		R
000057H	ICU7 - Capture Register	IPCPH7			R
000058H	EXTINT0 - External Interrupt Enable Register	ENIR0			RW

I/O map (4 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
000059H	EXTINT0 - External Interrupt Interrupt request Register	EIRR0			RW
00005AH	EXTINT0 - External Interrupt Level Select	ELVRL0	ELVR0		RW
00005BH	EXTINT0 - External Interrupt Level Select	ELVRH0			RW
00005CH	EXTINT1 - External Interrupt Enable Register	ENIR1			RW
00005DH	EXTINT1 - External Interrupt Interrupt request Register	EIRR1			RW
00005EH	EXTINT1 - External Interrupt Level Select	ELVRL1	ELVR1		RW
00005FH	EXTINT1 - External Interrupt Level Select	ELVRH1			RW
000060H	RLT0 - Timer Control Status Register Low	TMCSRL0	TMCSR0		RW
000061H	RLT0 - Timer Control Status Register High	TMCSRH0			RW
000062H	RLT0 - Reload Register Low	TMRLR0	TMR0		RW
000063H	RLT0 - Reload Register High	TMRHR0			RW
000064H	RLT1 - Timer Control Status Register Low	TMCSRL1	TMCSR1		RW
000065H	RLT1 - Timer Control Status Register High	TMCSRH1			RW
000066H	RLT1 - Reload Register Low	TMRLR1	TMR1		RW
000067H	RLT1 - Reload Register High	TMRHR1			RW
000068H	RLT2 - Timer Control Status Register Low	TMCSRL2	TMCSR2		RW
000069H	RLT2 - Timer Control Status Register High	TMCSRH2			RW
00006AH	RLT2 - Reload Register Low	TMRLR2	TMR2		RW
00006BH	RLT2 - Reload Register High	TMRHR2			RW
00006CH	RLT3 - Timer Control Status Register Low	TMCSRL3	TMCSR3		RW
00006DH	RLT3 - Timer Control Status Register High	TMCSRH3			RW

I/O map (5 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
00006EH	RLT3 - Reload Register Low	TMRLR3	TMR3		RW
00006FH	RLT3 - Reload Register High	TMRHR3			RW
000070H	RLT6 - Timer Control Status Register Low (dedic. RLT for PPG)	TMCSRL6	TMCSR6		RW
000071H	RLT6 - Timer Control Status Register High (dedic. RLT for PPG)	TMCSRH6			RW
000072H	RLT6 - Reload Register Low (dedic. RLT for PPG) - for writing		TMRLR6		RW
000072H	RLT6 - Reload Register Low (dedic. RLT for PPG) - for reading		TMR6		RW
000073H	RLT6 - Reload Register High (dedic. RLT for PPG) - for writing				RW
000073H	RLT6 - Reload Register High (dedic. RLT for PPG) - for reading				RW
000074H	PPG3-PPG0 - General Control register 1 Low	GCN1L0	GCN10		RW
000075H	PPG3-PPG0 - General Control register 1 High	GCN1H0			RW
000076H	PPG3-PPG0 - General Control register 2 Low	GCN2L0	GCN20		RW
000077H	PPG3-PPG0 - General Control register 2 High	GCN2H0			RW
000078H	PPG0 - Timer register		PTMR0		R
000079H	PPG0 - Timer register				R
00007AH	PPG0 - Period setting register		PCSR0		W
00007BH	PPG0 - Period setting register				W
00007CH	PPG0 - Duty cycle register		PDUT0		W
00007DH	PPG0 - Duty cycle register				W
00007EH	PPG0 - Control status register	PCNL0	PCN0		RW
00007FH	PPG0 - Control status register	PCNH0			RW
000080H	PPG1 - Timer register		PTMR1		R
000081H	PPG1 - Timer register				R
000082H	PPG1 - Period setting register		PCSR1		W
000083H	PPG1 - Period setting register				W

I/O map (6 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
000084H	PPG1 - Duty cycle register		PDUT1		W
000085H	PPG1 - Duty cycle register				W
000086H	PPG1 - Control status register	PCNL1	PCN1		RW
000087H	PPG1 - Control status register	PCNH1			RW
000088H	PPG2 - Timer register		PTMR2		R
000089H	PPG2 - Timer register				R
00008AH	PPG2 - Period setting register		PCSR2		W
00008BH	PPG2 - Period setting register				W
00008CH	PPG2 - Duty cycle register		PDUT2		W
00008DH	PPG2 - Duty cycle register				W
00008EH	PPG2 - Control status register	PCNL2	PCN2		RW
00008FH	PPG2 - Control status register	PCNH2			RW
000090H	PPG3 - Timer register		PTMR3		R
000091H	PPG3 - Timer register				R
000092H	PPG3 - Period setting register		PCSR3		W
000093H	PPG3 - Period setting register				W
000094H	PPG3 - Duty cycle register		PDUT3		W
000095H	PPG3 - Duty cycle register				W
000096H	PPG3 - Control status register	PCNL3	PCN3		RW
000097H	PPG3 - Control status register	PCNH3			RW
000098H	PPG7-PPG4 - General Control register 1 Low	GCN1L1	GCN11		RW
000099H	PPG7-PPG4 - General Control register 1 High	GCN1H1			RW
00009AH	PPG7-PPG4 - General Control register 2 Low	GCN2L1	GCN21		RW
00009BH	PPG7-PPG4 - General Control register 2 High	GCN2H1			RW
00009CH	PPG4 - Timer register		PTMR4		R
00009DH	PPG4 - Timer register				R
00009EH	PPG4 - Period setting register		PCSR4		W

I/O map (7 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
00009FH	PPG4 - Period setting register				W
0000A0H	PPG4 - Duty cycle register		PDUT4		W
0000A1H	PPG4 - Duty cycle register				W
0000A2H	PPG4 - Control status register	PCNL4	PCN4		RW
0000A3H	PPG4 - Control status register	PCNH4			RW
0000A4H	PPG5 - Timer register		PTMR5		R
0000A5H	PPG5 - Timer register				R
0000A6H	PPG5 - Period setting register		PCSR5		W
0000A7H	PPG5 - Period setting register				W
0000A8H	PPG5 - Duty cycle register		PDUT5		W
0000A9H	PPG5 - Duty cycle register				W
0000AAH	PPG5 - Control status register	PCNL5	PCN5		RW
0000ABH	PPG5 - Control status register	PCNH5			RW
0000ACH	I2C0 - Bus Status Register	IBSR0			R
0000ADH	I2C0 - Bus Control Register	IBCR0			RW
0000AEH	I2C0 - Ten bit Slave address Register Low	ITBAL0	ITBA0		RW
0000AFH	I2C0 - Ten bit Slave address Register High	ITBAH0			RW
0000B0H	I2C0 - Ten bit Address mask Register Low	ITMKL0	ITMK0		RW
0000B1H	I2C0 - Ten bit Address mask Register High	ITMKH0			RW
0000B2H	I2C0 - Seven bit Slave address Register	ISBA0			RW
0000B3H	I2C0 - Seven bit Address mask Register	ISMK0			RW
0000B4H	I2C0 - Data Register	IDAR0			RW
0000B5H	I2C0 - Clock Control Register	ICCR0			RW
0000B6H	I2C1 - Bus Status Register	IBSR1			R
0000B7H	I2C1 - Bus Control Register	IBCR1			RW
0000B8H	I2C1 - Ten bit Slave address Register Low	ITBAL1	ITBA1		RW

I/O map (8 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
0000B9H	I2C1 - Ten bit Slave address Register High	ITBAH1			RW
0000BAH	I2C1 - Ten bit Address mask Register Low	ITMKL1	ITMK1		RW
0000BBH	I2C1 - Ten bit Address mask Register High	ITMKH1			RW
0000BCH	I2C1 - Seven bit Slave address Register	ISBA1			RW
0000BDH	I2C1 - Seven bit Address mask Register	ISMK1			RW
0000BEH	I2C1 - Data Register	IDAR1			RW
0000BFH	I2C1 - Clock Control Register	ICCR1			RW
0000C0H	USART0 USART - Serial Mode Register	SMR0			RW
0000C1H	USART0 - Serial Control Register	SCR0			RW
0000C2H	USART0 - TX Register	TDR0			W
0000C2H	USART0 - RX Register	RDR0			R
0000C3H	USART0 - Serial Status	SSR0			RW
0000C4H	USART0 - Control/Com. Register	ECCR0			RW
0000C5H	USART0 - Ext. Status Register	ESCR0			RW
0000C6H	USART0 - Baud Rate Generator Register Low	BGRL0	BGR0		RW
0000C7H	USART0 - Baud Rate Generator Register High	BGRH0			RW
0000C8H	USART0 - Extended Serial Interrupt Register	ESIR0			RW
0000C9H	Reserved				
0000CAH	USART1 - Serial Mode Register	SMR1			RW
0000CBH	USART1 - Serial Control Register	SCR1			RW
0000CCH	USART1 - TX Register	TDR1			W
0000CCH	USART1 - RX Register	RDR1			R
0000CDH	USART1 - Serial Status	SSR1			RW
0000CEH	USART1 - Control/Com. Register	ECCR1			RW

I/O map (9 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
0000CFH	USART1 - Ext. Status Register	ESCR1			RW
0000D0H	USART1 - Baud Rate Generator Register Low	BGRL1	BGR1		RW
0000D1H	USART1 - Baud Rate Generator Register High	BGRH1			RW
0000D2H	USART1 - Extended Serial Interrupt Register	ESIR1			RW
0000D3H	Reserved				
0000D4H	USART2 - Serial Mode Register	SMR2			RW
0000D5H	USART2 - Serial Control Register	SCR2			RW
0000D6H	USART2 - TX Register	TDR2			W
0000D6H	USART2 - RX Register	RDR2			R
0000D7H	USART2 - Serial Status	SSR2			RW
0000D8H	USART2 - Control/Com. Register	ECCR2			RW
0000D9H	USART2 - Ext. Status Register	ESCR2			RW
0000DAH	USART2 - Baud Rate Generator Register Low	BGRL2	BGR2		RW
0000DBH	USART2 - Baud Rate Generator Register High	BGRH2			RW
0000DCH	USART2 - Extended Serial Interrupt Register	ESIR2			RW
0000DDH	Reserved				
0000DEH	USART3 - Serial Mode Register	SMR3			RW
0000DFH	USART3 - Serial Control Register	SCR3			RW
0000E0H	USART3 - TX Register	TDR3			W
0000E0H	USART3 - RX Register	RDR3			R
0000E1H	USART3 - Serial Status	SSR3			RW
0000E2H	USART3 - Control/Com. Register	ECCR3			RW
0000E3H	USART3 - Ext. Status Register	ESCR3			RW
0000E4H	USART3 - Baud Rate Generator Register Low	BGRL3	BGR3		RW
0000E5H	USART3 - Baud Rate Generator Register High	BGRH3			RW

I/O map (10 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
0000E6H	USART3 - Extended Serial Interrupt Register	ESIR3			RW
0000F0H	external bus	EXTBUS0			RW
000100H	DMA0 - Buffer address pointer low byte	BAPL0			RW
000101H	DMA0 - Buffer address pointer middle byte	BAPM0			RW
000102H	DMA0 - Buffer address pointer high byte	BAPH0			RW
000103H	DMA0 - DMA control register	DMACS0			RW
000104H	DMA0 - I/O register address pointer low byte	IOAL0	IOA0		RW
000105H	DMA0 - I/O register address pointer high byte	IOAH0			RW
000106H	DMA0 - Data counter low byte	DCTL0	DCT0		RW
000107H	DMA0 - Data counter high byte	DCTH0			RW
000108H	DMA1 - Buffer address pointer low byte	BAPL1			RW
000109H	DMA1 - Buffer address pointer middle byte	BAPM1			RW
00010AH	DMA1 - Buffer address pointer high byte	BAPH1			RW
00010BH	DMA1 - DMA control register	DMACS1			RW
00010CH	DMA1 - I/O register address pointer low byte	IOAL1	IOA1		RW
00010DH	DMA1 - I/O register address pointer high byte	IOAH1			RW
00010EH	DMA1 - Data counter low byte	DCTL1	DCT1		RW
00010FH	DMA1 - Data counter high byte	DCTH1			RW
000110H	DMA2 - Buffer address pointer low byte	BAPL2			RW
000111H	DMA2 - Buffer address pointer middle byte	BAPM2			RW
000112H	DMA2 - Buffer address pointer high byte	BAPH2			RW
000113H	DMA2 - DMA control register	DMACS2			RW
000114H	DMA2 - I/O register address pointer low byte	IOAL2	IOA2		RW

I/O map (11 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
000115H	DMA2 - I/O register address pointer high byte	IOAH2			RW
000116H	DMA2 - Data counter low byte	DCTL2	DCT2		RW
000117H	DMA2 - Data counter high byte	DCTH2			RW
000118H	DMA3 - Buffer address pointer low byte	BAPL3			RW
000119H	DMA3 - Buffer address pointer middle byte	BAPM3			RW
00011AH	DMA3 - Buffer address pointer high byte	BAPH3			RW
00011BH	DMA3 - DMA control register	DMACS3			RW
00011CH	DMA3 - I/O register address pointer low byte	IOAL3	IOA3		RW
00011DH	DMA3 - I/O register address pointer high byte	IOAH3			RW
00011EH	DMA3 - Data counter low byte	DCTL3	DCT3		RW
00011FH	DMA3 - Data counter high byte	DCTH3			RW
000120H	DMA4 - Buffer address pointer low byte	BAPL4			RW
000121H	DMA4 - Buffer address pointer middle byte	BAPM4			RW
000122H	DMA4 - Buffer address pointer high byte	BAPH4			RW
000123H	DMA4 - DMA control register	DMACS4			RW
000124H	DMA4 - I/O register address pointer low byte	IOAL4	IOA4		RW
000125H	DMA4 - I/O register address pointer high byte	IOAH4			RW
000126H	DMA4 - Data counter low byte	DCTL4	DCT4		RW
000127H	DMA4 - Data counter high byte	DCTH4			RW
000128H	DMA5 - Buffer address pointer low byte	BAPL5			RW
000129H	DMA5 - Buffer address pointer middle byte	BAPM5			RW
00012AH	DMA5 - Buffer address pointer high byte	BAPH5			RW
00012BH	DMA5 - DMA control register	DMACS5			RW

I/O map (12 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
00012CH	DMA5 - I/O register address pointer low byte	IOAL5	IOA5		RW
00012DH	DMA5 - I/O register address pointer high byte	IOAH5			RW
00012EH	DMA5 - Data counter low byte	DCTL5	DCT5		RW
00012FH	DMA5 - Data counter high byte	DCTH5			RW
000180H	CPU - General Purpose registers (RAM access)	GPR_RAM			RW
000380H	DMA0 - Interrupt select	DISEL0			RW
000381H	DMA1 - Interrupt select	DISEL1			RW
000382H	DMA2 - Interrupt select	DISEL2			RW
000383H	DMA3 - Interrupt select	DISEL3			RW
000384H	DMA4 - Interrupt select	DISEL4			RW
000385H	DMA5 - Interrupt select	DISEL5			RW
000386H - 00038FH	Reserved				
000390H	DMA7-DMA0 - status register	DSRL	DSR		RW
000391H	Reserved				
000392H	DMA7-DMA0 - stop status register	DSSRL	DSSR		RW
000393H	Reserved				
000394H	DMA7-DMA0 - enable register	DERL	DER		RW
000395H - 000398H	Reserved				
000399H	Unused				
0003A0H	Interrupt level register	ILR	ICR		RW
0003A1H	Interrupt Index register	IDX			RW
0003A2H	Interrupt vector Table base register	TBRL	TBR		RW
0003A3H	Interrupt vector Table base register	TBRH			RW
0003A4H	Delayed Interrupt register	DIRR			RW
0003A5H	Non maskable Interrupt register	NMI			RW

I/O map (13 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
0003A6H - 0003ADH	Reserved				
0003AEH	ROM mirror control register	ROMM			RW
0003AFH	EDSU configuration register	EDSU			RW
0003B0H	Memory patch control/status register ch 0/1		PFCS0		RW
0003B1H	Memory patch control/status register ch 0/1				RW
0003B2H	Memory patch control/status register ch 2/3		PFCS1		RW
0003B3H	Memory patch control/status register ch 2/3				RW
0003B4H	Memory patch control/status register ch 4/5		PFCS2		RW
0003B5H	Memory patch control/status register ch 4/5				RW
0003B6H	Memory patch control/status register ch 6/7		PFCS3		RW
0003B7H	Memory patch control/status register ch 6/7				RW
0003B8H	Memory Patch function - Patch address 0 low	PFAL0			RW
0003B9H	Memory Patch function - Patch address 0 middle	PFAM0			RW
0003BAH	Memory Patch function - Patch address 0 high	PFAH0			RW
0003BBH	Memory Patch function - Patch address 1 low	PFAL1			RW
0003BCH	Memory Patch function - Patch address 1 middle	PFAM1			RW
0003BDH	Memory Patch function - Patch address 1 high	PFAH1			RW
0003BEH	Memory Patch function - Patch address 2 low	PFAL2			RW
0003BFH	Memory Patch function - Patch address 2 middle	PFAM2			RW

I/O map (14 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
0003C0H	Memory Patch function - Patch address 2 high	PFAH2			RW
0003C1H	Memory Patch function - Patch address 3 low	PFAL3			RW
0003C2H	Memory Patch function - Patch address 3 middle	PFAM3			RW
0003C3H	Memory Patch function - Patch address 3 high	PFAH3			RW
0003C4H	Memory Patch function - Patch address 4 low	PFAL4			RW
0003C5H	Memory Patch function - Patch address 4 middle	PFAM4			RW
0003C6H	Memory Patch function - Patch address 4 high	PFAH4			RW
0003C7H	Memory Patch function - Patch address 5 low	PFAL5			RW
0003C8H	Memory Patch function - Patch address 5 middle	PFAM5			RW
0003C9H	Memory Patch function - Patch address 5 high	PFAH5			RW
0003CAH	Memory Patch function - Patch address 6 low	PFAL6			RW
0003CBH	Memory Patch function - Patch address 6 middle	PFAM6			RW
0003CCH	Memory Patch function - Patch address 6 high	PFAH6			RW
0003CDH	Memory Patch function - Patch address 7 low	PFAL7			RW
0003CEH	Memory Patch function - Patch address 7 middle	PFAM7			RW
0003CFH	Memory Patch function - Patch address 7 high	PFAH7			RW
0003D0H	Memory Patch function - Patch data 0	PFDL0	PFD0		RW
0003D1H	Memory Patch function - Patch data 0	PFDH0			RW
0003D2H	Memory Patch function - Patch data 1	PFDL1	PFD1		RW
0003D3H	Memory Patch function - Patch data 1	PFDH1			RW

I/O map (15 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
0003D4H	Memory Patch function - Patch data 2	PFDL2	PFD2		RW
0003D5H	Memory Patch function - Patch data 2	PFDH2			RW
0003D6H	Memory Patch function - Patch data 3	PFDL3	PFD3		RW
0003D7H	Memory Patch function - Patch data 3	PFDH3			RW
0003D8H	Memory Patch function - Patch data 4	PFDL4	PFD4		RW
0003D9H	Memory Patch function - Patch data 4	PFDH4			RW
0003DAH	Memory Patch function - Patch data 5	PFDL5	PFD5		RW
0003DBH	Memory Patch function - Patch data 5	PFDH5			RW
0003DCH	Memory Patch function - Patch data 6	PFDL6	PFD6		RW
0003DDH	Memory Patch function - Patch data 6	PFDH6			RW
0003DEH	Memory Patch function - Patch data 7	PFDL7	PFD7		RW
0003DFH	Memory Patch function - Patch data 7	PFDH7			RW
0003E0H - 0003EFH	Reserved				
0003F0H - 0003F2H	Reserved				
0003F3H	Flash Memory Timing Configuration register 1 (Main Flash)	MFMTCH			RW
0003F7H	Flash Memory Timing Configuration register 1 (Sat Flash)	SFMTCH			RW
0003F8H	Flash Memory Write Control register 0	FMWC0			RW
0003F9H	Flash Memory Write Control register 1	FMWC1			RW
0003FDH	Flash Memory Write Control register 5	FMWC5			RW
000401H	Clock select register	CKSR			RW
000402H	Clock Stabilisation select register	CKSSR			RW
000403H	Clock monitor register	CKMR			R
000404H	Clock Frequency control register Low	CKFCRL	CKFCR		RW
000405H	Clock Frequency control register High	CKFCRH			RW
000406H	PLL Control register Low	PLLCRL	PLLCR		RW
000408H	RC clock timer control register	RCTCR			RW

I/O map (16 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
000409H	Main clock timer control register	MCTCR			RW
00040AH	Sub clock timer control register	SCTCR			RW
00040BH	Reset cause and clock status register with clear function	RCCSRC			R
00040CH	Reset configuration register	RCR			RW
00040DH	Reset cause and clock status register	RCCSR			R
00040EH	Watch dog timer configuration register	WDTC			RW
00040FH	Watch dog timer clear pattern register	WDTCP			W
000410H - 000414H	Reserved				
000415H	Clock output activation register	COAR			RW
000416H	Clock output configuration register 0	COCR0			RW
000417H	Clock output configuration register 1	COCR1			RW
000418H	Clock Modulator control register	CMCR			RW
000419H	Unused				
00041AH	Clock Modulator Parameter register Low	CMPRL	CMPR		RW
00041BH	Clock Modulator Parameter register High	CMPRH			RW
00041CH - 00042BH	Reserved				
00042CH	Voltage Regulator Control register	VRCR			RW
00042DH - 00042FH	Reserved				
000430H	P00 - I/O Port Data Direction Register	DDR00			RW
000431H	P01 - I/O Port Data Direction Register	DDR01			RW
000432H	P02 - I/O Port Data Direction Register	DDR02			RW
000433H	P03 - I/O Port Data Direction Register	DDR03			RW
000434H	P04 - I/O Port Data Direction Register	DDR04			RW
000435H	P05 - I/O Port Data Direction Register	DDR05			RW

I/O map (17 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
000436H	P06 - I/O Port Data Direction Register	DDR06			RW
000437H	P07 - I/O Port Data Direction Register	DDR07			RW
000438H	P08 - I/O Port Data Direction Register	DDR08			RW
000439H	P09 - I/O Port Data Direction Register	DDR09			RW
00043AH	P10 - I/O Port Data Direction Register	DDR10			RW
00043BH - 000443H	Reserved				
000444H	P00 - I/O Port Port Input Enable Register	PIER00			RW
000445H	P01 - I/O Port Port Input Enable Register	PIER01			RW
000446H	P02 - I/O Port Port Input Enable Register	PIER02			RW
000447H	P03 - I/O Port Port Input Enable Register	PIER03			RW
000448H	P04 - I/O Port Port Input Enable Register	PIER04			RW
000449H	P05 - I/O Port Port Input Enable Register	PIER05			RW
00044AH	P06 - I/O Port Port Input Enable Register	PIER06			RW
00044BH	P07 - I/O Port Port Input Enable Register	PIER07			RW
00044CH	P08 - I/O Port Port Input Enable Register	PIER08			RW
00044DH	P09 - I/O Port Port Input Enable Register	PIER09			RW
00044EH	P10 - I/O Port Port Input Enable Register	PIER10			RW
00044FH - 000457H	Reserved				
000458H	P00 - I/O Port Port Input Level Register	PILR00			RW
000459H	P01 - I/O Port Port Input Level Register	PILR01			RW
00045AH	P02 - I/O Port Port Input Level Register	PILR02			RW

I/O map (18 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
00045BH	P03 - I/O Port Port Input Level Register	PILR03			RW
00045CH	P04 - I/O Port Port Input Level Register	PILR04			RW
00045DH	P05 - I/O Port Port Input Level Register	PILR05			RW
00045EH	P06 - I/O Port Port Input Level Register	PILR06			RW
00045FH	P07 - I/O Port Port Input Level Register	PILR07			RW
000460H	P08 - I/O Port Port Input Level Register	PILR08			RW
000461H	P09 - I/O Port Port Input Level Register	PILR09			RW
000462H	P10 - I/O Port Port Input Level Register	PILR10			RW
000463H - 00046BH	Reserved				
00046CH	P00 - I/O Port Extended Port Input Level Register	EPILR00			RW
00046DH	P01 - I/O Port Extended Port Input Level Register	EPILR01			RW
00046EH	P02 - I/O Port Extended Port Input Level Register	EPILR02			RW
00046FH	P03 - I/O Port Extended Port Input Level Register	EPILR03			RW
000470H	P04 - I/O Port Extended Port Input Level Register	EPILR04			RW
000471H	P05 - I/O Port Extended Port Input Level Register	EPILR05			RW
000472H	P06 - I/O Port Extended Port Input Level Register	EPILR06			RW
000473H	P07 - I/O Port Extended Port Input Level Register	EPILR07			RW
000474H	P08 - I/O Port Extended Port Input Level Register	EPILR08			RW
000475H	P09 - I/O Port Extended Port Input Level Register	EPILR09			RW
000476H	P10 - I/O Port Extended Port Input Level Register	EPILR10			RW
000477H - 00047FH	Reserved				

I/O map (19 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
000480H	P00 - I/O Port Port Output Drive Register	PODR00			RW
000481H	P01 - I/O Port Port Output Drive Register	PODR01			RW
000482H	P02 - I/O Port Port Output Drive Register	PODR02			RW
000483H	P03 - I/O Port Port Output Drive Register	PODR03			RW
000484H	P04 - I/O Port Port Output Drive Register	PODR04			RW
000485H	P05 - I/O Port Port Output Drive Register	PODR05			RW
000486H	P06 - I/O Port Port Output Drive Register	PODR06			RW
000487H	P07 - I/O Port Port Output Drive Register	PODR07			RW
000488H	P08 - I/O Port Port Output Drive Register	PODR08			RW
000489H	P09 - I/O Port Port Output Drive Register	PODR09			RW
00048AH	P10 - I/O Port Port Output Drive Register	PODR10			RW
00049CH - 0004A7H	Reserved				
0004A8H	P00 - I/O Port Pull-Up resistor Control Register	PUCR00			RW
0004A9H	P01 - I/O Port Pull-Up resistor Control Register	PUCR01			RW
0004AAH	P02 - I/O Port Pull-Up resistor Control Register	PUCR02			RW
0004ABH	P03 - I/O Port Pull-Up resistor Control Register	PUCR03			RW
0004ACH	P04 - I/O Port Pull-Up resistor Control Register	PUCR04			RW
0004ADH	P05 - I/O Port Pull-Up resistor Control Register	PUCR05			RW

I/O map (20 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
0004AEH	P06 - I/O Port Pull-Up resistor Control Register	PUCR06			RW
0004AFH	P07 - I/O Port Pull-Up resistor Control Register	PUCR07			RW
0004B0H	P08 - I/O Port Pull-Up resistor Control Register	PUCR08			RW
0004B1H	P09 - I/O Port Pull-Up resistor Control Register	PUCR09			RW
0004B2H	P10 - I/O Port Pull-Up resistor Control Register	PUCR10			RW
0004B3H - 0004BBH	Reserved				
0004BCH	P00 - I/O Port External Pin State Register	EPSR00			R
0004BDH	P01 - I/O Port External Pin State Register	EPSR01			R
0004BEH	P02 - I/O Port External Pin State Register	EPSR02			R
0004BFH	P03 - I/O Port External Pin State Register	EPSR03			R
0004C0H	P04 - I/O Port External Pin State Register	EPSR04			R
0004C1H	P05 - I/O Port External Pin State Register	EPSR05			R
0004C2H	P06 - I/O Port External Pin State Register	EPSR06			R
0004C3H	P07 - I/O Port External Pin State Register	EPSR07			R
0004C4H	P08 - I/O Port External Pin State Register	EPSR08			R
0004C5H	P09 - I/O Port External Pin State Register	EPSR09			R
0004C6H	P10 - I/O Port External Pin State Register	EPSR10			R
0004C7H - 0004CFH	Reserved				

I/O map (21 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
0004D0H	ADC analog input enable register 0	ADER0			RW
0004D1H	ADC analog input enable register 1	ADER1			RW
0004D2H	ADC analog input enable register 2	ADER2			RW
0004D3H - 0004D4H	Reserved				
0004D5H	Reserved				
0004D6H	Peripheral Resource Relocation Register 0	PRRR0			RW
0004D7H	Peripheral Resource Relocation Register 1	PRRR1			RW
0004D8H - 0004DBH	Reserved				
0004DCH	Peripheral Resource Relocation Register 6	PRRR6			RW
0004DDH	Peripheral Resource Relocation Register 7	PRRR7			RW
0004DEH	Peripheral Resource Relocation Register 8	PRRR8			RW
0004DFH	Peripheral Resource Relocation Register 9	PRRR9			RW
0004E0H	RTC - Sub Second Register L	WTBRL0	WTBR0		RW
0004E1H	RTC - Sub Second Register M	WTBRH0			RW
0004E2H	RTC - Sub-Second Register H	WTBR1			RW
0004E3H	RTC - Second Register	WTSR			RW
0004E4H	RTC - Minutes	WTMR			RW
0004E5H	RTC - Hour	WTHR			RW
0004E6H	RTC - Timer Control Extended Register	WTCER			RW
0004E7H	RTC - Clock select register	WTCKSR			RW
0004E8H	Reserved				
0004E9H	RTC - Timer Control Register H	WTCRH			RW
0004EAH	CAL - Calibration unit Control register	CUCR			RW

I/O map (22 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
0004EBH	Reserved				
0004ECH	CAL - Sub/RC-clock timer data register L	CUTDL	CUTD		RW
0004EDH	CAL - Sub/RC-clock timer data register H	CUTDH			RW
0004EEH	CAL - Main clock timer data register 2 L	CUTR2L	CUTR2		R
0004EFH	CAL - Main clock timer data register 2 H	CUTR2H			R
0004F0H	CAL - Main clock timer data register 1 L	CUTR1L	CUTR1		R
0004F1H	CAL - Main clock timer data register 1 H	CUTR1H			R
0004F2H - 0004F9H	Reserved				
0004FAH	RLT - Timer input select (for Cascading)	TMISR			RW
0004FBH - 00053DH	Reserved				
00053EH	USART7 - Serial Mode Register	SMR7			RW
00053FH	USART7 - Serial Control Register	SCR7			RW
000540H	USART7 - Serial TX Register	TDR7			W
000540H	USART7 - Serial RX Register	RDR7			R
000541H	USART7 - Serial Status Register	SSR7			RW
000542H	USART7 - Ext. Control/Com. Register	ECCR7			RW
000543H	USART7 - Ext. Status Com. Register	ESCR7			RW
000544H	USART7 - Baud Rate Generator Register	BGRL7	BGR7		RW
000545H	USART7 - Baud Rate Generator Register	BGRH7			RW
000546H	USART7 - Extended Serial Interrupt Register	ESIR7			RW
000548H	USART8 - Serial Mode Register	SMR8			RW

I/O map (23 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
000549H	USART8 - Serial Control Register	SCR8			RW
00054AH	USART8 - Serial TX Register	TDR8			W
00054AH	USART8 - Serial RX Register	RDR8			R
00054BH	USART8 - Serial Status Register	SSR8			RW
00054CH	USART8 - Ext. Control/Com. Register	ECCR8			RW
00054DH	USART8 - Ext. Status Com. Register	ESCR8			RW
00054EH	USART8 - Baud Rate Generator Register	BGRL8	BGR8		RW
00054FH	USART8 - Baud Rate Generator Register	BGRH8			RW
000550H	USART8 - Extended Serial Interrupt Register	ESIR8			RW
000552H	USART9 - Serial Mode Register	SMR9			RW
000553H	USART9 - Serial Control Register	SCR9			RW
000554H	USART9 - Serial TX Register	TDR9			W
000554H	USART9 - Serial RX Register	RDR9			R
000555H	USART9 - Serial Status Register	SSR9			RW
000556H	USART9 - Ext. Control/Com. Register	ECCR9			RW
000557H	USART9 - Ext. Status Com. Register	ESCR9			RW
000558H	USART9 - Baud Rate Generator Register	BGRL9	BGR9		RW
000559H	USART9 - Baud Rate Generator Register	BGRH9			RW
00055AH	USART9 - Extended Serial Interrupt Register	ESIR9			RW
000560H	ALARM0 - Control Status Register	ACSR0			RW
000561H	ALARM0 - Extended Control Status Register	AECSR0			RW
000562H	ALARM1 - Control Status Register	ACSR1			RW
000563H	ALARM1 - Extended Control Status Register	AECSR1			RW
000564H	PPG6 - Timer register		PTMR6		R
000565H	PPG6 - Timer register				R

I/O map (24 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
000566H	PPG6 - Period setting register		PCSR6		W
000567H	PPG6 - Period setting register				W
000568H	PPG6 - Duty cycle register		PDUT6		W
000569H	PPG6 - Duty cycle register				W
00056AH	PPG6 - Control status register	PCNL6	PCN6		RW
00056BH	PPG6 - Control status register	PCNH6			RW
00056CH	PPG7 - Timer register		PTMR7		R
00056DH	PPG7 - Timer register				R
00056EH	PPG7 - Period setting register		PCSR7		W
00056FH	PPG7 - Period setting register				W
000570H	PPG7 - Duty cycle register		PDUT7		W
000571H	PPG7 - Duty cycle register				W
000572H	PPG7 - Control status register	PCNL7	PCN7		RW
000573H	PPG7 - Control status register	PCNH7			RW
000574H	PPG11-PPG8 - General Control register 1 Low	GCN1L2	GCN12		RW
000575H	PPG11-PPG8 - General Control register 1 High	GCN1H2			RW
000576H	PPG11-PPG8 - General Control register 2 Low	GCN2L2	GCN22		RW
000577H	PPG11-PPG8 - General Control register 2 High	GCN2H2			RW
000578H	PPG8 - Timer register		PTMR8		R
000579H	PPG8 - Timer register				R
00057AH	PPG8 - Period setting register		PCSR8		W
00057BH	PPG8 - Period setting register				W
00057CH	PPG8 - Duty cycle register		PDUT8		W
00057DH	PPG8 - Duty cycle register				W
00057EH	PPG8 - Control status register	PCNL8	PCN8		RW
00057FH	PPG8 - Control status register	PCNH8			RW
000580H	PPG9 - Timer register		PTMR9		R

I/O map (25 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
000581H	PPG9 - Timer register				R
000582H	PPG9 - Period setting register		PCSR9		W
000583H	PPG9 - Period setting register				W
000584H	PPG9 - Duty cycle register		PDUT9		W
000585H	PPG9 - Duty cycle register				W
000586H	PPG9 - Control status register	PCNL9	PCN9		RW
000587H	PPG9 - Control status register	PCNH9			RW
000588H	PPG10 - Timer register		PTMR10		R
000589H	PPG10 - Timer register				R
00058AH	PPG10 - Period setting register		PCSR10		W
00058BH	PPG10 - Period setting register				W
00058CH	PPG10 - Duty cycle register		PDUT10		W
00058DH	PPG10 - Duty cycle register				W
00058EH	PPG10 - Control status register	PCNL10	PCN10		RW
00058FH	PPG10 - Control status register	PCNH10			RW
000590H	PPG11 - Timer register		PTMR11		R
000591H	PPG11 - Timer register				R
000592H	PPG11 - Period setting register		PCSR11		W
000593H	PPG11 - Period setting register				W
000594H	PPG11 - Duty cycle register		PDUT11		W
000595H	PPG11 - Duty cycle register				W
000596H	PPG11 - Control status register	PCNL11	PCN11		RW
000597H	PPG11 - Control status register	PCNH11			RW
000598H	PPG15-PPG12 - General Control register 1 Low	GCN1L3	GCN13		RW
000599H	PPG15-PPG12 - General Control register 1 High	GCN1H3			RW
00059AH	PPG15-PPG12 - General Control register 2 Low	GCN2L3	GCN23		RW
00059BH	PPG15-PPG12 - General Control register 2 High	GCN2H3			RW

I/O map (26 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
00059CH	PPG12 - Timer register		PTMR12		R
00059DH	PPG12 - Timer register				R
00059EH	PPG12 - Period setting register		PCSR12		W
00059FH	PPG12 - Period setting register				W
0005A0H	PPG12 - Duty cycle register		PDUT12		W
0005A1H	PPG12 - Duty cycle register				W
0005A2H	PPG12 - Control status register	PCNL12	PCN12		RW
0005A3H	PPG12 - Control status register	PCNH12			RW
0005A4H	PPG13 - Timer register		PTMR13		R
0005A5H	PPG13 - Timer register				R
0005A6H	PPG13 - Period setting register		PCSR13		W
0005A7H	PPG13 - Period setting register				W
0005A8H	PPG13 - Duty cycle register		PDUT13		W
0005A9H	PPG13 - Duty cycle register				W
0005AAH	PPG13 - Control status register	PCNL13	PCN13		RW
0005ABH	PPG13 - Control status register	PCNH13			RW
0005ACH	PPG14 - Timer register		PTMR14		R
0005ADH	PPG14 - Timer register				R
0005AEH	PPG14 - Period setting register		PCSR14		W
0005AFH	PPG14 - Period setting register				W
0005B0H	PPG14 - Duty cycle register		PDUT14		W
0005B1H	PPG14 - Duty cycle register				W
0005B2H	PPG14 - Control status register	PCNL14	PCN14		RW
0005B3H	PPG14 - Control status register	PCNH14			RW
0005B4H	PPG15 - Timer register		PTMR15		R
0005B5H	PPG15 - Timer register				R
0005B6H	PPG15 - Period setting register		PCSR15		W
0005B7H	PPG15 - Period setting register				W
0005B8H	PPG15 - Duty cycle register		PDUT15		W
0005B9H	PPG15 - Duty cycle register				W

I/O map (27 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
0005BAH	PPG15 - Control status register	PCNL15	PCN15		RW
0005BBH	PPG15 - Control status register	PCNH15			RW
0005BCH - 0006DFH	Reserved				
0006E0H	External bus Area configuration register 0	EACL0	EAC0		RW
0006E1H	External bus Area configuration register 0	EACH0			RW
0006E2H	External bus Area configuration register 1	EACL1	EAC1		RW
0006E3H	External bus Area configuration register 1	EACH1			RW
0006E4H	External bus Area configuration register 2	EACL2	EAC2		RW
0006E5H	External bus Area configuration register 2	EACH2			RW
0006E6H	External bus Area configuration register 3	EACL3	EAC3		RW
0006E7H	External bus Area configuration register 3	EACH3			RW
0006E8H	External bus Area configuration register 4	EACL4	EAC4		RW
0006E9H	External bus Area configuration register 4	EACH4			RW
0006EAH	External bus Area configuration register 5	EACL5	EAC5		RW
0006EBH	External bus Area configuration register 5	EACH5			RW
0006ECH	External bus Area select register 2	EAS2			RW
0006EDH	External bus Area select register 3	EAS3			RW
0006EEH	External bus Area select register 4	EAS4			RW
0006EFH	External bus Area select register 5	EAS5			RW
0006F0H	External bus Mode register	EBM			RW
0006F1H	External bus Clock and Function register	EBCF			RW

I/O map (28 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
0006F2H	External bus Address output enable register 0	EBAE0			RW
0006F3H	External bus Address output enable register 1	EBAE1			RW
0006F4H	External bus Address output enable register 2	EBAE2			RW
0006F5H	External bus Control signal register	EBCS			RW
0006F6H - 0006FFH	Reserved				
000700H	CAN0 - Control register	CTRLRL0	CTRLR0		RW
000701H	CAN0 - Control register	CTRLRH0			R
000702H	CAN0 - Status register	STATRL0	STATR0		RW
000703H	CAN0 - Status register	STATRH0			R
000704H	CAN0 - Error Counter (Transmit)	ERRCNTL0	ERRCNT0		R
000705H	CAN0 - Error Counter (Receive)	ERRCNTH0			R
000706H	CAN0 - Bit Timing Register	BTRL0	BTR0		RW
000707H	CAN0 - Bit Timing Register	BTRH0			RW
000708H	CAN0 - Interrupt Register	INTRL0	INTR0		R
000709H	CAN0 - Interrupt Register	INTRH0			R
00070AH	CAN0 - Test Register	TESTRL0	TESTR0		RW
00070BH	CAN0 - Test Register	TESTRH0			R
00070CH	CAN0 - BRP Extension register	BRPERL0	BRPER0		RW
00070DH	CAN0 - BRP Extension register	BRPERH0			R
00070EH - 00070FH	Reserved				
000710H	CAN0 - IF1 Command request register	IF1CREQL0	IF1CREQ0		RW
000711H	CAN0 - IF1 Command request register	IF1CREQH0			RW
000712H	CAN0 - IF1 Command Mask register	IF1CMSKL0	IF1CMSK0		RW
000713H	CAN0 - IF1 Command Mask register	IF1CMSKH0			R
000714H	CAN0 - IF1 Mask Register	IF1MSK1L0	IF1MSK10	IF1MSK0	RW
000715H	CAN0 - IF1 Mask Register	IF1MSK1H0			RW

I/O map (29 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
000716H	CAN0 - IF1 Mask Register	IF1MSK2L0	IF1MSK20		RW
000717H	CAN0 - IF1 Mask Register	IF1MSK2H0			RW
000718H	CAN0 - IF1 Arbitration register	IF1ARB1L0	IF1ARB10	1F1ARB0	RW
000719H	CAN0 - IF1 Arbitration register	IF1ARB1H0			RW
00071AH	CAN0 - IF1 Arbitration register	IF1ARB2L0	IF1ARB20		RW
00071BH	CAN0 - IF1 Arbitration register	IF1ARB2H0			RW
00071CH	CAN0 - IF1 Message Control Register	IF1MCTRL0	IF1MCTR0		RW
00071DH	CAN0 - IF1 Message Control Register	IF1MCTRH0			RW
00071EH	CAN0 - IF1 Data A1	IF1DTA1L0	IF1DTA10	IF1DTA0	RW
00071FH	CAN0 - IF1 Data A1	IF1DTA1H0			RW
000720H	CAN0 - IF1 Data A2	IF1DTA2L0	IF1DTA20		RW
000721H	CAN0 - IF1 Data A2	IF1DTA2H0			RW
000722H	CAN0 - IF1 Data B1	IF1DTB1L0	IF1DTB10	IF1DTB0	RW
000723H	CAN0 - IF1 Data B1	IF1DTB1H0			RW
000724H	CAN0 - IF1 Data B2	IF1DTB2L0	IF1DTB20		RW
000725H	CAN0 - IF1 Data B2	IF1DTB2H0			RW
000726H - 00073FH	Reserved				
000740H	CAN0 - IF2 Command request register	IF2CREQL0	IF2CREQ0		RW
000741H	CAN0 - IF2 Command request register	IF2CREQH0			RW
000742H	CAN0 - IF2 Command Mask register	IF2CMSKL0	IF2CMSK0		RW
000743H	CAN0 - IF2 Command Mask register	IF2CMSKH0			R
000744H	CAN0 - IF2 Mask Register	IF2MSK1L0	IF2MSK10	IF2MSK0	RW
000745H	CAN0 - IF2 Mask Register	IF2MSK1H0			RW
000746H	CAN0 - IF2 Mask Register	IF2MSK2L0	IF2MSK20		RW
000747H	CAN0 - IF2 Mask Register	IF2MSK2H0			RW
000748H	CAN0 - IF2 Arbitration register	IF2ARB1L0	IF2ARB10	IF2ARB0	RW
000749H	CAN0 - IF2 Arbitration register	IF2ARB1H0			RW
00074AH	CAN0 - IF2 Arbitration register	IF2ARB2L0	IF2ARB20		RW
00074BH	CAN0 - IF2 Arbitration register	IF2ARB2H0			RW

I/O map (30 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
00074CH	CAN0 - IF2 Message Control Register	IF2MCTRL0	IF2MCTR0		RW
00074DH	CAN0 - IF2 Message Control Register	IF2MCTRH0			RW
00074EH	CAN0 - IF2 Data A1	IF2DTA1L0	IF2DTA10	IF2DTA0	RW
00074FH	CAN0 - IF2 Data A1	IF2DTA1H0			RW
000750H	CAN0 - IF2 Data A2	IF2DTA2L0	IF2DTA20		RW
000751H	CAN0 - IF2 Data A2	IF2DTA2H0			RW
000752H	CAN0 - IF2 Data B1	IF2DTB1L0	IF2DTB10	IF2DTB0	RW
000753H	CAN0 - IF2 Data B1	IF2DTB1H0			RW
000754H	CAN0 - IF2 Data B2	IF2DTB2L0	IF2DTB20		RW
000755H	CAN0 - IF2 Data B2	IF2DTB2H0			RW
000756H - 000779H	Reserved				
000780H	CAN0 - Transmission Request Register	TREQR1L0	TREQR10	TREQR0	R
000781H	CAN0 - Transmission Request Register	TREQR1H0			R
000782H	CAN0 - Transmission Request Register	TREQR2L0	TREQR20		R
000783H	CAN0 - Transmission Request Register	TREQR2H0			R
000784H - 00078FH	Reserved				
000790H	CAN0 - New Data Register	NEWDT1L0	NEWDT10	NEWDT0	R
000791H	CAN0 - New Data Register	NEWDT1H0			R
000792H	CAN0 - New Data Register	NEWDT2L0	NEWDT20		R
000793H	CAN0 - New Data Register	NEWDT2H0			R
000794H - 00079FH	Reserved				
0007A0H	CAN0 - Interrupt Pending Register	INTPND1L0	INTPND10	INTPND0	R
0007A1H	CAN0 - Interrupt Pending Register	INTPND1H0			R
0007A2H	CAN0 - Interrupt Pending Register	INTPND2L0	INTPND20		R

I/O map (31 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
0007A3H	CAN0 - Interrupt Pending Register	INTPND2H0			R
0007A4H - 0007AFH	Reserved				
0007B0H	CAN0 - Message Valid Register	MSGVAL1L0	MSGVAL10	MSGVAL0	R
0007B1H	CAN0 - Message Valid Register	MSGVAL1H0			R
0007B2H	CAN0 - Message Valid Register	MSGVAL2L0	MSGVAL20		R
0007B3H	CAN0 - Message Valid Register	MSGVAL2H0			R
0007B4H - 0007CDH	Reserved				
0007CEH	CAN0 - Output enable register	COER0			RW
0007CFH - 0007FFH	Reserved				
000800H	CAN1 - Control register	CTRLRL1	CTRLR1		RW
000801H	CAN1 - Control register	CTRLRH1			R
000802H	CAN1 - Status register	STATRL1	STATR1		RW
000803H	CAN1 - Status register	STATRH1			R
000804H	CAN1 - Error Counter (Transmit)	ERRCNTL1	ERRCNT1		R
000805H	CAN1 - Error Counter (Receive)	ERRCNTH1			R
000806H	CAN1 - Bit Timing Register	BTRL1	BTR1		RW
000807H	CAN1 - Bit Timing Register	BTRH1			RW
000808H	CAN1 - Interrupt Register	INTRL1	INTR1		R
000809H	CAN1 - Interrupt Register	INTRH1			R
00080AH	CAN1 - Test Register	TESTRL1	TESTR1		RW
00080BH	CAN1 - Test Register	TESTRH1			R
00080CH	CAN1 - BRP Extension register	BRPERL1	BRPER1		RW
00080DH	CAN1 - BRP Extension register	BRPERH1			R
00080EH - 00080FH	Reserved				
000810H	CAN1 - IF1 Command request register	IF1CREQL1	IF1CREQ1		RW

I/O map (32 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
000811H	CAN1 - IF1 Command request register	IF1CREQH1			RW
000812H	CAN1 - IF1 Command Mask register	IF1CMSKL1	IF1CMSK1		RW
000813H	CAN1 - IF1 Command Mask register	IF1CMSKH1			R
000814H	CAN1 - IF1 Mask Register	IF1MSK1L1	IF1MSK11		RW
000815H	CAN1 - IF1 Mask Register	IF1MSK1H1			RW
000816H	CAN1 - IF1 Mask Register	IF1MSK2L1	IF1MSK21		RW
000817H	CAN1 - IF1 Mask Register	IF1MSK2H1			RW
000818H	CAN1 - IF1 Arbitration register	IF1ARB1L1	IF1ARB11		RW
000819H	CAN1 - IF1 Arbitration register	IF1ARB1H1			RW
00081AH	CAN1 - IF1 Arbitration register	IF1ARB2L1	IF1ARB21		RW
00081BH	CAN1 - IF1 Arbitration register	IF1ARB2H1			RW
00081CH	CAN1 - IF1 Message Control Register	IF1MCTRL1	IF1MCTR1		RW
00081DH	CAN1 - IF1 Message Control Register	IF1MCTRH1			RW
00081EH	CAN1 - IF1 Data A1	IF1DTA1L1	IF1DTA11		RW
00081FH	CAN1 - IF1 Data A1	IF1DTA1H1			RW
000820H	CAN1 - IF1 Data A2	IF1DTA2L1	IF1DTA21		RW
000821H	CAN1 - IF1 Data A2	IF1DTA2H1			RW
000822H	CAN1 - IF1 Data B1	IF1DTB1L1	IF1DTB11		RW
000823H	CAN1 - IF1 Data B1	IF1DTB1H1			RW
000824H	CAN1 - IF1 Data B2	IF1DTB2L1	IF1DTB21		RW
000825H	CAN1 - IF1 Data B2	IF1DTB2H1			RW
000826H - 00083FH	Reserved				
000840H	CAN1 - IF2 Command request register	IF2CREQL1	IF2CREQ1		RW
000841H	CAN1 - IF2 Command request register	IF2CREQH1			RW
000842H	CAN1 - IF2 Command Mask register	IF2CMSKL1	IF2CMSK1		RW
000843H	CAN1 - IF2 Command Mask register	IF2CMSKH1			R
000844H	CAN1 - IF2 Mask Register	IF2MSK1L1	IF2MSK11		RW
000845H	CAN1 - IF2 Mask Register	IF2MSK1H1			RW
000846H	CAN1 - IF2 Mask Register	IF2MSK2L1	IF2MSK21		RW

I/O map (33 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
000847H	CAN1 - IF2 Mask Register	IF2MSK2H1			RW
000848H	CAN1 - IF2 Arbitration register	IF2ARB1L1	IF2ARB11		RW
000849H	CAN1 - IF2 Arbitration register	IF2ARB1H1			RW
00084AH	CAN1 - IF2 Arbitration register	IF2ARB2L1	IF2ARB21		RW
00084BH	CAN1 - IF2 Arbitration register	IF2ARB2H1			RW
00084CH	CAN1 - IF2 Message Control Register	IF2MCTRL1	IF2MCTR1		RW
00084DH	CAN1 - IF2 Message Control Register	IF2MCTRH1			RW
00084EH	CAN1 - IF2 Data A1	IF2DTA1L1	IF2DTA11		RW
00084FH	CAN1 - IF2 Data A1	IF2DTA1H1			RW
000850H	CAN1 - IF2 Data A2	IF2DTA2L1	IF2DTA21		RW
000851H	CAN1 - IF2 Data A2	IF2DTA2H1			RW
000852H	CAN1 - IF2 Data B1	IF2DTB1L1	IF2DTB11		RW
000853H	CAN1 - IF2 Data B1	IF2DTB1H1			RW
000854H	CAN1 - IF2 Data B2	IF2DTB2L1	IF2DTB21		RW
000855H	CAN1 - IF2 Data B2	IF2DTB2H1			RW
000856H - 00087FH	Reserved				
000880H	CAN1 - Transmission Request Register	TREQR1L1	TREQR11		R
000881H	CAN1 - Transmission Request Register	TREQR1H1			R
000882H	CAN1 - Transmission Request Register	TREQR2L1	TREQR21		R
000883H	CAN1 - Transmission Request Register	TREQR2H1			R
000890H	CAN1 - New Data Register	NEWDT1L1	NEWDT11		R
000891H	CAN1 - New Data Register	NEWDT1H1			R
000892H	CAN1 - New Data Register	NEWDT2L1	NEWDT21		R
000893H	CAN1 - New Data Register	NEWDT2H1			R
000894H - 00089FH	Reserved				

I/O map (34 / 34)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Abbreviation 32-bit access	Access
0008A0H	CAN1 - Interrupt Pending Register	INTPND1L1	INTPND11		R
0008A1H	CAN1 - Interrupt Pending Register	INTPND1H1			R
0008A2H	CAN1 - Interrupt Pending Register	INTPND2L1	INTPND21		R
0008A3H	CAN1 - Interrupt Pending Register	INTPND2H1			R
0008B0H	CAN1 - Message Valid Register	MSGVAL1L1	MSGVAL11		R
0008B1H	CAN1 - Message Valid Register	MSGVAL1H1			R
0008B2H	CAN1 - Message Valid Register	MSGVAL2L1	MSGVAL21		R
0008B3H	CAN1 - Message Valid Register	MSGVAL2H1			R
0008CEH	CAN1 - Output enable register	COER1			RW
000C00H	External bus area (16-bit address up to 000FFFH)	EXTBUS1			RW
001000H	External bus area (Remaining RAM AREA)	EXTBUS1			RW

■ INTERRUPT VECTOR TABLE

Interrupt vector table (1 / 4)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
0	3FC	CALLV0	No	-	
1	3F8	CALLV1	No	-	
2	3F4	CALLV2	No	-	
3	3F0	CALLV3	No	-	
4	3EC	CALLV4	No	-	
5	3E8	CALLV5	No	-	
6	3E4	CALLV6	No	-	
7	3E0	CALLV7	No	-	
8	3DC	RESET	No	-	
9	3D8	INT9	No	-	
10	3D4	EXCEPTION	No	-	
11	3D0	NMI	No	-	Non-Maskable Interrupt
12	3CC	DLY	No	12	Delayed Interrupt
13	3C8	RC_TIMER	No	13	RC Timer
14	3C4	MC_TIMER	No	14	Main Clock Timer
15	3C0	SC_TIMER	No	15	Sub Clock Timer
16	3BC	RESERVED	No	16	Reserved
17	3B8	EXTINT0	Yes	17	External Interrupt 0
18	3B4	EXTINT1	Yes	18	External Interrupt 1
19	3B0	EXTINT2	Yes	19	External Interrupt 2
20	3AC	EXTINT3	Yes	20	External Interrupt 3
21	3A8	EXTINT4	Yes	21	External Interrupt 4
22	3A4	EXTINT5	Yes	22	External Interrupt 5
23	3A0	EXTINT6	Yes	23	External Interrupt 6
24	39C	EXTINT7	Yes	24	External Interrupt 7
25	398	EXTINT8	Yes	25	External Interrupt 8
26	394	EXTINT9	Yes	26	External Interrupt 9

Interrupt vector table (2 / 4)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
27	390	EXTINT10	Yes	27	External Interrupt 10
28	38C	EXTINT11	Yes	28	External Interrupt 11
29	388	EXTINT12	Yes	29	External Interrupt 12
30	384	EXTINT13	Yes	30	External Interrupt 13
31	380	EXTINT14	Yes	31	External Interrupt 14
32	37C	EXTINT15	Yes	32	External Interrupt 15
33	378	CAN0	No	33	CAN Controller 0
34	374	CAN1	No	34	CAN Controller 1
35	370	PPG0	Yes	35	Programmable Pulse Generator 0
36	36C	PPG1	Yes	36	Programmable Pulse Generator 1
37	368	PPG2	Yes	37	Programmable Pulse Generator 2
38	364	PPG3	Yes	38	Programmable Pulse Generator 3
39	360	PPG4	Yes	39	Programmable Pulse Generator 4
40	35C	PPG5	Yes	40	Programmable Pulse Generator 5
41	358	PPG6	Yes	41	Programmable Pulse Generator 6
42	354	PPG7	Yes	42	Programmable Pulse Generator 7
43	350	PPG8	Yes	43	Programmable Pulse Generator 8
44	34C	PPG9	Yes	44	Programmable Pulse Generator 9
45	348	PPG10	Yes	45	Programmable Pulse Generator 10
46	344	PPG11	Yes	46	Programmable Pulse Generator 11
47	340	PPG12	Yes	47	Programmable Pulse Generator 12
48	33C	PPG13	Yes	48	Programmable Pulse Generator 13
49	338	PPG14	Yes	49	Programmable Pulse Generator 14
50	334	PPG15	Yes	50	Programmable Pulse Generator 15
51	330	RLT0	Yes	51	Reload Timer 0
52	32C	RLT1	Yes	52	Reload Timer 1
53	328	RLT2	Yes	53	Reload Timer 2
54	324	RLT3	Yes	54	Reload Timer 3
55	320	PPGRLT	Yes	55	Reload Timer 6 - dedicated for PPG

Interrupt vector table (3 / 4)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
56	31C	ICU0	Yes	56	Input Capture Unit 0
57	318	ICU1	Yes	57	Input Capture Unit 1
58	314	ICU2	Yes	58	Input Capture Unit 2
59	310	ICU3	Yes	59	Input Capture Unit 3
60	30C	ICU4	Yes	60	Input Capture Unit 4
61	308	ICU5	Yes	61	Input Capture Unit 5
62	304	ICU6	Yes	62	Input Capture Unit 6
63	300	ICU7	Yes	63	Input Capture Unit 7
64	2FC	OCU0	Yes	64	Output Compare Unit 0
65	2F8	OCU1	Yes	65	Output Compare Unit 1
66	2F4	OCU2	Yes	66	Output Compare Unit 2
67	2F0	OCU3	Yes	67	Output Compare Unit 3
68	2EC	OCU4	Yes	68	Output Compare Unit 4
69	2E8	OCU5	Yes	69	Output Compare Unit 5
70	2E4	OCU6	Yes	70	Output Compare Unit 6
71	2E0	OCU7	Yes	71	Output Compare Unit 7
72	2DC	FRT0	Yes	72	Free Running Timer 0
73	2D8	FRT1	Yes	73	Free Running Timer 1
74	2D4	IIC0	Yes	74	I2C interface
75	2D0	IIC1	Yes	75	I2C interface
76	2CC	ADC0	Yes	76	A/D Converter
77	2C8	ALARM0	No	77	Alarm Comparator 0
78	2C4	ALARM1	No	78	Alarm Comparator 1
79	2C0	LINR0	Yes	79	LIN USART 0 RX
80	2BC	LINT0	Yes	80	LIN USART 0 TX
81	2B8	LINR1	Yes	81	LIN USART 1 RX
82	2B4	LINT1	Yes	82	LIN USART 1 TX
83	2B0	LINR2	Yes	83	LIN USART 2 RX
84	2AC	LINT2	Yes	84	LIN USART 2 TX

Interrupt vector table (4 / 4)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
85	2A8	LINR3	Yes	85	LIN USART 3 RX
86	2A4	LINT3	Yes	86	LIN USART 3 TX
87	2A0	MAIN_FLASH	No	87	Main Flash memory
88	29C	SAT_FLASH	No	88	Satellite Flash memory (only MB96F348H/T)
89	298	LINR7	Yes	89	LIN USART 7 RX (not available on MB96F348TSA/HSA/TWA/HWA)
90	294	LINT7	Yes	90	LIN USART 7 TX (not available on MB96F348TSA/HSA/TWA/HWA)
91	290	LINR8	Yes	91	LIN USART 8 RX (not available on MB96F348TSA/HSA/TWA/HWA)
92	28C	LINT8	Yes	92	LIN USART 8 TX (not available on MB96F348TSA/HSA/TWA/HWA)
93	288	LINR9	Yes	93	LIN USART 9 RX (not available on MB96F348TSA/HSA/TWA/HWA)
94	284	LINT9	Yes	94	LIN USART 9 TX (not available on MB96F348TSA/HSA/TWA/HWA)
95	280	RTC0	No	95	Real Timer Clock (not available on MB96F348TSA/HSA/TWA/HWA)
96	27C	CAL0	No	96	Clock Calibration Unit (not available on MB96F348TSA/HSA/TWA/HWA)

■ HANDLING DEVICES

Special care is required for the following when handling the device:

- Latch-up prevention
- Treatment of unused pins
- External clock
- Precautions for when not using a sub clock signal
- Notes on PLL clock mode operation
- Power supply pins (VCC/VSS)
- Crystal Oscillator Circuit
- Turn on Sequence of Power Supply to A/D Converter and Analog Inputs
- Connection of Unused Pins of A/D Converter
- Notes on Energization
- Stabilization of power supply voltage

1. Preventing latch-up

- CMOS IC chips may suffer latch-up under the following conditions:
  - A voltage higher than VCC or lower than VSS is applied to an input or output pin.
  - A voltage higher than the rated voltage is applied between VCC and VSS.
  - The AVCC power supply is applied before the VCC voltage.
- Latch-up may increase the power supply current drastically, causing thermal damage to the device.
- For the same reason, also be careful not to let the analog power-supply voltage (AVCC, AVRH) exceed the digital power-supply voltage.

2. Treatment of unused pins

- Unused input pins may be left open when the input is disabled (corresponding bit of Port Input Enable register PIER = 0).
- Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. To prevent latch-up, those resistors should be more than 2 kΩ.
- Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

3. External clock usage

- To use external clock, drive the X0 pin and leave X1 pin open.

4. Precautions for when not using a sub clock signal

- If you do not connect pins X0A and X1A to an oscillator, use a pull-down resistor on the X0A pin, and leave the X1A pin open.

5. Notes on PLL clock mode operation

- If the PLL clock mode is selected and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the freely oscillating PLL. Performance of this operation, however, cannot be guaranteed.

6. Power supply pins (VCC/VSS)

- Ensure that all VCC-level power supply pins are at the same potential. In addition, ensure the same for all VSS-level power supply pins. If there are more than one VCC or VSS systems, the device may operate incorrectly even within the guaranteed operating range.
- Connect VCC and VSS to the device from the power supply with lowest possible impedance.

- As a measure against power supply noise, connect a capacitor of about 0.1 µF as a bypass capacitor between VCC and VSS as close as possible to VCC and VSS pins.

7. Crystal Oscillator Circuit

- Noise at X0 or X1 pins may possibly cause abnormal operation. Make sure to provide bypass capacitors with shortest distance to X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuit not cross the lines of other circuits.
- It is highly recommended to provide a printed circuit board art work surrounding X0 and X1 pins with a ground area for stabilizing the operation.
- It is highly recommended to evaluate the quartz/MCU system at the quartz manufacturer.

8. Turn on Sequence of Power Supply to A/D Converter and Analog Inputs

- Make sure to turn the A/D converter power supply (AVCC, AVRH, AVRL) and analog inputs (ANn) on after turning the digital power supply (VCC) on.
- Turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, make sure that the voltage does not exceed AVRH or AVCC (turning the analog and digital power supplies simultaneously on or off is acceptable).

9. Connection of Unused Pins of A/D Converter

- Connect unused pins of A/D converter as AVCC = VCC, AVSS = AVRH = AVRL = VSS.

10. Notes on Energization

- To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50µs from 0.2 V to 2.7 V.

11. Stabilization of power supply voltage

- If the power supply voltage varies acutely even within the operation assurance range of the Vcc power supply voltage, a malfunction may occur. The Vcc power supply voltage must therefore be stabilized. As stabilization guidelines, stabilize the power supply voltage so that Vcc ripple fluctuations (peak to peak value) in the commercial frequencies (50 to 60 Hz) fall within 10% of the standard Vcc power supply voltage and the transient fluctuation rate becomes 0.1V/µs or less in instantaneous fluctuation for power supply switching.

■ ELECTRICAL CHARACTERISTICS

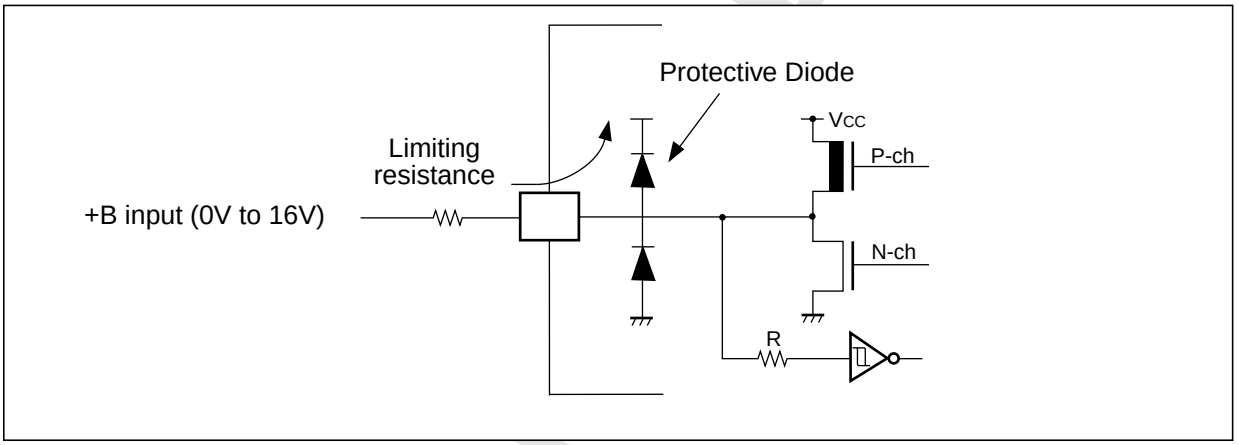
1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	V_{SS} - 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$ *1
	AVRH, AVRL	V_{SS} - 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq$ AVRH, $AV_{CC} \geq$ AVRL, AVRH > AVRL, AVRL $\geq AV_{SS}$
Input voltage	V_I	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_I \leq V_{CC}$ + 0.3V *2
Output voltage	V_O	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_O \leq V_{CC}$ + 0.3V *2
Maximum Clamp Current	I_{CLAMP}	-4.0	+4.0	mA	Applicable to general purpose I/O pins *3
Total Maximum Clamp Current	$\Sigma\|I_{CLAMP}\|$	-	40	mA	Applicable to general purpose I/O pins *3
“L” level maximum output current	I_{OL1}	-	15	mA	Normal outputs for normal drive output port setting
“L” level average output current	I_{OLAV1}	-	5	mA	Normal outputs for normal drive output port setting
“L” level maximum overall output current	ΣI_{OL1}	-	100	mA	Normal outputs for normal drive output port setting
“L” level average overall output current	ΣI_{OLAV1}	-	50	mA	Normal outputs for normal drive output port setting
“H” level maximum output current	I_{OH1}	-	-15	mA	Normal outputs for normal drive output port setting
“H” level average output current	I_{OHAV1}	-	-5	mA	Normal outputs for normal drive output port setting
“H” level maximum overall output current	ΣI_{OH1}	-	-100	mA	Normal outputs for normal drive output port setting
“H” level average overall output current	ΣI_{OHAV1}	-	-50	mA	Normal outputs for normal drive output port setting
Power consumption	P_D	-	600	mW	
Operating temperature	T_A	0	+70	°C	MB96V300B
		-40	+125*4		others
Operating temperature at Flash erase/ write	T_{AF}	-40	+105	°C	
Storage temperature	T_{STG}	-55	+150	°C	

*1: Set AV_{CC} and V_{CC} to the same voltage. Make sure that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} neither when the power is switched on.

*2: V_I and V_O should not exceed V_{CC} + 0.3 V. V_I should not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the I_{CLAMP} rating supercedes the V_I rating. Input/output voltages of standard ports depend on V_{CC}.

*3: • Applicable to all general purpose I/O pins (Pnn_m)
• Use within recommended operating conditions.
• Use at DC voltage (current)
• The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
• The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
• Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
• Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
• Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistant low voltage reset in internal vector mode).
• Sample recommended circuits:



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

*4 If used exceeding T_A = +105°C, be sure to contact Fujitsu for reliability limitations.

*

2. Recommended Conditions

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	Vcc, DVcc	3.0	-	5.5	V	
Smoothing capacitor at C pin	C_S	4.7	-	10	µF	Use a X7R Ceramic Capacitor
Operating temperature	T_A	0	-	+70	°C	MB96V300B
		-40	-	+125*1		others

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the devices electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

*1: If used exceeding T_A = +105°C, be sure to contact Fujitsu for reliability limitations.

3. DC characteristics

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC}= 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input “H” voltage	V_{IH}	-	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	0.8 V_{CC}	-	V_{CC} + 0.3	V	
		-	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	0.7 V_{CC}	-	V_{CC} + 0.3	V	
		-	Port inputs if AUTOMOTIVE Hysteresis input is selected	0.8 V_{CC}	-	V_{CC} + 0.3	V	
		-	Port inputs if TTL input is selected	2.0	-	V_{CC} + 0.3	V	
	V_{IHR}	RSTX	-	0.8 V_{CC}	-	V_{CC} + 0.3	V	RSTX input pin (CMOS Hysteresis)
	V_{IHM}	MD2-MD0	-	V_{CC} - 0.3	-	V_{CC} + 0.3	V	MDx input pins
	V_{IHX0S}	X0,X0A	-	2.5	-	V_{CC} + 0.3	V	External clock in “Oscillation mode”
Input “H” voltage	V_{IHX0F}	X0	-	0.8 V_{CC}	-	V_{CC} + 0.3	V	External clock in “Fast Clock Input mode” (Not available in MB96V300, MB96F34xY/R/A)
Input “L” voltage	V_{IL}	-	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	V_{SS} - 0.3	-	0.2 V_{CC}	V	
		-	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	V_{SS} - 0.3	-	0.3 V_{CC}	V	
		-	Port inputs if AUTOMOTIVE Hysteresis input is selected	V_{SS} - 0.3	-	0.5 V_{CC}	V	
		-	Port inputs if TTL input is selected	V_{SS} - 0.3	-	0.8	V	
	V_{ILR}	RSTX	-	V_{SS} - 0.3	-	0.2 V_{CC}	V	RSTX input pin (CMOS Hysteresis)
	V_{ILM}	MD2-MD0	-	V_{SS} - 0.3	-	V_{SS} + 0.3	V	MDx input pins
	V_{ILX0S}	X0, X0A	-	V_{SS} - 0.3	-	0.5	V	External clock in “Oscillation mode”

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC}= 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
	V_{ILX0F}	X0	-	V_{SS} - 0.3	-	0.2 V_{CC}	V	External clock in “Fast Clock Input mode” (Not available in MB96V300, MB96F34xY/R/A)
Output “H” voltage	V_{OH2}	Normal outputs	4.5V ≤ V_{CC} ≤ 5.5V I_{OH} = -2mA 3.0V ≤ V_{CC} < 4.5V I_{OH} = -1.6mA	V_{CC} - 0.5	-	-	V	Driving strength set to 2mA
	V_{OH5}	Normal outputs	4.5V ≤ V_{CC} ≤ 5.5V I_{OH} = -5mA 3.0V ≤ V_{CC} < 4.5V I_{OH} = -3mA	V_{CC} - 0.5	-	-	V	Driving strength set to 5mA
Output “H” voltage	V_{OH3}	I^2C outputs	4.5V ≤ V_{CC} ≤ 5.5V I_{OH} = -3mA 3.0V ≤ V_{CC} < 4.5V I_{OH} = -2mA	V_{CC} - 0.5	-	-	V	
Output “L” voltage	V_{OL2}	Normal outputs	4.5V ≤ V_{CC} ≤ 5.5V I_{OL} = +2mA 3.0V ≤ V_{CC} < 4.5V I_{OL} = +1.6mA	-	-	0.4	V	Driving strength set to 2mA
	V_{OL5}	Normal outputs	4.5V ≤ V_{CC} ≤ 5.5V I_{OL} = +5mA 3.0V ≤ V_{CC} < 4.5V I_{OL} = +3mA	-	-	0.4	V	Driving strength set to 5mA
Output “L” voltage	V_{OL3}	I^2C outputs	4.5V ≤ V_{CC} ≤ 5.5V I_{OL} = +3mA 3.0V ≤ V_{CC} < 4.5V I_{OL} = +2mA	-	-	0.4	V	
Input leak current	I_{IL}	Pnn_m	V_{CC} = 5.5V V_{SS} < V_I < V_{CC}	-1	-	+1	µA	
Pull-up resistance	R_{UP}	Pnn_m, RSTX	-	25	50	100	kΩ	

Note: Input/output voltages of ports depend on V_{CC}.

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC}= 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition	Value			temp	Remarks
			Typ	Max	Unit		
Power supply current in Run modes*	I_{CCPLL}	PLL Run mode with CLKS1/2 = 56MHz = CLKB = CLKP1, CLKP2 = 28MHz	44	57	mA	25˚C	CLKRC and CLKSC stopped. Core voltage at 1.9V
			45	60		125˚C	
		PLL Run mode with CLKS1/2 = 48MHz, CLKB = CLKP1/2 = 24MHz	25	34	mA	25˚C	CLKRC and CLKSC stopped. Core voltage at 1.9V
			26	37		125˚C	
	I_{CCMAIN}	Main Run mode with CLKS1/2=CLKB = CLKP1/2 = 4MHz	4.5	5.5	mA	25˚C	CLKPLL, CLKSC and CLKRC stopped
			5.1	8.5		125˚C	
	I_{CCRCH}	RC Run mode with CLKS1=CLKS2=CLKB = CLKP1/2 = 2MHz	2.9	4	mA	25˚C	CLKMC, CLKPLL and CLKSC stopped
			3.5	6.5		125˚C	
	I_{CCRCL}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 100kHz, SMCR:LPMS=0	0.4	0.6	mA	25˚C	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode
			0.9	3.5		125˚C	
		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 100kHz, SMCR:LPMS=1	0.15	0.25	mA	25˚C	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode, no Flash programming/erasing allowed.
			0.65	3.2		125˚C	
Power supply current in Run modes*	I_{CCSUB}	Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz	0.1	0.2	mA	25˚C	CLKMC, CLKPLL and CLKRC stopped, no Flash programming/ erasing allowed.
			0.6	3		125˚C	

Parameter	Symbol	Condition	Value			temp	Remarks
			Typ	Max	Unit		
Power supply current in Sleep modes*	I_{CCSPLL}	PLL Sleep mode with CLKS1/2 = 48MHz, CLKP1/2 = 24MHz	9	10.5	mA	25˚C	CLKRC and CLKSC stopped.
			9.7	13		125˚C	
		PLL Sleep mode with CLKS1/2 = CLKP1 = 56MHz, CLKP2 = 28MHz	14	15.5	mA	25˚C	CLKRC and CLKSC stopped.
			14.8	18		125˚C	
	$I_{CCSMAIN}$	Main Sleep mode with CLKS1/2 = CLKP1/2 = 4MHz	1.5	1.8	mA	25˚C	CLKPLL CLKRC and CLKSC stopped
			2	4.5		125˚C	
	I_{CCSRCH}	RC Sleep mode with CLKS1/2 = CLKP1/2 = 2MHz	0.8	1.3	mA	25˚C	CLKMC, CLKPLL and CLKSC stopped
			1.4	4		125˚C	
	I_{CCSRCL}	RC Sleep mode with CLKS1/2 = CLKP1/2 = 100kHz, SMCR:LPMSS=0	0.3	0.5	mA	25˚C	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode
			0.8	3.4		125˚C	
		RC Sleep mode with CLKS1/2 = CLKP1/2 = 100kHz, SMCR:LPMSS=1	0.06	0.15	mA	25˚C	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode
			0.56	3		125˚C	
Power supply current in Sleep modes*	I_{CCSSUB}	Sub Sleep mode with CLKS1/2 = CLKP1/2 = 32kHz	0.04	0.12	mA	25˚C	CLKMC, CLKPLL and CLKRC stopped
			0.54	2.9		125˚C	

Parameter	Symbol	Condition	Value			temp	Remarks
			Typ	Max	Unit		
Power supply current in Timer modes*	I_{CCTPLL}	PLL Timer mode with CLKMC = 4MHz, CLKPLL = 56MHz	1.6	2	mA	25˚C	CLKRC and CLKSC stopped. Core voltage at 1.9V
			2.1	4.8		125˚C	
	$I_{CCTMAIN}$	Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS=0	0.35	0.5	mA	25˚C	CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in high power mode
			0.85	3.3		125˚C	
		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS=1	0.1	0.15	mA	25˚C	CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in low power mode
			0.6	2.9		125˚C	
	I_{CCTRCH}	RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS=0	0.35	0.5	mA	25˚C	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode
			0.85	3.3		125˚C	
		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS=1	0.1	0.15	mA	25˚C	CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode
			0.6	2.9		125˚C	
	I_{CCTRCL}	RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS=0	0.3	0.45	mA	25˚C	CLKMC, CLKPLL and CLKSC stopped. Voltage in high power mode
			0.8	3.2		125˚C	
		RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS=1	0.05	0.1	mA	25˚C	CLKMC, CLKPLL and CLKSC stopped. Voltage in low power mode
			0.55	2.8		125˚C	

Parameter	Symbol	Condition	Value			temp	Remarks
			Typ	Max	Unit		
Power supply current in Timer modes*	I_{CCTSUB}	Sub Timer mode with CLKSC = 32kHz	0.03	0.1	mA	25˚C	CLKMC, CLKPLL and CLKRC stopped
			0.53	2.8		125˚C	
Stop Mode	I_{CCH}	VRCR:LPMB[2:0] = “110”	0.02	0.08	mA	25˚C	Core voltage at 1.8V
			0.52	2.8		125˚C	
		VRCR:LPMB[2:0] = “000”	0.015	0.06	mA	25˚C	Core voltage at 1.2V
			0.4	2.3		125˚C	
Power supply current for active Low Voltage detector	I_{CCLVD}	Low voltage detector enabled (RCR:LVDE=’1’)	70	100	µA	25˚C	This current must be added to all Power supply currents above
			70	100		125˚C	
Clock modulator current	$I_{CCCLOMO}$	Clock modulator enabled (CMCR:PDX = ‘1’)	3	4	mA	25˚C	Must be added to all current above
			3	4		125˚C	
Flash Write/Erase current	$I_{CCFLASH}$		15	40	mA	25˚C	Must be added to all current above
			15	40		125˚C	
Input capacitance	C_{IN}	-	5	15	pF		

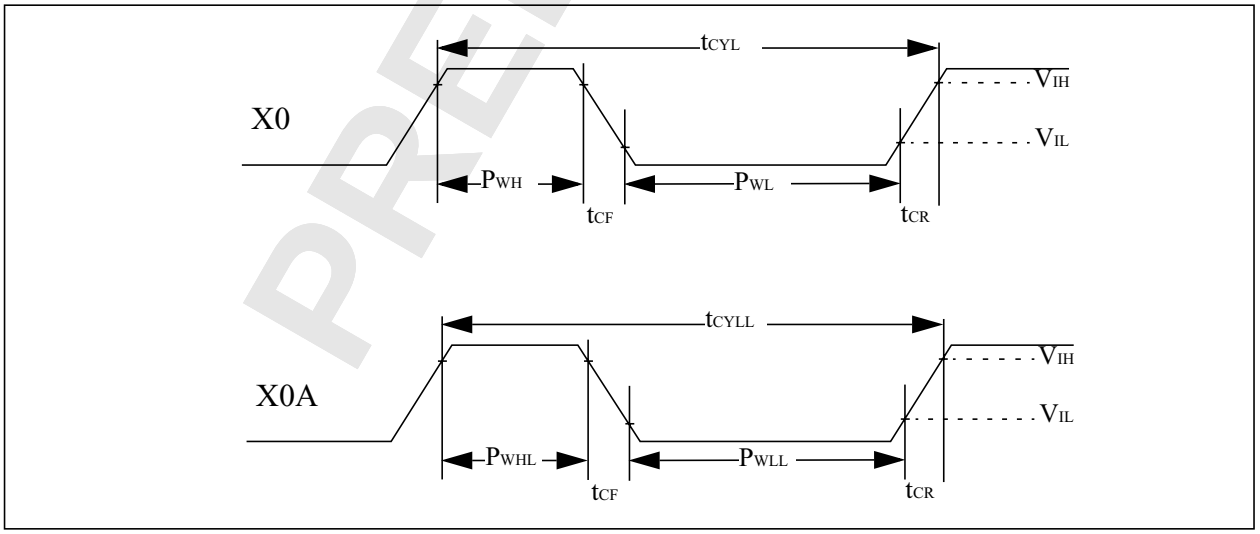
* The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. See chapter 10 of the Harware Manual for further details about voltage regulator control.

4. AC Characteristics

Source Clock timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC}= 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	-	16	MHz	When using an oscillation circuit, PLL off
			3.5	-	16	MHz	When using an oscillation circuit, PLL on
			0	-	4	MHz	When using an external clock, PLL off
			3.5	-	4	MHz	When using an external clock, PLL on
Clock frequency	f_{FCI}	X0	0	-	56	MHz	When using an external clock in “Fast Clock Input mode” (not available in MB96V300, MB96F34xY/R/A)
Clock frequency	f_{CL}	X0A, X1A	32	32.768	100	kHz	When using an oscillation circuit
			0	-	100	kHz	When using an external clock
Clock frequency	f_{CR}	-	50	100	200	kHz	When using slow frequency of RC oscillator
			1	2	4	MHz	When using fast frequency of RC oscillator
Clock frequency	f_{CLKVCO}	-	50	-	200	MHz	VCO output frequency of PLL (CLKVCO)
Input clock pulse width	P_{WH}, P_{WL}	X0	8	-	-	ns	Duty ratio is about 30% to 70%
Input clock pulse width	P_{WHL}, P_{WLL}	X0A	5	-	-	µs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	-	-	5	ns	When using external clock



Internal Clock timing

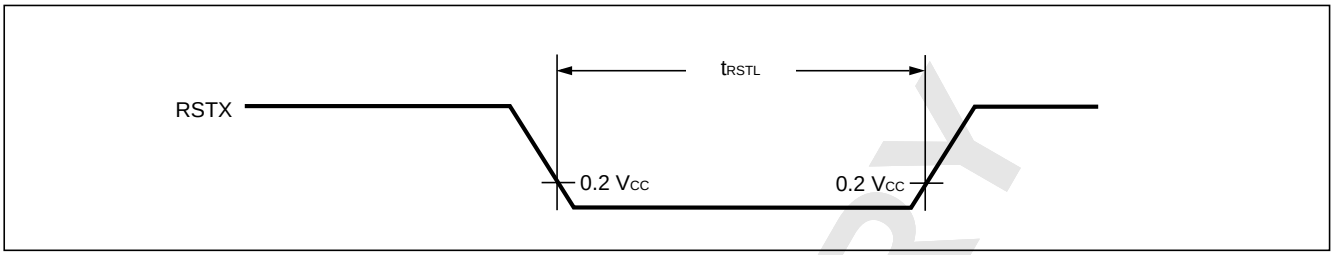
(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC}= 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Core Voltage Settings				Unit	Remarks
		1.8V		1.9V			
		Min	Max	Min	Max		
Internal System clock frequency (CLKS1 and CLKS2)	f_{CLKS1}, f_{CLKS2}	0	92	0	96	MHz	
		0	68	0	74	MHz	MB96F34xY/R
Internal CPU clock frequency (CLKB), internal peripheral clock frequency (CLKP1)	f_{CLKB}, f_{CLKP1}	0	52	0	56	MHz	
Internal peripheral clock frequency (Clock CLKP2)	f_{CLKP2}	0	28	0	32	MHz	

External Reset timing

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC}= 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

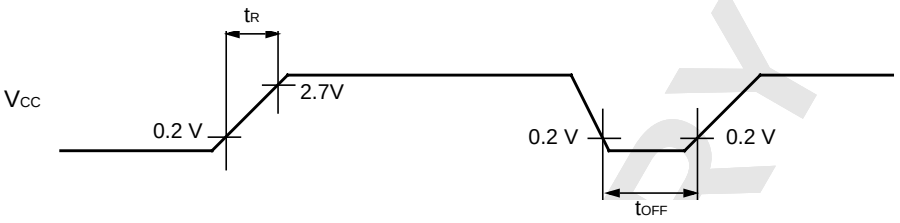
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Reset input time	t_{RSTL}	RSTX	500	-	-	ns	



Power On Reset timing

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC}= 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power on rise time	t_R	Vcc	0.05	-	30	ms	
Power off time	t_{OFF}	Vcc	1	-	-	ms	Due to repetitive operation



If you change the power supply too rapidly, a power-on reset may occur.
We recommend that you startup smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However if voltage drops are below 1 V/s, you can operate while using the PLL clock.

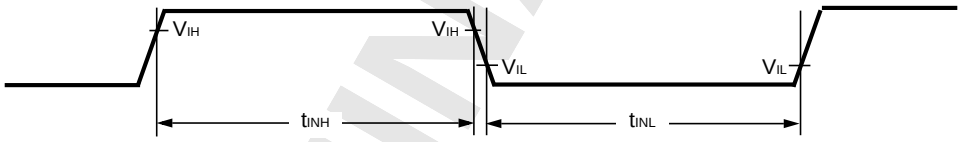
External Input timing

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC}= 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value		Unit	Used Pin input function
				Min	Max		
Input pulse width	t_{INH} t_{INL}	INTn	—	200	—	ns	External Interrupt
		NMI					NMI
		Pnn_m		t_{CLKP1} + 200 (t_{CLKP1}=1/f_{CLKP1})	—	ns	General Purpose IO
		TINn					Reload Timer
		TTGn					PPG Trigger input
		ADTG					AD Converter Trigger
		FRCKn					Free Running Timer external clock
		INn					Input Capture

Note : Relocated Resource Inputs have same characteristics

External Pin input



External Bus timing

Basic Timing

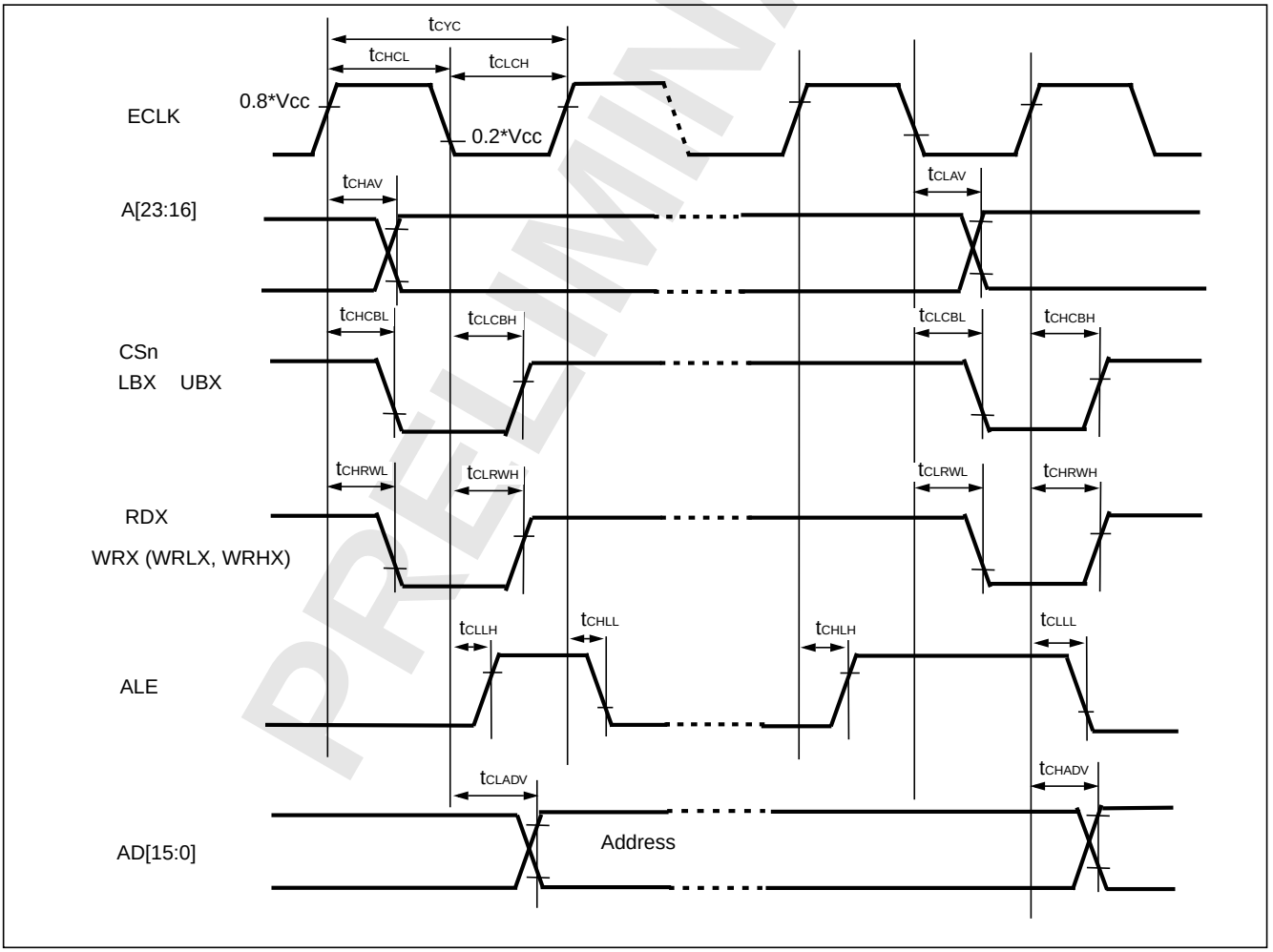
(T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive}=5mA,C_L=50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	—	25	—	ns	
	t_{CHCL}		—	t_{CYC}/2-5	t_{CYC}/2+5	ns	if CLKB duty cycle is 50%
	t_{CLCH}		—	t_{CYC}/2-5	t_{CYC}/2+5	ns	
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX,ECLK	—	-20	20	ns	
	t_{CHCBL}		—	-20	20	ns	
	t_{CLCBH}		—	-20	20	ns	
	t_{CLCBL}		—	-20	20	ns	
ECLK → ALE time	t_{CHLH}	ALE, ECLK	—	-10	10	ns	
	t_{CHLL}		—	-10	10	ns	
	t_{CLLH}		—	-10	10	ns	
	t_{CLLL}		—	-10	10	ns	
ECLK → address valid time	t_{CHAV}	A[23:16],ECLK	—	-15	15	ns	
	t_{CLAV}		—	-15	15	ns	
ECLK → address valid time	t_{CLADV}	AD[15:0],ECLK	—	-15	15	ns	
	t_{CHADV}		—	-15	15	ns	
ECLK → RDX /WRX time	t_{CHRWH}	RDX, WRX, WRLX,WRHX, ECLK	—	-10	10	ns	
	t_{CHRWL}		—	-10	10	ns	
	t_{CLRWH}		—	-10	10	ns	
	t_{CLRWL}		—	-10	10	ns	

(T_A = –40 °C to +125 °C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive}=5mA,C_L=50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	—	30	—	ns	
	t_{CHCL}		—	t_{CYC}/2-8	t_{CYC}/2+8	ns	if CLKB duty cycle is 50%
	t_{CLCH}		—	t_{CYC}/2-8	t_{CYC}/2+8	ns	
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX,ECLK	—	-25	25	ns	
	t_{CHCBL}		—	-25	25	ns	
	t_{CLCBH}		—	-25	25	ns	
	t_{CLCBL}		—	-25	25	ns	

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK → ALE time	t_{CHLH}	ALE, ECLK	—	-15	15	ns	
	t_{CHLL}		—	-15	15	ns	
	t_{CLLH}		—	-15	15	ns	
	t_{CLLL}		—	-15	15	ns	
ECLK → address valid time	t_{CHAV}	A[23:16],ECLK	—	-20	20	ns	
	t_{CLAV}		—	-20	20	ns	
ECLK → address valid time	t_{CLADV}	AD[15:0],ECLK	—	-20	20	ns	
	t_{CHADV}		—	-20	20	ns	
ECLK → RDX /WRX time	t_{CHRWH}	RDX, WRX, WRLX, WRHX, ECLK	—	-15	15	ns	
	t_{CHRWL}		—	-15	15	ns	
	t_{CLRWH}		—	-15	15	ns	
	t_{CLRWL}		—	-15	15	ns	



Refer to the Hardware Manual for detailed Timing Charts.

Bus Timing (Read)

(T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive}=5mA,C_L=50pF

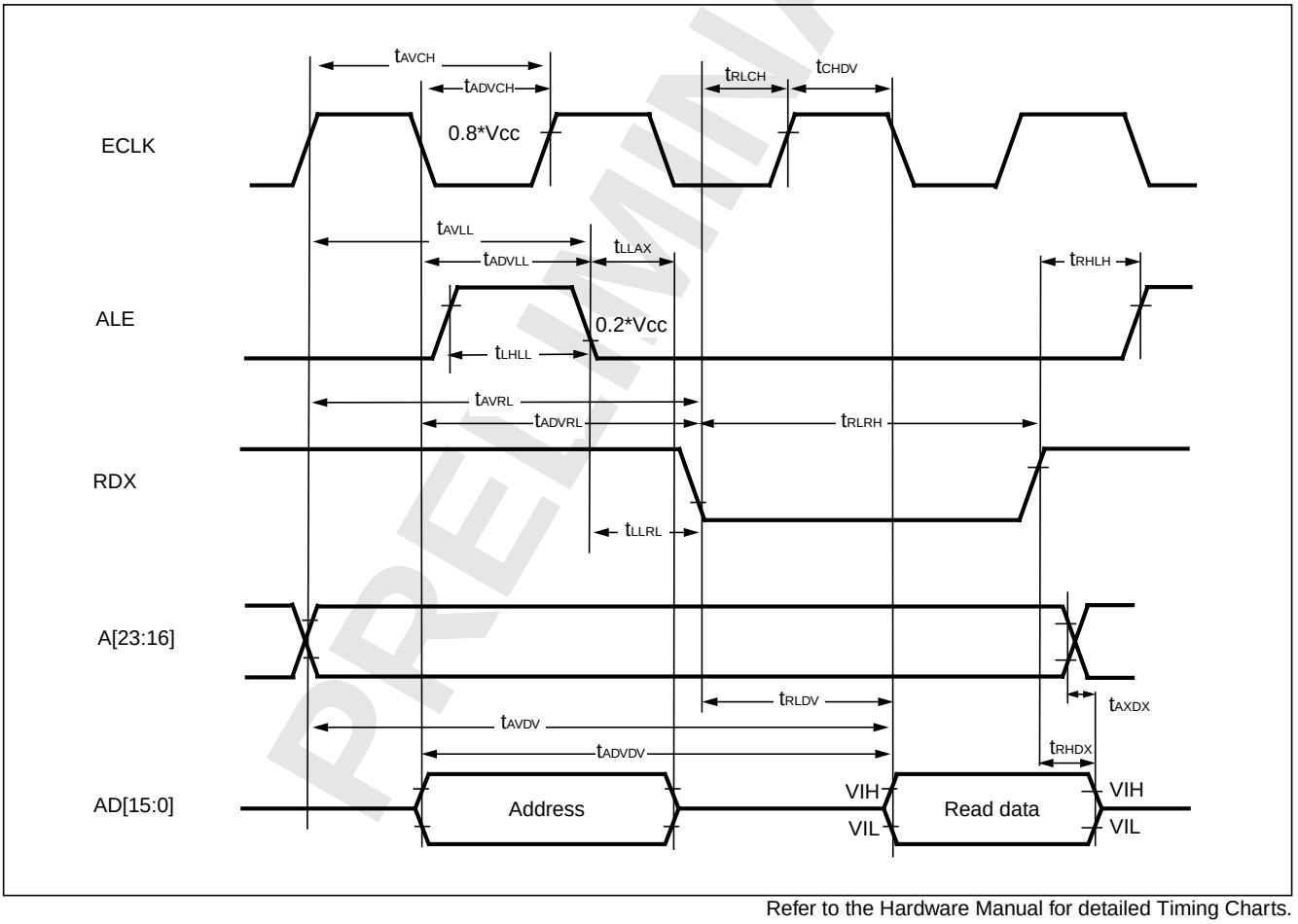
Parameter	Sym-bol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 – 5$	—	ns	
			EACL:STS=1	$t_{CYC} – 5$	—	ns	
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 – 5$	—	ns	
Valid address ⇒ ALE ↓ time	t_{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	$t_{CYC} – 15$	—	ns	
			EACL:STS=1 and EACL:ACE=0	$3t_{CYC}/2 – 15$	—	ns	
			EACL:STS=0 and EACL:ACE=1	$2t_{CYC} – 15$	—	ns	
			EACL:STS=1 and EACL:ACE=1	$5t_{CYC}/2 – 15$	—	ns	
	t_{ADVLL}	ALE,AD[15 :0]	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 – 15$	—	ns	
			EACL:STS=1 and EACL:ACE=0	$t_{CYC} – 15$	—	ns	
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 – 15$	—	ns	
			EACL:STS=1 and EACL:ACE=1	$2t_{CYC} – 15$	—	ns	
ALE ↓ ⇒ Address valid time	t_{LLAX}	ALE, AD[15 :0]	EACL:STS=0	$t_{CYC}/2 – 15$	—	ns	
			EACL:STS=1	-15	—	ns	
Valid address ⇒ RDX ↓ time	t_{AVRL}	RDX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2 – 15$	—	ns	
			EACL:ACE=1	$5t_{CYC}/2 – 15$	—	ns	
Valid address ⇒ RDX ↓ time	t_{ADVRL}	RDX,AD[15 :0]	EACL:ACE=0	$t_{CYC} – 15$	—	ns	
			EACL:ACE=1	$2t_{CYC} – 15$	—	ns	
Valid address ⇒ Valid data input	t_{AVDV}	A[23:16], AD[15;0]	EACL:ACE=0	—	$3t_{CYC} – 55$	ns	w/o cycle extension
			EACL:ACE=1	—	$4t_{CYC} – 55$	ns	
Valid address ⇒ Valid data input	t_{ADVDV}	AD[15 :0]	EACL:ACE=0	—	$5t_{CYC}/2 – 55$	ns	w/o cycle extension;
			EACL:ACE=1	—	$7t_{CYC}/2 – 55$	ns	
RDX pulse width	t_{RLRH}	RDX	—	$3\ t_{CYC}/2 – 5$	—	ns	w/o cycle extension
RDX ↓ ⇒ Valid data input	t_{RLDV}	RDX, AD[15:0]	—	—	$3\ t_{CYC}/2 – 50$	ns	w/o cycle extension
RDX ↑ ⇒ Data hold time	t_{RHDX}	RDX, AD[15:0]	—	0	—	ns	
Address valid ⇒ Data hold time	t_{AXDX}	A[23:16], AD[15:0]	—	0	—	ns	
RDX ↑ ⇒ ALE ↑ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYC}/2 – 10$	—	ns	
			other ECL:STS, EACL:ACE setting	$t_{CYC}/2 – 10$	—	ns	

Parameter	Sym-bol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ ECLK ↑ time	t_{AVCH}	A[23:16], ECLK	—	t_{CYC} – 15	—	ns	
	t_{ADVCH}	AD[15:0], ECLK	—	$t_{CYC}/2$ – 15	—	ns	
RDX ↓ ⇒ ECLK ↑ time	t_{RLCH}	RDX, CLK	—	$t_{CYC}/2$ – 10	—	ns	
ALE ↓ ⇒ RDX ↓ time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{CYC}/2$ – 10	—	ns	
			EACL:STS=1	– 10	—	ns	
ECLK↑ ⇒ Valid data input	t_{CHDV}	AD[15:0], ECLK	—	—	t_{CYC} – 50	ns	

(T_A = –40 °C to +125 °C, V_{CC} = , V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive}=5mA,C_L=50pF)

Parameter	Sym-bol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2$ – 8	—	ns	
			EACL:STS=1	t_{CYC} – 8	—	ns	
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2$ – 8	—	ns	
Valid address ⇒ ALE ↓ time	t_{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	t_{CYC} – 20	—	ns	
			EACL:STS=1 and EACL:ACE=0	$3t_{CYC}/2$ – 20	—	ns	
			EACL:STS=0 and EACL:ACE=1	$2t_{CYC}$ – 20	—	ns	
			EACL:STS=1 and EACL:ACE=1	$5t_{CYC}/2$ – 20	—	ns	
	t_{ADVLL}	ALE,AD[15 :0]	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2$ – 20	—	ns	
			EACL:STS=1 and EACL:ACE=0	t_{CYC} – 20	—	ns	
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2$ – 20	—	ns	
			EACL:STS=1 and EACL:ACE=1	$2t_{CYC}$ – 20	—	ns	
ALE ↓ ⇒ Address valid time	t_{LLAX}	ALE, AD[15 :0]	EACL:STS=0	$t_{CYC}/2$ – 20	—	ns	
			EACL:STS=1	-20	—	ns	
Valid address ⇒ RDX ↓ time	t_{AVRL}	RDX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2$ – 20	—	ns	
			EACL:ACE=1	$5t_{CYC}/2$ – 20	—	ns	
Valid address ⇒ RDX ↓ time	t_{ADVRL}	RDX,AD[15 :0]	EACL:ACE=0	t_{CYC} – 20	—	ns	
			EACL:ACE=1	$2t_{CYC}$ – 20	—	ns	
Valid address ⇒ Valid data input	t_{AVDV}	A[23:16], AD[15;0]	EACL:ACE=0	—	$3t_{CYC}$ – 60	ns	w/o cycle extension
			EACL:ACE=1	—	$4t_{CYC}$ – 60	ns	
Valid address ⇒ Valid data input	t_{ADVDV}	AD[15 :0]	EACL:ACE=0	—	$5t_{CYC}/2$ – 60	ns	w/o cycle extension;
			EACL:ACE=1	—	$7t_{CYC}/2$ – 60	ns	
RDX pulse width	t_{RLRH}	RDX	—	$3t_{CYC}/2$ – 8	—	ns	w/o cycle extension

Parameter	Sym-bol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
RDX ↓ ⇒ Valid data input	t_{RLDV}	RDX, AD[15:0]	—	—	$3t_{CYC}/2 - 55$	ns	w/o cycle extension
RDX ↑ ⇒ Data hold time	t_{RHDX}	RDX, AD[15:0]	—	0	—	ns	
Address valid ⇒ Data hold time	t_{AXDX}	A[23:16]	—	0	—	ns	
RDX ↑ ⇒ ALE ↑ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYC}/2 - 15$	—	ns	
			other ECL:STS, EACL:ACE setting	$t_{CYC}/2 - 15$	—	ns	
Valid address ⇒ ECLK ↑ time	t_{AVCH}	A[23:16], ECLK	—	$t_{CYC} - 20$	—	ns	
	t_{ADVCH}	AD[15:0], ECLK	—	$t_{CYC}/2 - 20$	—	ns	
RDX ↓ ⇒ ECLK ↑ time	t_{RLCH}	RDX, CLK	—	$t_{CYC}/2 - 15$	—	ns	
ALE ↓ ⇒ RDX ↓ time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{CYC}/2 - 15$	—	ns	
			EACL:STS=1	– 15	—	ns	
ECLK↑ ⇒ Valid data input	t_{CHDV}	AD[15:0], ECLK	—	—	$t_{CYC} - 55$	ns	



Refer to the Hardware Manual for detailed Timing Charts.

Bus Timing (Write)

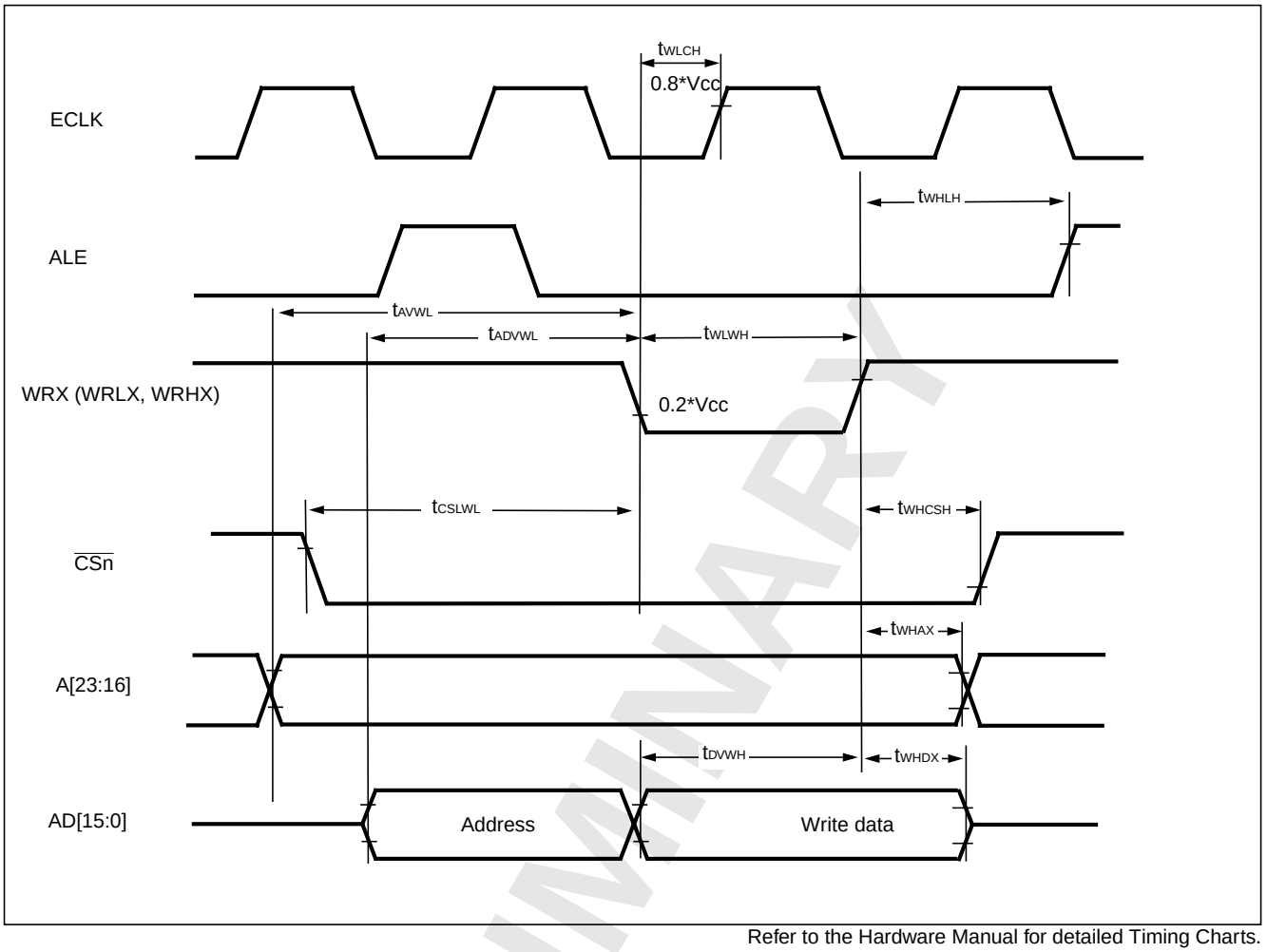
(T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive}=5mA,C_L=50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ WRX ↓ time	t_{AVWL}	WRX, WRLX, WRHX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2$ – 15	—	ns	
			EACL:ACE=1	$5t_{CYC}/2$ – 15	—	ns	
Valid address ⇒ WRX ↓ time	t_{ADVWL}	WRX, WRLX, WRHX, AD[15:0]	EACL:ACE=0	t_{CYC} – 15		ns	
			EACL:ACE=1	$2t_{CYC}$ – 15		ns	
WRX pulse width	t_{WLWH}	WRX, WRXL, WRHX	—	t_{CYC} – 5	—	ns	w/o cycle extension
Valid data output ⇒ WRX ↑ time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	—	t_{CYC} – 20	—	ns	w/o cycle extension
WRX ↑ ⇒ Data hold time	t_{WHDX}	WRX, WRLX, WRHX, AD[15:0]	—	$t_{CYC}/2$ – 15	—	ns	
WRX ↑ ⇒ Address valid time	t_{WHAX}	WRX, WRLX, WRHX, A[23:16]	EACL:STS=0	$t_{CYC}/2$ – 15	—	ns	
WRX ↑ ⇒ ALE ↑ time	t_{WHLH}	WRX, WRLX, WRHX, ALE	EBM:ACE=1 and EACL:STS=1	$2t_{CYC}$ – 10	—	ns	
			other EBM:ACE and EACL:STS setting	t_{CYC} – 10	—	ns	
WRX ↓ ⇒ ECLK ↑ time	t_{WLCH}	WRX, WRLX, WRHX, ECLK	—	$t_{CYC}/2$ – 10	—	ns	
WRX ⇒ CSn time	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:ACE=0	—	$3t_{CYC}/2$ – 15	ns	
			EACL:ACE=1	—	$5t_{CYC}/2$ – 15	ns	
WRX ⇒ CSn time	t_{WHCSH}	WRX, WRLX, WRHX, CSn	EACL:STS=0	$t_{CYC}/2$ – 15	—	ns	

(T_A = –40 °C to +125 °C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive}=5mA,C_L=50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ WRX ↓ time	t_{AVWL}	WRX, WRLX, WRHX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2$ – 20	—	ns	
			EACL:ACE=1	$5t_{CYC}/2$ – 20	—	ns	
Valid address ⇒ WRX ↓ time	t_{ADVWL}	WRX, WRLX, WRHX, AD[15:0]	EACL:ACE=0	t_{CYC} – 20			
			EACL:ACE=1	$2t_{CYC}$ – 20			

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
WRX pulse width	t_{WLWH}	WRX, WRLX, WRHX	—	t_{CYC} – 8	—	ns	w/o cycle extension
Valid data output ⇒ WRX ↑ time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	—	t_{CYC} – 25	—	ns	w/o cycle extension
WRX ↑ ⇒ Data hold time	t_{WHDX}	WRX, WRLX, WRHX, AD[15:0]	—	$t_{CYC}/2$ – 20	—	ns	
WRX ↑ ⇒ Address valid time	t_{WHAX}	WRX, WRLX, WRHX, A[23:16]	EACL:STS=0	$t_{CYC}/2$ – 20	—	ns	
WRX ↑ ⇒ ALE ↑ time	t_{WHLH}	WRX, WRLX, WRHX, ALE	EBM:ACE=1 and EACL:STS=1	$2t_{CYC}$ – 15	—	ns	
			other EBM:ACE and EACL:STS setting	t_{CYC} – 15	—	ns	
WRX ↓ ⇒ ECLK ↑ time	t_{WLCH}	WRX, WRLX, WRHX, ECLK	—	$t_{CYC}/2$ – 15	—	ns	
CSn ⇒ WRX time	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:ACE=0	—	$3t_{CYC}/2$ – 20	ns	
			EACL:ACE=1	—	$5t_{CYC}/2$ – 20	ns	
WRX ⇒ CSn time	t_{WHCSH}	WRX, WRLX, WRHX, CSn	EACL:STS=0	$t_{CYC}/2$ – 20	—	ns	



Refer to the Hardware Manual for detailed Timing Charts.

Ready Input Timing

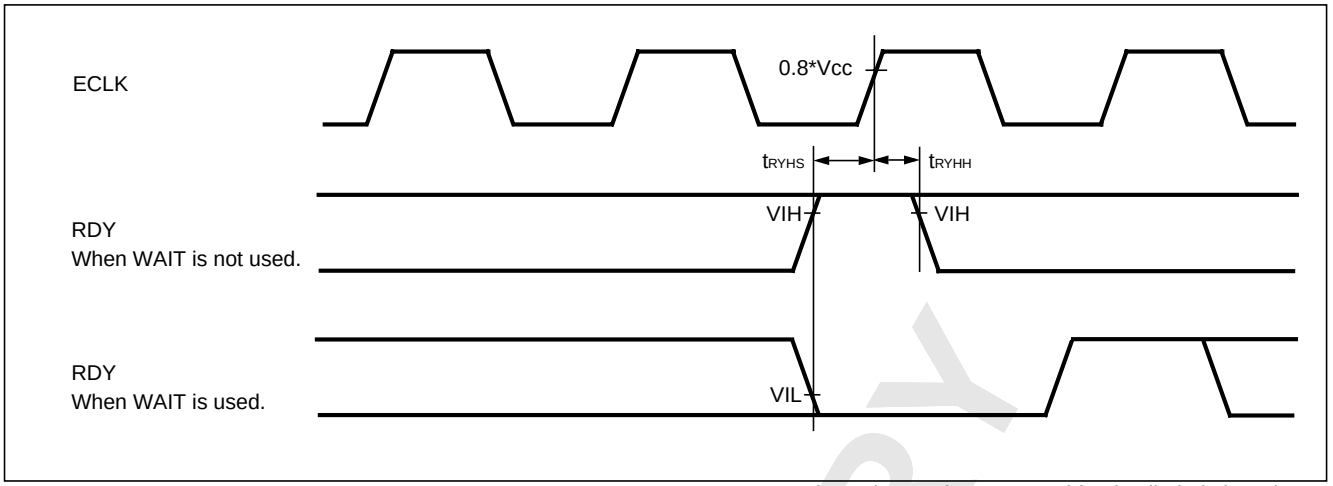
(T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive}=5mA,C_L=50pF)

Parameter	Sym-bol	Pin	Test Condition	Rated Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	35	—	ns	
RDY hold time	t_{RYHH}	RDY		0	—	ns	

(T_A = –40 °C to +125 °C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive}=5mA,C_L=50pF)

Parameter	Sym-bol	Pin	Test Condition	Rated Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	45	—	ns	
RDY hold time	t_{RYHH}	RDY		0	—	ns	

Note : If the RDY setup time is insufficient, use the auto-ready function.



Refer to the Hardware Manual for detailed Timing Charts.

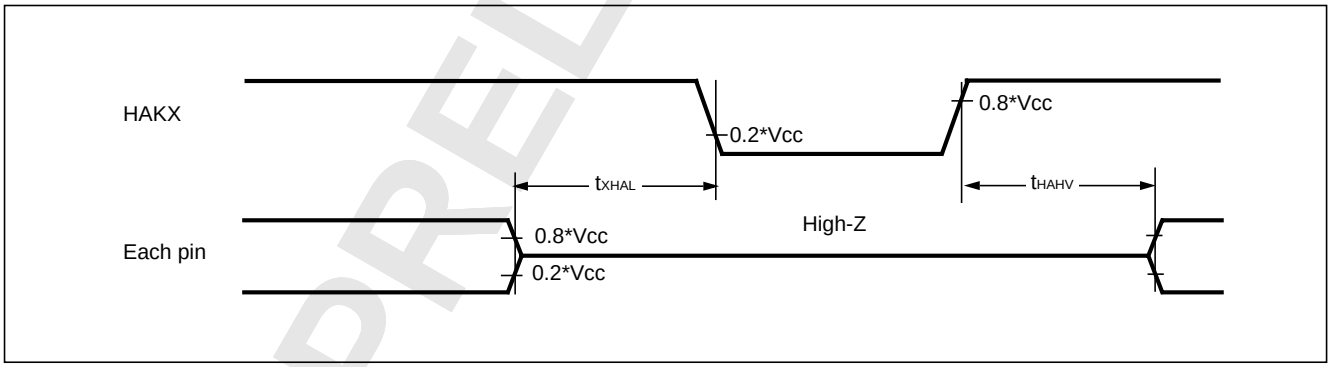
Hold Timing

(T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive}=5mA,C_l=50pF)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating ⇒ HAKX ↓ time	t_{XHAL}	HAKX	—	t_{CYC} – 20	t_{CYC} + 20	ns	
HAKX ↑ time ⇒ Pin valid time	t_{HAHV}	HAKX		t_{CYC} – 20	t_{CYC} + 20	ns	

(T_A = –40 °C to +125 °C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive}=5mA,C_l=50pF)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating ⇒ HAKX ↓ time	t_{XHAL}	HAKX	—	t_{CYC} – 25	t_{CYC} + 25	ns	
HAKX ↑ time ⇒ Pin valid time	t_{HAHV}	HAKX		t_{CYC} – 25	t_{CYC} + 25	ns	



Refer to the Hardware Manual for detailed Timing Charts.

USART timing

(T_A = -40˚C to 125˚C, V_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, IO_{drive}=5mA, C_L=50pF)

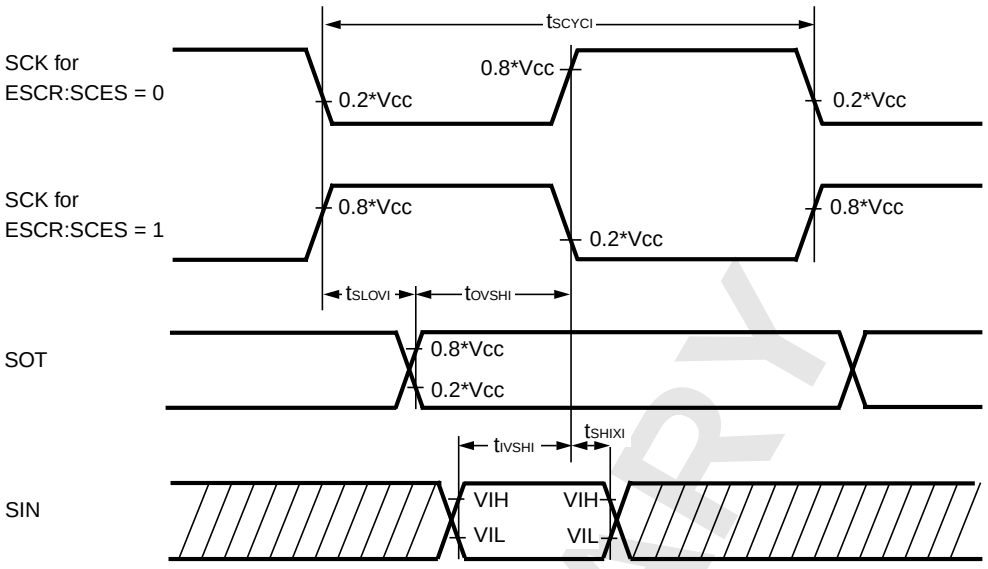
Parameter	Symbol	Pin	Condition	V_{CC} = AV_{CC}= 4.5V to 5.5V		V_{CC} = AV_{CC}= 3.0V to 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal Shift Clock Mode	4 t_{CLKP1}	—	4 t_{CLKP1}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKn, SOTn		-20	+20	-30	+30	ns
SOT → SCK ↑ delay time	t_{OVSHI}	SCKn, SOTn		$N*t_{CLKP1}$ - 20 *1	—	$N*t_{CLKP1}$ - 30 *1	—	
Valid SIN → SCK ↑	t_{IVSHI}	SCKn, SINn		t_{CLKP1} + 45	—	t_{CLKP1} + 55	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCKn, SINn		0	—	0	—	ns
Serial clock “L” pulse width	t_{SLSHE}	SCKn	External Shift Clock Mode	t_{CLKP1} + 10	—	t_{CLKP1} + 10	—	ns
Serial clock “H” pulse width	t_{SHSLE}	SCKn		t_{CLKP1} + 10	—	t_{CLKP1} + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKn, SOTn		—	2 t_{CLKP1} + 45	—	2 t_{CLKP1} + 55	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCKn, SINn		t_{CLKP1}/2 + 10	—	t_{CLKP1}/2 + 10	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SCKn, SINn		t_{CLKP1} + 10	—	t_{CLKP1} + 10	—	ns
SCK fall time	t_{FE}	SCKn		—	20	—	20	ns
SCK rise time	t_{RE}	SCKn		—	20	—	20	ns

Notes:
- AC characteristic in CLK synchronized mode.
- C_L is load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “MB96300 Super series HARDWARE MANUAL”
- t_{CLKP1} is the cycle time of the peripheral clock 1 (CLKP1), Unit : ns

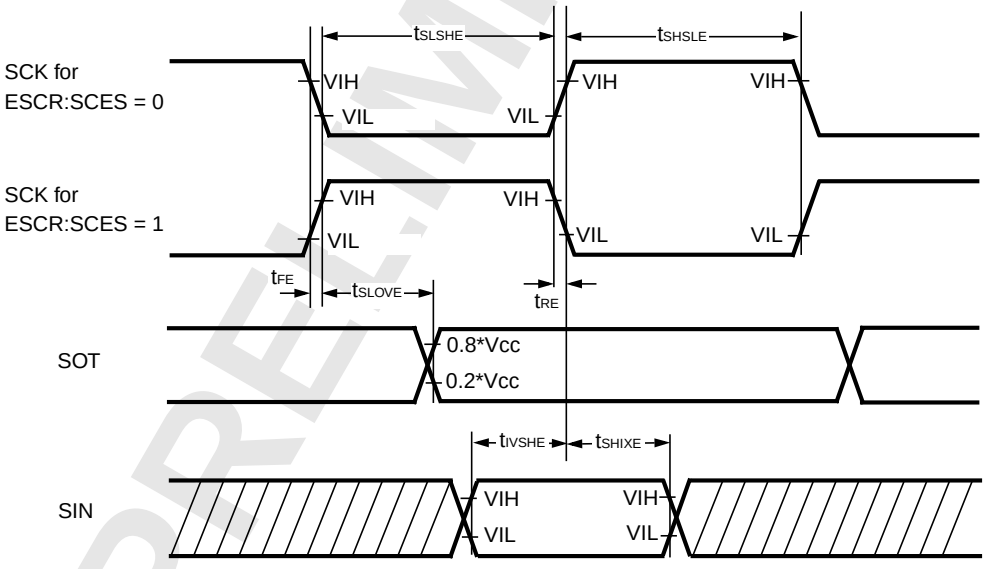
*1: Parameter N depends on t_{SCYCI} and can be calculated as:
- if t_{SCYCI} = 2*k*t_{CLKP1}, then N = k, where k is an integer > 2
- if t_{SCYCI} = (2*k+1)*t_{CLKP1}, then N = k+1, where k is an integer > 1

Examples:

t_{SCYCI}	N
4*t_{CLKP1}	2
5*t_{CLKP1}, 6*t_{CLKP1}	3
7*t_{CLKP1}, 8*t_{CLKP1}	4
...	...



Internal Shift Clock Mode



External Shift Clock Mode

I²C Timing

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC}= 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

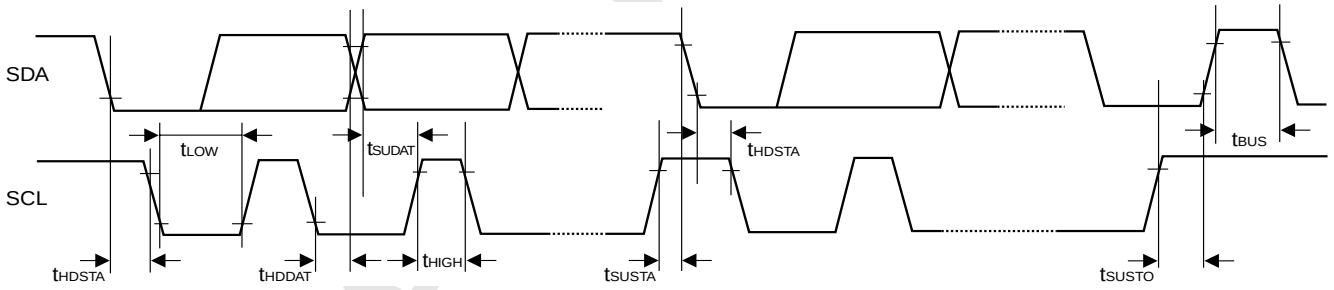
Parameter	Symbol	Condition	Standard-mode		Fast-mode*4		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz
Hold time (repeated) START condition SDA↓→SCL↓	t_{HDSTA}		4.0	—	0.6	—	µs
"L" width of the SCL clock	t_{LOW}		4.7	—	1.3	—	µs
"H" width of the SCL clock	t_{HIGH}		4.0	—	0.6	—	µs
Set-up time for a repeated START condition SCL↑→SDA↓	t_{SUSTA}		4.7	—	0.6	—	µs
Data hold time SCL↓→SDA↓↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs
Data set-up time SDA↓↑→SCL↑	t_{SUDAT}		250	—	100	—	ns
Set-up time for STOP condition SCL↑→SDA↑	t_{SUSTO}		4.0	—	0.6	—	µs
Bus free time between a STOP and START condition	t_{BUS}		4.7	—	1.3	—	µs

*1 : R,C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*2 : The maximum t_{HDDAT} have only to be met if the device does not stretch the "L" width (t_{LOW}) of the SCL signal.

*3 : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SUDAT} \geq 250$ ns must then be met.

*4 : For use at over 100 kHz, set the peripheral clock 1 to at least 6 MHz.



5. Analogue Digital Converter

(T_A = -40 ˚C to +125 ˚C, 3.0 V ≤ AVRH - AVRL, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	-3	-	+3	LSB	
Nonlinearity error	-	-	-2.5	-	+2.5	LSB	
Differential nonlinearity error	-	-	-1.9	-	+1.9	LSB	
Zero reading voltage	V_{OT}	ANn	AVRL - 1.5	AVRL+ 0.5	AVRL + 2.5	LSB	
Full scale reading voltage	V_{FST}	ANn	AVRH - 3.5	AVRH - 1.5	AVRH + 0.5	LSB	
Compare time	-	-	1.0	-	16,500	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			2.0	-	-	µs	3.0V ≤ AV_{CC} < 4.5V
Sampling time	-	-	0.5	-	-	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			1.2	-	-	µs	3.0V ≤ AV_{CC} < 4.5V
Analog port input current	I_{AIN}	ANn	-1	-	+1	µA	T_A = 25 ˚C
			-3	-	+3	µA	T_A = 125 ˚C
Analog input voltage range	V_{AIN}	ANn	AVRL	-	AVRH	V	
Reference voltage range	AVRH	AVRH/ AVRH2	0.75 AVcc	-	AVcc	V	
	AVRL	AVRL	AV_{SS}	-	0.25 AV_{CC}	V	
Power supply current	I_A	AVcc	-	2.5	5	mA	AC Converter active
	I_{AH}	AVcc	-	-	5	µA	AD Converter not operated *1
Reference voltage current	I_R	AVRH/ AVRL	-	0.7	1	mA	AC Converter active
	I_{RH}	AVRH/ AVRL	-	-	5	µA	AD Converter not operated
Offset between input channels	-	ANn	-	-	TBD	LSB	

*1: If A/D converter is not operating, a current when CPU is stopped is applicable (VCC = AVCC = AVRH = 5.0 V) .

Note : The accuracy gets worse as AVRH - AVRL becomes smaller.

Definition of A/D Converter Terms

Resolution: Analog variation that is recognized by an A/D converter.

Non linearity error: Deviation between a line across zero-transition line (“00 0000 0000” <--> “00 0000 0001”) and full-scale transition line (“11 1111 1110” <--> “11 1111 1111”) and actual conversion characteristics.

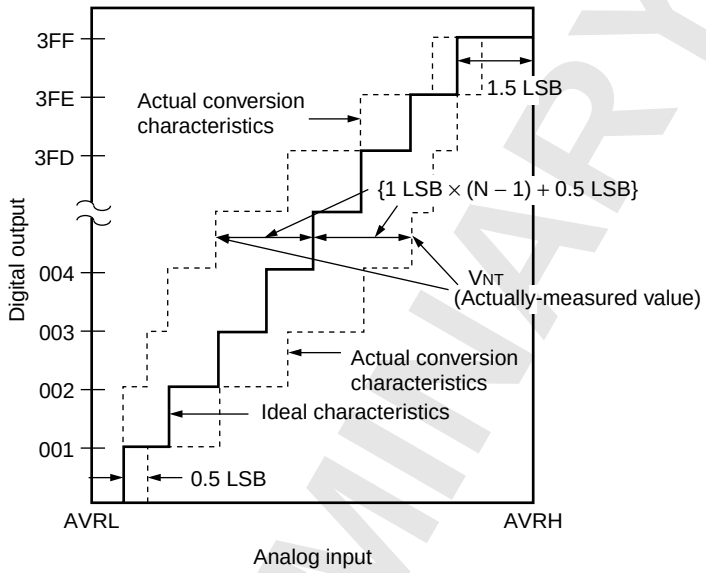
Differential linearity error: Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.

Total error: Difference between an actual value and an ideal value. A total error includes zero transition error, full-scale transition error, and linear error.

Zero reading voltage: Input voltage which results in the minimum conversion value.

Full scale reading voltage: Input voltage which results in the maximum conversion value.

Total error



$$\text{Total error of digital output "N"} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

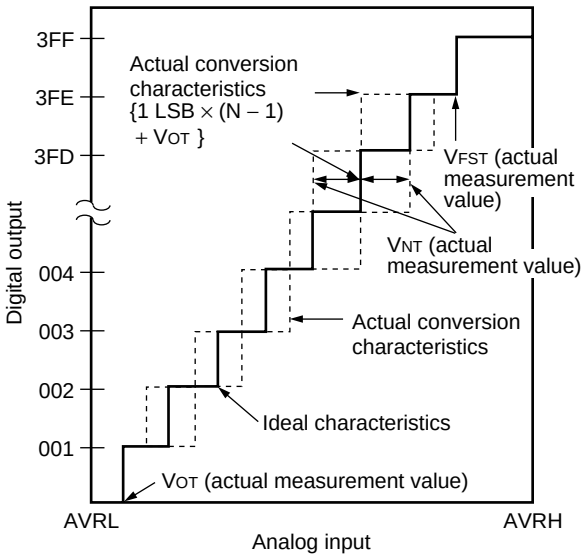
$$1\ \text{LSB} = (\text{Ideal value})\ \frac{AVRH - AVRL}{1024}\ [\text{V}]$$

V_{OT} (Ideal value) = AVRL + 0.5 LSB [V]

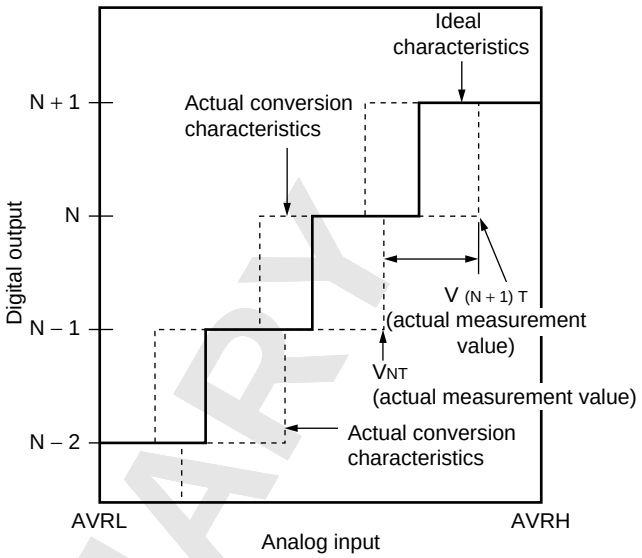
V_{FST} (Ideal value) = AVRH – 1.5 LSB [V]

V_{NT} : A voltage at which digital output transitions from (N – 1) to N.

Non linearity error



Differential linearity error



$$\text{Non linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

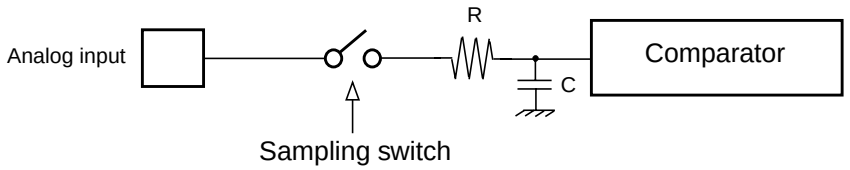
V_{OT} : Voltage at which digital output transits from "000_H" to "001_H."
V_{FST} : Voltage at which digital output transits from "$3FE_H$" to "$3FF_H$."

Notes on A/D Converter Section

- About the external impedance of the analog input and its sampling time

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

- Analog input circuit model:



Reference values:

- R = 2.6 kΩ (Max)
- C = 8.5 pF (Max)

To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time (T_{samp}) is longer than the minimum value. Usually, this value is set to 7τ, where τ = RC. If you include the external input resistance (R_{ext}) connected to the analog input, the sampling time is expressed:

T_{samp} [min] = 7.(R_{ext} + R).C

If the sampling time cannot be sufficient, connect a capacitor of about 0.1 mF to the analog input pin.

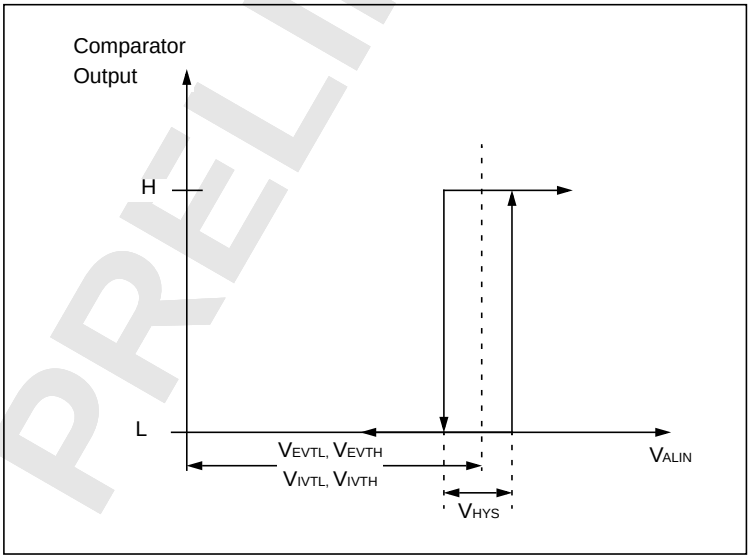
- About the error

The accuracy gets worse as |AVRH - AVRL| becomes smaller.

6. Alarm Comparator

(T_A = -40 ˚C to +125 ˚C, V_{CC} = AV_{CC} = 3.0V - 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power supply current	I_{A5ALMF}	AV_{CC}	-	25	40	µA	Alarm comparator enabled in fast mode (one channel)
	I_{A5ALMS}		-	7	10	µA	Alarm comparator enabled in slow mode (one channel)
	I_{A5ALMH}		-	-	5	µA	Alarm comparator disabled
ALARM pin input current	I_{ALIN}	ALARM0, ALARM1	-1	-	+1	µA	T_A = 25 ˚C
			-3	-	+3	µA	T_A = 125 ˚C
ALARM pin input voltage range	V_{ALIN}		0	-	AV_{CC}	V	
External low threshold	V_{EVTL}		0.36 * AV_{CC} -5%	0.36 * AV_{CC}	0.36 * AV_{CC} +5%	V	INTREF=0
External high threshold	V_{EVTH}		0.78 * AV_{CC} -3%	0.78 * AV_{CC}	0.78 * AV_{CC} +3%	V	INTREF=0
Internal low threshold	V_{IVTL}		1.15	1.25	1.35	V	INTREF=1
Internal high threshold	V_{IVTH}		2.45	2.55	2.65	V	INTREF=1
Switching hysteresis	V_{HYS}		50	-	250	mV	
Comparison time	t_{COMPF}		-	0.1	-	µs	CMD=1 (fast)
	t_{COMPS}		-	-	100	µs	CMD=0 (slow)



7. LOW VOLTAGE DETECTOR CHARACTERISTICS

(T_A = -40 ˚C to +125 ˚C, V_{CC} = AV_{CC} = 3.0V - 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power consumptiont	I_{CCLVD}	V_{CC}	-	75	100	µA	
Level 0	V_{DL0}		2.7	-	2.95	V	
Level 1	V_{DL1}		2.9	-	3.2	V	
Level 2	V_{DL2}		3.1	-	3.4	V	
Level 3	V_{DL3}		3.5	-	3.85	V	
Level 4	V_{DL4}		3.6	-	3.95	V	
Level 5	V_{DL5}		3.7	-	4.05	V	
Level 6	V_{DL6}		3.8	-	4.15	V	
Level 7	V_{DL7}		3.9	-	4.3	V	
Level 8	V_{DL8}		4.0	-	4.4	V	
Level 9	V_{DL9}		4.1	-	4.5	V	
Level 10	V_{DL10}		Not supported for this device				
Level 11	V_{DL11}						
Level 12	V_{DL12}						
Level 13	V_{DL13}						
Level 14	V_{DL14}						
Level 15	V_{DL15}						

8. FLASH memory program/erase characteristics

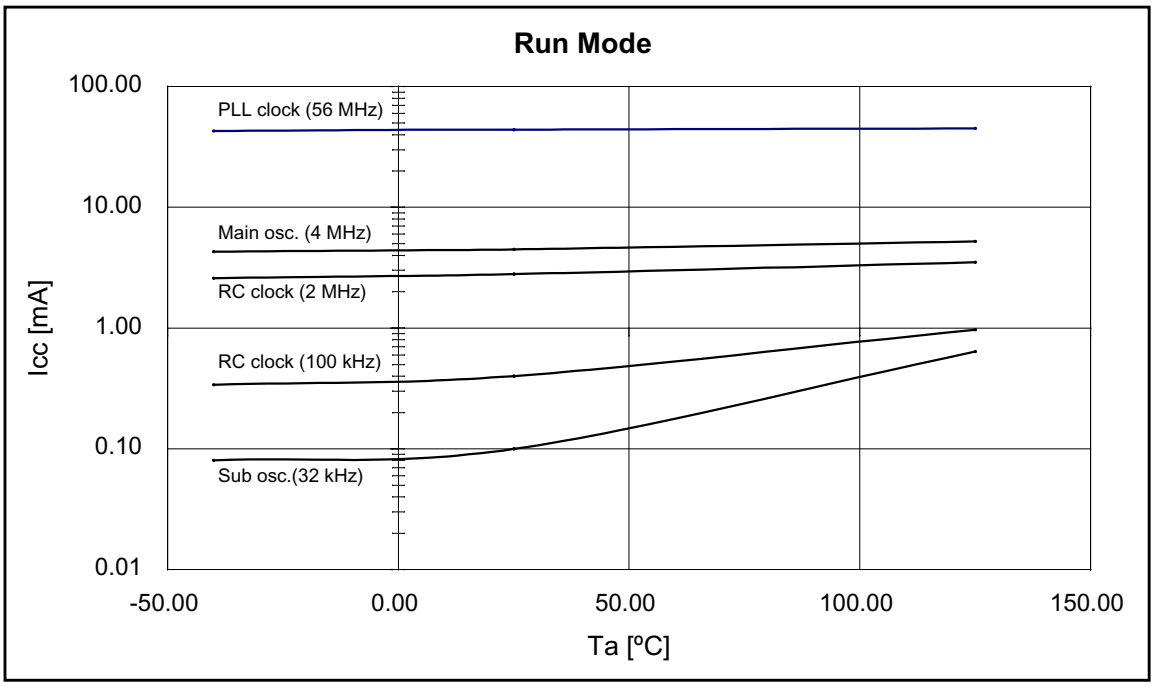
(T_A = 25°C, Vcc = 5.0V)

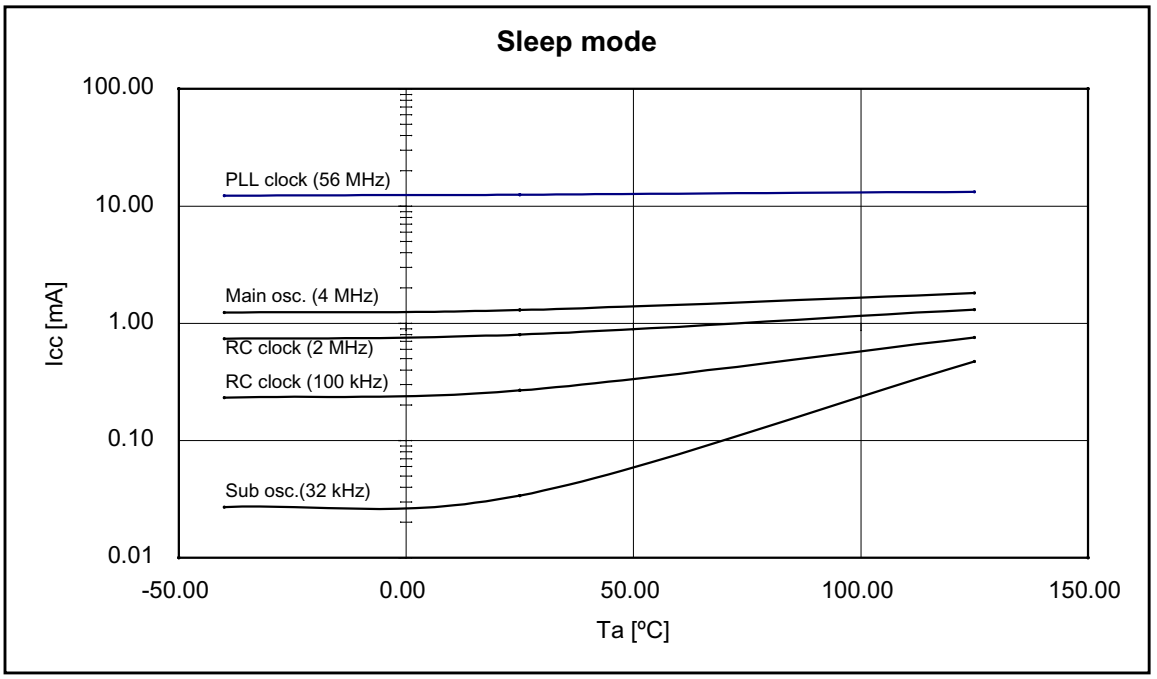
Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.9	3.6	s	Erasure programming time not included
Chip erase time	-	n*0.9	n*3.6	s	n is the number of Flash sector of the device
Word (16-bit width) programming time	-	23	370	us	System overhead time not included
Programme/Erase cycle	10 000			cycle	100 000 cycles for T_j < 105 °C
Flash data retention time	20			year	*1

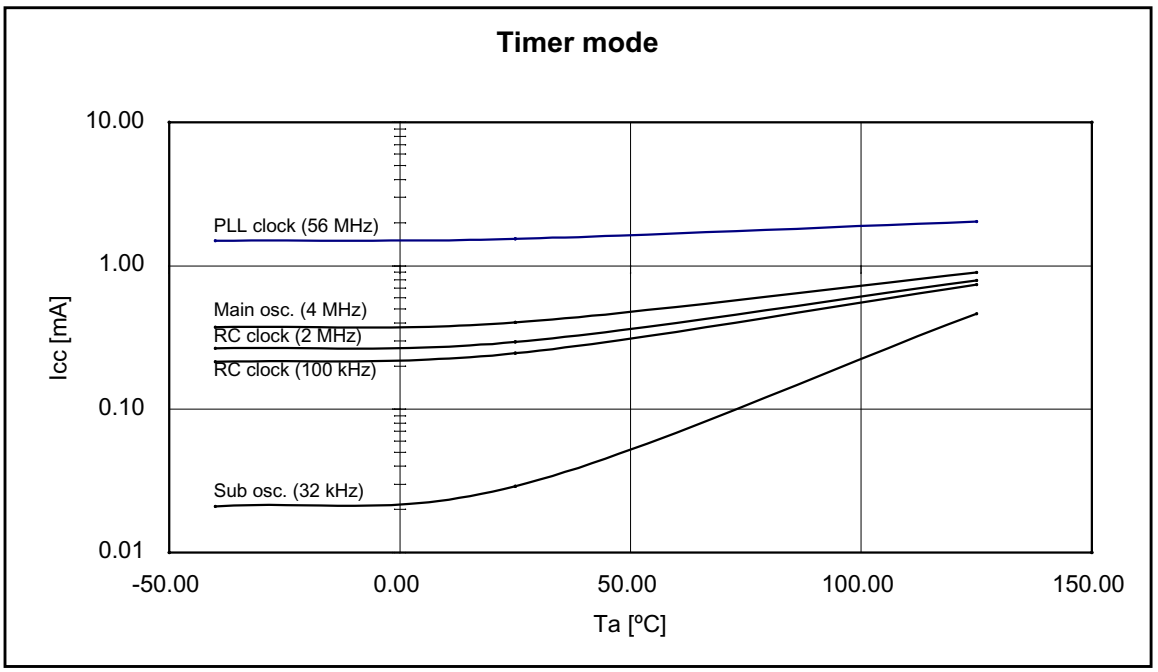
*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into into normalized value at 85°C))

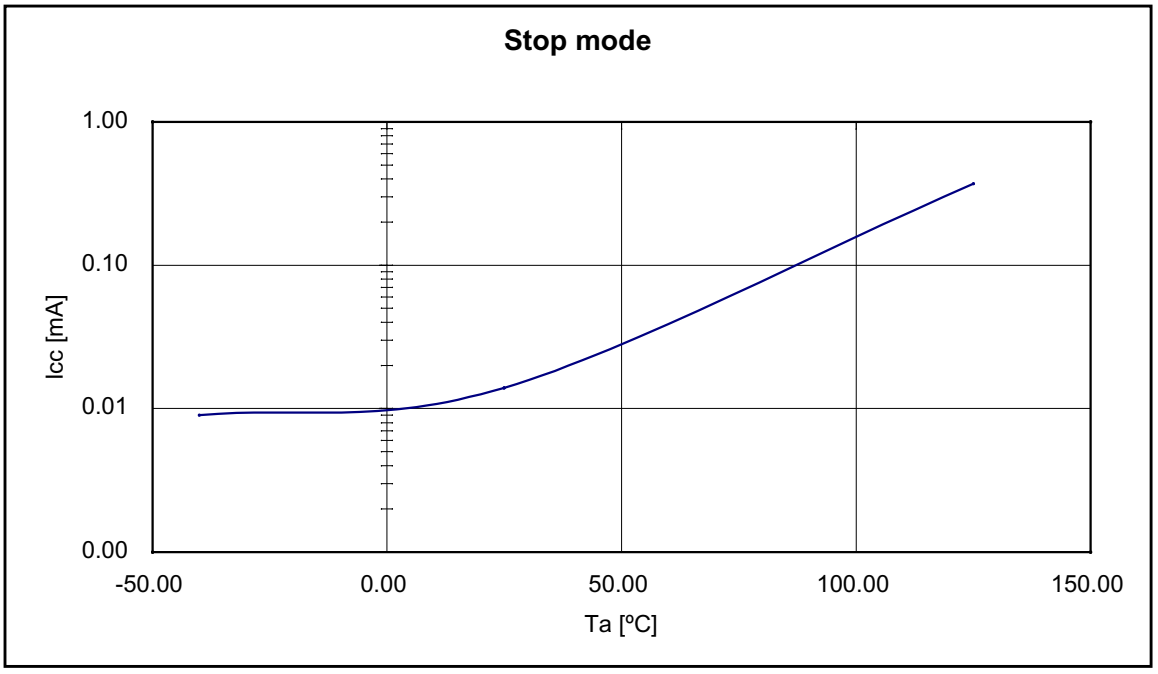
■ EXAMPLE CHARACTERISTICS

The diagrams below show the characteristics of one measured sample of MB96F348HSB with typical process parameters.






Timer mode
10.00
1.00
0.10
0.01
Icc [mA]
PLL clock (56 MHz)
Main osc. (4 MHz)
RC clock (2 MHz)
RC clock (100 kHz)
Sub osc. (32 kHz)
-50.00
0.00
50.00
100.00
150.00
Ta [ºC]


Stop mode
1.00
0.10
0.01
0.00
Icc [mA]
-50.00
0.00
50.00
100.00
150.00
Ta [ºC]

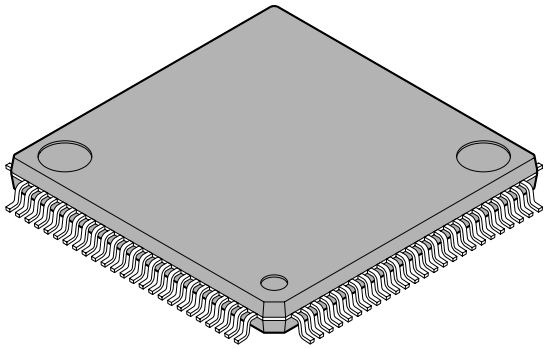
Used settings

Mode	Selected Source Clock	Clock/Regulator Settings
Run mode	PLL	CLKS1 = CLKS2 = CLKB = CLKP1 = 56 MHz CLKP2 = 28 MHz Regulator in High Power Mode Core Voltage = 1.9 V
	Main osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 4 MHz Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock fast	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 2 MHz Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock slow	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 100 kHz Regulator in High Power Mode Core Voltage = 1.8 V
	Sub osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32 kHz Regulator in Low Power Mode A Core Voltage = 1.8 V
Sleep mode	PLL	CLKS1 = CLKS2 = CLKP1 = 56 MHz CLKP2 = 28 MHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.9 V
	Main osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 4 MHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock fast	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 2 MHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock slow	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 100 kHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.8 V
	Sub osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32 kHz (CLKB is stopped in this mode) Regulator in Low Power Mode A Core Voltage = 1.8 V

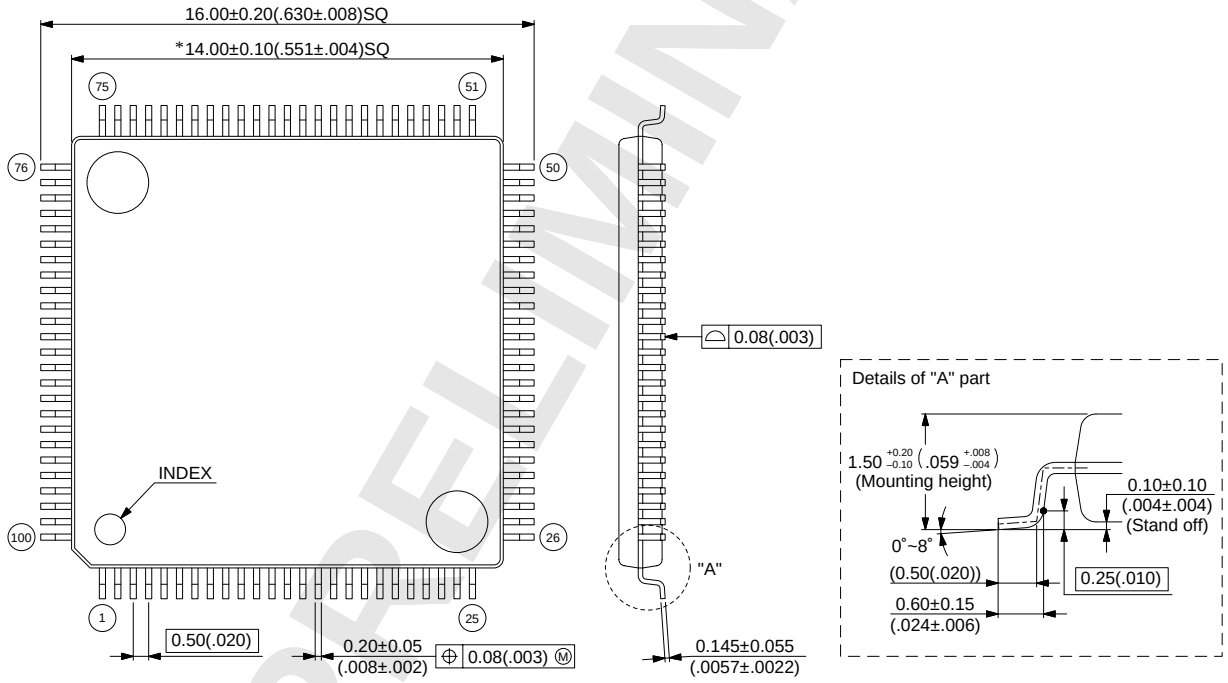
Used settings

Mode	Selected Source Clock	Clock/Regulator Settings
Timer mode	PLL	CLKMC = 4 MHz, CLKPLL = 56 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.9 V
	Main osc.	CLKMC = 4 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	RC clock fast	CLKRC = 2 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	RC clock slow	CLKRC = 100 kHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	Sub osc.	CLKSC = 100 kHz (System clocks are stopped in this mode) Regulator in Low Power Mode A, Core Voltage = 1.8 V
Stop mode	stopped	(All clocks are stopped in this mode) Regulator in Low Power Mode B

■ PACKAGE DIMENSION MB96(F)34x LQFP 100P

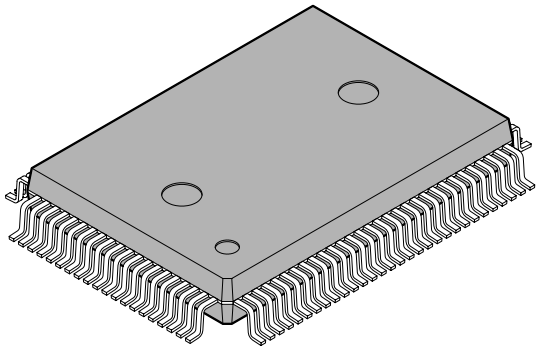
100-pin plastic LQFP		
 (FPT-100P-M20)	Lead pitch	0.50 mm
	Package width × package length	14.0 mm × 14.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm Max
	Weight	0.65 g
	Code (Reference)	P-LFQFP100-14×14-0.50

100-pin plastic LQFP
(FPT-100P-M20)

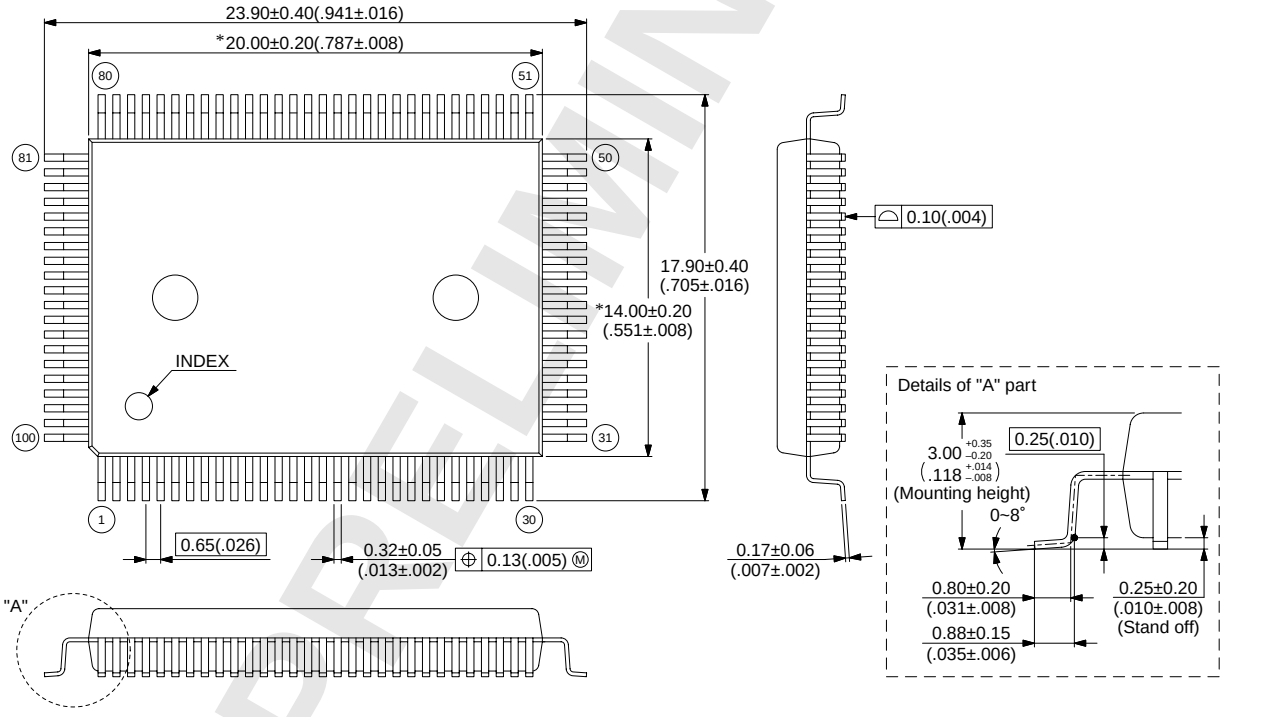


Dimensions in mm (inches).
Note: The values in parentheses are reference values

■ PACKAGE DIMENSION MB96(F)34x QFP 100P

100-pin plastic QFP		
 (FPT-100P-M22)	Lead pitch	0.65 mm
	Package width × package length	14.00 × 20.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	3.35 mm MAX
	Code (Reference)	P-QFP100-14×20-0.65

100-pin plastic QFP
(FPT-100P-M22)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

■ ORDERING INFORMATION

MCU with CAN controller

Part number	Satellite flash memory	Subclock	Persistant Low Voltage Reset	Package	Remarks
MB96F346YSA PQC-GSE2	No	No	Yes	100 pin Plastic QFP (FPT-100P-M22)	
MB96F346RSA PQC-GSE2			No		
MB96F346YWA PQC-GSE2		Yes	Yes		
MB96F346RWA PQC-GSE2			No		
MB96F346YSA PMC-GSE2		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)	
MB96F346RSA PMC-GSE2			No		
MB96F346YWA PMC-GSE2		Yes	Yes		
MB96F346RWA PMC-GSE2			No		
MB96F347YSA PQC-GSE2	No	No	Yes	100 pin Plastic QFP (FPT-100P-M22)	
MB96F347RSA PQC-GSE2			No		
MB96F347YWA PQC-GSE2		Yes	Yes		
MB96F347RWA PQC-GSE2			No		
MB96F347YSA PMC-GSE2		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)	
MB96F347RSA PMC-GSE2			No		
MB96F347YWA PMC-GSE2		Yes	Yes		
MB96F347RWA PMC-GSE2			No		
MB96F348TSB PQC-GSE2	Yes	No	Yes	100 pin Plastic QFP (FPT-100P-M22)	
MB96F348HSB PQC-GSE2			No		
MB96F348TWB PQC-GSE2		Yes	Yes		
MB96F348HWB PQC-GSE2			No		
MB96F348TSB PMC-GSE2		No	Yes	100 pin Plastic LQFP (FPT-100P-M20)	
MB96F348HSB PMC-GSE2			No		
MB96F348TWB PMC-GSE2		Yes	Yes		
MB96F348HWB PMC-GSE2			No		
MB96V300BRB-ES	Emulated by ext. RAM	Yes	No	416 pin Plastic BGA (BGA416-M02)	For evaluation

MCU without CAN controller

Part number	Satellite flash memory	Subclock	Package	Remarks
MB96F346ASA PQC-GSE2	No	No	100 pin Plastic QFP (FPT-100P-M22)	
MB96F346AWA PQC-GSE2		Yes		
MB96F346ASA PMC-GSE2		No	100 pin Plastic LQFP (FPT-100P-M20)	
MB96F346AWA PMC-GSE2		Yes		
MB96F347ASA PQC-GSE2	No	No	100 pin Plastic QFP (FPT-100P-M22)	
MB96F347AWA PQC-GSE2		Yes		
MB96F347ASA PMC-GSE2		No	100 pin Plastic LQFP (FPT-100P-M20)	
MB96F347AWA PMC-GSE2		Yes		
MB96F348ASA PQC-GSE2	No	No	100 pin Plastic QFP (FPT-100P-M22)	
MB96F348AWA PQC-GSE2		Yes		
MB96F348ASA PMC-GSE2		No	100 pin Plastic LQFP (FPT-100P-M20)	
MB96F348AWA PMC-GSE2		Yes		
MB96F348CSB PQC-GSE2	Yes	No	100 pin Plastic QFP (FPT-100P-M22)	
MB96F348CWB PQC-GSE2		Yes		
MB96F348CSB PMC-GSE2		No	100 pin Plastic LQFP (FPT-100P-M20)	
MB96F348CWB PMC-GSE2		Yes		

■ REVISION HISTORY

Revision	Date	Modification
1	2007-05-07	Creation
2	2007-05-10	External bus hold timing update
3	2007-05-23	Electrical characteristics updates
4	2007-08-02	Electrical characteristics updates, Product lineup, changes and ordering information
5	2007-09-12	Addition of the electrical charcateristic examples and the LVD characteristics specifications, updates of the DC charcateristics. Pin circuit type drawing modifications.