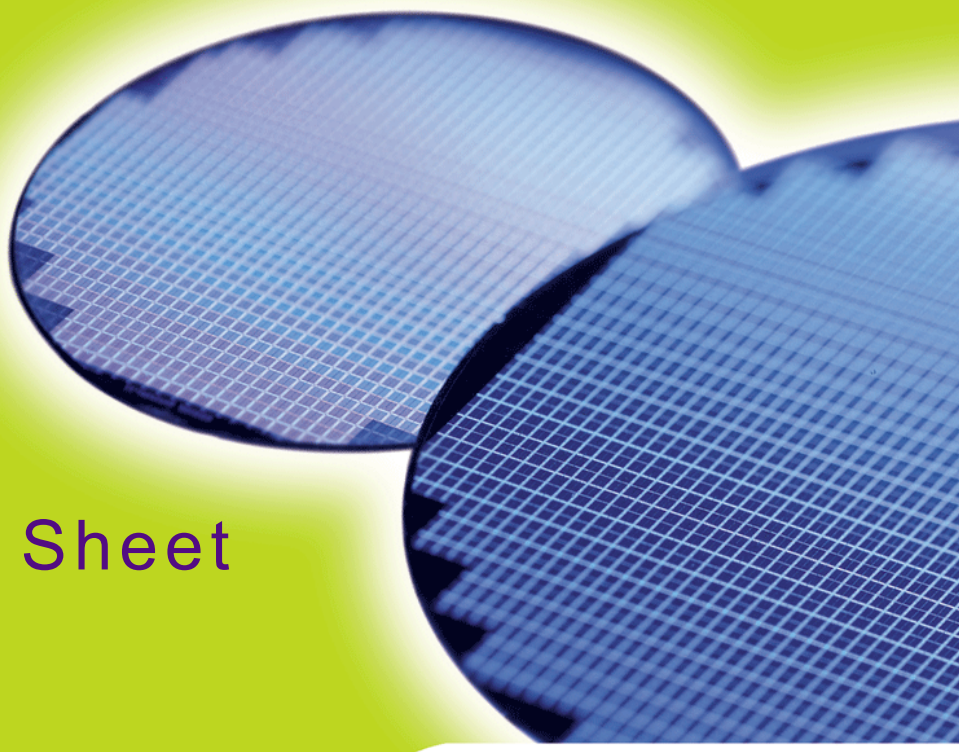
October 2007

HYS64T128020EDL–[25F/2.5/3/3S/3.7]–C
HYS64T256020EDL–[25F/2.5/3/3S/3.7]–C

200-Pin SO-DIMM DDR2 SDRAM Modules
DDR2 SDRAM
SO-DIMM SDRAM
RoHS Compliant



Internet Data Sheet

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HYS64T128020EDL–[25F/2.5/3/3S/3.7]–C, HYS64T256020EDL–[25F/2.5/3/3S/3.7]–C

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1 Overview

This chapter gives an overview of the 200-pin Small-Outline DDR2 SDRAM modules product family and describes its main characteristics.

1.1 Features

- 200-Pin PC2-6400, PC2-5300 and PC2-4200 DDR2 SDRAM memory modules.
- 128M × 64, 256M × 64 module organization and 64M × 16 and 128M × 8 chip organization
- 1 GB and 2 GB modules built with 1-Gbit DDR2 SDRAMs in PG-TFBGA-84 and PG-TFBGA-60 chipsize packages
- Standard Double-Data-Rate-Two Synchronous DRAMs (DDR2 SDRAM) with a single + 1.8 V (± 0.1 V) power supply
- All speed grades faster than DDR2-400 comply with DDR2-400 timing specifications.
- Programmable CAS Latencies (3, 4, 5 and 6), Burst Length (8 & 4).
- Auto Refresh (CBR) and Self Refresh
- Auto Refresh for temperatures above 85 °C t_{REFI} = 3.9 µs.
- Programmable self refresh rate via EMRS2 setting.
- Programmable partial array refresh via EMRS2 settings.
- DCC enabling via EMRS2 setting.
- All inputs and outputs SSTL_1.8 compatible
- Off-Chip Driver Impedance Adjustment (OCD) and On-Die Termination (ODT)
- Serial Presence Detect with E^2PROM
- SO-DIMM Dimensions (nominal): 30 mm high, 67.6 mm wide
- Based on standard reference layouts Raw Cards 'A' and 'F'
- RoHS compliant products[1)]

TABLE 1
Performance Table

QAG Speed Code			**–25F**	**–2.5**	**–3**	**–3S**	**–3.7**	**Unit**
DRAM Speed Grade		**DDR2**	**–800D**	**–800E**	**–667C**	**–667D**	**–533C**	
Module Speed Grade		**PC2**	**–6400D**	**–6400E**	**–5300C**	**–5300D**	**–4200C**	
CAS-RCD-RP latencies			**5–5–5**	**6–6–6**	**4–4–4**	**5–5–5**	**4–4–4**	t_{CK}
Max. Clock Frequency	CL3	f_{CK3}	200	200	200	200	200	MHz
	CL4	f_{CK4}	266	266	333	266	266	MHz
	CL5	f_{CK5}	400	333	333	333	266	MHz
	CL6	f_{CK6}	–	400	–	–	–	MHz
Min. RAS-CAS-Delay		t_{RCD}	12.5	15	12	15	15	ns
Min. Row Precharge Time		t_{RP}	12.5	15	12	15	15	ns
Min. Row Active Time		t_{RAS}	45	45	45	45	45	ns
Min. Row Cycle Time		t_{RC}	57.5	60	57	60	60	ns

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

1.2 Description

The Qimonda HYS64T[128/256]020EDL-[25F/2.5/3/3S/3.7]-C module family are small-outline DIMM modules “SO-DIMMs” with 30 mm height based on DDR2 technology. DIMMs are available as non-ECC modules in128M × 64 (1GB), 256M × 64 (2GB) in organization and density, intended for mounting into 200-pin connector sockets.

The memory array is designed with 1 Gbit Double-Data-Rate-Two (DDR2) Synchronous DRAMs. Decoupling capacitors are mounted on the PCB board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and are write protected; the second 128 bytes are available to the customer.

green Product

TABLE 2
Ordering Information for RoHS Compliant Products

Product Type[1)]	Compliance Code[2)]	Description	SDRAM Technology
PC2-6400-555			
HYS64T128020EDL–25F–C	1GB 2R×16 PC2–6400S–555–12–A0	2 Ranks, Non-ECC	1Gbit (×16)
HYS64T256020EDL–25F–C	2GB 2R×8 PC2–6400S–555–12–F0	2 Ranks, Non-ECC	1Gbit (×8)
PC2-6400-666			
HYS64T128020EDL–2.5–C	1GB 2R×16 PC2–6400S–666–12–A0	2 Ranks, Non-ECC	1Gbit (×16)
HYS64T256020EDL–2.5–C	2GB 2R×8 PC2–6400S–666–12–F0	2 Ranks, Non-ECC	1Gbit (×8)
PC2-5300-444			
HYS64T128020EDL–3–C	1GB 2R×16 PC2–5300S–444–12–A0	2 Ranks, Non-ECC	1Gbit (×16)
HYS64T256020EDL–3–C	2GB 2R×8 PC2–5300S–444–12–F0	2 Ranks, Non-ECC	1Gbit (×8)
PC2-5300-555			
HYS64T128020EDL–3S–C	1GB 2R×16 PC2–5300S–555–12–A0	2 Ranks, Non-ECC	1Gbit (×16)
HYS64T256020EDL–3S–C	2GB 2R×8 PC2–5300S–555–12–F0	2 Ranks, Non-ECC	1Gbit (×8)
PC2-4200-444			
HYS64T128020EDL–3.7–C	1GB 2R×16 PC2–4200S–444–12–A0	2 Ranks, Non-ECC	1Gbit (×16)
HYS64T256020EDL–3.7–C	2GB 2R×8 PC2–4200S–444–12–F0	2 Ranks, Non-ECC	1Gbit (×8)

1) For detailed information regarding Product Type of Qimonda please see chapter "Product Type Nomenclature" of this datasheet.

2) The Compliance Code is printed on the module label and describes the speed grade, for example "PC2–6400S–555–12–F0" where 6400S means Small-Outline DIMM modules with 6.40 GB/sec Module Bandwidth and "555–12" means Column Address Strobe (CAS) latency =5, Row Column Delay (RCD) latency = 5 and Row Precharge (RP) latency = 5 using the latest JEDEC SPD Revision 1.2 and produced on the Raw Card "F".

TABLE 3
Address Format

DIMM Density	Module Organization	Memory Ranks	ECC/ Non-ECC	# of SDRAMs	# of row/bank/column bits	Raw Card
2GB	256M × 64	2	Non-ECC	16	14/3/10	F
1GB	128M × 64	2	Non-ECC	8	13/3/10	A

TABLE 4
Components on Modules

Product Type[1)2)]	DRAM Components[1)]	DRAM Density	DRAM Organisation
HYS64T256020EDL	HYB18T1G800CF	512Mbit	64M × 16
HYS64T128020EDL	HYB18T1G160CF	1Gbit	128M × 8

1) Green Product
2) For a detailed description of all functionalities of the DRAM components on these modules see the component data sheet.

2 Pin Configurations

2.1 Pin Configurations

The pin configuration of the Small Outline DDR2 SDRAM DIMM is listed by function in **Table 5** (200 pins). The abbreviations used in columns Pin Type and Buffer Type are explained in **Table 6** and **Table 7** respectively. The Pin numbering is depicted in **Figure 1**

TABLE 5
Pin Configuration of SO-DIMM

Pin No.	Name	Pin Type	Buffer Type	Function
Clock Signals				
30	CK0	I	SSTL	**Clock Signals 1:0, Complement Clock Signals 1:0** The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and the falling edge of $\overline{CK}$. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
164	CK1	I	SSTL	
32	$\overline{CK0}$	I	SSTL	
166	$\overline{CK1}$	I	SSTL	
79	CKE0	I	SSTL	**Clock Enable Rank 1:0** Activates the DDR2 SDRAM CK signal when HIGH and deactivates the CK signal when LOW. By deactivating the clocks, CKE LOW initiates the Power Down Mode or the Self Refresh Mode. *Note: 2 Ranks module*
80	CKE1	I	SSTL	
	NC	NC	—	**Not Connected** *Note: 1-rank module*
Control Signals				
110	$\overline{S0}$	I	SSTL	**Chip Select Rank 1:0** Enables the associated DDR2 SDRAM command decoder when LOW and disables the command decoder when HIGH. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{S0}$; Rank 1 is selected by $\overline{S1}$. Ranks are also called "Physical banks".2 Ranks module
115	$\overline{S1}$	I	SSTL	
	NC	NC	—	**Not Connected** *Note: 1-rank module*
108	$\overline{RAS}$	I	SSTL	**Row Address Strobe** When sampled at the cross point of the rising edge of CK, and falling edge of $\overline{CK}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation to be executed by the SDRAM.
113	$\overline{CAS}$	I	SSTL	**Column Address Strobe**

Pin No.	Name	Pin Type	Buffer Type	Function
109	$\overline{WE}$	I	SSTL	**Write Enable**
Address Signals				
107	BA0	I	SSTL	**Bank Address Bus 2:0** Selects which DDR2 SDRAM internal bank of four or eight is activated.
106	BA1	I	SSTL	
85	BA2	I	SSTL	**Bank Address Bus 2** Greater than 512Mb DDR2 SDRAMS
	NC	NC	SSTL	**Less than 1Gb DDR2 SDRAMS**
102	A0	I	SSTL	**Address Bus 12:0** During a Bank Activate command cycle, defines the row address when sampled at the cross-point of the rising edge of CK and falling edge of $\overline{CK}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is HIGH, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is LOW, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is HIGH, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is LOW, then BA0-BAn are used to define which bank to precharge.
101	A1	I	SSTL	
100	A2	I	SSTL	
99	A3	I	SSTL	
98	A4	I	SSTL	
97	A5	I	SSTL	
94	A6	I	SSTL	
92	A7	I	SSTL	
93	A8	I	SSTL	
91	A9	I	SSTL	
105	A10	I	SSTL	
	AP	I	SSTL	
90	A11	I	SSTL	
89	A12	I	SSTL	**Address Signal 12** *Note: Module based on 256 Mbit or larger dies*
116	A13	I	SSTL	**Address Signal 13** *Note: 1 Gbit based module*
	NC	NC	—	**Not Connected** *Note: Module based on 512 Mbit or smaller dies*
86	A14	I	SSTL	**Address Signal 14** *Note: 2 Gbit based module*
	NC	NC	—	**Not Connected** *Note: Module based on 1 Gbit or smaller dies*
Data Signals				
5	DQ0	I/O	SSTL	**Data Bus 63:0** *Note: Data Input / Output pins*
7	DQ1	I/O	SSTL	
17	DQ2	I/O	SSTL	
19	DQ3	I/O	SSTL	
4	DQ4	I/O	SSTL	
6	DQ5	I/O	SSTL	
14	DQ6	I/O	SSTL	
16	DQ7	I/O	SSTL	
23	DQ8	I/O	SSTL	

Pin No.	Name	Pin Type	Buffer Type	Function
25	DQ9	I/O	SSTL	**Data Bus 63:0** *Note: Data Input / Output pins*
35	DQ10	I/O	SSTL	
37	DQ11	I/O	SSTL	
20	DQ12	I/O	SSTL	
22	DQ13	I/O	SSTL	
36	DQ14	I/O	SSTL	
38	DQ15	I/O	SSTL	
43	DQ16	I/O	SSTL	
45	DQ17	I/O	SSTL	
55	DQ18	I/O	SSTL	
57	DQ19	I/O	SSTL	
44	DQ20	I/O	SSTL	
46	DQ21	I/O	SSTL	
56	DQ22	I/O	SSTL	
58	DQ23	I/O	SSTL	
61	DQ24	I/O	SSTL	
63	DQ25	I/O	SSTL	
73	DQ26	I/O	SSTL	
75	DQ27	I/O	SSTL	
62	DQ28	I/O	SSTL	
64	DQ29	I/O	SSTL	
74	DQ30	I/O	SSTL	
76	DQ31	I/O	SSTL	
123	DQ32	I/O	SSTL	
125	DQ33	I/O	SSTL	
135	DQ34	I/O	SSTL	
137	DQ35	I/O	SSTL	
124	DQ36	I/O	SSTL	
126	DQ37	I/O	SSTL	
134	DQ38	I/O	SSTL	
136	DQ39	I/O	SSTL	
141	DQ40	I/O	SSTL	
143	DQ41	I/O	SSTL	
151	DQ42	I/O	SSTL	
153	DQ43	I/O	SSTL	
140	DQ44	I/O	SSTL	
142	DQ45	I/O	SSTL	
152	DQ46	I/O	SSTL	
154	DQ47	I/O	SSTL	
157	DQ48	I/O	SSTL	

Pin No.	Name	Pin Type	Buffer Type	Function
159	DQ49	I/O	SSTL	**Data Bus 63:0** *Note: Data Input / Output pins*
173	DQ50	I/O	SSTL	
175	DQ51	I/O	SSTL	
158	DQ52	I/O	SSTL	
160	DQ53	I/O	SSTL	
174	DQ54	I/O	SSTL	
176	DQ55	I/O	SSTL	
179	DQ56	I/O	SSTL	
181	DQ57	I/O	SSTL	
189	DQ58	I/O	SSTL	
191	DQ59	I/O	SSTL	
180	DQ60	I/O	SSTL	
182	DQ61	I/O	SSTL	
192	DQ62	I/O	SSTL	
194	DQ63	I/O	SSTL	
Data Strobe Signals				
13	DQS0	I/O	SSTL	**Data Strobe Bus 7:0** The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode the data strobe is sourced by the DDR2 SDRAM and is sent at the leading edge of the data window. $\overline{\text{DQS}}$ signals are complements, and timing is relative to the cross-point of respective DQS and $\overline{\text{DQS}}$. If the module is to be operated in single ended strobe mode, all $\overline{\text{DQS}}$ signals must be tied on the system board to V_{SS} and DDR2 SDRAM mode registers programmed appropriately.
11	$\overline{\text{DQS0}}$	I/O	SSTL	
31	DQS1	I/O	SSTL	
29	$\overline{\text{DQS1}}$	I/O	SSTL	
51	DQS2	I/O	SSTL	
49	$\overline{\text{DQS2}}$	I/O	SSTL	
70	DQS3	I/O	SSTL	
68	$\overline{\text{DQS3}}$	I/O	SSTL	
131	DQS4	I/O	SSTL	
129	$\overline{\text{DQS4}}$	I/O	SSTL	
148	DQS5	I/O	SSTL	
146	$\overline{\text{DQS5}}$	I/O	SSTL	
169	DQS6	I/O	SSTL	
167	$\overline{\text{DQS6}}$	I/O	SSTL	
188	DQS7	I/O	SSTL	
186	$\overline{\text{DQS7}}$	I/O	SSTL	
Data Mask Signals				

Pin No.	Name	Pin Type	Buffer Type	Function
10	DM0	I	SSTL	**Data Mask Bus 7:0** The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is LOW but blocks the write operation if it is HIGH. In Read mode, DM lines have no effect.
26	DM1	I	SSTL	
52	DM2	I	SSTL	
67	DM3	I	SSTL	
130	DM4	I	SSTL	
147	DM5	I	SSTL	
170	DM6	I	SSTL	
185	DM7	I	SSTL	
EEPROM				
197	SCL	I	CMOS	**Serial Bus Clock** This signal is used to clock data into and out of the SPD EEPROM and Thermal sensor.
195	SDA	I/O	OD	**Serial Bus Data** This is a bidirectional pin use to transfer data into and out of the SPD EEPROM and Thermal sensor. A resistor must be connected from SDA to V_{DDSPD} on the motherboard to act as a pull-up.
198	SA0	I	CMOS	**Serial Address Select Bus 2:0** Address pins used to select the SPD and Thermal sensor base address.
200	SA1	I	CMOS	
50	$\overline{EVENT}$	O	OD	**EVENT** The optional EVENT pin is reserved for use to flag critical module temperature and is used in conjunction with Thermal Sensor.
	NC	—	—	**Not Connected** Not connected on modules without temperature sensors.
Power Supplies				
1	V_{REF}	AI	—	**I/O Reference Voltage** Reference voltage for the SSTL-18 inputs.
199	V_{DDSPD}	PWR	—	**EEPROM Power Supply** Power supplies for Serial Presence Detect, Thermal Sensor and ground for the module.
81,82,87,88,95,96,103,104, 111,112,117,118	V_{DD}	PWR	—	**Power Supply** Power supplies for core, I/O and ground for the module.
2,3,8,9,12,15,18,21,24,27,28, 33,34,39,40,41,42,47,48,53, 54,59,60,65,66,71,72,77,78, 121,122,127,128,132,133,138,13 9,144,145,149,150,155,156, 161,162,165,168, 171,172,177, 178,183,184,187,190,193,196	V_{SS}	GND	—	**Ground Plane** Power supplies for core, I/O, Serial Presence Detect, Thermal Sensor and ground for the module.
Other pins				
114	ODT0	I	SSTL	**On-Die Termination Control 1:0**

Pin No.	Name	Pin Type	Buffer Type	Function
119	ODT1	I	SSTL	**On-Die Termination Control 1** Asserts on-die termination for DQ, DM, DQS, and $\overline{\text{DQS}}$ signals if enabled via the DDR2 SDRAM mode register. *Note: 2 Rank modules*
	NC	NC	—	**Not Connected** *Note: 1 Rank modules*
69,83,84,120,163	NC	NC	—	**Not connected** Pins not connected on Qimonda SO-DIMMs

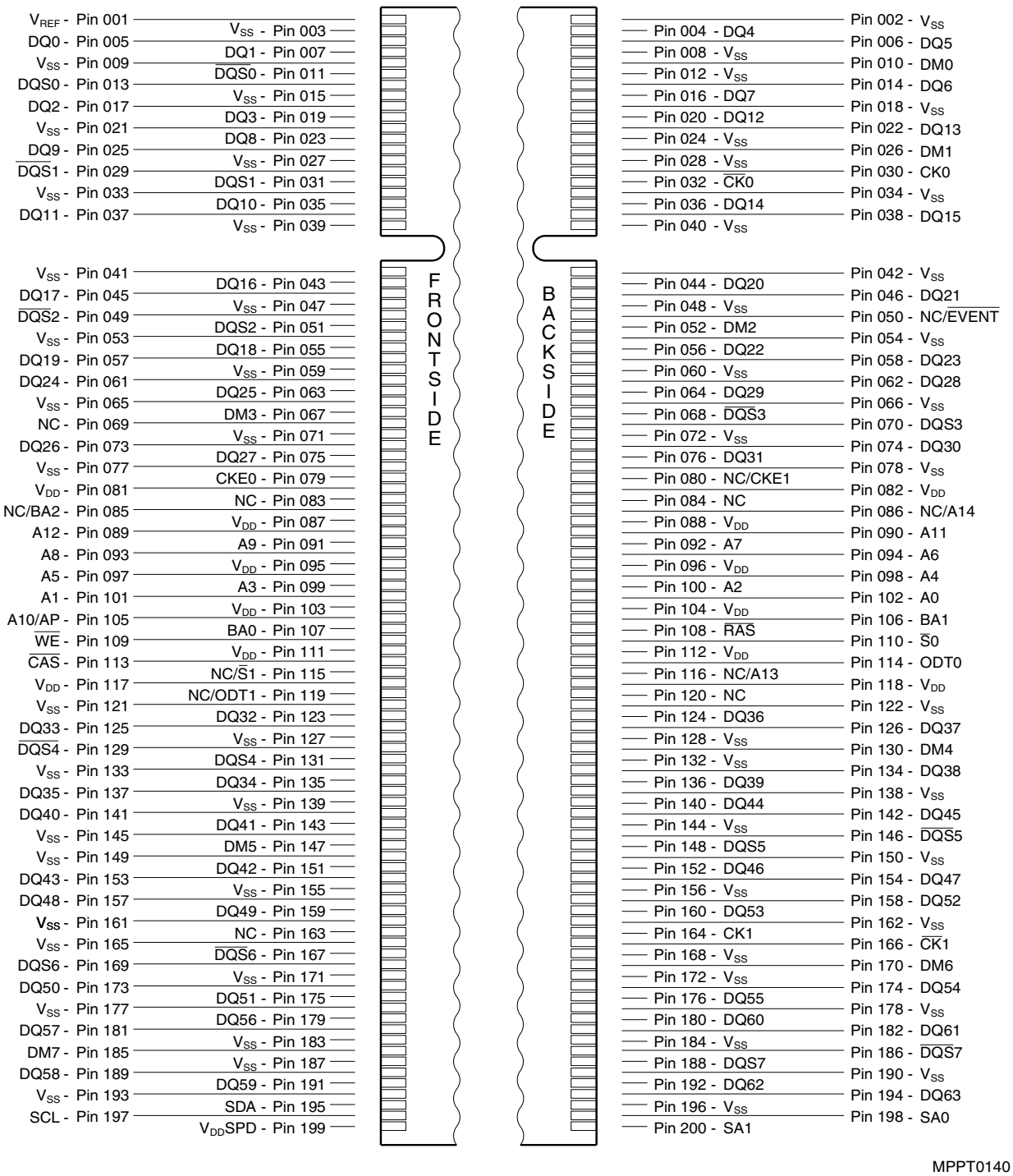
TABLE 6
Abbreviations for pin Type

Abbreviation	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

TABLE 7
Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL_18)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tri-state, and allows multiple devices to share as a wire-OR.

FIGURE 1
Pin Configuration SO-DIMM (200 pin)



3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Attention: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TABLE 8
Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	–1.0	+2.3	V	1)
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	–0.5	+2.3	V	1)1)
V_{DDL}	Voltage on V_{DDL} pin relative to V_{SS}	–0.5	+2.3	V	1)1)
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.5	+2.3	V	1)

1) When V_{DD} and V_{DDQ} and V_{DDL} are less than 500 mV; V_{REF} may be equal to or less than 300 mV.

TABLE 9
Environmental Requirements

Parameter	Symbol	Values		Unit	Note
		Min.	Max.		
Operating temperature (ambient)	T_{OPR}	0	+65	°C	
Storage Temperature	T_{STG}	– 50	+100	°C	1)
Barometric Pressure (operating & storage)	PBar	+69	+105	kPa	2)
Operating Humidity (relative)	H_{OPR}	10	90	%	
Storage Humidity (without condensation)	H_{STG}	5	95	%	

1) Storage Temperature is the case surface temperature on the center/top side of the DRAM.
2) Up to 3000 m.

TABLE 10
DRAM Component Operating Temperature Range

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
T_{CASE}	Operating Temperature	0	95	°C	1)2)3)4)

1) Operating Temperature is the case surface temperature on the center / top side of the DRAM.
2) The operating temperature range are the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0 - 95 °C under all other specification parameters.
3) Above 85 °C the Auto-Refresh command interval has to be reduced to t_{REFI}= 3.9 µs
4) When operating this product in the 85 °C to 95 °C T_{CASE} temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to “1”. When the High Temperature Self Refresh is enabled there is an increase of I_{DD6} by approximately 50%

3.2 DC Operating Conditions

TABLE 11
Supply Voltage Levels and DC Operating Conditions

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Device Supply Voltage	V_{DD}	1.7	1.8	1.9	V	
Output Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V	1)
Input Reference Voltage	V_{REF}	0.49 × V_{DDQ}	0.5 × V_{DDQ}	0.51 × V_{DDQ}	V	2)
SPD Supply Voltage	V_{DDSPD}	1.7	—	3.6	V	
DC Input Logic High	$V_{IH(DC)}$	V_{REF} + 0.125	—	V_{DDQ} + 0.3	V	
DC Input Logic Low	$V_{IL\ (DC)}$	– 0.30	—	V_{REF} – 0.125	V	
In / Output Leakage Current	I_L	– 5	—	5	µA	3)

1) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}
2) Peak to peak AC noise on V_{REF} may not exceed ± 2% V_{REF} (DC). V_{REF} is also expected to track noise in V_{DDQ}.
3) Input voltage for any connector pin under test of 0 V ≤ V_{IN} ≤ V_{DDQ} + 0.3 V; all other pins at 0 V. Current is per pin

3.3 Timing Characteristics

3.3.1 Speed Grade Definitions

TABLE 12
Speed Grade Definition

Speed Grade			DDR2–800D		DDR2–800E		Unit	Note
QAG Sort Name			–25F		–2.5			
CAS-RCD-RP latencies			5–5–5		6–6–6		t_{CK}	
Parameter		Symbol	Min.	Max.	Min.	Max.	—	
Clock Period	@ CL = 3	t_{CK}	5	8	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3.75	8	3.75	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	2.5	8	3	8	ns	1)2)3)4)
	@ CL = 6	t_{CK}	2.5	8	2.5	8	ns	1)2)3)4)
Row Active Time		t_{RAS}	45	70k	45	70k	ns	1)2)3)4)5)
Row Cycle Time		t_{RC}	57.5	—	60	—	ns	1)2)3)4)
RAS-CAS-Delay		t_{RCD}	12.5	—	15	—	ns	1)2)3)4)
Row Precharge Time		t_{RP}	12.5	—	15	—	ns	1)2)3)4)

TABLE 13
Speed Grade Definition

Speed Grade			DDR2–667C		DDR2–667D		DDR2–533C		Unit	Note
QAG Sort Name			–3		–3S		–3.7			
CAS-RCD-RP latencies			4–4–4		5–5–5		4–4–4		t_{CK}	
Parameter		Symbol	Min.	Max.	Min.	Max.	Min.	Max.	—	
Clock Period	@ CL = 3	t_{CK}	5	8	5	8	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3	8	3.75	8	3.75	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	3	8	3	8	3.75	8	ns	1)2)3)4)
Row Active Time		t_{RAS}	45	70k	45	70k	45	70k	ns	1)2)3)4)5)
Row Cycle Time		t_{RC}	57	—	60	—	60	—	ns	1)2)3)4)
RAS-CAS-Delay		t_{RCD}	12	—	15	—	15	—	ns	1)2)3)4)
Row Precharge Time		t_{RP}	12	—	15	—	15	—	ns	1)2)3)4)

1) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) mentioned in Component datasheet.

2) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode
3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ}
4) The output timing reference voltage level is V_{TT}.
5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.

3.3.2 Component AC Timing Parameters

TABLE 14
DRAM Component Timing Parameter by Speed Grade - DDR2–800 and DDR2–667

Parameter	Symbol	DDR2–800		DDR2–667		Unit	Note[2)3)5)6)7)8)]
		Min.	Max.	Min.	Max.		
CAS to CAS command delay	t_{CCD}	2	—	2	—	nCK	
Average clock high pulse width	$t_{CH.AVG}$	0.48	0.52	0.48	0.52	$t_{CK.AVG}$	10)11)
Average clock period	$t_{CK.AVG}$	2500	8000	3000	8000	ps	
CKE minimum pulse width (high and low pulse width)	t_{CKE}	3	—	3	—	nCK	12)
Average clock low pulse width	$t_{CL.AVG}$	0.48	0.52	0.48	0.52	$t_{CK.AVG}$	10)11)
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{nRP}	—	WR + t_{nRP}	—	nCK	13)14)
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	t_{IS} + $t_{CK\ .AVG}$ + t_{IH}	—	t_{IS} + $t_{CK\ .AVG}$ + t_{IH}	—	ns	
DQ and DM input hold time	$t_{DH.BASE}$	125	—	175	—	ps	15)19)20)
DQ and DM input pulse width for each input	t_{DIPW}	0.35	—	0.35	—	$t_{CK.AVG}$	
DQS input high pulse width	t_{DQSH}	0.35	—	0.35	—	$t_{CK.AVG}$	
DQS input low pulse width	t_{DQSL}	0.35	—	0.35	—	$t_{CK.AVG}$	
DQS-DQ skew for DQS & associated DQ signals	t_{DQSQ}	—	200	—	240	ps	16)
DQS latching rising transition to associated clock edges	t_{DQSS}	– 0.25	+ 0.25	– 0.25	+ 0.25	$t_{CK.AVG}$	17)
DQ and DM input setup time	$t_{DS.BASE}$	50	—	100	—	ps	18)19)20)
DQS falling edge hold time from CK	t_{DSH}	0.2	—	0.2	—	$t_{CK.AVG}$	17)
DQS falling edge to CK setup time	t_{DSS}	0.2	—	0.2	—	$t_{CK.AVG}$	17)
Four Activate Window for 1KB page size products	t_{FAW}	35	—	37.5	—	ns	35)
Four Activate Window for 2KB page size products	t_{FAW}	45	—	50	—	ns	35)
CK half pulse width	t_{HP}	Min($t_{CH.ABS}$, $t_{CL.ABS}$)	—	Min($t_{CH.ABS}$, $t_{CL.ABS}$)	—	ps	21)
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	—	$t_{AC.MAX}$	ps	9)22)
Address and control input hold time	$t_{IH.BASE}$	250	—	275	—	ps	23)25)

Parameter	Symbol	DDR2–800		DDR2–667		Unit	Note[2)3)5)6)7)8)]
		Min.	Max.	Min.	Max.		
Control & address input pulse width for each input	t_{IPW}	0.6	—	0.6	—	$t_{CK.AVG}$	
Address and control input setup time	$t_{IS.BASE}$	175	—	200	—	ps	24)25)
DQ low impedance time from CK/$\overline{CK}$	$t_{LZ.DQ}$	2 x $t_{AC.MIN}$	$t_{AC.MAX}$	2 x $t_{AC.MIN}$	$t_{AC.MAX}$	ps	9)22)
DQS/$\overline{DQS}$ low-impedance time from CK / $\overline{CK}$	$t_{LZ.DQS}$	$t_{AC.MIN}$	$t_{AC.MAX}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	9)22)
MRS command to ODT update delay	t_{MOD}	0	12	0	12	ns	35)
Mode register set command cycle time	t_{MRD}	2	—	2	—	nCK	
OCD drive mode output delay	t_{OIT}	0	12	0	12	ns	35)
DQ/DQS output hold time from DQS	t_{QH}	$t_{HP} - t_{QHS}$	—	$t_{HP} - t_{QHS}$	—	ps	26)
DQ hold skew factor	t_{QHS}	—	300	—	340	ps	27)
Average periodic refresh Interval	t_{REFI}	—	7.8	—	7.8	µs	28)29)
		—	3.9	—	3.9	µs	28)30)
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	127.5	—	127.5	—	ns	31)
Precharge-All (8 banks) command period	t_{RP}	$t_{RP} + 1 \times t_{CK}$	—	$t_{RP} + 1 \times t_{CK}$	—	ns	
Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	$t_{CK.AVG}$	32)33)
Read postamble	t_{RPST}	0.4	0.6	0.4	0.6	$t_{CK.AVG}$	32)34)
Active to active command period for 1KB page size products	t_{RRD}	7.5	—	7.5	—	ns	35)
Active to active command period for 2KB page size products	t_{RRD}	10	—	10	—	ns	35)
Internal Read to Precharge command delay	t_{RTP}	7.5	—	7.5	—	ns	35)
Write preamble	t_{WPRE}	0.35	—	0.35	—	$t_{CK.AVG}$	
Write postamble	t_{WPST}	0.4	0.6	0.4	0.6	$t_{CK.AVG}$	
Write recovery time	t_{WR}	15	—	15	—	ns	35)
Internal write to read command delay	t_{WTR}	7.5	—	7.5	—	ns	35)36)
Exit power down to read command	t_{XARD}	2	—	2	—	nCK	
Exit active power-down mode to read command (slow exit, lower power)	t_{XARDS}	8 – AL	—	7 – AL	—	nCK	
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	2	—	nCK	
Exit self-refresh to a non-read command	t_{XSNR}	t_{RFC} +10	—	t_{RFC} +10	—	ns	35)
Exit self-refresh to read command	t_{XSRD}	200	—	200	—	nCK	
Write command to DQS associated clock edges	WL	RL – 1		RL–1		nCK	

1) For details and notes see the relevant Qimonda component data sheet

2) V_{DDQ} = 1.8 V ± 0.1V; V_{DD} = 1.8 V ± 0.1 V.
3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
4) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
5) The CK / $\overline{CK}$ input reference level (for timing reference to CK / $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode. component
6) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
7) The output timing reference voltage level is V_{TT}. component datasheet
8) New units, '$t_{CK.AVG}$' and 'nCK', are introduced in DDR2–667 and DDR2–800. Unit '$t_{CK.AVG}$' represents the actual $t_{CK.AVG}$ of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges. Note that in DDR2–400 and DDR2–533, 't_{CK}' is used for both concepts. Example: t_{XP} = 2 [nCK] means; if Power Down exit is registered at Tm, an Active command may be registered at Tm + 2, even if (Tm + 2 - Tm) is 2 x $t_{CK.AVG}$ + $t_{ERR.2PER(Min)}$.
9) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{ERR(6\text{-}10per)}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{ERR(6\text{-}10PER).MIN}$ = – 272 ps and $t_{ERR(6\text{-}10PER).MAX}$ = + 293 ps, then $t_{DQSCK.MIN(DERATED)}$ = $t_{DQSCK.MIN}$ – $t_{ERR(6\text{-}10PER).MAX}$ = – 400 ps – 293 ps = – 693 ps and $t_{DQSCK.MAX(DERATED)}$ = $t_{DQSCK.MAX}$ – $t_{ERR(6\text{-}10PER).MIN}$ = 400 ps + 272 ps = + 672 ps. Similarly, $t_{LZ.DQ}$ for DDR2–667 derates to $t_{LZ.DQ.MIN(DERATED)}$ = - 900 ps – 293 ps = – 1193 ps and $t_{LZ.DQ.MAX(DERATED)}$ = 450 ps + 272 ps = + 722 ps. (Caution on the MIN/MAX usage!)
10) Input clock jitter spec parameter. These parameters component datasheet are referred to as 'input clock jitter spec parameters' and these parameters apply to DDR2–667 and DDR2–800 only. The jitter specified is a random jitter meeting a Gaussian distribution.
11) These parameters are specified per their average values, however it is understood that the relationship component datasheet between the average timing and the absolute instantaneous timing holds all the times (min. and max of SPEC values are to be used for calculations component datasheet).
12) $t_{CKE.MIN}$ of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of t_{IS} + 2 x t_{CK} + t_{IH}.
13) DAL = WR + RU{t_{RP}(ns) / t_{CK}(ns)}, where RU stands for round up. WR refers to the tWR parameter stored in the MRS. For t_{RP}, if the result of the division is not already an integer, round up to the next highest integer. t_{CK} refers to the application clock period. Example: For DDR2–533 at t_{CK} = 3.75 ns with t_{WR} programmed to 4 clocks. t_{DAL} = 4 + (15 ns / 3.75 ns) clocks = 4 + (4) clocks = 8 clocks.
14) $t_{DAL.nCK}$ = WR [nCK] + $t_{nRP.nCK}$ = WR + RU{t_{RP} [ps] / $t_{CK.AVG}$[ps] }, where WR is the value programmed in the EMR.
15) Input waveform timing t_{DH} with differential data strobe enabled MR[bit10] = 0, is referenced from the differential data strobe crosspoint to the input signal crossing at the $V_{IH.DC}$ level for a falling signal and from the differential data strobe crosspoint to the input signal crossing at the $V_{IL.DC}$ level for a rising signal applied to the device under test. DQS, DQS signals must be monotonic between $V_{IL.DC.MAX}$ and $V_{IH.DC.MIN}$. See **Figure 3**.
16) t_{DQSQ}: Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output slew rate mismatch between DQS / $\overline{DQS}$ and associated DQ in any given cycle.
17) These parameters are measured from a data strobe signal ((L/U/R)DQS / $\overline{DQS}$) crossing to its respective clock signal (CK / $\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT.PER}$, $t_{JIT.CC}$, etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.
18) Input waveform timing t_{DS} with differential data strobe enabled MR[bit10] = 0, is referenced from the input signal crossing at the $V_{IH.AC}$ level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the $V_{IL.AC}$ level to the differential data strobe crosspoint for a falling signal applied to the device under test. DQS, DQS signals must be monotonic between $V_{il(DC)MAX}$ and $V_{ih(DC)MIN}$. See **Figure 3**.
19) If t_{DS} or t_{DH} is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.
20) These parameters are measured from a data signal ((L/U)DM, (L/U)DQ0, (L/U)DQ1, etc.) transition edge to its respective data strobe signal ((L/U/R)DQS / $\overline{DQS}$) crossing.
21) t_{HP} is the minimum of the absolute half period of the actual input clock. t_{HP} is an input parameter but not an input specification parameter. It is used in conjunction with t_{QHS} to derive the DRAM output timing t_{QH}. The value to be used for t_{QH} calculation is determined by the following equation; t_{HP} = MIN ($t_{CH.ABS}$, $t_{CL.ABS}$), where, $t_{CH.ABS}$ is the minimum of the actual instantaneous clock high time; $t_{CL.ABS}$ is the minimum of the actual instantaneous clock low time.
22) t_{HZ} and t_{LZ} transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (t_{HZ}), or begins driving (t_{LZ}) .
23) input waveform timing is referenced from the input signal crossing at the $V_{IL.DC}$ level for a rising signal and $V_{IH.DC}$ for a falling signal applied to the device under test. See **Figure 4**.
24) Input waveform timing is referenced from the input signal crossing at the $V_{IH.AC}$ level for a rising signal and $V_{IL.AC}$ for a falling signal applied to the device under test. See **Figure 4**.
25) These parameters are measured from a command/address signal (CKE, CS, RAS, CAS, WE, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK / $\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT.PER}$, $t_{JIT.CC}$,

etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

26) $t_{QH} = t_{HP} - t_{QHS}$, where: t_{HP} is the minimum of the absolute half period of the actual input clock; and t_{QHS} is the specification value under the max column. {The less half-pulse width distortion present, the larger the t_{QH} value is; and the larger the valid data eye will be.} Examples: 1) If the system provides t_{HP} of 1315 ps into a DDR2–667 SDRAM, the DRAM provides t_{QH} of 975 ps minimum. 2) If the system provides t_{HP} of 1420 ps into a DDR2–667 SDRAM, the DRAM provides t_{QH} of 1080 ps minimum.

27) t_{QHS} accounts for: 1) The pulse duration distortion of on-chip clock circuits, which represents how well the actual t_{HP} at the input is transferred to the output; and 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are independent of each other, due to data pin skew, output pattern effects, and pchannel to n-channel variation of the output drivers.

28) The Auto-Refresh command interval has be reduced to 3.9 µs when operating the DDR2 DRAM in a temperature range between 85 °C and 95 °C.

29) 0 °C≤ T_{CASE} ≤ 85 °C.

30) 85 °C < T_{CASE} ≤ 95 °C.

31) A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device.

32) t_{RPST} end point and t_{RPRE} begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (t_{RPST}), or begins driving (t_{RPRE}). **Figure 2** shows a method to calculate these points when the device is no longer driving (t_{RPST}), or begins driving (t_{RPRE}) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

33) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT.PER}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{JIT.PER.MIN}$ = – 72 ps and $t_{JIT.PER.MAX}$ = + 93 ps, then $t_{RPRE.MIN(DERATED)} = t_{RPRE.MIN} + t_{JIT.PER.MIN}$ = 0.9 x $t_{CK.AVG}$ – 72 ps = + 2178 ps and $t_{RPRE.MAX(DERATED)} = t_{RPRE.MAX} + t_{JIT.PER.MAX}$ = 1.1 x $t_{CK.AVG}$ + 93 ps = + 2843 ps. (Caution on the MIN/MAX usage!).

34) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT.DUTY}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{JIT.DUTY.MIN}$ = – 72 ps and $t_{JIT.DUTY.MAX}$ = + 93 ps, then $t_{RPST.MIN(DERATED)} = t_{RPST.MIN} + t_{JIT.DUTY.MIN}$ = 0.4 x $t_{CK.AVG}$ – 72 ps = + 928 ps and $t_{RPST.MAX(DERATED)} = t_{RPST.MAX} + t_{JIT.DUTY.MAX}$ = 0.6 x $t_{CK.AVG}$ + 93 ps = + 1592 ps. (Caution on the MIN/MAX usage!).

35) For these parameters, the DDR2 SDRAM device is characterized and verified to support t_{nPARAM} = RU{t_{PARAM} / $t_{CK.AVG}$}, which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support t_{nRP} = RU{t_{RP} / $t_{CK.AVG}$}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR2–667 5–5–5, of which t_{RP} = 15 ns, the device will support t_{nRP} = RU{t_{RP} / $t_{CK.AVG}$} = 5, i.e. as long as the input clock jitter specifications are met, Precharge command at Tm and Active command at Tm + 5 is valid even if (Tm + 5 - Tm) is less than 15 ns due to input clock jitter.

36) t_{WTR} is at lease two clocks (2 x t_{CK}) independent of operation frequency.

FIGURE 2
Method for calculating transitions and endpoint

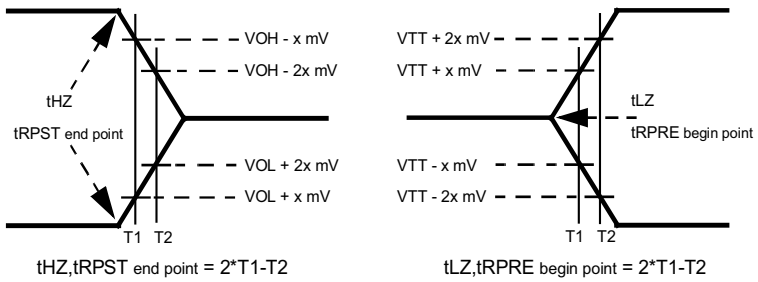


FIGURE 3
Differential input waveform timing t_{DS} and t_{DH}

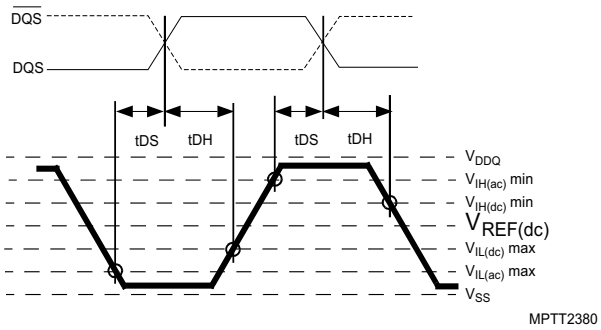


FIGURE 4
Differential input waveform timing t_{IS} and t_{IH}

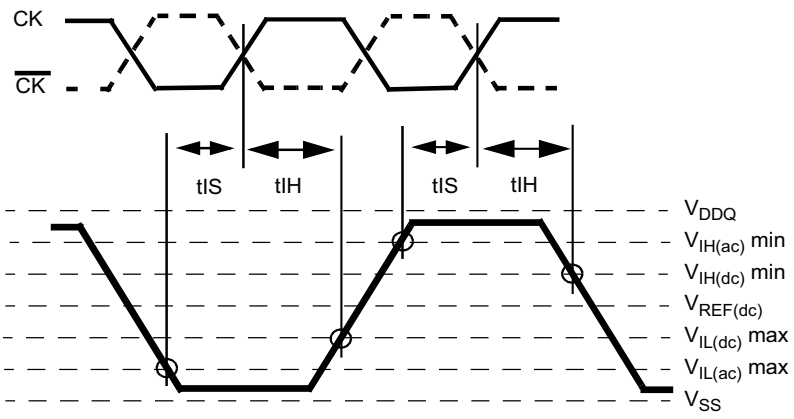


TABLE 15
DRAM Component Timing Parameter by Speed Grade - DDR2–533

Parameter	Symbol	DDR2–533		Unit	Notes[2)3)4)5)6)7)]
		Min.	Max.		
$\overline{CAS}$ A to $\overline{CAS}$ B command period	t_{CCD}	2	—	t_{CK}	
CK, $\overline{CK}$ high-level width	t_{CH}	0.45	0.55	t_{CK}	
CKE minimum high and low pulse width	t_{CKE}	3	—	t_{CK}	
CK, $\overline{CK}$ low-level width	t_{CL}	0.45	0.55	t_{CK}	
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	t_{CK}	8)
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	t_{IS} + t_{CK} + t_{IH}	—	ns	9)
DQ and DM input hold time (differential data strobe)	$t_{DH.BASE}$	225	—	ps	10)
DQ and DM input hold time (single ended data strobe)	$t_{DH1.BASE}$	–25	—	ps	11)
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	t_{CK}	
DQS input HIGH pulse width (write cycle)	t_{DQSH}	0.35	—	t_{CK}	
DQS input LOW pulse width (write cycle)	t_{DQSL}	0.35	—	t_{CK}	
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	300	ps	11)
Write command to 1st DQS latching transition	t_{DQSS}	– 0.25	+ 0.25	t_{CK}	
DQ and DM input setup time (differential data strobe)	$t_{DS.BASE}$	100	—	ps	11)
DQ and DM input setup time (single ended data strobe)	$t_{DS1.BASE}$	–25	—	ps	11)
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	t_{CK}	
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	t_{CK}	
Four Activate Window period	t_{FAW}	37.5	—	ns	
Four Activate Window period	t_{FAW}	50	—	ns	13)
Clock half period	t_{HP}	MIN. (t_{CL}, t_{CH})			12)
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	ps	13)
Address and control input hold time	$t_{IH.BASE}$	375	—	ps	11)
Address and control input pulse width (each input)	t_{IPW}	0.6	—	t_{CK}	
Address and control input setup time	$t_{IS.BASE}$	250	—	ps	11)
DQ low-impedance time from CK / $\overline{CK}$	$t_{LZ(DQ)}$	2 × $t_{AC.MIN}$	$t_{AC.MAX}$	ps	14)
DQS low-impedance from CK / $\overline{CK}$	$t_{LZ(DQS)}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	14)
MRS command to ODT update delay	t_{MOD}	0	12	ns	

Parameter	Symbol	DDR2–533		Unit	Notes[2)3)4)5)6)7)]
		Min.	Max.		
Mode register set command cycle time	t_{MRD}	2	—	t_{CK}	
OCD drive mode output delay	t_{OIT}	0	12	ns	
Data output hold time from DQS	t_{QH}	$t_{HP} - t_{QHS}$	—		
Data hold skew factor	t_{QHS}	—	400	ps	
Average periodic refresh Interval	t_{REFI}	—	7.8	µs	14)15)
Average periodic refresh Interval	t_{REFI}	—	3.9	µs	16)18)
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	127.5	—	ns	17)
Precharge-All (8 banks) command period	t_{RP}	$t_{RP} + 1 \times t_{CK}$	—	ns	
Read preamble	t_{RPRE}	0.9	1.1	t_{CK}	14)
Read postamble	t_{RPST}	0.40	0.60	t_{CK}	14)
Active bank A to Active bank B command period	t_{RRD}	7.5	—	ns	14)18)
Active bank A to Active bank B command period	t_{RRD}	10	—	ns	16)22)
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	
Write preamble	t_{WPRE}	0.25	—	t_{CK}	
Write postamble	t_{WPST}	0.40	0.60	t_{CK}	19)
Write recovery time for write without Auto-Precharge	t_{WR}	15	—	ns	
Internal Write to Read command delay	t_{WTR}	7.5	—	ns	20)
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	t_{CK}	21)
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	6 – AL	—	t_{CK}	21)
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	t_{CK}	
Exit Self-Refresh to non-Read command	t_{XSNR}	t_{RFC} +10	—	ns	
Exit Self-Refresh to Read command	t_{XSRD}	200	—	t_{CK}	
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}		t_{CK}	22)

1) For details and notes see the relevant Qimonda component data sheet
2) V_{DDQ} = 1.8 V ± 0.1V; V_{DD} = 1.8 V ± 0.1 V.
3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
4) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
5) The CK / $\overline{CK}$ input reference level (for timing reference to CK / $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode. component
6) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
7) The output timing reference voltage level is V_{TT}. component datasheet
8) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MR.

9) The clock frequency is allowed to change during self-refresh mode or precharge power-down mode.
10) For timing definition, refer to the Component data sheet.
11) Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output Slew Rate mis-match between DQS / $\overline{\text{DQS}}$ and associated DQ in any given cycle.
12) MIN (t_{CL}, t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}).
13) The t_{HZ}, t_{RPST} and t_{LZ}, t_{RPRE} parameters are referenced to a specific voltage level, which specify when the device output is no longer driving ($t_{HZ,}$ t_{RPST}), or begins driving ($t_{LZ,}$ t_{RPRE}). t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions.These parameters are verified by design and characterization, but not subject to production test.
14) The Auto-Refresh command interval has be reduced to 3.9 µs when operating the DDR2 DRAM in a temperature range between 85 °C and 95 °C.
15) 0 °C≤ T_{CASE} ≤ 85 °C.
16) 85 °C < T_{CASE} ≤ 95 °C.
17) A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device
18) The t_{RRD} timing parameter depends on the page size of the DRAM organization.
19) The maximum limit for the t_{WPST} parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
20) Minimum t_{WTR} is two clocks when operating the DDR2-SDRAM at frequencies ≤ 200 MHz.
21) User can choose two different active power-down modes for additional power saving via MRS address bit A12. In “standard active power-down mode” (MR, A12 = “0”) a fast power-down exit timing t_{XARD} can be used. In “low active power-down mode” (MR, A12 =”1”) a slow power-down exit timing t_{XARDS} has to be satisfied.
22) WR must be programmed to fulfill the minimum requirement for the t_{WR} timing parameter, where WR_{MIN}[cycles] = t_{WR}(ns)/t_{CK}(ns) rounded up to the next integer value. t_{DAL} = WR + (t_{RP}/t_{CK}). For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MRS.

3.3.3 ODT AC Electrical Characteristics

This chapter describes the ODT AC electrical characteristics.

TABLE 16
ODT AC Characteristics and Operating Conditions for DDR2-667 & DDR2-800

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
t_{AOND}	ODT turn-on delay	2	2	n_{CK}	1)
t_{AON}	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.7 ns	ns	1)2)
t_{AONPD}	ODT turn-on (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	1)
t_{AOFD}	ODT turn-off delay	2.5	2.5	n_{CK}	1)
t_{AOF}	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.6 ns	ns	1)3)
t_{AOFPD}	ODT turn-off (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2.5 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	1)
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	—	n_{CK}	1)
t_{AXPD}	ODT Power Down Exit Latency	8	—	n_{CK}	1)

1) New units, “$t_{CK.AVG}$” and “n_{CK}”, are introduced in DDR2-667 and DDR2-800. Unit “$t_{CK.AVG}$” represents the actual $t_{CK.AVG}$ of the input clock under operation. Unit “n_{CK}” represents one clock cycle of the input clock, counting the actual clock edges. Note that in DDR2-400 and DDR2-533, “t_{CK}” is used for both concepts. Example: t_{XP} = 2 [n_{CK}] means; if Power Down exit is registered at T_m, an Active command may be registered at T_m + 2, even if (T_m + 2 - T_m) is 2 x $t_{CK.AVG}$ + $t_{ERR.2PER(Min)}$.
2) ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from t_{AOND}, which is interpreted differently per speed bin. For DDR2-667/800, t_{AOND} is 2 clock cycles after the clock edge that registered a first ODT HIGH counting the actual input clock edges.

3) ODT turn off time min is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD}, which is interpreted differently per speed bin. For DDR2-667/800, if $t_{CK(avg)}$ = 3 ns is assumed, t_{AOFD} is 1.5 ns (= 0.5 x 3 ns) after the second trailing clock edge counting from the clock edge that registered a first ODT LOW and by counting the actual input clock edges.

TABLE 17
ODT AC Characteristics and Operating Conditions for DDR2-533

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
t_{AOND}	ODT turn-on delay	2	2	t_{CK}	
t_{AON}	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX}$ + 1 ns	ns	1)
t_{AONPD}	ODT turn-on (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	
t_{AOFD}	ODT turn-off delay	2.5	2.5	t_{CK}	
t_{AOF}	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.6 ns	ns	2)
t_{AOFPD}	ODT turn-off (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2.5 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	—	t_{CK}	
t_{AXPD}	ODT Power Down Exit Latency	8	—	t_{CK}	

1) ODT turn on time min. is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from t_{AOND}, which is interpreted differently per speed bin. For DDR2-400/533, t_{AOND} is 10 ns (= 2 x 5 ns) after the clock edge that registered a first ODT HIGH if t_{CK} = 5 ns.

2) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD}. Both are measured from t_{AOFD}, which is interpreted differently per speed bin. For DDR2-400/533, t_{AOFD} is 12.5 ns (= 2.5 x 5 ns) after the clock edge that registered a first ODT HIGH if t_{CK} = 5 ns.

3.4 I_{DD} Specifications and Conditions

List of tables defining I_{DD} Specifications and Conditions.

TABLE 18
I_{DD} Measurement Conditions

Parameter	Symbol	Note[1)2) 3)4)5)]
Operating Current 0 One bank Active - Precharge; $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD0}	
Operating Current 1 One bank Active - Read - Precharge; I_{OUT} = 0 mA, BL = 4, $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, $t_{RCD} = t_{RCD.MIN}$, AL = 0, CL = CL_{MIN}; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD1}	6)
Precharge Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD2N}	
Precharge Power-Down Current Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2P}	
Precharge Quiet Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2Q}	
Active Standby Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX}$, $t_{RP} = t_{RP.MIN}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; I_{OUT} = 0 mA.	I_{DD3N}	
Active Power-Down Current All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to LOW (Fast Power-down Exit);	$I_{DD3P(0)}$	
Active Power-Down Current All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to HIGH (Slow Power-down Exit);	$I_{DD3P(1)}$	
Operating Current - Burst Read All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CKMIN}$; $t_{RAS} = t_{RASMAX}$; $t_{RP} = t_{RPMIN}$; CKE is HIGH, CS is HIGH between valid commands; Address inputs are SWITCHING; Data bus inputs are SWITCHING; I_{OUT} = 0mA.	I_{DD4R}	6)
Operating Current - Burst Write All banks open; Continuous burst writes; BL = 4; AL = 0, CL = CL_{MIN}; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX.}$, $t_{RP} = t_{RP.MAX}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING;	I_{DD4W}	
Burst Refresh Current $t_{CK} = t_{CK.MIN.}$, Refresh command every $t_{RFC} = t_{RFC.MIN}$ interval, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5B}	
Distributed Refresh Current $t_{CK} = t_{CK.MIN.}$, Refresh command every $t_{RFC} = t_{REFI}$ interval, CKE is LOW and $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5D}	

Parameter	Symbol	Note[1)2) 3)4)5)]
Self-Refresh Current CKE ≤ 0.2 V; external clock off, CK and $\overline{CK}$ at 0 V; Other control and address inputs are FLOATING, Data bus inputs are FLOATING. I_{DD6} current values are guaranteed up to T_{CASE} of 85 °C max.	I_{DD6}	
All Bank Interleave Read Current All banks are being interleaved at minimum t_{RC} without violating t_{RRD} using a burst length of 4. Control and address bus inputs are STABLE during DESELECTS. I_{out} = 0 mA.	I_{DD7}	6)

1) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ± 0.1 V
2) I_{DD} specifications are tested after the device is properly initialized and I_{DD} parameter are specified with ODT disabled.
3) Definitions for I_{DD} see **Table 19**
4) For two rank modules: All active current measurements in the same I_{DD} current mode. The other rank is in I_{DD2P} Precharge Power-Down Mode.
5) For details and notes see the relevant Qimonda component data sheet.
6) I_{DD1}, I_{DD4R} and I_{DD7} current measurements are defined with the outputs disabled (I_{OUT} = 0 mA). To achieve this on module level the output buffers can be disabled using an EMRS(1) (Extended Mode Register Command) by setting A12 bit to HIGH.

TABLE 19
Definitions for I_{DD}

Parameter	Description
LOW	$V_{IN} \leq V_{IL(ac).MAX}$, HIGH is defined as $V_{IN} \geq V_{IH(ac).MIN}$
STABLE	Inputs are stable at a HIGH or LOW level
FLOATING	Inputs are V_{REF} = V_{DDQ} /2
SWITCHING	Inputs are changing between HIGH and LOW every other clock (once per 2 cycles) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per cycle) for DQ signals not including mask or strobes.

TABLE 20

I_{DD} Specification for HYS64T[128/256]020EDL-[25F/2.5/3]-C

Product Type	HYS64T128020EDL-25F-C	HYS64T256020EDL-25F-C	HYS64T128020EDL-2.5-C	HYS64T256020EDL-2.5-C	HYS64T128020EDL-3-C	HYS64T256020EDL-3-C	Unit	Note[1)]
Organization	1GB	2GB	1GB	2GB	1GB	2GB		
	2 Rank	2 Rank	2 Rank	2 Rank	2 Rank	2 Rank		
	×64	×64	×64	×64	×64	×64		
	-25F	-25F	-2.5	-2.5	-3	-3		
Symbol	Max.	Max.	Max.	Max.	Max.	Max.		
I_{DD0}	476	824	472	820	450	768	mA	2)
I_{DD1}	500	856	496	850	480	800	mA	2)
I_{DD2N}	536	1072	536	1070	500	992	mA	3)
I_{DD2P}	80	160	80	160	80	160	mA	3)
I_{DD2Q}	496	992	496	990	460	912	mA	3)
I_{DD3N}	576	1152	576	1150	520	1040	mA	3)4)
$I_{DD3P(MRS=0)}$	280	560	280	560	260	528	mA	3)
$I_{DD3P(MRS=1)}$	120	240	120	240	120	240	mA	3)5)
I_{DD4R}	760	1276	760	1300	680	1168	mA	2)
I_{DD4W}	820	1336	820	1340	740	1208	mA	2)
I_{DD5B}	824	1648	824	1650	790	1584	mA	2)
I_{DD5D}	96	192	96	190	100	192	mA	3)6)
I_{DD6}	48	96	48	96	48	96	mA	3)6)
I_{DD7}	1112	1776	1112	1780	1012	1640	mA	2)

1) Calculated values from component data. ODT disabled. I_{DD1}, I_{DD4R} and I_{DD7} are defined with the outputs disabled.
2) The other rank is in I_{DD2P} Precharge Power-Down Current mode
3) Both ranks are in the same I_{DD}current mode
4) Slow: MRS(12)=1
5) Fast: MRS(12)=0
6) I_{DD5D} and I_{DD6} values are for $0°C \leq T_{Case} \leq 85°C$

TABLE 21

I_{DD} Specification for HYS64T[128/256]020EDL-[3S/3.7]-C

Product Type	HYS64T128020EDL-3S-C	HYS64T256020EDL-3S-C	HYS64T128020EDL-3.7-C	HYS64T256020EDL-3.7-C	Unit	Note[1)]
Organization	1GB	2GB	1GB	2GB		
	2 Rank	2 Rank	2 Rank	2 Rank		
	×64	×64	×64	×64		
	-3S	-3S	-3.7	-3.7		
Symbol	Max.	Max.	Max.	Max.		
I_{DD0}	448	768	424	720	mA	2)
I_{DD1}	476	800	448	740	mA	2)
I_{DD2N}	496	992	440	880	mA	3)
I_{DD2P}	80	160	80	160	mA	3)
I_{DD2Q}	456	912	432	860	mA	3)
I_{DD3N}	520	1040	464	930	mA	3)4)
$I_{DD3P(\ MRS\ =\ 0)}$	264	528	240	480	mA	3)
$I_{DD3P(\ MRS\ =\ 1)}$	120	240	120	240	mA	3)5)
I_{DD4R}	684	1168	608	1040	mA	2)
I_{DD4W}	740	1208	660	1080	mA	2)
I_{DD5B}	792	1584	780	1560	mA	2)
I_{DD5D}	96	192	96	190	mA	3)6)
I_{DD6}	48	96	48	96	mA	3)6)
I_{DD7}	1012	1624	980	1640	mA	2)

1) Calculated values from component data. ODT disabled. $I_{DD1,}$ I_{DD4R} and I_{DD7} are defined with the outputs disabled.
2) The other rank is in I_{DD2P} Precharge Power-Down Current mode
3) Both ranks are in the same I_{DD}current mode
4) Slow: MRS(12)=1
5) Fast: MRS(12)=0
6) I_{DD5D} and I_{DD6} values are for $0°C \leq T_{Case} \leq 85°C$

4 SPD Codes

This chapter lists all hexadecimal byte values stored in the EEPROM of the products described in this data sheet. SPD stands for serial presence detect. All values with XX in the table are module specific bytes which are defined during production.

List of SPD Code Tables

TABLE 22
HYS64T[128/256]020EDL-[25F/2.5]-C

Product Type		**HYS64T128020EDL–25F–C**	**HYS64T256020EDL–25F–C**	**HYS64T128020EDL–2.5–C**	**HYS64T256020EDL–2.5–C**
Organization		**1 GByte**	**2 GByte**	**1 GByte**	**2 GByte**
		×64	**×64**	**×64**	**×64**
		2 Ranks (×16)	**2 Ranks (×8)**	**2 Ranks (×16)**	**2 Ranks (×8)**
Label Code		**PC2–6400S–555**	**PC2–6400S–555**	**PC2–6400S–666**	**PC2–6400S–666**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80	80
1	Total number of Bytes in EEPROM	08	08	08	08
2	Memory Type (DDR2)	08	08	08	08
3	Number of Row Addresses	0D	0E	0D	0E
4	Number of Column Addresses	0A	0A	0A	0A
5	DIMM Rank and Stacking Information	61	61	61	61
6	Data Width	40	40	40	40
7	Not used	00	00	00	00
8	Interface Voltage Level	05	05	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	25	25	25	25
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	40	40	40	40

Product Type		HYS64T128020EDL–25F–C	HYS64T256020EDL–25F–C	HYS64T128020EDL–2.5–C	HYS64T256020EDL–2.5–C
Organization		1 GByte	2 GByte	1 GByte	2 GByte
		×64	×64	×64	×64
		2 Ranks (×16)	2 Ranks (×8)	2 Ranks (×16)	2 Ranks (×8)
Label Code		PC2–6400S–555	PC2–6400S–555	PC2–6400S–666	PC2–6400S–666
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX	HEX
11	Error Correction Support (non-ECC, ECC)	00	00	00	00
12	Refresh Rate and Type	82	82	82	82
13	Primary SDRAM Width	10	08	10	08
14	Error Checking SDRAM Width	00	00	00	00
15	Not used	00	00	00	00
16	Burst Length Supported	0C	0C	0C	0C
17	Number of Banks on SDRAM Device	08	08	08	08
18	Supported CAS Latencies	70	70	70	70
19	DIMM Mechanical Characteristics	01	01	01	01
20	DIMM Type Information	04	04	04	04
21	DIMM Attributes	00	00	00	00
22	Component Attributes	07	07	07	07
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	25	25	30	30
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	40	40	45	45
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	3D	3D	3D	3D
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	50	50	50	50
27	$t_{RP.MIN}$ [ns]	32	32	3C	3C
28	$t_{RRD.MIN}$ [ns]	28	1E	28	1E
29	$t_{RCD.MIN}$ [ns]	32	32	3C	3C
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D	2D
31	Module Density per Rank	80	01	80	01
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	17	17	17	17
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	25	25	25	25
34	$t_{DS.MIN}$ [ns]	05	05	05	05

Product Type		HYS64T128020EDL–25F–C	HYS64T256020EDL–25F–C	HYS64T128020EDL–2.5–C	HYS64T256020EDL–2.5–C
Organization		1 GByte	2 GByte	1 GByte	2 GByte
		×64	×64	×64	×64
		2 Ranks (×16)	2 Ranks (×8)	2 Ranks (×16)	2 Ranks (×8)
Label Code		PC2–6400S–555	PC2–6400S–555	PC2–6400S–666	PC2–6400S–666
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX	HEX
35	$t_{DH.MIN}$ [ns]	12	12	12	12
36	$t_{WR.MIN}$ [ns]	3C	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E	1E
39	Analysis Characteristics	00	00	00	00
40	t_{RC} and t_{RFC} Extension	06	06	06	06
41	$t_{RC.MIN}$ [ns]	39	39	3C	3C
42	$t_{RFC.MIN}$ [ns]	7F	7F	7F	7F
43	$t_{CK.MAX}$ [ns]	80	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	14	14	14	14
45	$t_{QHS.MAX}$ [ns]	1E	1E	1E	1E
46	PLL Relock Time	00	00	00	00
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	53	51	53	51
48	Psi(T-A) DRAM	58	60	58	60
49	ΔT_0 (DT0)	57	4F	57	4F
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	38	3D	38	3D
51	ΔT_{2P} (DT2P)	38	3D	38	3D
52	ΔT_{3N} (DT3N)	28	2C	28	2C
53	$\Delta T_{3P.fast}$ (DT3P fast)	3B	35	3B	35
54	$\Delta T_{3P.slow}$ (DT3P slow)	32	24	32	24
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	4C	46	4C	46
56	ΔT_{5B} (DT5B)	21	24	21	24
57	ΔT_7 (DT7)	2D	27	2D	27
58	Psi(ca) PLL	00	00	00	00

Product Type		HYS64T128020EDL–25F–C	HYS64T256020EDL–25F–C	HYS64T128020EDL–2.5–C	HYS64T256020EDL–2.5–C
Organization		**1 GByte**	**2 GByte**	**1 GByte**	**2 GByte**
		×64	**×64**	**×64**	**×64**
		2 Ranks (×16)	**2 Ranks (×8)**	**2 Ranks (×16)**	**2 Ranks (×8)**
Label Code		**PC2–6400S–555**	**PC2–6400S–555**	**PC2–6400S–666**	**PC2–6400S–666**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
59	Psi(ca) REG	00	00	00	00
60	ΔT_{PLL} (DTPLL)	00	00	00	00
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00	00	00
62	SPD Revision	12	12	12	12
63	Checksum of Bytes 0-62	ED	4C	14	73
64	Manufacturer's JEDEC ID Code (1)	7F	7F	7F	7F
65	Manufacturer's JEDEC ID Code (2)	7F	7F	7F	7F
66	Manufacturer's JEDEC ID Code (3)	7F	7F	7F	7F
67	Manufacturer's JEDEC ID Code (4)	7F	7F	7F	7F
68	Manufacturer's JEDEC ID Code (5)	7F	7F	7F	7F
69	Manufacturer's JEDEC ID Code (6)	51	51	51	51
70	Manufacturer's JEDEC ID Code (7)	00	00	00	00
71	Manufacturer's JEDEC ID Code (8)	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx
73	Product Type, Char 1	36	36	36	36
74	Product Type, Char 2	34	34	34	34
75	Product Type, Char 3	54	54	54	54
76	Product Type, Char 4	31	32	31	32
77	Product Type, Char 5	32	35	32	35
78	Product Type, Char 6	38	36	38	36
79	Product Type, Char 7	30	30	30	30
80	Product Type, Char 8	32	32	32	32
81	Product Type, Char 9	30	30	30	30
82	Product Type, Char 10	45	45	45	45

Product Type		HYS64T128020EDL–25F–C	HYS64T256020EDL–25F–C	HYS64T128020EDL–2.5–C	HYS64T256020EDL–2.5–C
Organization		**1 GByte**	**2 GByte**	**1 GByte**	**2 GByte**
		×64	**×64**	**×64**	**×64**
		2 Ranks (×16)	**2 Ranks (×8)**	**2 Ranks (×16)**	**2 Ranks (×8)**
Label Code		**PC2–6400S–555**	**PC2–6400S–555**	**PC2–6400S–666**	**PC2–6400S–666**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
83	Product Type, Char 11	44	44	44	44
84	Product Type, Char 12	4C	4C	4C	4C
85	Product Type, Char 13	32	32	32	32
86	Product Type, Char 14	35	35	2E	2E
87	Product Type, Char 15	46	46	35	35
88	Product Type, Char 16	43	43	43	43
89	Product Type, Char 17	20	20	20	20
90	Product Type, Char 18	20	20	20	20
91	Module Revision Code	1x	1x	1x	1x
92	Test Program Revision Code	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00
128 - 255	Blank for customer use	FF	FF	FF	FF

TABLE 23
HYS64T[128/256]020EDL-[3/3S]-C

Product Type		**HYS64T128020EDL–3–C**	**HYS64T256020EDL–3–C**	**HYS64T128020EDL–3S–C**	**HYS64T256020EDL–3S–C**
Organization		**1 GByte**	**2 GByte**	**1 GByte**	**2 GByte**
		×64	**×64**	**×64**	**×64**
		2 Ranks (×16)	**2 Ranks (×8)**	**2 Ranks (×16)**	**2 Ranks (×8)**
Label Code		**PC2–5300S–444**	**PC2–5300S–444**	**PC2–5300S–555**	**PC2–5300S–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80	80
1	Total number of Bytes in EEPROM	08	08	08	08
2	Memory Type (DDR2)	08	08	08	08
3	Number of Row Addresses	0D	0E	0D	0E
4	Number of Column Addresses	0A	0A	0A	0A
5	DIMM Rank and Stacking Information	61	61	61	61
6	Data Width	40	40	40	40
7	Not used	00	00	00	00
8	Interface Voltage Level	05	05	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	30	30	30	30
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	45	45	45	45
11	Error Correction Support (non-ECC, ECC)	00	00	00	00
12	Refresh Rate and Type	82	82	82	82
13	Primary SDRAM Width	10	08	10	08
14	Error Checking SDRAM Width	00	00	00	00
15	Not used	00	00	00	00
16	Burst Length Supported	0C	0C	0C	0C
17	Number of Banks on SDRAM Device	08	08	08	08
18	Supported CAS Latencies	38	38	38	38
19	DIMM Mechanical Characteristics	01	01	01	01
20	DIMM Type Information	04	04	04	04
21	DIMM Attributes	00	00	00	00

Product Type		HYS64T128020EDL–3–C	HYS64T256020EDL–3–C	HYS64T128020EDL–3S–C	HYS64T256020EDL–3S–C
Organization		1 GByte	2 GByte	1 GByte	2 GByte
		×64	×64	×64	×64
		2 Ranks (×16)	2 Ranks (×8)	2 Ranks (×16)	2 Ranks (×8)
Label Code		PC2–5300S–444	PC2–5300S–444	PC2–5300S–555	PC2–5300S–555
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX	HEX
22	Component Attributes	07	07	07	07
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	30	30	3D	3D
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	45	45	50	50
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	50	50	50	50
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	60	60	60	60
27	$t_{RP.MIN}$ [ns]	30	30	3C	3C
28	$t_{RRD.MIN}$ [ns]	28	1E	28	1E
29	$t_{RCD.MIN}$ [ns]	30	30	3C	3C
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D	2D
31	Module Density per Rank	80	01	80	01
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	20	20	20	20
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	27	27	27	27
34	$t_{DS.MIN}$ [ns]	10	10	10	10
35	$t_{DH.MIN}$ [ns]	17	17	17	17
36	$t_{WR.MIN}$ [ns]	3C	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E	1E
39	Analysis Characteristics	00	00	00	00
40	t_{RC} and t_{RFC} Extension	06	06	06	06
41	$t_{RC.MIN}$ [ns]	39	39	3C	3C
42	$t_{RFC.MIN}$ [ns]	7F	7F	7F	7F
43	$t_{CK.MAX}$ [ns]	80	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	18	18	18	18
45	$t_{QHS.MAX}$ [ns]	22	22	22	22

Product Type		**HYS64T128020EDL–3–C**	**HYS64T256020EDL–3–C**	**HYS64T128020EDL–3S–C**	**HYS64T256020EDL–3S–C**
Organization		**1 GByte**	**2 GByte**	**1 GByte**	**2 GByte**
		×64	**×64**	**×64**	**×64**
		2 Ranks (×16)	**2 Ranks (×8)**	**2 Ranks (×16)**	**2 Ranks (×8)**
Label Code		**PC2–5300S–444**	**PC2–5300S–444**	**PC2–5300S–555**	**PC2–5300S–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
46	PLL Relock Time	00	00	00	00
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	53	51	53	51
48	Psi(T-A) DRAM	58	60	58	60
49	ΔT_0 (DT0)	4F	47	4F	47
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	34	39	34	39
51	ΔT_{2P} (DT2P)	38	3D	38	3D
52	ΔT_{3N} (DT3N)	24	28	24	28
53	$\Delta T_{3P.fast}$ (DT3P fast)	37	31	37	31
54	$\Delta T_{3P.slow}$ (DT3P slow)	32	24	32	24
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	44	3E	44	3E
56	ΔT_{5B} (DT5B)	1F	22	1F	22
57	ΔT_7 (DT7)	29	24	29	23
58	Psi(ca) PLL	00	00	00	00
59	Psi(ca) REG	00	00	00	00
60	ΔT_{PLL} (DTPLL)	00	00	00	00
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00	00	00
62	SPD Revision	12	12	12	12
63	Checksum of Bytes 0-62	F5	55	28	87
64	Manufacturer’s JEDEC ID Code (1)	7F	7F	7F	7F
65	Manufacturer’s JEDEC ID Code (2)	7F	7F	7F	7F
66	Manufacturer’s JEDEC ID Code (3)	7F	7F	7F	7F
67	Manufacturer’s JEDEC ID Code (4)	7F	7F	7F	7F
68	Manufacturer’s JEDEC ID Code (5)	7F	7F	7F	7F
69	Manufacturer’s JEDEC ID Code (6)	51	51	51	51

Product Type		HYS64T128020EDL–3–C	HYS64T256020EDL–3–C	HYS64T128020EDL–3S–C	HYS64T256020EDL–3S–C
Organization		1 GByte	2 GByte	1 GByte	2 GByte
		×64	×64	×64	×64
		2 Ranks (×16)	2 Ranks (×8)	2 Ranks (×16)	2 Ranks (×8)
Label Code		PC2–5300S–444	PC2–5300S–444	PC2–5300S–555	PC2–5300S–555
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX	HEX
70	Manufacturer's JEDEC ID Code (7)	00	00	00	00
71	Manufacturer's JEDEC ID Code (8)	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx
73	Product Type, Char 1	36	36	36	36
74	Product Type, Char 2	34	34	34	34
75	Product Type, Char 3	54	54	54	54
76	Product Type, Char 4	31	32	31	32
77	Product Type, Char 5	32	35	32	35
78	Product Type, Char 6	38	36	38	36
79	Product Type, Char 7	30	30	30	30
80	Product Type, Char 8	32	32	32	32
81	Product Type, Char 9	30	30	30	30
82	Product Type, Char 10	45	45	45	45
83	Product Type, Char 11	44	44	44	44
84	Product Type, Char 12	4C	4C	4C	4C
85	Product Type, Char 13	33	33	33	33
86	Product Type, Char 14	43	43	53	53
87	Product Type, Char 15	20	20	43	43
88	Product Type, Char 16	20	20	20	20
89	Product Type, Char 17	20	20	20	20
90	Product Type, Char 18	20	20	20	20
91	Module Revision Code	1x	1x	1x	1x
92	Test Program Revision Code	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx

Product Type		**HYS64T128020EDL–3–C**	**HYS64T256020EDL–3–C**	**HYS64T128020EDL–3S–C**	**HYS64T256020EDL–3S–C**
Organization		**1 GByte**	**2 GByte**	**1 GByte**	**2 GByte**
		×64	**×64**	**×64**	**×64**
		2 Ranks (×16)	**2 Ranks (×8)**	**2 Ranks (×16)**	**2 Ranks (×8)**
Label Code		**PC2–5300S–444**	**PC2–5300S–444**	**PC2–5300S–555**	**PC2–5300S–555**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
94	Module Manufacturing Date Week	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00
128 - 255	Blank for customer use	FF	FF	FF	FF

TABLE 24
HYS64T[128/256]020EDL-3.7-C

Product Type		HYS64T128020EDL–3.7–C	HYS64T256020EDL–3.7–C
Organization		1 GByte	2 GByte
		×64	×64
		2 Ranks (×16)	2 Ranks (×8)
Label Code		PC2–4200S–444	PC2–4200S–444
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2
Byte#	**Description**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80
1	Total number of Bytes in EEPROM	08	08
2	Memory Type (DDR2)	08	08
3	Number of Row Addresses	0D	0E
4	Number of Column Addresses	0A	0A
5	DIMM Rank and Stacking Information	61	61
6	Data Width	40	40
7	Not used	00	00
8	Interface Voltage Level	05	05
9	t_{CK} @ CL_{MAX} (Byte 18) [ns]	3D	3D
10	t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns]	50	50
11	Error Correction Support (non-ECC, ECC)	00	00
12	Refresh Rate and Type	82	82
13	Primary SDRAM Width	10	08
14	Error Checking SDRAM Width	00	00
15	Not used	00	00
16	Burst Length Supported	0C	0C
17	Number of Banks on SDRAM Device	08	08
18	Supported CAS Latencies	38	38
19	DIMM Mechanical Characteristics	01	01
20	DIMM Type Information	04	04
21	DIMM Attributes	00	00
22	Component Attributes	07	07
23	t_{CK} @ CL_{MAX} -1 (Byte 18) [ns]	3D	3D
24	t_{AC} SDRAM @ CL_{MAX} -1 [ns]	50	50
25	t_{CK} @ CL_{MAX} -2 (Byte 18) [ns]	50	50
26	t_{AC} SDRAM @ CL_{MAX} -2 [ns]	60	60
27	$t_{RP.MIN}$ [ns]	3C	3C
28	$t_{RRD.MIN}$ [ns]	28	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C

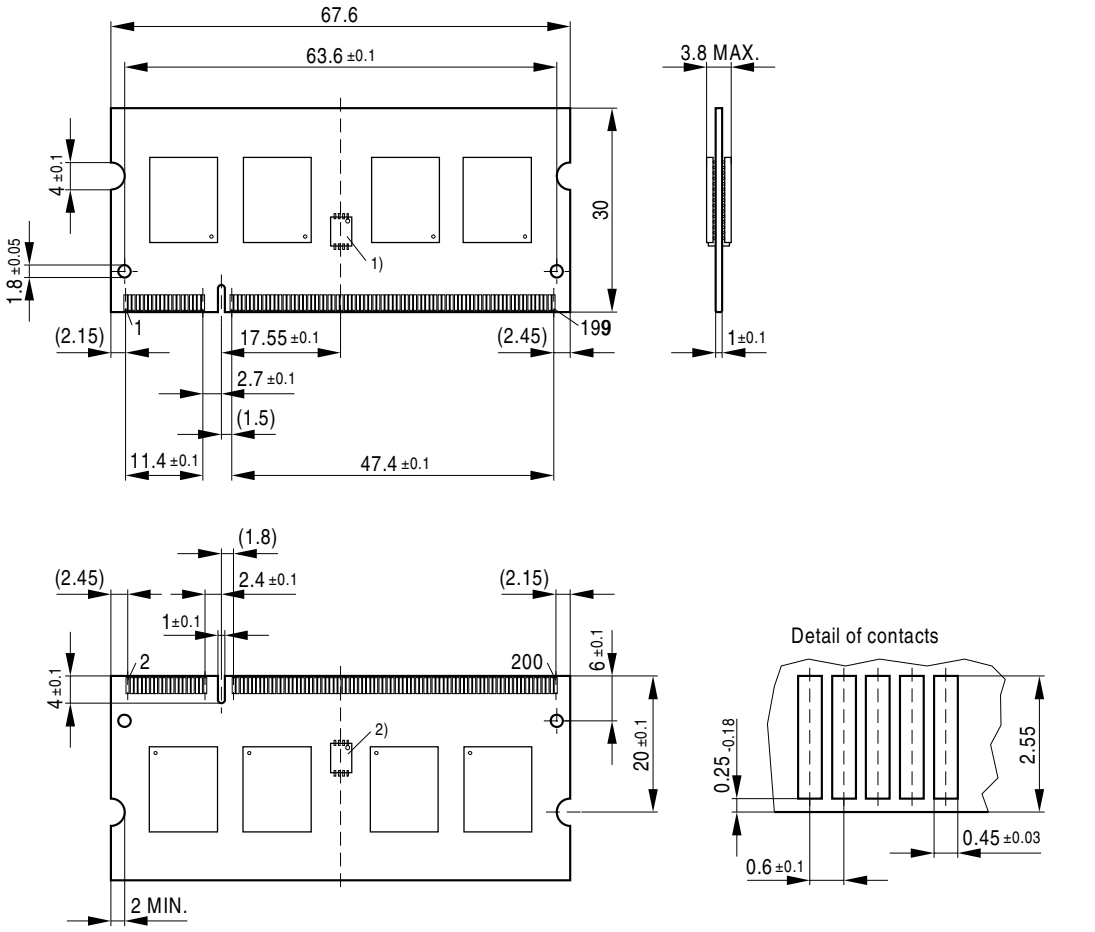
Product Type		**HYS64T128020EDL–3.7–C**	**HYS64T256020EDL–3.7–C**
Organization		**1 GByte**	**2 GByte**
		×64	**×64**
		2 Ranks (×16)	**2 Ranks (×8)**
Label Code		**PC2–4200S–444**	**PC2–4200S–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**
30	$t_{RAS.MIN}$ [ns]	2D	2D
31	Module Density per Rank	80	01
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	25	25
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	37	37
34	$t_{DS.MIN}$ [ns]	10	10
35	$t_{DH.MIN}$ [ns]	22	22
36	$t_{WR.MIN}$ [ns]	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E
39	Analysis Characteristics	00	00
40	t_{RC} and t_{RFC} Extension	06	06
41	$t_{RC.MIN}$ [ns]	3C	3C
42	$t_{RFC.MIN}$ [ns]	7F	7F
43	$t_{CK.MAX}$ [ns]	80	80
44	$t_{DQSQ.MAX}$ [ns]	1E	1E
45	$t_{QHS.MAX}$ [ns]	28	28
46	PLL Relock Time	00	00
47	$T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta	53	51
48	Psi(T-A) DRAM	58	60
49	ΔT_0 (DT0)	47	3F
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM)	2E	32
51	ΔT_{2P} (DT2P)	38	3D
52	ΔT_{3N} (DT3N)	20	23
53	$\Delta T_{3P.fast}$ (DT3P fast)	32	2C
54	$\Delta T_{3P.slow}$ (DT3P slow)	32	24
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W)	3C	36
56	ΔT_{5B} (DT5B)	1F	22
57	ΔT_7 (DT7)	27	24
58	Psi(ca) PLL	00	00
59	Psi(ca) REG	00	00
60	ΔT_{PLL} (DTPLL)	00	00
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00
62	SPD Revision	12	12

Product Type		HYS64T128020EDL–3.7–C	HYS64T256020EDL–3.7–C
Organization		1 GByte	2 GByte
		×64	×64
		2 Ranks (×16)	2 Ranks (×8)
Label Code		PC2–4200S–444	PC2–4200S–444
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2
Byte#	**Description**	**HEX**	**HEX**
63	Checksum of Bytes 0-62	4B	AB
64	Manufacturer's JEDEC ID Code (1)	7F	7F
65	Manufacturer's JEDEC ID Code (2)	7F	7F
66	Manufacturer's JEDEC ID Code (3)	7F	7F
67	Manufacturer's JEDEC ID Code (4)	7F	7F
68	Manufacturer's JEDEC ID Code (5)	7F	7F
69	Manufacturer's JEDEC ID Code (6)	51	51
70	Manufacturer's JEDEC ID Code (7)	00	00
71	Manufacturer's JEDEC ID Code (8)	00	00
72	Module Manufacturer Location	xx	xx
73	Product Type, Char 1	36	36
74	Product Type, Char 2	34	34
75	Product Type, Char 3	54	54
76	Product Type, Char 4	31	32
77	Product Type, Char 5	32	35
78	Product Type, Char 6	38	36
79	Product Type, Char 7	30	30
80	Product Type, Char 8	32	32
81	Product Type, Char 9	30	30
82	Product Type, Char 10	45	45
83	Product Type, Char 11	44	44
84	Product Type, Char 12	4C	4C
85	Product Type, Char 13	33	33
86	Product Type, Char 14	2E	2E
87	Product Type, Char 15	37	37
88	Product Type, Char 16	43	43
89	Product Type, Char 17	20	20
90	Product Type, Char 18	20	20
91	Module Revision Code	1x	1x
92	Test Program Revision Code	xx	xx
93	Module Manufacturing Date Year	xx	xx
94	Module Manufacturing Date Week	xx	xx
95 - 98	Module Serial Number	xx	xx

Product Type		**HYS64T128020EDL–3.7–C**	**HYS64T256020EDL–3.7–C**
Organization		**1 GByte**	**2 GByte**
		×64	**×64**
		2 Ranks (×16)	**2 Ranks (×8)**
Label Code		**PC2–4200S–444**	**PC2–4200S–444**
JEDEC SPD Revision		**Rev. 1.2**	**Rev. 1.2**
Byte#	**Description**	**HEX**	**HEX**
99 - 127	Not used	00	00
128 - 255	Blank for customer use	FF	FF

5 Package Outlines

FIGURE 5
Package Outline Raw Card A L-DIM-200-31



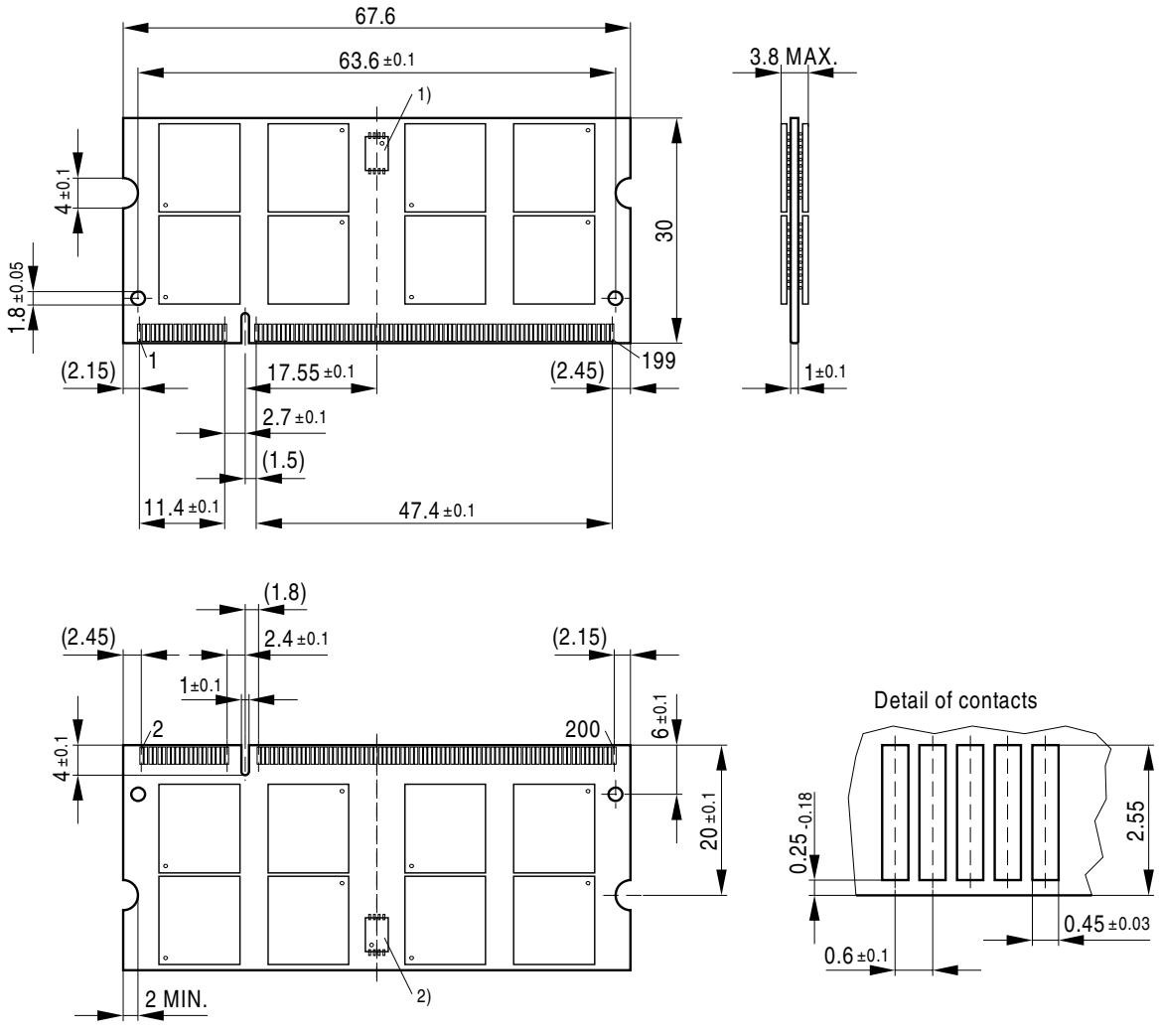
- Drawing according to ISO 8015
- General tolerances ±0.15
- Dimensions in mm

FPO_L_-DIM____-200-031

Notes

1. *Thermal Sensor (Optional)*
2. *SPD or Combidevice (if used then no Thermal Sensor needed)*

FIGURE 6
Package Outline Raw Card F - L-DIM-200-34



FPO_L_-DIM____-200-034

- Drawing according to ISO 8015
- General tolerances ±0.13
- Dimensions in mm

Notes

1. *SPD or Combidevice(if used then no Thermal Sensor needed).*
2. *Thermal Sensor (Optional)*

6 Product Type Nomenclature

Qimonda's nomenclature uses simple coding combined with some proprietary coding. **Table 25** provides examples for module and component product type number as well as the field number. The detailed field description together with possible values and coding explanation is listed for modules in **Table 26** and for components in **Table 27**.

TABLE 25
Nomenclature Fields and Examples

Example for	Field Number										
	1	2	3	4	5	6	7	8	9	10	11
Micro-DIMM	HYS	64	T	64/128	0	2	0	K	M	–5	–A
DDR2 DRAM	HYB	18	T	512/1G	16		0	A	C	–5	

TABLE 26
DDR2 DIMM Nomenclature

Field	Description	Values	Coding
1	Qimonda Module Prefix	HYS	Constant
2	Module Data Width [bit]	64	Non-ECC
		72	ECC
3	DRAM Technology	T	DDR2
4	Memory Density per I/O [Mbit]; Module Density[1)]	32	256 MByte
		64	512 MByte
		128	1 GByte
		256	2 GByte
		512	4 GByte
5	Raw Card Generation	0 .. 9	Look up table
6	Number of Module Ranks	0, 2, 4	1, 2, 4
7	Product Variations	0 .. 9	Look up table
8	Package, Lead-Free Status	A .. Z	Look up table
9	Module Type	D	SO-**D**IMM
		M	**M**icro-DIMM
		R	**R**egistered
		U	**U**nbuffered
		F	**F**ully Buffered

Field	Description	Values	Coding
10	Speed Grade	–19F	PC2–8500 6–6–6
		–1.9	PC2–8500 7–7–7
		–25F	PC2–6400 5–5–5
		–2.5	PC2–6400 6–6–6
		–3	PC2–5300 4–4–4
		–3S	PC2–5300 5–5–5
		–3.7	PC2–4200 4–4–4
		–5	PC2–3200 3–3–3
11	Die Revision	–A	First
		–B	Second

1) Multiplying “Memory Density per I/O” with “Module Data Width” and dividing by 8 for Non-ECC and 9 for ECC modules gives the overall module memory density in MBytes as listed in column “Coding”.

TABLE 27
DDR2 DRAM Nomenclature

Field	Description	Values	Coding
1	Qimonda Component Prefix	HYB	Constant
2	Interface Voltage [V]	18	SSTL_18
3	DRAM Technology	T	DDR2
4	Component Density [Mbit]	256	256 Mbit
		512	512 Mbit
		1G	1 Gbit
		2G	2 Gbit
5+6	Number of I/Os	40	×4
		80	×8
		16	×16
7	Product Variations	0 .. 9	Look up table
8	Die Revision	A	First
		B	Second
9	Package, Lead-Free Status	C	FBGA, lead-containing
		F	FBGA, lead-free
10	Speed Grade	–19F	PC2–8500 6–6–6
		–1.9	PC2–8500 7–7–7
		–25F	PC2–6400 5–5–5
		–2.5	PC2–6400 6–6–6
		–3	PC2–5300 4–4–4
		–3S	PC2–5300 5–5–5
		–3.7	PC2–4200 4–4–4
		–5	PC2–3200 3–3–3

Contents

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For further information on technology, delivery terms and conditions and prices please contact your nearest Qimonda Office.

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Qimonda Office.
Qimonda Components may only be used in life-support devices or systems with the express written approval of Qimonda, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.