

# DALLAS

SEMICONDUCTOR

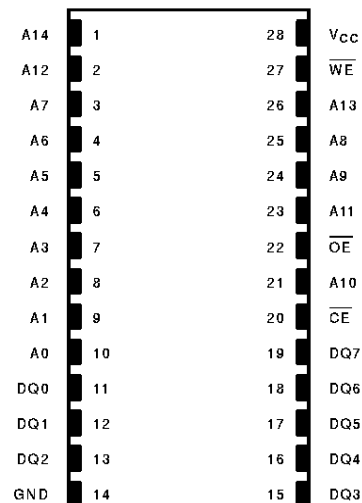
## DS1630Y/AB, DS1630YLPM/ABLPM

### Partitionable 256K NV SRAM

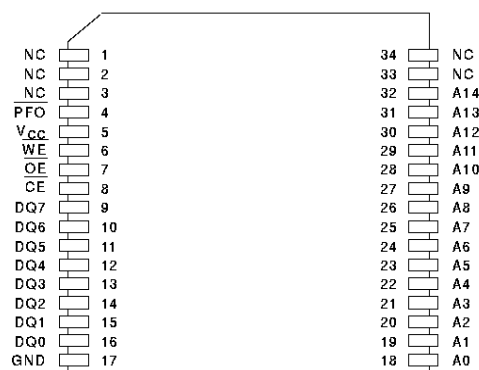
#### FEATURES

- Data retention in the absence of  $V_{CC}$
- Data is automatically protected during power loss
- Directly replaces 32K x 8 volatile static RAMs or EEPROMs
- Write protects selected blocks of memory regardless of  $V_{CC}$  status when programmed
- Unlimited write cycles
- Low-power CMOS
- Over 10 years of data retention
- Standard 28-pin JEDEC pinout (DS1630Y/AB)
- Available in access times as fast as 70 ns
- Read cycle time equals write cycle time
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Full  $\pm 10\%$  operating range (DS1630Y and DS1630YLPM)
- Optional  $\pm 5\%$  operation range (DS1630AB and DS1630ABLPM)
- Optional industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , designated IND
- Optional low profile module (LPM)
  - Fits into standard 68-pin PLCC surface mountable socket
  - 255 mils package height
  - Power fail output warns processor of impending power failure

#### PIN ASSIGNMENT



28-PIN ENCAPSULATED PACKAGE  
(740 MIL EXTENDED)



34-PIN LOW PROFILE MODULE (LPM)

**PIN DESCRIPTION**

A0 - A14	- Address Inputs
$\overline{CE}$	- Chip Enable
GND	- Ground
DQ0 - DQ7	- Data In/Data Out
$V_{CC}$	- Power (+5V)
$\overline{WE}$	- Write Enable
$\overline{OE}$	- Output Enable
NC	- No Connect

**ORDERING INFORMATION**

DS1630AB-XXX	28-pin thru-hole module
└─70	70 ns access
└─85	85 ns access
└─100	100 ns access
└─120	120 ns access
DS1630ABLPM-XXX	34-pin low profile module
└─70	70 ns access
└─100	100 ns access
DS1630Y-XXX	28-pin thru-hole module
└─70	70 ns access
└─85	85 ns access
└─100	100 ns access
└─120	120 ns access
DS1630YLP-XXX	34-pin low profile module
└─70	70 ns access
└─100	100 ns access

**DESCRIPTION**

The DS1630Y/AB 256K Nonvolatile SRAM is a 262, 144-bit, fully static SRAM organized as 32,768 words by 8 bits. The DS1630Y/AB has a self-contained lithium energy source and control circuitry that constantly monitors  $V_{CC}$  for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent garbled data. In addition, the device has the ability to unconditionally write protect blocks of memory so that inadvertent write cycles do not corrupt program and special data space. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for micro-processor interface. The nonvolatile SRAM can be used in place of existing 32K x 8 SRAMs directly conforming to the popular bytewise 28256 EEPROM, allowing direct substitution while enhancing performance. The DS1630YLP/ABLPM is a low profile module that fits into a standard 68-pin PLCC surface mountable socket and is functionally equivalent to the DS1630Y/AB. The DS1630YLP/ABLPM also provides a power fail output that warns a processor of impending power failure.

**READ MODE**

The DS1630Y/AB executes a read cycle whenever  $\overline{WE}$  (Write Enable) is inactive (high) and  $\overline{CE}$  (Chip Enable) is active (low). The unique address specified by the 15 address inputs ( $A_0 - A_{14}$ ) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within  $t_{ACC}$  (Access Time) after the last address input signal is stable, providing that  $\overline{CE}$  and  $\overline{OE}$  (Output Enable) access times are also satisfied. If  $\overline{OE}$  and  $\overline{CE}$  access times are not satisfied, then data access must be measured from the later occurring signal ( $\overline{CE}$  or  $\overline{OE}$ ) and the limiting parameter is either  $t_{CC}$  for  $\overline{CE}$  or  $t_{OE}$  for  $\overline{OE}$  rather than address access.

**WRITE MODE**

The DS1630Y/AB is in the write mode whenever the  $\overline{WE}$  and  $\overline{CE}$  signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of  $\overline{CE}$  or  $\overline{WE}$  will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of  $\overline{CE}$  or  $\overline{WE}$ . All address inputs must be kept valid throughout the write cycle.  $\overline{WE}$  must return to the high state for a minimum recovery time ( $t_{WR}$ ) before another cycle can be initiated. The  $\overline{OE}$  control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ( $\overline{CE}$  and  $\overline{OE}$  active) then  $\overline{WE}$  will disable the outputs in  $t_{ODP}$  from its falling edge.

**DATA RETENTION MODE**

The DS1630Y provides full functional capability for  $V_{CC}$  greater than 4.5 volts and write protects by 4.37V nominal ( $V_{CC}$  greater than 4.75V and write protect at 4.62V nominal for DS1630AB). Data is maintained in the absence of  $V_{CC}$  without any additional support circuitry. The DS1630Y/AB constantly monitors  $V_{CC}$ . Should the supply voltage decay, the RAM will automatically write protect itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As  $V_{CC}$  falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when  $V_{CC}$  rises above approximately 3.0 volts, the power switching circuit connects external  $V_{CC}$  to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after  $V_{CC}$  exceeds 4.5 volts (4.75 volts for the DS1630AB).

**FRESHNESS SEAL AND SHIPPING**

The N1LY/AB is shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When  $V_{CC}$  is applied at a level of greater than  $V_{TP}$ , the lithium energy source is enabled for battery backup operation.

**PARTITION PROGRAMMING MODE**

The register controlling the partition switch is selected by recognition of a specific binary pattern which is sent on address lines A11 - A14. These address lines are the four upper order address lines being sent to RAM. The pattern is sent by 20 consecutive read cycles with the exact pattern as shown in Table 1. Pattern matching must be accomplished using read cycles; any write cycles will reset the pattern matching circuitry. If this pattern is matched perfectly, then the 21st through 24th

read cycle will load the partition switch. Since there are 16 possible write protected partitions the size of each partition is 32K/16 or 2K x 8. Each partition is represented by one of the 16 bits contained in the 21st through 24th read cycle as defined by A11 through A14 and shown in Table 2. A logical 1 in a bit location sets that partition to write protect. A logical 0 in a bit location disables write protection. For example, if during the pattern match sequence bit 22 on address pin A12 was a 1, this would cause the partition register location for partition 5 to be set to a 1. This in turn would cause the N1LY/AB to inhibit  $\overline{WE}$  internally when A14 A13 A12 A11 = 0101. Note that while setting the partition register, data which is being accessed from the RAM should be ignored as the purpose of the 24 read cycles is to set the partition switch and not for the purpose of accessing data from RAM.

**PATTERN MATCH TO WRITE PARTITION REGISTER** Table 1

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A11	1	0	1	1	1	1	0	0	1	1	1	0	0	0	0	0	1	1	0	1	X	X	X	X
A12	1	1	1	1	1	0	0	1	1	1	0	0	1	0	1	1	0	0	0	0	X	X	X	X
A13	1	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	0	0	1	X	X	X	X
A14	1	1	0	0	0	1	1	1	0	0	1	0	0	0	1	0	1	0	0	0	X	X	X	X

↙ FIRST BITS ENTERED

↘ LAST GROUP ENTERED

**PARTITION REGISTER MAPPING** Table 2

Address Pin	Bit number in pattern match sequence	Partition Number	Address State Affected (A <sub>14</sub> A <sub>13</sub> A <sub>12</sub> A <sub>11</sub> )
A11	BIT 21	PARTITION 0	0000
A12	BIT 21	PARTITION 1	0001
A13	BIT 21	PARTITION 2	0010
A14	BIT 21	PARTITION 3	0011
A11	BIT 22	PARTITION 4	0100
A12	BIT 22	PARTITION 5	0101
A13	BIT 22	PARTITION 6	0110
A14	BIT 22	PARTITION 7	0111
A11	BIT 23	PARTITION 8	1000
A12	BIT 23	PARTITION 9	1001
A13	BIT 23	PARTITION 10	1010
A14	BIT 23	PARTITION 11	1011
A11	BIT 24	PARTITION 12	1100
A12	BIT 24	PARTITION 13	1101
A13	BIT 24	PARTITION 14	1110
A14	BIT 24	PARTITION 15	1111

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground	-0.5V to +7.0V
Operating Temperature	0°C to 70°C, -40°C to +85°C for ind parts
Storage Temperature	-40°C to +70°C, -40°C to +85°C for ind parts
Soldering Temperature	260°C for 10 seconds

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1630Y Power Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V	
DS1630AB Power Supply Voltage	V <sub>CC</sub>	4.75	5.0	5.25	V	
Logic 1	V <sub>IH</sub>	2.2		V <sub>CC</sub>	V	
Logic 0	V <sub>IL</sub>	0.0		+0.8	V	

**DC ELECTRICAL CHARACTERISTICS**(0°C to 70°C; V<sub>CC</sub>=5V ± 10% for DS1630Y)(0°C to 70°C; V<sub>CC</sub>=5V ± 5% for DS1630AB)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I <sub>IL</sub>	-1.0		+1.0	μA	
I/O Leakage Current CE ≥ V <sub>IH</sub> ≤ V <sub>CC</sub>	I <sub>IO</sub>	-1.0		+1.0	μA	
Output Current @ 2.4V	I <sub>OH</sub>	-1.0			mA	
Output Current @ 0.4V	I <sub>OL</sub>	2.0			mA	15
Standby Current $\overline{CE} = 2.2V$	I <sub>CCS1</sub>		5.0	10.0	mA	
Standby Current $\overline{CE} = V_{CC} - 0.5V$	I <sub>CCS2</sub>		3.0	5.0	mA	
Operating Current	I <sub>CCO1</sub>			85	mA	
Write Protection Voltage (DS1630Y)	V <sub>TP</sub>	4.25	4.37	4.5	V	
Write Protection Voltage (DS1630AB)	V <sub>TP</sub>	4.50	4.62	4.75	V	

**CAPACITANCE**(t<sub>A</sub> = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C <sub>IN</sub>		5	10	pF	
Input/Output Capacitance	C <sub>I/O</sub>		5	10	pF	

(0°C to 70°C; V<sub>CC</sub>=5V ± 5% for DS1630AB)(0°C to 70°C; V<sub>CC</sub>=5V ± 10% for DS1630Y)**AC ELECTRICAL CHARACTERISTICS**

		DS1630Y/AB-70		DS1630Y/AB-85			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	70		85		ns	
Access Time	t <sub>ACC</sub>		70		85	ns	
$\overline{\text{OE}}$ to Output Valid	t <sub>OE</sub>		35		45	ns	
$\overline{\text{CE}}$ to Output Valid	t <sub>CO</sub>		70		85	ns	
$\overline{\text{OE}}$ or $\overline{\text{CE}}$ to Output Valid	t <sub>COE</sub>	5		5		ns	5
Output High Z from Deselection	t <sub>OD</sub>		25		30	ns	5
Output Hold from Address Change	t <sub>OH</sub>	5		5		ns	
Write Cycle Time	t <sub>WC</sub>	70		85		ns	
Write Pulse Width	t <sub>WP</sub>	55		65		ns	3
Address Setup Time	t <sub>AW</sub>	0		0		ns	
Write Recovery Time	t <sub>WR1</sub> t <sub>WR2</sub>	10 10		10 10		ns ns	13 14
Output High Z from $\overline{\text{WE}}$	t <sub>ODW</sub>		25		30	ns	5
Output Active from $\overline{\text{WE}}$	t <sub>OEW</sub>	5		5		ns	5
Data Setup Time	t <sub>DS</sub>	30		35		ns	4
Data Hold Time	t <sub>DH1</sub> t <sub>DH2</sub>	5 5		5 5		ns ns	13 14
		DS1630Y/AB-100		DS1630Y/AB-120			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Read Cycle Time	t <sub>RC</sub>	100		120		ns	
Access Time	t <sub>ACC</sub>		100		120	ns	
$\overline{\text{OE}}$ to Output Valid	t <sub>OE</sub>		50		60	ns	
$\overline{\text{CE}}$ to Output Valid	t <sub>CO</sub>		100		120	ns	
$\overline{\text{OE}}$ or $\overline{\text{CE}}$ to Output Valid	t <sub>COE</sub>	5		5		ns	5
Output High Z from Deselection	t <sub>OD</sub>		35		35	ns	5
Output Hold from Address Change	t <sub>OH</sub>	5		5		ns	
Write Cycle Time	t <sub>WC</sub>	100		120		ns	
Write Pulse Width	t <sub>WP</sub>	75		90		ns	3
Address Setup Time	t <sub>AW</sub>	0		0		ns	
Write Recovery Time	t <sub>WR1</sub> t <sub>WR2</sub>	10 10		10 10		ns ns	13 14
Output High Z from $\overline{\text{WE}}$	t <sub>ODW</sub>		35		35	ns	5
Output Active from $\overline{\text{WE}}$	t <sub>OEW</sub>	5		5		ns	5
Data Setup Time	t <sub>DS</sub>	40		50		ns	4
Data Hold Time	t <sub>DH1</sub> t <sub>DH2</sub>	5 5		5 5		ns ns	13 14

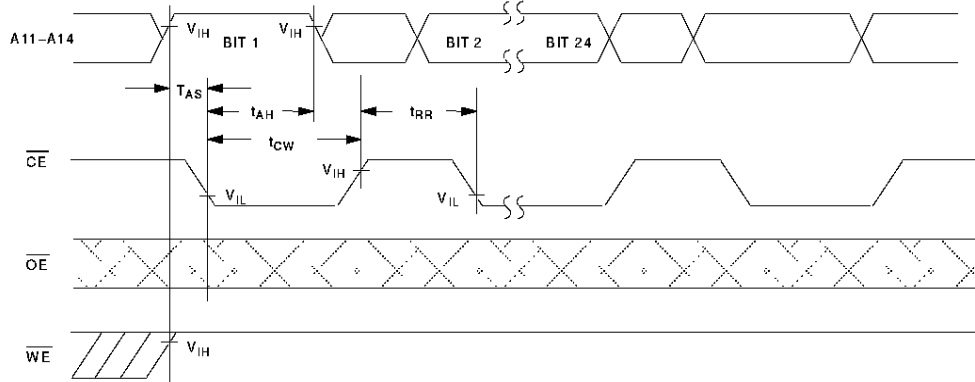
**AC ELECTRICAL CHARACTERISTICS**

(0°C to 70°C;  $V_{CC1}=4.50V$  to  $5.50V$ )\*

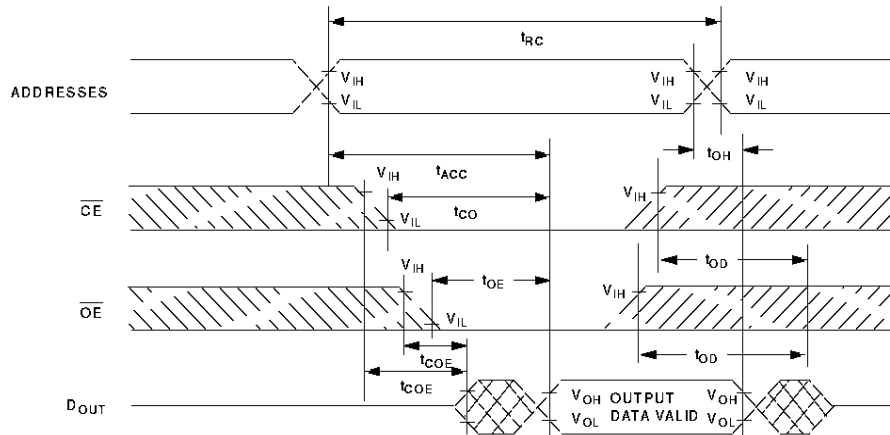
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	$t_{AS}$	0			ns	
Address Hold	$t_{AH}$	50			ns	
Read Recovery	$t_{RR}$	10			ns	
CE Pulse Width	$t_{CW}$	75			ns	

\*For loading partition register

**TIMING DIAGRAM: LOADING PARTITION REGISTER**

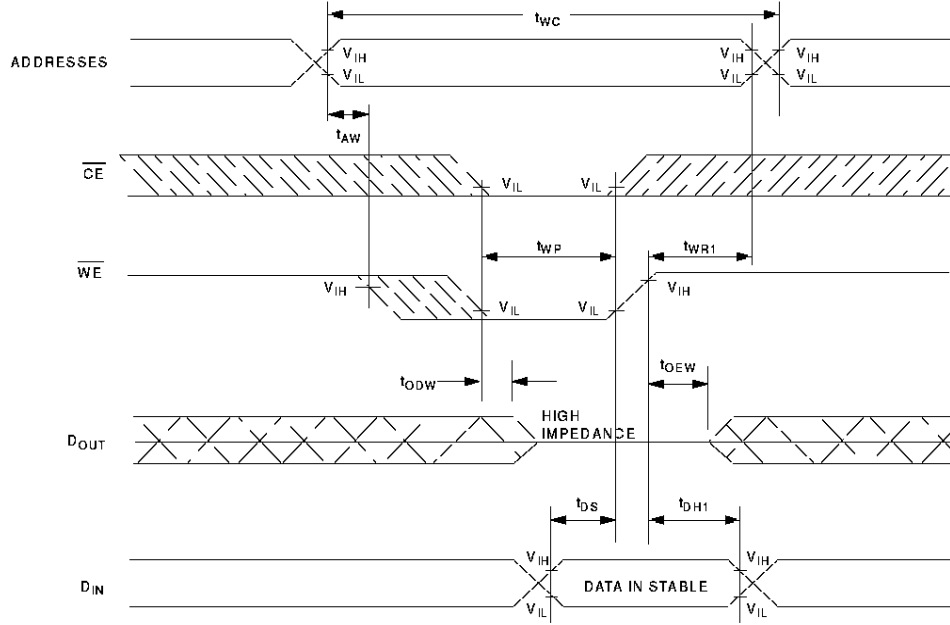


**READ CYCLE**



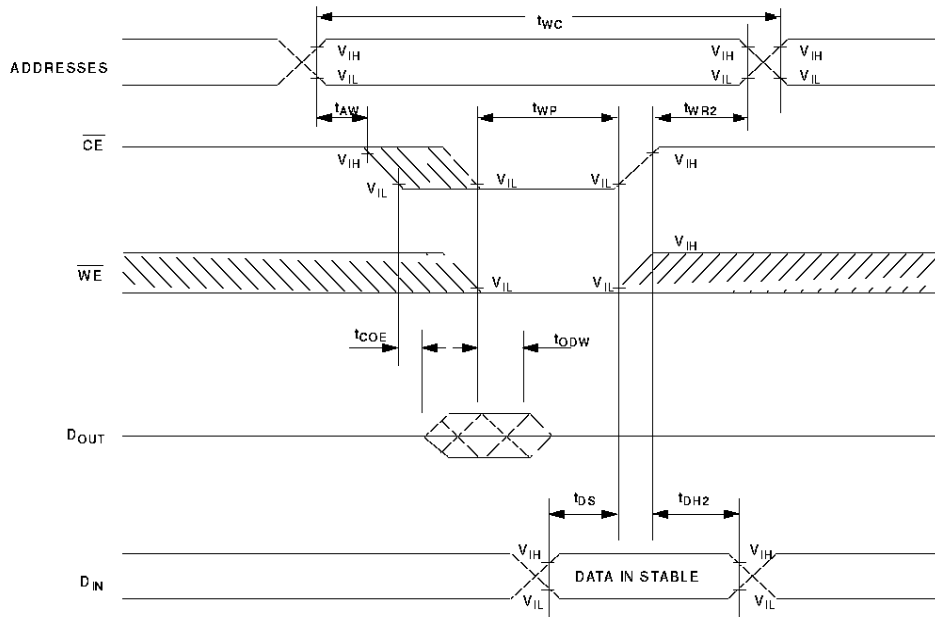
SEE NOTE 1

**WRITE CYCLE 1**



SEE NOTES 2, 6, AND 7

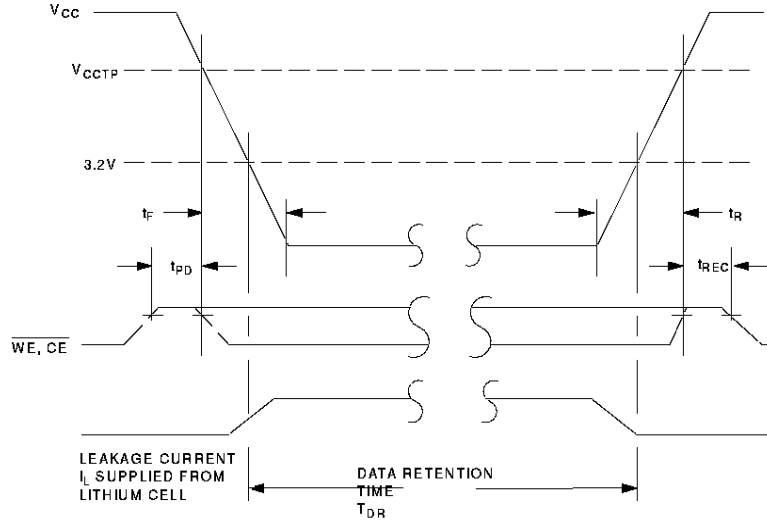
**WRITE CYCLE 2**



SEE NOTES 2 AND 8



**POWER-DOWN/POWER-UP CONDITION**



See note 12.

**POWER-DOWN/POWER-UP TIMING**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
$t_{PD}$	$\overline{CE}$ , $\overline{WE}$ at $V_{IH}$ before Power-Down	0			$\mu s$	12
$t_F$	$V_{CC}$ slew from 4.5V to 0V ( $\overline{CE}$ at $V_{IH}$ )	300			$\mu s$	
$t_R$	$V_{CC}$ slew from 0V to 4.5V ( $\overline{CE}$ at $V_{IH}$ )	0			$\mu s$	
$t_{REC}$	$\overline{CE}$ , $\overline{WE}$ at $V_{IH}$ after Power-Up	25		125	ms	

( $t_A = 25^\circ C$ )

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
$t_{DR}$	Expected Data Retention Time	10			years	9, 11

**WARNING:**

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

**NOTES:**

1.  $\overline{WE}$  is high for a read cycle.
2.  $\overline{OE} = V_{IH}$  or  $V_{IL}$ . If  $\overline{OE} = V_{IH}$  during write cycle, the output buffers remain in a high impedance state.
3.  $t_{WP}$  is specified as the logical AND of  $\overline{CE}$  and  $\overline{WE}$ .  $t_{WP}$  is measured from the latter of  $\overline{CE}$  or  $\overline{WE}$  going low to the earlier of  $\overline{CE}$  or  $\overline{WE}$  going high.
4.  $t_{DS}$  is measured from the earlier of  $\overline{CE}$  or  $\overline{WE}$  going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the  $\overline{CE}$  low transition occurs simultaneously with or latter than the  $\overline{WE}$  low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the  $\overline{CE}$  high transition occurs prior to or simultaneously with the  $\overline{WE}$  high transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
8. If  $\overline{WE}$  is low or the  $\overline{WE}$  low transition occurs prior to or simultaneously with the  $\overline{CE}$  low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1630Y/AB has a built-in switch that disconnects the lithium source until  $V_{CC}$  is first applied by the user. The expected  $t_{DR}$  is defined as accumulative time in the absence of  $V_{CC}$  starting from the time power is first applied by the user.
10. All DC operating conditions, DC electrical characteristics, and AC electrical characteristics apply to both standard parts and those designated IND. Parts with the IND designation meet specifications over a temperature range of -40°C to +85°C.
11. The expected data retention time for parts designated IND meet or exceed the specified  $t_{DR}$  at 25°C. IND parts which are continuously exposed to 85°C will have a  $t_{DR}$  of 2 years. The amount of time that IND parts are exposed to temperatures of less than 85°C will significantly prolong data retention time. For example, parts exposed continuously to temperatures of 70°C will have a  $t_{DR}$  of 7 years.
12. In a power down condition the voltage on any pin may not exceed the voltage on  $V_{CC}$ .
13.  $t_{WR1}$ ,  $t_{DH1}$  are measured from  $\overline{WE}$  going high.
14.  $t_{WR2}$ ,  $t_{DH2}$  are measured from  $\overline{CE}$  going high.
15. The power fail output signal ( $\overline{PFO}$ ) is driven active ( $V_{OL}=0.4V$ ) when the  $V_{CC}$  trip point occurs. While active, the  $\overline{PFO}$  pin can sink 4 mA and will maintain a maximum output voltage of 0.4 volts. When inactive, the voltage output of  $\overline{PFO}$  is 2.4 volts minimum and will source a current of 1 mA. This signal is only present on the DS1630YLPM/ABLPM.

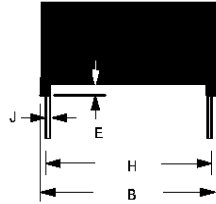
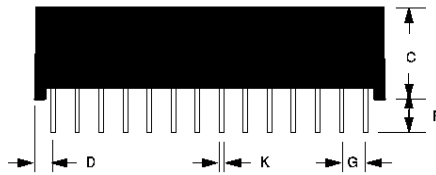
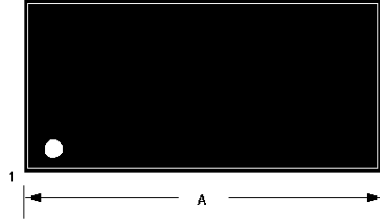
**DC TEST CONDITIONS**

Outputs Open  
t Cycle = 200 ns  
All voltages are referenced to ground

**AC TEST CONDITIONS**

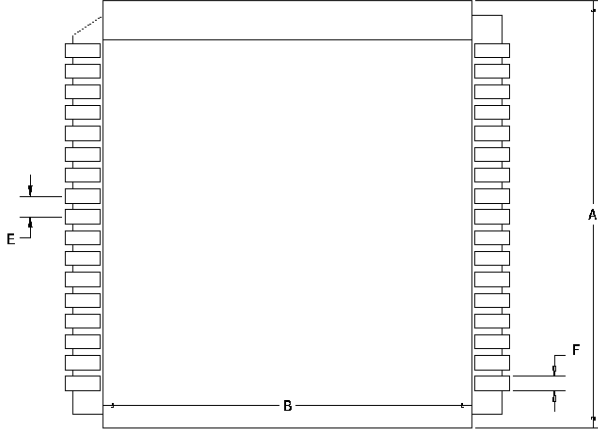
Output Load: 100 pF + 1TTL Gate  
Input Pulse Levels: 0 - 3.0V  
Timing Measurement Reference Levels  
Input: 1.5V  
Output: 1.5V  
Input pulse Rise and Fall Times: 5 ns

**DS1630Y/AB NONVOLATILE SRAM 28 PIN 740 MIL MODULE**

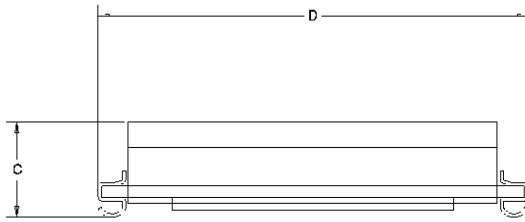


PKG	28-PIN		
	DIM	MIN	MAX
A	IN.	1.480	1.500
	MM	37.60	38.10
B	IN.	0.720	0.740
	MM	18.29	18.80
C	IN.	0.355	0.375
	MM	9.02	9.52
D	IN.	0.080	0.110
	MM	2.03	2.79
E	IN.	0.015	0.025
	MM	0.38	0.63
F	IN.	0.120	0.160
	MM	3.05	4.06
G	IN.	0.090	0.110
	MM	2.29	2.79
H	IN.	0.590	0.630
	MM	14.99	16.00
J	IN.	0.008	0.012
	MM	0.20	0.30
K	IN.	0.015	0.021
	MM	0.38	0.53

**DS1630YLPM/ABLPM 34-PIN LOW PROFILE MODULE (LPM)**



PKG	INCHES	
	DIM	MIN
A	0.955	0.970
B	0.840	0.855
C	0.230	0.250
D	0.975	0.995
E	0.050 BSC	
F	0.015	0.025



Suggested 68-pin PLCC surface mountable sockets with leads on two sides only are:

- McKenzie                    34P-SMT-3
- Harwin                      HIS-40001-04
- Dallas Semiconductor    DS34PIN-PLC

For recommended prototype/breadboard sockets, contact the Dallas Semiconductor factory.