LINEAR SYSTEMS

SST440
MONOLITHIC DUAL
N-CHANNEL JFET

micross

Linear Systems replaces discontinued Siliconix SST440

The SST440 is a tightly matched Monolithic Dual N-Channel JFET

The SST440 are monolithic dual JFETs mounted in a SOIC package. The monolithic dual chip design reduces parasitics and gives better performance at very high frequencies while ensuring extremely tight matching. These devices are an excellent choice for use as wideband differential amplifiers in demanding test and measurement applications. The SST440 is a direct replacement for discontinued Siliconix SST440.

The 8 Pin SOIC provides ease of manufacturing, and the symmetrical pinout prevents improper orientation. (See Packaging Information).

SST440 Applications:

- Wideband Differential Amps
- High-Speed,Temp-Compensated Single-Ended Input Amps
- High-Speed Comparators
- Impedance Converters and vibrations detectors.

FEATURES	
Direct Replacement for SILICONIX SST440	
HIGH CMRR	CMRR ≥ 85dB
LOW GATE LEAKAGE	I_{GSS} ≤ 1 pA
ABSOLUTE MAXIMUM RATINGS [1] @ 25°C (unless otherwise noted)	
Maximum Temperatures	
Storage Temperature	-65°C to +150°C
Operating Junction Temperature	-55°C to +135°C
Maximum Power Dissipation	
Continuous Power Dissipation (Total)	500mW
Maximum Currents	
Gate Current	50mA
Maximum Voltages	
Gate to Drain	-25V
Gate to Source	-25V
Gate to Gate	±50V

MATCHING CHARACTERISTICS @ 25°C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate to Source Cutoff Voltage			10	mV	V_{DG} = 10V, I_D = 5mA
$\Delta\lvert V_{GS1} - V_{GS2} \rvert / \Delta T$	Differential Gate to Source Cutoff Voltage Change with Temperature		20		µV/°C	V_{DG} = 10V, I_D = 5mA T_A = -55°C to +125°C
I_{DSS1} / I_{DSS2}	Gate to Source Saturation Current Ratio		0.07			V_{DS} = 10V, V_{GS} = 0V
G_{fs1} / G_{fs2}	Forward Transconductance Ratio [2]		0.97			V_{DS} = 10V, I_D = 5mA, f = 1kHz
CMRR	Common Mode Rejection Ratio		85		dB	V_{DG} = 5 to 10V, I_D = 5mA

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	-25			V	I_G = -1µA, V_{DS} = 0V
$V_{GS(off)}$	Gate to Source Cutoff Voltage	-1	-3.5	-6	V	V_{DS} = 10V, I_D = 1nA
I_{DSS}	Gate to Source Saturation Current	6	15	30	mA	V_{DS} = 10V, V_{GS} = 0V
I_{GSS}	Gate Leakage Current [3]		-1	-500	pA	V_{GS} = -15V, V_{DS} = 0V
I_G	Gate Operating Current		-1	-500	pA	V_{DG} = 10V, I_D = 5mA
g_{fs}	Forward Transconductance	4.5	6	9	mS	V_{DS} = 10V, I_D= 5mA, f = 1kHz
g_{os}	Output Conductance		70	200	µS	
C_{ISS}	Input Capacitance		3		pF	V_{DS} = 10V, I_D = 5mA, f = 1MHz
C_{RSS}	Reverse Transfer Capacitance		1		pF	
e_n	Equivalent Input Noise Voltage		4		nV/√Hz	V_{DS} = 10V, I_D = 5mA, f = 10kHz

Notes:
1. Absolute Maximum ratings are limiting values above which serviceability may be impaired
2. Pulse Test: PW ≤ 300µs Duty Cycle ≤ 3%
3. Assumes smaller value in numerator

Available Packages:

SST440 in SOIC
SST440 available as bare die

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Please contact Micross for full package and die dimensions:

Email: chipcomponents@micross.com
Web: www.micross.com/distribution.aspx

SOIC (Top View)