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Revision 278298-001

Level One(TM) IXP1200 Network Processor

General Description

The Level One™ IXP1200 Network Processor delivers high-performance processing power and flexibility to a wide variety of networking and telecommunications products. Providing the best attributes of a custom network ASIC and an embedded microprocessor, the IXP1200 Network Processor combines an ARM® architecture compatible Intel® StrongARM® microprocessor with six programmable multithreaded microengines that together can switch 2.5 million packets/second in a single chip.

- **Applications**
  - LAN-WAN Switches
  - WAN Switches
  - Telecommunications Systems
  - Broadband Cable Products
  - Remote Access Switches
- **Six Integrated Programmable Microengines**
  - Operating frequency at 162 MHz
  - Multi-thread support of four threads per microengine
  - Single-cycle ALU and shift operations
  - Zero context swap overhead
  - Large register set: 128 General Purpose and 128 Transfer Registers
  - 1K x 32-bit instruction Control Store
  - Access to the IX Bus Unit, PCI DMA channels, SRAM, and SDRAM
- **ARM® architecture compatible Intel® StrongARM® Core**
  - High performance, low-power, 32-bit RISC processor
  - Operating frequency at 162 MHz
  - 16 Kbyte instruction cache
  - 8 Kbyte data cache
  - 1 Kbyte mini-cache for data that is used once and then discarded
  - Write buffer
  - Memory management unit

Features

  - Access to the IX Bus Interface Unit, PCI Unit and SDRAM Unit via the ARM® AMBA Bus
- **High Bandwidth I/O Bus**
  - Intel 64-bit, 66 MHz IX Bus
  - 4.2 Gb/s peak bandwidth
  - 64-bit or dual 32-bit IX Bus options
- **Integrated 32-bit, 66 MHz PCI Interface**
  - PCI 2.1 compliant Bus Master
  - 264 Mbytes/s peak burst mode operation
  - I^2O support for StrongARM® Core
  - Dual DMA channels
- **Industry Standard 64-bit SDRAM Interface**
  - Peak bandwidth 648 Mbytes/s
  - Address up to 128 Mbytes of SDRAM
  - Memory bandwidth optimization through bank switching
  - Read-modify-write support
  - Parity protected data
  - Byte aligner/merger
- **Industry Standard 32-bit SRAM Interface**
  - Peak bandwidth of 334 Mbytes/s
  - Address up to 8 Mbytes of SRAM
  - 8 Mbytes FlashROM for booting StrongARM® Core
  - Supports atomic push/pop operations
  - Supports atomic bit set and bit clear operations
  - Memory bandwidth improvement by reduced read/write turnaround bus cycles
- **Other Integrated Features**
  - Hardware Hash Unit for generating 48 or 64-bit adaptive polynomial hash keys
  - Serial UART port
  - Real Time Clock
  - Four general purpose I/O pins
  - Four 24-bit timers with CPU watchdog support
  - JTAG Support for IEEE 1149.1

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    - 4 Kbyte Scratchpad Memory
- **432-pin, ESBGA package**
- **2 V CMOS device**
    - 3.3 V tolerant I/O
- **IXP1200 Network Processor Development Environment**
    - Integrated Development Environment
    - Text Editor
    - Microcode Assembler
    - StrongARM® and Microcode Linker
    - Cycle- and data-accurate simulator of the IXP1200 Network Processor

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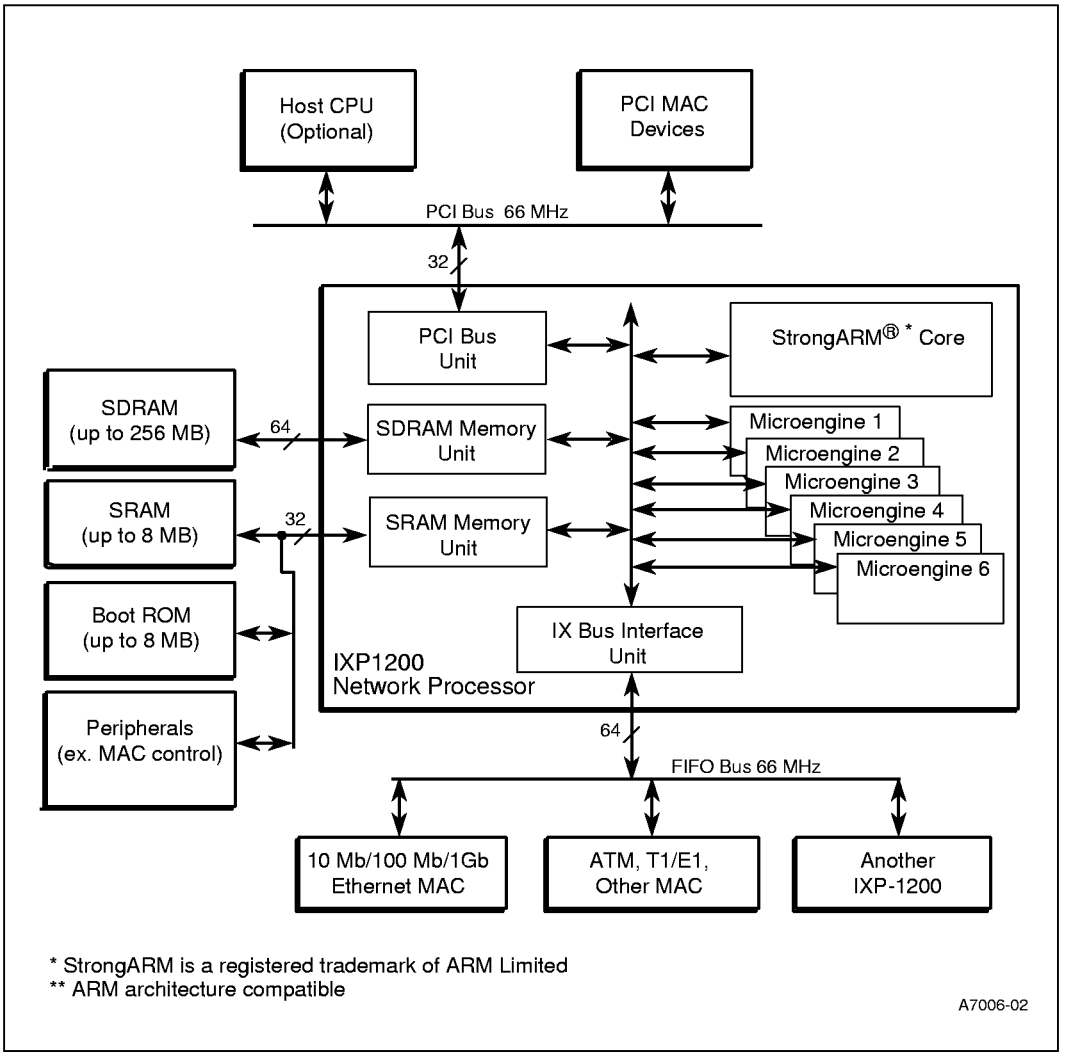
SECTION 1 - PROCESSOR DESCRIPTION

The Level One™ IXP1200 Network Processor is a highly integrated, hybrid data processor that delivers high-performance parallel processing power and flexibility to a wide variety of networking, communications, and other data-intensive products. The IXP1200 Network Processor is designed specifically as a data control element for applications that require access to a fast memory subsystem, a fast interface to I/O devices such as network MAC devices, and processing power to perform efficient manipulation on bits, bytes, words, and doubleword (Dword) data.

The IXP1200 Network Processor is combined with six independent 32-bit RISC data engines with hardware multithread support that provide over 1 giga-operations per second. The microengines contain the processing power to perform tasks typically reserved for high speed ASICs. In LAN switching applications, the six microengines are capable of performing 100% of the packet forwarding at Layer-3 for 2.5 million Ethernet packets per second. The IXP1200 Network Processor can then be used for more complex tasks such as address learning, building and maintaining forwarding tables, and network management.

Figure 1: Level One™ IXP1200 Network Processor Block Diagram



1.1 Introduction

The Level One™ IXP1200 Network Processor is a highly integrated, hybrid data processor that delivers high-performance parallel processing power and flexibility to a wide variety of networking, communications, and other data-intensive products. The IXP1200 Network Processor is designed specifically as a data control element for applications that require access to a fast memory subsystem, a fast interface to I/O devices such as network MAC devices, and processing power to perform efficient manipulation on bits, bytes, words, and doubleword (Dword) data.

The IXP1200 Network Processor technology is defined as a loosely-coupled, hybrid parallel processor set, integrating an ARM® architecture compatible Intel® StrongARM® Core with an array of RISC data engines. Maximum throughput can be maintained by isolating them from memory accesses and the resulting latencies. This is done by decoupling the functional units for the IX Bus, PCI Bus, SDRAM, and SRAM interfaces from the execution pipelines through the extensive use of FIFO queues, and event task signaling. Semaphore mechanisms and thread-level support are implemented in hardware, allowing for zero-overhead context switching between threads executing on the microengines.

Up to four thread-level tasks can be allocated per microengine for a total of twenty-four threads in a single IXP1200 Network Processor. Multiple IXP1200 Network Processor devices can be aggregated in a serial or parallel fashion, or in serial-parallel combinations to support diverse applications. Support chips can assist the system designer in using the IXP1200 Network Processor in these multiprocessor designs.

A full suite of software tools is available from Level One™ for microengine code development, simulation and target hardware debug. These tools and can be used in conjunction with third-party StrongARM® software tools and Realtime Operating Systems to build a complete embedded solution.

1.2 Related Documents

- Level One® IXP1200 Network Processor Programmer's Reference Manual
- Level One® IXP1200 Network Processor Development Tools User's Guide
- Level One® IXP1200 Network Processor Hardware Reference Manual
- Level One® IXP1200 Network Processor Software Reference Manual
- ARM V4.0 Architecture Reference

Important clarification: In this and related IXP1200 Network Processor documents, a Word is equal to 16 bits, a doubleword (Dword) is equal to 32 bits, and a quadword (Qword) is equal to 64 bits. StrongARM® documents and the ARM V4.0 Architecture Reference typically refer to a Word as being equal to 32 bits, and a halfword as being equal to 16-bits. A future release of the IXP1200 Network Processor document set will incorporate consistent terminology for all data sizes.

SECTION 2 - FUNCTIONAL UNITS

2.1 IXP1200 Network Processor

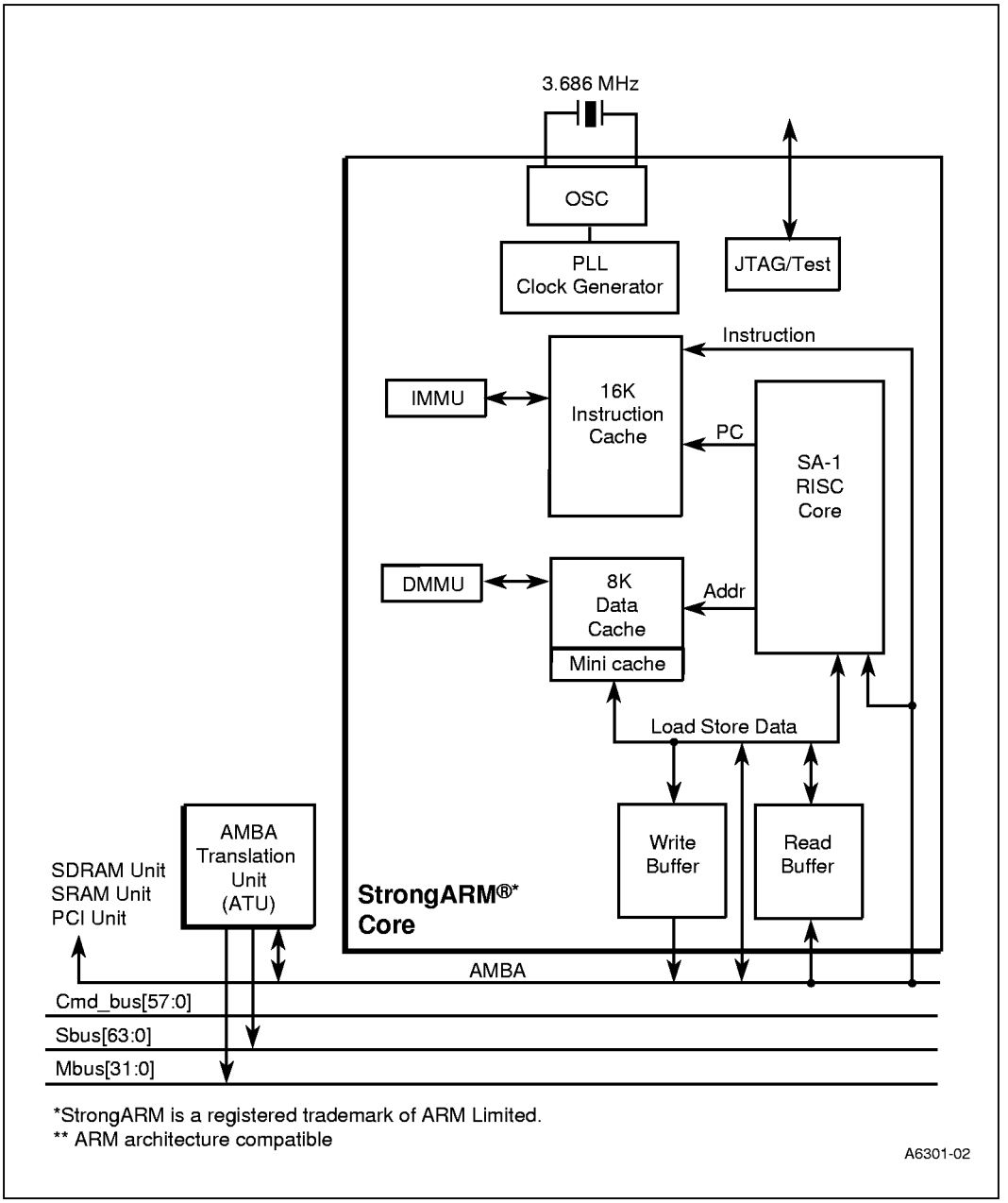
The IXP1200 Network Processor is the same industry standard 32-bit RISC processor as used in applications such as network computers, PDAs, palmtop computers and portable telephones. The differentiating feature of the IXP1200 Network Processor is that it provides very high performance in a low-power, compact design. This makes is feasible to combine it with a collection of other dedicated execution units on the same silicon die.

The IXP1200 Network Processor and six RISC microengines provide the processing power required to forward 2.5 million Ethernet packets per second through the IXP1200 Network Processor using 16, 10/100 ports at full line rate, full-duplex. A multi-IXP1200 Network Processor system scales linearly so that, for example, a system comprised of eight IXP1200 Network processors (128, 10/100Mb Ethernet ports total) can process over 19 million packets per second.

The designer can partition his application by allocating microengines, threads, and network processor tasks. If necessary, multiple IXP1200 Network Processor devices can be used to aggregate CPU MIPs, increase data bandwidth, increase port fanout and density, or some combination of all three metrics.

When used with an input clock frequency of 3.6864 MHz, the network processor operates at a core speed (Fcore) of 162 MHz.

Figure 2: StrongARM® Core Block Diagram



2.2 Microengines

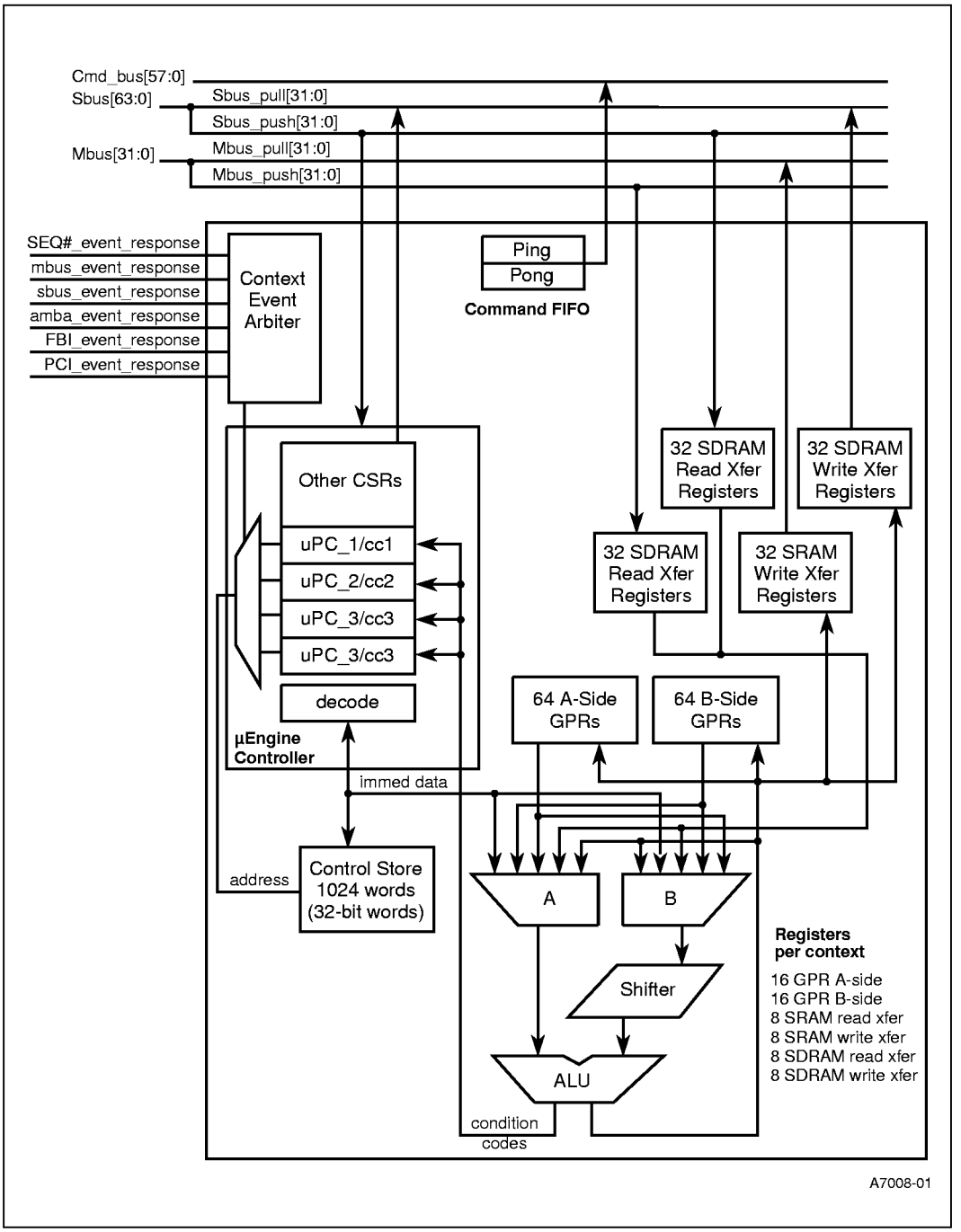
Six 32-bit, multithreaded RISC microengines perform data movement and processing without assistance from the IXP1200 Network Processor. Each microengine has four independent program counters, zero overhead context switching and hardware semaphores from other hardware units to ensure that each microengine can be fully utilized.

A microengine's powerful ALU and shifter perform both ALU and shift operations in a single cycle. The instruction set was specifically designed for networking and communications applications that require bit, byte, word and Dword operations to forward data quickly and efficiently. Each microengine contains a large amount of local memory and registers: 4 Kbytes organized as 1024 by 32 bits of high-speed RAM Control Store for

microcode execution, 128 32-bit General Purpose Registers, and 128 32-bit transfer registers to service the SRAM and SDRAM units.

When used with an input clock frequency of 3.6864 MHz, the microengines operate at a core speed (Fcore) of 162 MHz.

Figure 3: IXP1200 Network Processor Microengine Block Diagram



2.3 IX Bus Interface Unit and IX Bus

The IX Bus Interface Unit is responsible for servicing fast peripherals, such as MAC-layer devices, on the IX Bus (FIFO Bus). This includes moving data to and from the IXP1200 Network Processor Receive and Transmit FIFOs.

The IX Bus provides a 4.2 Gb/s interface to peripheral devices. The IX Bus was specifically designed to provide a simple and efficient interface. The IX Bus can be configured as either a 64-bit, bidirectional bus or as two 32-bit, unidirectional buses operating at up to 66 MHz.

The IX Bus Interface Unit contains the Transmit and Receive FIFO elements, chip-level Control Status Registers (CSRs), a 4 Kbyte Scratchpad RAM, and a Hash Unit for generating 48- and 64-bit hash keys.

The IX Bus consists of 64 data pins, 23 control pins, and a clock input pin with a typical operating frequency of 66 MHz. A sideband control bus operating in parallel to the IX Bus, called the ReadyBus, consists of eight additional data pins and five control pins.

The ReadyBus is synchronous to the IX Bus clock, but it's operation is controlled by a programmable hardware sequencer. ReadyBus cycles are separate and distinct from IX Bus cycles. Up to twelve sequencer commands are loaded at chip initialization time, and run in a continuous loop. The commands can consist of sampling FIFO status for the IX Bus devices, sending Flow Control messages to MAC devices, and reads/writes to other IXP1200 Network Processor devices as required by the application design. Refer to the *IXP1200 Network Processor Hardware Reference Manual* for specific details on using the ReadyBus.

2.3.1 IX Bus Access Behavior

There are two basic modes of IX Bus operation. This is a configuration option only and is not intended to be used "on the fly" to switch between modes.

- 64-Bit Bidirectional Mode

  The entire 64-bit data path FDAT[63:0] is used for reads, or writes to IX Bus devices. The IXP1200 Network Processor will always drive and receive all 64-bits of the IX Bus in this mode. Valid bytes are indicated on FBE[7:0] driven by the IXP1200 Network Processor during writes, and by the target IX Bus resource on reads.

- 32-bit Unidirectional Mode

  The IX Bus is split into independent 32-bit Transmit and 32-bit Receive data paths. Transmit data is driven on FDAT[63:32] and Receive data is input on FDAT[31:0]. In this mode, the Transmit path is always driven, and the Receive path is always an input. Valid bytes are identified for the Transmit path by FBE[7:4] signals. Valid bytes are identified for the Receive path by FBE[3:0].

Each basic mode has two additional modes depending on the number of IX Bus devices and ports being used. 1-2 MAC mode for a one or two devices, and 3+ MAC mode when using three to seven devices. Bus timing, and the functions of the IX Bus signals are slightly different in each mode. These functional definitions per IX Bus mode are listed in Section 3.6 and Section 3.7.

In addition, a shared IX Bus mode is supported in 64-bit Bidirectional mode. Refer to the list at the bottom of Table 20 for the signals that the IX Bus masters must drive and IX Bus slaves must tri-state.

The IX Bus, and Level One™ devices using the IX Bus such as the IXF440 Octal Fast Ethernet Media Access Controller and the IXF1002 Dual Port Gigabit Ethernet Media Access Controller observe a pipelined bus protocol. When cycles are ended early on receive cycles, the pipeline continues to cause several extra bus cycles depending on when the EOP signal was asserted. Data is a "don't care" for these trailing bus cycles, except in the case of a status transfer where the IX Bus burst includes a possible status transfer if the device were programmed to support it.

The tables below show the number of total IX Bus data cycles that will occur for a burst with EOP asserted at specific clocks for 64 bit and 32 bit IX Bus modes. In each case, the tables show IX Bus cycles with and without the optional status transfer cycle. Refer to the IX Bus Protocol Timing diagrams (Figure 17 through Figure 37) when interpreting these tables.

Table 1: 64-bit IX Bus Receive Remainder Cycles, No Status Transfer

EOP signaled on this cycle:	1	2	3	4	5	6	7	8
# of bus cycles in burst:	5	6	7	8	8	8	8	8
# of Don't Care cycles:	4	4	4	4	3	2	1	0

Table 2: 64-bit IX Bus Receive Remainder Cycles, with Status Transfer

EOP signaled on this cycle:	1	2	3	4	5	6	7	8
# of bus cycles in burst:	5	6	7	8	8	8	8	8
Status transfer	1	1	1	1	1	1	1	Note 1
# of Don't Care cycles:	3	3	3	3	2	1	0	0

NOTE:
1. Status transfer cycle occurs on a subsequent dedicated IX Bus status cycle.

Table 2: 32-bit IX Bus Receive Remainder Cycles, No Status Transfer

EOP signaled on this cycle:	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
# of bus cycles in burst:	5	6	7	8	9	10	11	12	13	14	15	16	16	16	16	16
# of Don't Care cycles:	4	4	4	4	4	4	4	4	4	4	4	4	3	2	1	0

Table 3: 32-bit IX Bus Receive Remainder Cycles, with Status Transfer

EOP signaled on this cycle:	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
# of bus cycles in burst:	5	6	7	8	9	10	11	12	13	14	15	16	16	16	16	16
Status transfer	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	Note 1

NOTE:
1. Status transfer cycle occurs on a subsequent IX Bus cycle.

In both 32-bit and 64-bit modes, all of the associated FBE# signals (four Transmit FBE#s and four Receive FBE#s in 32 bit mode, and eight Transmit/Receive FBE#s for 64-bit mode) are driven low on a transmit. The last bus transfer, identified by the assertion of EOP, indicates the number of valid bytes of this last transfer by driving only the valid FBE# signals.

Similarly for Receive cycles, in both 32-bit and 64-bit modes, all associated FBE# signals must be driven low by the peripheral or MAC device, and must identify the number of valid bytes on the last transfer driven with EOP. The IXP1200 Network Processor uses this information to update the RCV_CTL register's Valid Bytes field. Driving fewer than the four or eight FBE#s except for the last transfer with EOP may cause undefined behavior.

2.4 SDRAM, SRAM Units

The IXP1200 Network Processor supports two high performance memory units. The SRAM Unit provides fast memory that can be used to store look-up tables. The SDRAM Unit provides lower cost memory for forwarding information and transmit queues. Both units contain features that improve memory bandwidth utilization.

2.4.1 SDRAM Unit

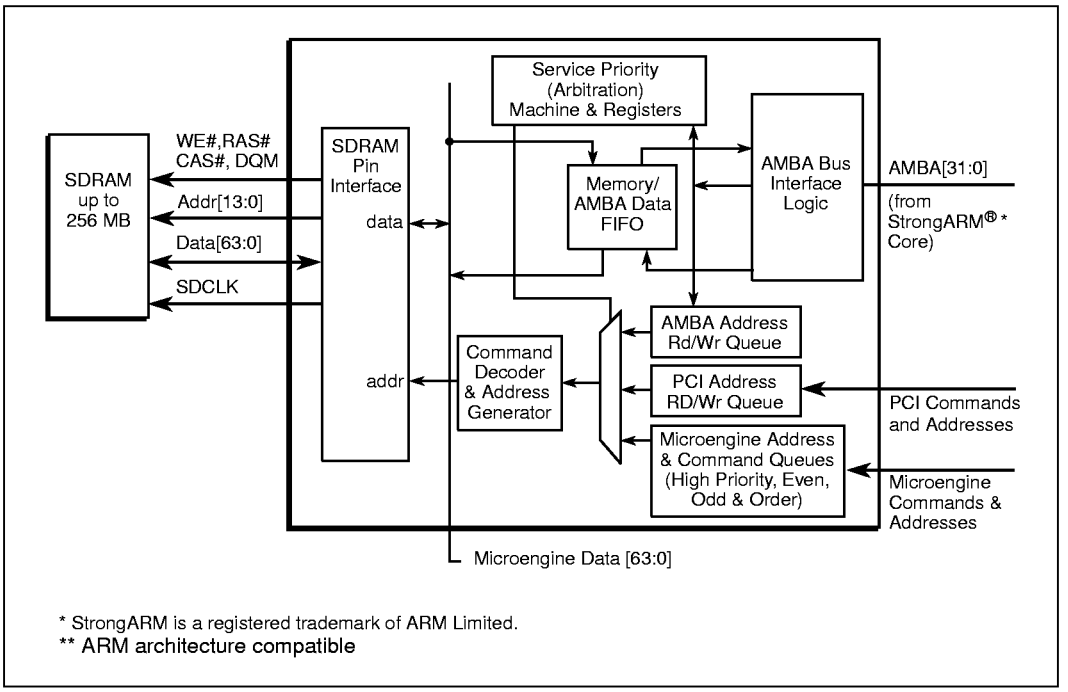
The IXP1200 Network Processor provides an SDRAM Unit to access low cost, high bandwidth memory for mass data storage. The StrongARM® processor address space allows up to 256 Mbytes of SDRAM to be addressed, although the IXP1200 Network Processor allows only up to 128 Mbytes. The SDRAM interface operates at 81 MHz, providing a peak bandwidth of 648 Mbytes per second.

Bus cycles are generated by requests from the PCI Unit including PCI DMA cycles, the StrongARM® Core, and the microengines.

The SDRAM is operated by commands that are loaded into command queues within the unit. The SDRAM unit decodes the command, reads or writes the data, then deletes the command from the head of the queue. The read and write sources may be SDRAM memory locations, transfer registers, or the transmit and receive FIFOs in the IX Bus Interface Unit. Refer to the *IXP1200 Network Processor Hardware Reference Manual* for details on how these requests are queued, prioritized, and serviced by the SDRAM Unit.

Figure 4 details the major components of the SDRAM Unit.

Figure 4: SDRAM Unit Block Diagram



The SDRAM bus consists of 14 Row/Column address bits, 64 data bits, 1 parity data bit, RAS#, CAS#, Write Enable, Buffer Direction Control, and a synchronous output clock running at one-half the IXP1200 Network Processor core frequency, typically 81 MHz.

The PCI, microengines, and StrongARM® Core require single byte, word, and longword write capabilities. The SDRAM unit supports this using a read-modify-write technique. As data is written from the PCI or StrongARM® Core to SDRAM, a quadword is read from SDRAM. The IXP1200 Network Processor then updates only the bytes that were enabled and writes the entire quadword of data back to SDRAM memory. (Note that the bytes do not have to be consecutive.) These three steps are performed automatically.

The SDRAM Unit has parity protection across the 64-bit data. If parity generation and checking is enabled via a control status register, writes will generate parity into the array, and reads will check parity. A Parity error interrupt can be enabled to signal the StrongARM® Core.

SDRAMs with an access time of 6 ns are required with an Fcore frequency of 162 MHz.

2.4.2 SDRAM Bus Access Behavior

- The number of quadwords transferred by the SDRAM Unit is determined by the requesting interface (Core, microengine, or PCI). No speculative cycles are generated. The SDRAM unit may reorder SDRAM accesses for best performance.
- Accesses are always Quadword (64-bit) cycles on the SDRAM bus.
- Accesses from the StrongARM® Core - byte, word and Lword accesses generated from the StrongARM® Core are supported. Byte, word, and Lword writes result in Read-Modify-Write cycles to SDRAM memory space. Consecutive Lword writes over the AMBA bus to the same Quadword address are buffered and aggregated into Quadword writes to the SDRAM. Read accesses using the Prefetch Memory

address space allow the SDRAM Unit to prefetch Quadword data to be supplied to the AMBA bus using 32-bit burst cycles.

- Accesses from the microengines - the microcode SDRAM instruction defines the number of 64-bit accesses to make, up to 16 Qwords with one microengine command. Only Qword accesses are supported. Less than 8 bytes can be written when using the byte mask within an instruction, but result in R-M-W cycles.

2.4.3 SDRAM Configurations

Table 2: SDRAM Configurations

Total Memory	# of Chips	Size DRAM	Configuration (per bank)	Internal Banks	Bank Bits	RAS Bits	CAS Bits
8 Mbytes	4	16 Mbit	512 K x 16-bit	2	1	11	8
16 Mbytes	8	16 Mbit	1 M x 8-bit	2	1	11	9
32 Mbytes	4	64 Mbit	2 M x 16-bit	2	1	13	8
64 Mbytes	8	64 Mbit	4 M x 8-bit	2	1	13	9
32 Mbytes	4	64 Mbit	1 M x 16-bit	4	2	12	8
64 Mbytes	8	64 Mbit	2 M x 8-bit	4	2	12	9
64 Mbytes	4	128 Mbit	2 M x 16-bit	4	2	12	9
128 Mbytes	8	128 Mbit	4 M x 8-bit	4	2	12	10

2.4.4 SRAM Unit

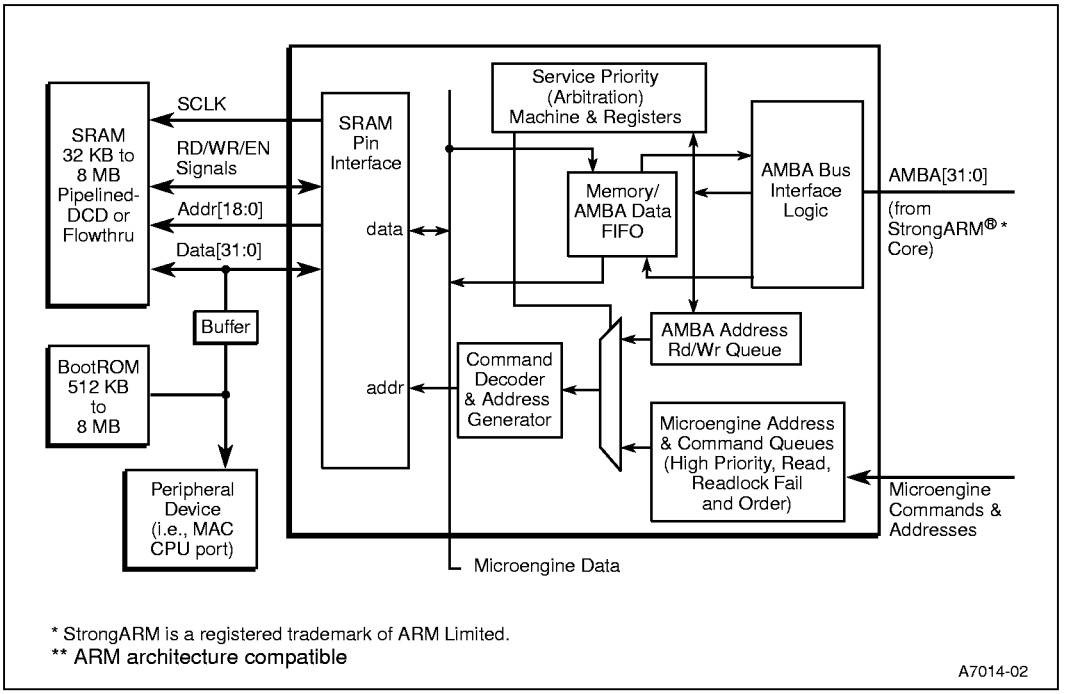
The IXP1200 Network Processor provides an SRAM Unit for very high bandwidth memory for storage of lookup tables and other data for the packet processing microengines. The SRAM Unit controls the SRAM (up to 8 Mbytes), BootROM (up to 8 Mbytes) for booting, and the SlowPort for peripheral device access. The I/O signal timing is determined by internal address decodes and configuration registers for the BootROM and SlowPort address regions. The SRAM Unit includes an 8 entry Push/Pop register list for fast queue operations, bit test, set and clear instructions for atomic bit operations, and an 8 entry CAM for Read Locks.

The SRAM Unit accessed the SRAM via a 32-bit bus operating at one-half the IXP1200 Network Processor core frequency, typically 81 MHz, which provides a peak bandwidth of 334 Mbytes per second.

The SRAM Unit supports both Pipelined Burst and Flowthru SRAM types. The bus is also used to attach BootROM and can be used to interface other peripheral devices such as custom interface logic or MAC management ports. The SRAM interface provides three separate timing domains for the three device types: SRAM, BootROM, and Peripheral (also referred to as SlowPort access).

Figure 5 details the major components of the SRAM Unit.

Figure 5: SRAM Unit Block Diagram



The SRAM bus consists of 19 address bits, 32 data bits, 4 chip enable bits, 8 buffer and read/write control signals, a synchronous output clock (SCLK) running at one-half the IXP1200 Network Processor core frequency, and a synchronous input clock (SACLK). When using Flowthru SRAM types, it is recommended to route the SCLK signal from the SRAMs back to the SACLK input. Routing this trace identically to the DQ data signals will skew the SACLK slightly to track the return data trace propagation delay. When using Pipelined/DCD SRAMs, the SACLK input is not used and may be held inactive with a pulldown to GND to save power.

The SRAM Unit receives memory requests from seven sources: the StrongARM® Core and each of the six microengines. Refer to the *IXP1200 Network Processor Hardware Reference Manual* for details on the prioritization and queues provided for servicing these requests.

2.4.4.1 SRAM Types Supported

Pipeline Burst DCD (double cycle deselect) type: 150 MHz, tKQ=3.8 ns*, 3.3 V

* may be recharacterized to relax specification to 133 MHz, tKQ=4.2 ns

Flowthru type: 94 MHz, tKQmin= 9 ns cycle time, 3.3 V

2.4.4.2 SRAM Configurations

Table 3: SRAM Configurations

Total Memory	# of Chips (Maximum of 8)	Size of SRAM	Device Organization
1 Mbytes	8	1 Mbit	32 K x 32-bit
2 Mbytes	8	2 Mbit	64 K x 32-bit
2 Mbytes	8	2 Mbit	128 K x 16-bit
4 Mbytes	8	4 Mbit	128 K x 32-bit
4 Mbytes	8	4 Mbit	256 K x 16-bit
8 Mbytes (maximum)	8	8 Mbit	256 K x 32-bit

2.4.4.3 BootROM Configurations

Table 4: BootROM Configurations

Total Memory	# of Chips (Maximum of 8)	Size of Boot ROM	Device Organization
512 Kbytes (min)	2	2 Mbit	128 K x 16-bit
2 Mbytes	8	2 Mbit	128 K x 16-bit
4 Mbytes	8	4 Mbit	256 K x 16-bit
6 Mbytes	6	6 Mbit	512 K x 16-bit
8 Mbytes (maximum)	8	8 Mbit	512 K x 16-bit

2.4.4.4 SRAM Bus Access Behavior

- The SRAM controller within the IXP1200 Network Processor will never initiate automatic bursting. Bursting is controlled by the requestor StrongARM® core or microengine) depending on the type and number of SRAM accesses needed.
- Accesses are always Lword 32-bit cycles on the SRAM bus.
- The IXP1200 Network Processor always drives the address for each data cycle. No external address generation or address advance control to SRAM devices is required.
- Accesses from the StrongARM® Core:
  - — Byte, Word and Lword accesses generated from the StrongARM® instructions are supported.
  - — Bit operations are supported via StrongARM® Core accesses to the SRAM Alias Address Space to perform the same operations as a microengine can accomplish implicitly in a microinstruction (Push, Pop, Bit Test and Set, CAM operations, Lock/Unlock, etc.).
  - — Bit, Byte, and Word writes result in Read-Modify-Write cycles.
  - — Declare memory-mapped I/O as non-cachable to prevent line fill burst cycles, and disable caching and write buffering to ensure I/O device coherency.
  - — For best performance, use Lword accesses to avoid R-M-W cycles on the SRAM bus that will occur with byte and word accesses.
- Accesses from the microengines:
  - — The microcode SRAM instruction defines the number of 32-bit accesses to make, up to 8 Dwords with one microengine command.
  - — Only Bit and Dword accesses are supported.
  - — Bit write accesses result in R-M-W cycles.
  - — Unlike the StrongARM® Core, the microengine microinstruction allows you to perform bit operations within the instruction (Push, Pop, Bit Test and Set, CAM operations, Lock/Unlock, etc.).

2.5 PCI Unit

The PCI Unit provides an industry standard 32-bit PCI bus to interface to PCI peripheral devices such as host processors and MAC devices. The PCI Unit supports operating speeds from 33 MHz up to 66 MHz, and is compliant with the *PCI Local Bus Specification, Revision 2.1*. This unit contains:

- Arbitration logic to support up to three PCI bus masters,
- PCI Intelligent I/O (I_2O),
- Two DMA channels
- Four 24-bit timers

Refer to the *IXP1200 Network Processor Hardware Reference Manual* for details on PCI bus behavior for Target and Initiator modes, configuration and register definitions.

The PCI interface is specified to operate from 33 MHz up to 66 MHz. Above 33 MHz operation, two PCI devices are supported only, the IXP1200 Network Processor and a second PCI device. To increase the number of PCI devices supported or to add connectors to the bus at the higher PCI bus speeds, a PCI-to-PCI bridge device, such the Intel 21150, 21152, or 21153 is required.

Both PCI Initiator and Target cycles are supported. As a target device, the IXP1200 Network Processor responds as a Medium Speed device asserting DEVSEL# two PCI_CLK cycles after FRAME# was asserted.

2.6 Device Reset

The IXP1200 Network Processor can be reset by the following:

- Hardware Reset via RESET_IN# pin
- Software Reset by StrongARM® Core or by PCI device write to the RESET_CSR register
- PCI Reset via the PCI_RST# pin
- Watchdog Timer expiration

Refer to the Hardware Reference Manual for complete details of the internal Reset function logic.

2.6.1 Hardware Initiated Reset

The IXP1200 Network Processor provides the RESET_IN# pin so that an external device can reset the IXP1200 Network Processor. Asserting this pin will reset the internal functions as well generate an external reset via the RESET_OUT# pin.

Upon power-up, RESET_IN# must remain asserted for 150 ms after V_{DD} and V_{DDX} are stable to properly reset the IXP1200 Network Processor and ensure that the PXTAL clock input and PLL Clock generator are stable.

While RESET_IN# is asserted, the processor will perform idle cycles. When RESET_IN# is released, the StrongARM® processor will begin execution from address 0. If RESET_IN# is asserted while the StrongARM® Core is executing, the current instruction will terminate abnormally, and the on-chip caches, MMU, and write buffer will be disabled.

2.6.2 Software Initiated Reset

The StrongARM® Core and a device on the PCI Bus can reset specific functions in the IXP1200 Network Processor by writing to the RESET_CSR PCI registers. In most cases, only the individual microengines are reset and the external RESET_OUT# pin will be asserted via this register. The ability to reset the other functions is provided for debugging. The SRAM Unit is always reset when the StrongARM® Core is reset. The StrongARM® Core and the SRAM unit are held in reset for 5000 system clock cycles to ensure a proper reset. The other functions that can be reset via the RESET_CSR PCI registers will be properly reset when consecutive writes are performed to assert and de-assert the reset.

2.6.3 PCI Initiated Reset

The IXP1200 Network Processor can be reset by a device on the PCI bus when the IXP1200 Network Processor is not the PCI Central Function device (PCI_CFG[0] = 0) and PCI_RST# is an input. The entire IXP1200 Network Processor is reset during a PCI Initiated Reset. When the IXP1200 Network Processor is assigned as the PCI Central Function device (PCI_CFG[0] = 1), the IXP1200 Network Processor drives PCI_RST# as an output to the other devices on the PCI bus.

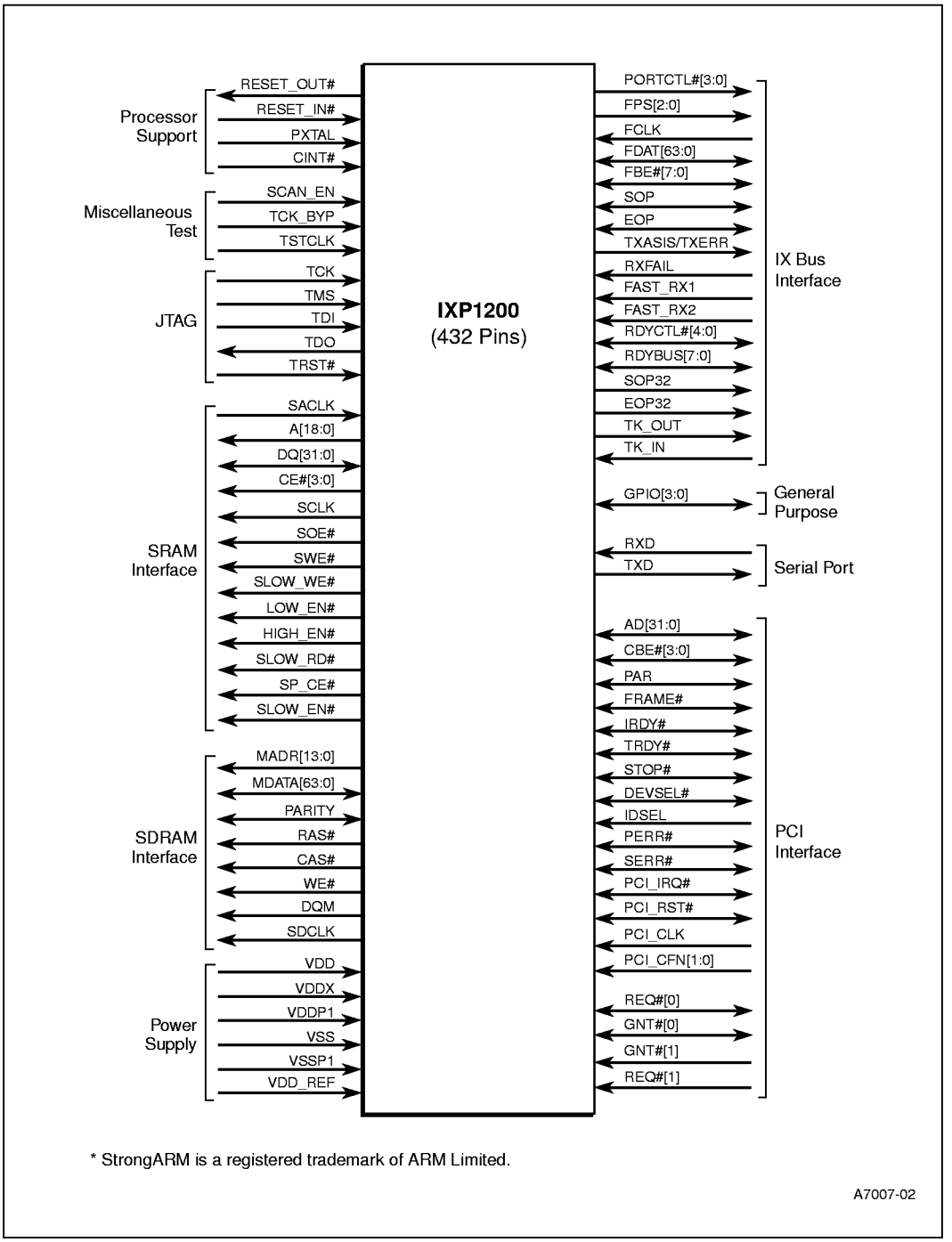
2.6.4 Watchdog Timer Initiated Reset

The IXP1200 Network Processor provides a watchdog timer that can reset the StrongARM® Core. The StrongARM® Core should be programmed to reset the watchdog timer periodically to ensure that the timer does not expire. If the watchdog timer expires, it is assumed the StrongARM® Core has ceased executing instructions properly. The reset generated by the Watchdog Timer will reset each of the functions in the IXP1200 Network Processor. It does not generate an external reset by asserting the RESET_OUT# pin.

SECTION 3 - SIGNAL DESCRIPTION

3.1 Pinout Diagram

Figure 6: Pinout Diagram



3.2 Pin Type Legend

The IXP1200 Network Processor signals are categorized into one of several groups: Processor Support, Miscellaneous/Test, JTAG, SRAM Interface, SDRAM Interface, FIFO Bus Interface, General Purpose, Serial Port, and PCI Interface. Table 5 defines the signal type abbreviations used in the Pin Description section.

Table 5: Signal Type Abbreviations

Signal Type	Description
I	Standard input only. There are 2 types of inputs (I1,I2) for the IXP1200 Network Processor. Refer to Table 27 and Table 28 for more information.
O	Standard output only. There are 4 types of outputs (O1,O2,O3,O4) for the IXP1200 Network Processor. Refer to Table 27 and Table 28 for more information.
TS	Tri-state output.
STS	Sustained tri-state. Active low signal owned and driven by one and only one agent at a time. The agent that drives this pin low must drive it high for at least one clock before letting it float. A new agent cannot start driving this signal any sooner than one clock after the previous owner tri-states it. A pullup is required to sustain the inactive state until another agent drives it, and it must be provided by the central resource (that is, on a PC board).
P	Power Supply.
OD	Standard open drain allows multiple devices to share as a wire-OR. A pullup is required to sustain the inactive state until another agent drives it, and it must be provided by the central resource.

3.3 Pin Description, Grouped by Function

3.3.1 Processor Support Pins

Table 6: Processor Support Pins

Processor Support Signal Names	Pin #	Type	Total	Pin Descriptions
PXTAL	B4	I1	1	Input connection for system oscillator. Typically 3.686 MHz. Drives internal PLL clock generator.
CINT#	Y28	I1	1	External interrupt input to StrongARM® Core.
RESET_OUT#	A5	O4	1	IXP1200 Network Processor System Reset Output. Asserted when: • RESET_IN# is asserted. • PCI arbiter function disabled (PCI_CFN[0]=0) and PCI_RST# is asserted. • A soft reset is initiated.
RESET_IN#	C6	I1	1	IXP1200 Network Processor System Reset Input. If asserted, the IXP1200 Network Processor will perform a system reset and will assert RESET_OUT#. If PCI Central Function is enabled (PCI_CFN[0]=1), PCI_RST# output will also be asserted.
Totals:			4	

3.3.2 SRAM Interface Pins

Table 7: SRAM Interface Pins (Sheet 1 of 2)

SRAM Interface Signal Names	Pin #	Type	Total	Pin Descriptions
A[18:0]				
[18]	A28			
[17]	B28			
[16]	D27			
[15]	E28			
[14]	D30			
[13]	D31			
[12]	E29			
[11]	F28			
[10]	E30	O4	19	Address outputs
[9]	E31			
[8]	F29			
[7]	F30			
[6]	F31			
[5]	G29			
[4]	H28			
[3]	G30			
[2]	G31			
[1]	H29			
[0]	J28			
DQ[31:0]				
[31]	H30			
[30]	J30			
[29]	J31			
[28]	K29			
[27]	L28			
[26]	K30			
[25]	K31			
[24]	L29			
[23]	M28			
[22]	L30			
[21]	L31			
[20]	M29			
[19]	N28			
[18]	M30			
[17]	M31			
[16]	N29	I1/O4	32	32 Bidirectional data signals
[15]	N30			
[14]	N31			
[13]	P29			
[12]	R28			
[11]	P30			
[10]	R29			
[9]	R30			
[8]	R31			
[7]	T28			
[6]	T29			
[5]	T30			
[4]	T31			
[3]	U29			
[2]	U28			
[1]	V30			
[0]	V29			
CE#[3:0]				
[3]	A26			
[2]	B26	O4	4	SRAM bus chip enable outputs.
[1]	C26			
[0]	A27			

Table 7: SRAM Interface Pins (Sheet 2 of 2)

SRAM Interface Signal Names	Pin #	Type	Total	Pin Descriptions
SCLK	W31	O3	1	SRAM Clock - Frequency is one half the speed of the core clock (½ * Fcore).
SACLK	B24	I1	1	SRAM clock input, used to compensate for skew in data path when using Flowthru SRAMs. Must be connected to SCLK when using Flowthru devices. Not used with Pipelined devices and should be pulled low.
SOE#	W30	O4	1	SRAM output enable.
SWE#	Y30	O4	1	SRAM write enable.
SLOW_WE#	W28	O4	1	Slow asynchronous interface write enable (Flash, ROM or MAC).
LOW_EN#	D26	O4	1	Low order SRAM bank enable and buffer direction select for slow interface. When used as the buffer direction select: 0 = write and 1 = read.
HIGH_EN#	C27	O4	1	High order SRAM bank enable.
SLOW_EN#	Y29	O4	1	Slow device enable: 0 = Slow device (BootROM or SlowPort), 1=SRAM.
SP_CE#	W29	O4	1	Slow asynchronous interface chip enable output.
SLOW_RD#	Y31	O4	1	Slow asynchronous interface read enable output.
Totals:			65	

3.3.3 SDRAM Interface Pins

Table 8: SDRAM Interface Pins (Sheet 1 of 2)

SDRAM Interface Signal Names	Pin #	Type	Total	Pin Descriptions
MADR[13:0]				
[13]	AD1			
[12]	AC3			
[11]	AC2			
[10]	AC1			
[9]	AB3			
[8]	AA4			
[7]	AB2	O4	14	Multiplexed Row/Column address outputs.
[6]	AB1			
[5]	AA3			
[4]	AA1			
[3]	Y3			
[2]	W4			
[1]	Y2			
[0]	Y1			
MDATA[63:0]				
[63]	AH6			
[62]	AJ5			
[61]	AL4			
[60]	AK4			
[59]	AH5			
[58]	AH2			
[57]	AH1			
[56]	AG3			
[55]	AF4			
[54]	AG2			
[53]	AG1			
[52]	AF3			
[51]	AF2			
[50]	AF1			
[49]	AE3			
[48]	AD4			
[47]	AE2			
[46]	AE1			
[45]	U4	I1/O1	64	64 Bidirectional data signals.
[44]	V2			
[43]	U3			
[42]	U2			
[41]	U1			
[40]	T4			
[39]	T3			
[38]	T2			
[37]	T1			
[36]	R3			
[35]	R4			
[34]	P2			
[33]	P3			
[32]	N1			
[31]	N2			
[30]	N3			
[29]	M1			
[28]	M2			
[27]	N4			
[26]	M3			

Table 8: SDRAM Interface Pins (Sheet 2 of 2)

SDRAM Interface Signal Names	Pin #	Type	Total	Pin Descriptions
[25] [24] [23] [22] [21] [20] [19] [18] [17] [16] [15] [14] [13] [12] [11] [10] [9] [8] [7] [6] [5] [4] [3] [2] [1] [0]	L1 L2 M4 L3 K1 K3 J1 J2 J3 H1 H2 J4 H3 G1 G2 H4 G3 F1 F2 F3 E1 E2 F4 E3 D1 D2			
RAS#	W2	O4	1	Row Address Select output. Precharge cycle indicated if asserted with WE#.
CAS#	W3	O4	1	Column Address Select output.
WE#	W1	O4	1	Write Enable output.
DQM	V3	O4	1	Data Buffer Direction Control output.
PARITY	AK5	I1/O1	1	Bidirectional Data Parity bit. Pullup if not used.
SDCLK	AD2	O3	1	SDRAM Clock output. Frequency is one half the speed of the core clock (½ * Fcore).
Totals:			84	

3.3.4 IX Bus Interface Pins

Table 9: IX Bus Interface Pins (Sheet 1 of 4)

IX Bus Signal Names	Pin #	Type	Total	Pin Descriptions
FCLK	AB30	I1	1	IX Bus Clock input. All IX Bus transfers are synchronized to this clock. Typical operating frequency 33 MHz - 66 MHz.
PORTCTL#[3:0] [3] [2] [1] [0]	 AC30 AC31 AB29 AA28	O1/TS	4	Port Control outputs. Used to select the transmit and/or receive mode for IX Bus devices, typically MAC devices. In 64-bit bidirectional IX Bus mode, this is a 4-bit bus used to select both transmit and receive modes. In 32-bit unidirectional IX Bus mode, bits [1:0] are used to select the receive port and bits [3:2] are used to select the transmit port. In a shared IX Bus system, these pins will be tri-stated when the current master yields the IX Bus.
FPS[2:0] [2] [1] [0]	 AC29 AD31 AD30	O4/TS	3	MAC Port Select outputs. In 64-bit bidirectional IX Bus mode, it is used to select one of eight MAC ports from a MAC device. In 32-bit unidirectional IX Bus mode, it is used to select one of eight MAC receive ports from the selected MAC device (GPIO[3:1] used for transmit port select). See IX Bus control signal decode tables. In a shared IX Bus system, these pins will be tri-stated when the current master yields the IX Bus.
FDAT[63:0] [63] [62] [61] [60] [59] [58] [57] [56] [55] [54] [53] [52] [51] [50] [49] [48] [47] [46] [45] [44] [43] [42] [41] [40] [39] [38] [37] [36] [35] [34] [33] [32] [31]	 AC28 AD29 AE31 AE30 AF31 AF30 AF29 AG31 AG30 AF28 AG29 AH31 AH30 AH27 AK28 AL28 AJ27 AH26 AK27 AL27 AJ26 AK26 AL26 AJ25 AH24 AK25 AL25 AJ24 AH23 AK24 AL24 AJ23 AK23	I2/O2/TS	64	IX Data Bus. One 64 bit bus in bidirectional IX Bus mode. Two 32-bit buses in unidirectional IX Bus mode where bits [63:32] are used for Transmit Data output and [31:0] are used for Receive Data inputs. In a shared IX Bus system, these pins will be tri-stated when the current master yields the IX Bus.

Table 9: IX Bus Interface Pins (Sheet 2 of 4)

IX Bus Signal Names	Pin #	Type	Total	Pin Descriptions
[30] [29] [28] [27] [26] [25] [24] [23] [22] [21] [20] [19] [18] [17] [16] [15] [14] [13] [12] [11] [10] [9] [8] [7] [6] [5] [4] [3] [2] [1] [0]	AL23 AJ22 AH21 AK22 AL22 AJ21 AH20 AK21 AL21 AJ20 AH19 AK20 AL20 AJ19 AK19 AL19 AJ18 AH17 AK18 AJ17 AK17 AL17 AH16 AJ16 AK16 AL16 AJ15 AH15 AK14 AJ14 AL13			
FBE#[7:0] [7] [6] [5] [4] [3] [2] [1] [0]	 AK13 AJ13 AL12 AK12 AH13 AJ12 AL11 AK11	I2/O2/ TS	8	Bidirectional Byte Enables. One 8-bit bus in 64-bit bidirectional IX Bus mode. Two 4-bit buses in 32-bit unidirectional IX Bus mode where bits [7:4] are used for Transmit Byte Enables and [3:0] used for Receive Byte Enables. In a shared IX Bus system, these pins will be tri-stated when the current master yields the IX Bus.
TXASIS/TXERR	AL10	O4/TS	1	Transmit As Is/Transmit Error output. When asserted on the first data transfer of a transmit packet, indicates to the MAC not to pad or append CRC bytes to the packet, even if the ports were programmed to do so. When asserted on the final data transfer along with EOP, the MAC should transmit the packet with an MII error (if programmed) and a symbol error. In a shared IX Bus system, these pins will be tri-stated when the current master yields the IX Bus.
RXFAIL	AK10	I1/O1/ TS	1	Receive Packet Failure. As Input, asserted by a MAC device if a packet was received with errors. Mimics the behavior of EOP to terminate an IX Bus cycle. As Output, driven when no receive cycle in-progress. In a shared IX Bus system, these pins will be tri-stated when the current master yields the IX Bus.
FAST_RX1	AH11	I1	1	Ready Input from Fast MAC port 1 (i.e. Gigabit port).
FAST_RX2	AJ10	I1	1	Ready Input from Fast MAC port 2 (i.e. Gigabit port).

Table 9: IX Bus Interface Pins (Sheet 3 of 4)

IX Bus Signal Names	Pin #	Type	Total	Pin Descriptions
RDYCTL#[4:0] [4] [3] [2] [1] [0]	 AK6 AL6 AJ7 AH8 AK7	I1/O4/ TS	5	Bidirectional Ready Control signals. In 64-bit Bidirectional IX Bus Mode: • 1-2 MAC mode: Bits [3:0] are used to enable the transmit or receive FIFO Ready Flags and bit [4] is used as a flow control enable for MAC 2 (GPIO[0] is used as a flow control enable for MAC 1). • 3+ MAC mode: The transmit and receive FIFO Ready, the flow control, and inter-processor communication enables are decoded from all five bits. • In a shared IX Bus system the IXP1200 Network Processor Ready Bus Master drives this bus. IXP1200 Network Processor slave devices snoop these pins as inputs. In 32-bit Unidirectional Mode: • 1-2 MAC mode: Bits [3:0] are used to enable the transmit or receive FIFO Ready Flags and bit [4] is used as a flow control enable for MAC 1. GPIO[0] is used as a flow control enable for MAC 0. • 3+ MAC mode: Bits [3:0] are used to enable the FIFO Ready Flags, enable shared IX Bus communications, and enable flow control inputs. Bit [4] is used as an active low enable for an external decoder for the PORTCTL[1:0] signals.
RDYBUS[7:0] [7] [6] [5] [4] [3] [2] [1] [0]	 AL9 AK9 AJ9 AL8 AK8 AH9 AJ8 AL7	I1/O4	8	Bidirectional Ready Bus data. • Inputs the Transmit and Receive Ready Flags from IX Bus devices. • Outputs flow control data to IX Bus devices. • Shared IX Bus I/O data bus. In a shared IX Bus system, the Ready Bus Master drives this bus and the Slave snoops.
SOP	AH12	I1/O4/ TS	1	Start of Packet indication. • Input in 32-bit unidirectional IX Bus mode. • Input/Output in 64-bit bidirectional IX Bus mode. • In a shared IX Bus system, this pin will be tri-stated when the current master yields the IX Bus.
EOP	AJ11	I1/O4/ TS	1	End of Packet indication. • Input in 32-bit unidirectional IX Bus mode. • Input/Output in 64-bit bidirectional IX Bus mode. • In a shared IX Bus system, this pin will be tri-stated when the current master yields the IX Bus.
SOP32	AJ6	O4	1	Transmit Start Of Packet indication. • Output in 32-bit unidirectional IX Bus modes. • 64-bit bidirectional 3+ MAC mode, is IX Bus Request output indication. • 64-bit bidirectional 1-2 MAC mode, not used in and should be left unconnected. • In shared IX Bus mode, used as IX Bus Request output.

Table 9: IX Bus Interface Pins (Sheet 4 of 4)

IX Bus Signal Names	Pin #	Type	Total	Pin Descriptions
EOP32	AL5	I1/O4	1	Transmit End Of Packet. • 32-bit unidirectional IX Bus modes, Transmit End Of Packet indication. • 64-bit bidirectional IX Bus modes, single-chip operation, this input should be pulled high. • In shared IX Bus mode, as an input indicates IX Bus Request Pending from another device.
TK_OUT	AA29	O1	1	Token Output. Used to pass ownership of the IX Bus in a shared IX Bus system in 64-bit bidirectional IX Bus mode. In 32-bit unidirectional mode this bit is unused and should be left unconnected.
TK_IN	AB31	I1	1	Token Input. 64-bit bidirectional IX Bus Mode: If asserted, this device has been given ownership of the IX Bus in a shared IX Bus system. During Reset, used to configure the device as Initial IX Bus Master. 1= device is Initial Master, 0= device is slave. In 32-bit unidirectional mode this input is not used and should be pulled high.
Totals:			103	

3.3.5 General Purpose I/Os

Table 10: General Purpose I/Os

General Purpose I/O Signal Names	Pin #	Type	Total	Pin Descriptions
GPIO[3:1] [3] [2] [1]	 A25 B25 D24	I1/O4	3	Bidirectional General Purpose pins. Bidirectional IX Bus mode: Accessible by StrongARM® Core. Configurable as Input or Output. Unidirectional IX Bus mode: Dedicated to IX Bus Interface, used as an output for Transmit Port selects [2:0].
GPIO[0]	C25	I1/O4	1	Bidirectional General Purpose I/O pin. 1-2 MAC mode (Uni or Bidirectional mode): Dedicated to the FBI unit. Is output for Flow Control indication to MAC 0. 3+ MAC 64-bit Bidirectional IX Bus mode: Accessible to the StrongARM® Core. Configurable as Input or Output. 3+ MAC 32-bit Unidirectional IX Bus mode: Output dedicated to the FBI Unit. Active low enable for an external PORTCTL[3:2] decoder.
Totals:			4	

3.3.6 Serial Port (UART) Pins

Table 11: Serial Port (UART) Pins

Serial Port (UART) Signal Names	Pin #	Type	Total	Pin Descriptions
RXD	D23	I1	1	UART Receive data.
TXD	C24	O1	1	UART Transmit data.
Totals:			2	

3.3.7 PCI Interface Pins

Table 12: PCI Interface Pins (Sheet 1 of 3)

PCI Interface Signal Names	Pin #	Type	Total	Pin Descriptions
AD[31:0] [31] [30] [29] [28] [27] [26] [25] [24] [23] [22] [21] [20] [19] [18] [17] [16] [15] [14] [13] [12] [11] [10] [9] [8] [7] [6] [5] [4] [3] [2] [1] [0]	 B20 A20 C19 C18 B18 D17 C17 A16 D16 A15 B15 C15 B14 D15 C14 A13 A10 B10 D11 C10 A9 B9 C9 A8 D9 C8 A7 B7 D8 C7 A6 B6	I2/ O2/ TS	32	Address/data. These signals are multiplexed address and data bus. The IXP1200 Network Processor receives addresses as target and drives addresses as master. It receives write data and drives read data as target. It drives write data and receives read data as master.
CBE#[3:0] [3] [2] [1] [0]	 B16 B13 C11 B8	I2/ O2/ TS	4	Command byte enables. These signals are multiplexed command and byte enable signals. The IXP1200 Network Processor receives commands as target and drives commands as master. It receives byte enables as target and drives byte enables as master.
PAR	D12	I2/ O2/ TS	1	Parity. This signal carries even parity for AD and CBE# pins. It has the same receive and drive characteristics as the address and data bus, except that it is one PCI cycle later.

Table 12: PCI Interface Pins (Sheet 2 of 3)

PCI Interface Signal Names	Pin #	Type	Total	Pin Descriptions
FRAME#	C13	I2/ O2/ STS	1	FRAME# indicates the beginning and duration of an access. The IXP1200 Network Processor receives as target and drives as master.
IRDY#	A12	I2/ O2/ STS	1	Initiator ready. Indicates the master's ability to complete the current data phase of the transaction. The IXP1200 Network Processor receives as target and drives as master.
TRDY#	B12	I2/ O2/ STS	1	Target ready. Indicates the target's ability to complete the current data phase of the transaction. The IXP1200 Network Processor drives as target and receives as master.
STOP#	C12	I2/ O2/ STS	1	Stop. Indicates that the target is requesting the master to stop the current transaction. The IXP1200 Network Processor drives as target and receives as master.
DEVSEL#	D13	I2/ O2/ STS	1	Device Select. Indicates that the target has decoded its address as the target of the current access. The IXP1200 Network Processor drives as target and receives as initiator.
IDSEL	C16	I2	1	Initialization Device Select. Used as Chip Select during PCI Configuration Space read and write transactions.
PERR#	A11	I2/O2/ STS	1	Parity error. Used to report data parity errors. The IXP1200 Network Processor asserts this when it receives bad data parity as target of a write or master of a read.
SERR#	B11	I2/ O2/ OD	1	System Error. As an input, it can cause an interrupt to the StrongARM® Core if the IXP1200 Network Processor is selected for PCI Central Function support (PCI_CFN[0]=1). As an output it can be asserted by the IXP1200 Network Processor by writing the SERR bit in the PCI control register, or in response to a PCI address parity error when not providing PCI Central Function support (PCI_CFN[0]=0).
PCI_IRQ#	A22	I2/O2/ OD	1	PCI Interrupt Request. As output, used to interrupt the PCI Host Processor. It is asserted when there is a doorbell set or there are messages on the I_2O outbound post list. This is usually connected to INTA# on the PCI bus. As Input, It is asserted when there is a doorbell set or there are messages on the I 2 O outbound post list.
PCI_RST#	C21	I2/ O2/ TS	1	PCI Reset. • When providing PCI Central Function support (PCI_CFN[0]=1), PCI _RST# is an output controlled by the StrongARM® Core. Used to reset the PCI Bus. • When not providing PCI Central Function (PCI_CFN[0]=0), PCI_RST# is an input, and when asserted resets the IXP1200 Network Processor StrongARM® Core, all registers, all transaction queues, and all PCI related state.
PCI_CLK	D20	I2	1	PCI Clock input. Reference for PCI signals and internal operations. PCI clock is typically 33 or 66 MHz.

Table 12: PCI Interface Pins (Sheet 3 of 3)

PCI Interface Signal Names	Pin #	Type	Total	Pin Descriptions
PCI_CFN[0]	A24	I2	1	PCI Central Function select input. When PCI_CFN[0]=1, the IXP1200 Network Processor provides the PCI Central Function support and: • PCI_RST# is an output asserted by the PCI unit when initiated by the StrongARM® Core. • IXP1200 Network Processor provides bus parking during reset. • SERR# is an input, when asserted will generate an interrupt to the StrongARM® Core. When PCI_CFN[0]=0, PCI central function is disabled and: • PCI_RST# is an input asserted by the Host processor. • The IXP1200 Network Processor does not provide bus parking during reset.
PCI_CFN[1]	C23	I2	1	PCI Arbitration Enable, PCI_CFN[1] When PCI_CFN[1]=1, enables the internal PCI arbiter to perform bus arbitration. When PCI_CFN[1]=0, disables internal PCI bus arbiter.
GNT#[0]	B21	I2/O2	1	PCI Bus Master Grant 1. Internal PCI arbiter is enabled (PCI_CFN[1] = 1): Pin is an output to grant a PCI device 1 control of the PCI bus. (The IXP1200 Network Processor is PCI device 0 in this case) Internal PCI arbiter is disabled (PCI_CFN[1] = 0): Pin is an input that indicates that the IXP1200 Network Processor can assert FRAME# and become the bus master. If the IXP1200 Network Processor is idle when GNT#[0] is asserted, it parks the PCI bus.
REQ#[0]	A21	I2/O2	1	PCI Bus Master Request 1. Internal PCI arbiter is enabled (PCI_CFN[1] = 1): Pin is an input indicating an external PCI device is requesting use of the PCI bus. Internal PCI arbiter is disabled (PCI_CFN[1] = 0): Pin is an output indicating that the IXP1200 Network Processor is requesting use of the PCI bus.
GNT#[1]	C20	I2/O2	1	PCI Bus Master Grant 2. Internal PCI arbiter is enabled (PCI_CFN[1] = 1): Pin is an output to grant a PCI device 2 control of the PCI bus (The IXP1200 Network Processor is PCI device 0 in this case.) When Internal PCI arbiter is disabled (PCI_CNF[1]=0, GNT#[1] should be connected to GND through a pulldown resistor of 10 KOhms.
REQ#[1]	D19	I2/O2	1	PCI Bus Master Request 2. Internal PCI arbiter is enabled (PCI_CFN[1] = 0): This input indicates that PCI device 2 is requesting to take control of the PCI bus. When Internal PCI arbiter is disabled (PCI_CFN[1] = 0), REQ#[1] is undefined and should be tied to VDDX through a pullup resistor of 10 KOhms.
Totals:			54	

3.3.8 Power Supply Pins

Table 13: Power Supply Pins

Supply Signal Names	Pin #	Type	Total	Pin Descriptions
VDD		P	17	IXP1200 Network Processor Core supply (2 V).
	A19, B19, B27, H31, J29, K2, L4, Y4, AA2, AA30, AA31, AC4, AD3, AD28, AE29, AG4, AG28			
Total VDD pins			17	
VDDX		P	40	IXP1200 Network Processor I/O supply (3.3 V).
	A1, A31,B2, B30, C3, C29, D4, D7, D10, D14, D18, D22, D25, D28, G4, G28, K4, K28, P4, P28, V4, V28, AB4, AB28, AE4, AE28, AH4, AH7, AH10, AH14, AH18, AH22, AH25, AH28, AJ3, AJ29, AK2, AK30, AL1, AL31			
Total VDDX pins			40	
VDD_REF	E4	P	1	IXP1200 Network Processor 3.3 V reference - used to bias the ESD circuitry Can be tied directly to VDDX external to chip.
VSSP1	A4	P	1	IXP1200 Network Processor PLL ground Can be tied directly to VSS external to chip.
VDDP1	D5	P	1	IXP1200 Network Processor PLL supply (2 V) typical. Can be tied directly to VDD external to chip.
Total			3	
VSS		P	48	IXP1200 Network Processor ground.
	A2, A3, A14, A17, A18, A29, A30, B1, B3, B17, B29, B31, C1, C2, C4, C28, C30, C31, D3, D29, P1, P31, R1, R2, U30, U31, V1, V31, AH3, AH29, AJ1, AJ2, AJ4, AJ28, AJ30, AJ31, AK1, AK3, AK15, AK29, AK31, AL2, AL3, AL14, AL15, AL18, AL29, AL30			
Total VSS pins			48	
Total Power Supply Pins			108	

3.3.9 JTAG Interface Pins

Table 14: JTAG Interface Pins

JTAG Interface Pin Name	Pin #	Type	Total	Pin Description
TCK	A23	I1	1	Test Interface reference clock. This clock times all the transfers on the JTAG test interface.
TMS	C22	I1	1	Test Interface mode select. Causes state transitions on the test access port (TAP) controller.
TDI	B22	I1	1	Test Interface data input. The serial input through which JTAG instructions and test data enter the JTAG interface.
TDO	D21	O1	1	Test Interface data output. The serial output through which test instruction and data from the test logic leave the IXP1200 Network Processor.
TRST#	B23	I1	1	Test Interface RESET. When asserted low, the TAP controller is asynchronously forced to enter a reset state, and disables the JTAG port. This pin must be driven or held low to achieve normal device operation.
Totals:			5	

3.3.10 Miscellaneous Test Pins

Table 15: Miscellaneous Test Pins

Processor Support Signal Names	Pin #	Type	Total	Pin Descriptions
SCAN_EN	C5	I1	1	For test purposes only. Used to enable internal scan chains for chip testing. This pin should be connected to ground through a pulldown resistor.
TCK_BYP	D6	I1	1	For test purposes only. Bypass PPL for Test/debug.
TSTCLK	B5	I1	1	For test purposes only. Used as clock input when bypassing the internal PPL clock generator. For Normal operation, this pin should be connected to ground through a 10 KOhm pulldown resistor.
Totals:			3	

3.3.11 Pin Usage Summary

Table 16: Pin Usage Summary

Type	Quantity
Inputs	21
Outputs	68
Bidirectional	235
Total Signal	324
Power	108
Overall Totals:	432

3.4 Pin/Signal List

Table 17: Pin Table in Pin Order (Sheet 1 of 4)

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
A1	VDDX	B1	VSS	C1	VSS
A2	VSS	B2	VDDX	C2	VSS
A3	VSS	B3	VSS	C3	VDDX
A4	VSSP1	B4	PXTAL	C4	VSS
A5	RESET_OUT#	B5	TSTCLK	C5	SCAN_EN
A6	AD[1]	B6	AD[0]	C6	RESET_IN#
A7	AD[5]	B7	AD[4]	C7	AD[2]
A8	AD[8]	B8	CBE#[0]	C8	AD[6]
A9	AD[11]	B9	AD[10]	C9	AD[9]
A10	AD[15]	B10	AD[14]	C10	AD[12]
A11	PERR#	B11	SERR#	C11	CBE#[1]
A12	IRDY#	B12	TRDY#	C12	STOP#
A13	AD[16]	B13	CBE#[2]	C13	FRAME#
A14	VSS	B14	AD[19]	C14	AD[17]
A15	AD[22]	B15	AD[21]	C15	AD[20]
A16	AD[24]	B16	CBE#[3]	C16	IDSEL
A17	VSS	B17	VSS	C17	AD[25]
A18	VSS	B18	AD[27]	C18	AD[28]
A19	VDD	B19	VDD	C19	AD[29]
A20	AD[30]	B20	AD[31]	C20	GNT#[1]
A21	REQ#[0]	B21	GNT#[0]	C21	PCI_RST#
A22	PCI_IRQ#	B22	TDI	C22	TMS
A23	TCK	B23	TRST#	C23	PCI_CFN[1]
A24	PCI_CFN[0]	B24	SACLK	C24	TXD
A25	GPIO[3]	B25	GPIO[2]	C25	GPIO[0]
A26	CE#[3]	B26	CE#[2]	C26	CE#[1]
A27	CE#[0]	B27	VDD	C27	HIGH_EN#
A28	A[18]	B28	A[17]	C28	VSS
A29	VSS	B29	VSS	C29	VDDX
A30	VSS	B30	VDDX	C30	VSS
A31	VDDX	B31	VSS	C31	VSS
D1	MDATA[1]	E1	MDATA[5]	J1	MDATA[19]
D2	MDATA[0]	E2	MDATA[4]	J2	MDATA[18]
D3	VSS	E3	MDATA[2]	J3	MDATA[17]
D4	VDDX	E4	VDD_REF	J4	MDATA[14]
D5	VDDP1	E28	A[15]	J28	A[0]

Table 17: Pin Table in Pin Order (Sheet 2 of 4)

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
D6	TCK_BYP	E29	A[12]	J29	VDD
D7	VDDX	E30	A[10]	J30	DQ[30]
D8	AD[3]	E31	A[9]	J31	DQ[29]
D9	AD[7]	F1	MDATA[8]	K1	MDATA[21]
D10	VDDX	F2	MDATA[7]	K2	VDD
D11	AD[13]	F3	MDATA[6]	K3	MDATA[20]
D12	PAR	F4	MDATA[3]	K4	VDDX
D13	DEVSEL#	F28	A[11]	K28	VDDX
D14	VDDX	F29	A[8]	K29	DQ[28]
D15	AD[18]	F30	A[7]	K30	DQ[26]
D16	AD[23]	F31	A[6]	K31	DQ[25]
D17	AD[26]	G1	MDATA[12]	L1	MDATA[25]
D18	VDDX	G2	MDATA[11]	L2	MDATA[24]
D19	REQ#[1]	G3	MDATA[9]	L3	MDATA[22]
D20	PCI_CLK	G4	VDDX	L4	VDD
D21	TDO	G28	VDDX	L28	DQ[27]
D22	VDDX	G29	A[5]	L29	DQ[24]
D23	RXD	G30	A[3]	L30	DQ[22]
D24	GPIO[1]	G31	A[2]	L31	DQ[21]
D25	VDDX	H1	MDATA[16]	M1	MDATA[29]
D26	LOW_EN#	H2	MDATA[15]	M2	MDATA[28]
D27	A[16]	H3	MDATA[13]	M3	MDATA[26]
D28	VDDX	H4	MDATA[10]	M4	MDATA[23]
D29	VSS	H28	A[4]	M28	DQ[23]
D30	A[14]	H29	A[1]	M29	DQ[20]
D31	A[13]	H30	DQ[31]	M30	DQ[18]
		H31	VDD	M31	DQ[17]
N1	MDATA[32]	U1	MDATA[41]	AA1	MADR[4]
N2	MDATA[31]	U2	MDATA[42]	AA2	VDD
N3	MDATA[30]	U3	MDATA[43]	AA3	MADR[5]
N4	MDATA[27]	U4	MDATA[45]	AA4	MADR[8]
N28	DQ[19]	U28	DQ[2]	AA28	PORTCTL#[0]
N29	DQ[16]	U29	DQ[3]	AA29	TK_OUT
N30	DQ[15]	U30	VSS	AA30	VDD
N31	DQ[14]	U31	VSS	AA31	VDD
P1	VSS	V1	VSS	AB1	MADR[6]
P2	MDATA[34]	V2	MDATA[44]	AB2	MADR[7]
P3	MDATA[33]	V3	DQM	AB3	MADR[9]

Table 17: Pin Table in Pin Order (Sheet 3 of 4)

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
P4	VDDX	V4	VDDX	AB4	VDDX
P28	VDDX	V28	VDDX	AB28	VDDX
P29	DQ[13]	V29	DQ[0]	AB29	PORTCTL#[1]
P30	DQ[11]	V30	DQ[1]	AB30	FCLK
P31	VSS	V31	VSS	AB31	TK_IN
R1	VSS	W1	WE#	AC1	MADR[10]
R2	VSS	W2	RAS#	AC2	MADR[11]
R3	MDATA[36]	W3	CAS#	AC3	MADR[12]
R4	MDATA[35]	W4	MADR[2]	AC4	VDD
R28	DQ[12]	W28	SLOW_WE#	AC28	FDAT[63]
R29	DQ[10]	W29	SP_CE#	AC29	FPS[2]
R30	DQ[9]	W30	SOE#	AC30	PORTCTL#[3]
R31	DQ[8]	W31	SCLK	AC31	PORTCTL#[2]
T1	MDATA[37]	Y1	MADR[0]	AD1	MADR[13]
T2	MDATA[38]	Y2	MADR[1]	AD2	SDCLK
T3	MDATA[39]	Y3	MADR[3]	AD3	VDD
T4	MDATA[40]	Y4	VDD	AD4	MDATA[48]
T28	DQ[7]	Y28	CINT#	AD28	VDD
T29	DQ[6]	Y29	SLOW_EN#	AD29	FDAT[62]
T30	DQ[5]	Y30	SWE#	AD30	FPS[0]
T31	DQ[4]	Y31	SLOW_RD#	AD31	FPS[1]
AE1	MDATA[46]	AH9	RDYBUS[2]	AJ10	FAST_RX2
AE2	MDATA[47]	AH10	VDDX	AJ11	EOP
AE3	MDATA[49]	AH11	FAST_RX1	AJ12	FBE#[2]
AE4	VDDX	AH12	SOP	AJ13	FBE#[6]
AE28	VDDX	AH13	FBE#[3]	AJ14	FDAT[1]
AE29	VDD	AH14	VDDX	AJ15	FDAT[4]
AE30	FDAT[60]	AH15	FDAT[3]	AJ16	FDAT[7]
AE31	FDAT[61]	AH16	FDAT[8]	AJ17	FDAT[11]
AF1	MDATA[50]	AH17	FDAT[13]	AJ18	FDAT[14]
AF2	MDATA[51]	AH18	VDDX	AJ19	FDAT[17]
AF3	MDATA[52]	AH19	FDAT[20]	AJ20	FDAT[21]
AF4	MDATA[55]	AH20	FDAT[24]	AJ21	FDAT[25]
AF28	FDAT[54]	AH21	FDAT[28]	AJ22	FDAT[29]
AF29	FDAT[57]	AH22	VDDX	AJ23	FDAT[32]
AF30	FDAT[58]	AH23	FDAT[35]	AJ24	FDAT[36]
AF31	FDAT[59]	AH24	FDAT[39]	AJ25	FDAT[40]
AG1	MDATA[53]	AH25	VDDX	AJ26	FDAT[43]

Table 17: Pin Table in Pin Order (Sheet 4 of 4)

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
AG2	MDATA[54]	AH26	FDAT[46]	AJ27	FDAT[47]
AG3	MDATA[56]	AH27	FDAT[50]	AJ28	VSS
AG4	VDD	AH28	VDDX	AJ29	VDDX
AG28	VDD	AH29	VSS	AJ30	VSS
AG29	FDAT[53]	AH30	FDAT[51]	AJ31	VSS
AG30	FDAT[55]	AH31	FDAT[52]	AK1	VSS
AG31	FDAT[56]	AJ1	VSS	AK2	VDDX
AH1	MDATA[57]	AJ2	VSS	AK3	VSS
AH2	MDATA[58]	AJ3	VDDX	AK4	MDATA[60]
AH3	VSS	AJ4	VSS	AK5	PARITY
AH4	VDDX	AJ5	MDATA[62]	AK6	RDYCTL#[4]
AH5	MDATA[59]	AJ6	SOP32	AK7	RDYCTL#[0]
AH6	MDATA[63]	AJ7	RDYCTL#[2]	AK8	RDYBUS[3]
AH7	VDDX	AJ8	RDYBUS[1]	AK9	RDYBUS[6]
AH8	RDYCTL#[1]	AJ9	RDYBUS[5]	AK10	RXFAIL
AK11	FBE#[0]	AL1	VDDX	AL22	FDAT[26]
AK12	FBE#[4]	AL2	VSS	AL23	FDAT[30]
AK13	FBE#[7]	AL3	VSS	AL24	FDAT[33]
AK14	FDAT[2]	AL4	MDATA[61]	AL25	FDAT[37]
AK15	VSS	AL5	EOP32	AL26	FDAT[41]
AK16	FDAT[6]	AL6	RDYCTL#[3]	AL27	FDAT[44]
AK17	FDAT[10]	AL7	RDYBUS[0]	AL28	FDAT[48]
AK18	FDAT[12]	AL8	RDYBUS[4]	AL29	VSS
AK19	FDAT[16]	AL9	RDYBUS[7]	AL30	VSS
AK20	FDAT[19]	AL10	TXASIS	AL31	VDDX
AK21	FDAT[23]	AL11	FBE#[1]		
AK22	FDAT[27]	AL12	FBE#[5]		
AK23	FDAT[31]	AL13	FDAT[0]		
AK24	FDAT[34]	AL14	VSS		
AK25	FDAT[38]	AL15	VSS		
AK26	FDAT[42]	AL16	FDAT[5]		
AK27	FDAT[45]	AL17	FDAT[9]		
AK28	FDAT[49]	AL18	VSS		
AK29	VSS	AL19	FDAT[15]		
AK30	VDDX	AL20	FDAT[18]		
AK31	VSS	AL21	FDAT[22]		

3.5 Signals Listed in Alphabetical Order

Table 18: Pin Table in Alphabetical Order (Sheet 1 of 4)

Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
A[0]	J28	FDAT[42]	AK26	RDYCTL#[4]	AK6
A[1]	H29	FDAT[43]	AJ26	REQ#[0]	A21
A[10]	E30	FDAT[44]	AL27	REQ#[1]	D19
A[11]	F28	FDAT[45]	AK27	RESET_IN#	C6
A[12]	E29	FDAT[46]	AH26	RESET_OUT#	A5
A[13]	D31	FDAT[47]	AJ27	RXD	D23
A[14]	D30	FDAT[48]	AL28	RXFAIL	AK10
A[15]	E28	FDAT[49]	AK28	SACLK	B24
A[16]	D27	FDAT[5]	AL16	SCAN_EN	C5
A[17]	B28	FDAT[50]	AH27	SCLK	W31
A[18]	A28	FDAT[51]	AH30	SDCLK	AD2
A[2]	G31	FDAT[52]	AH31	SERR#	B11
A[3]	G30	FDAT[53]	AG29	SLOW_EN#	Y29
A[4]	H28	FDAT[54]	AF28	SLOW_RD#	Y31
A[5]	G29	FDAT[55]	AG30	SLOW_WE#	W28
A[6]	F31	FDAT[56]	AG31	SOE#	W30
A[7]	F30	FDAT[57]	AF29	SOP	AH12
A[8]	F29	FDAT[58]	AF30	SOP32	AJ6
A[9]	E31	FDAT[59]	AF31	SP_CE#	W29
AD[0]	B6	FDAT[6]	AK16	STOP#	C12
AD[1]	A6	FDAT[60]	AE30	SWE#	Y30
AD[10]	B9	FDAT[61]	AE31	TCK	A23
AD[11]	A9	FDAT[62]	AD29	TCK_BYP	D6
AD[12]	C10	FDAT[63]	AC28	TDI	B22
AD[13]	D11	FDAT[7]	AJ16	TDO	D21
AD[14]	B10	FDAT[8]	AH16	TK_IN	AB31
AD[15]	A10	FDAT[9]	AL17	TK_OUT	AA29
AD[16]	A13	FPS[0]	AD30	TMS	C22
AD[17]	C14	FPS[1]	AD31	TRDY#	B12
AD[18]	D15	FPS[2]	AC29	TRST#	B23
AD[19]	B14	FRAME#	C13	TSTCLK	B5
AD[2]	C7	GNT#[0]	B21	TXASIS	AL10
AD[20]	C15	GNT#[1]	C20	TXD	C24
AD[21]	B15	GPIO[0]	C25	VDD	A19
AD[22]	A15	GPIO[1]	D24	VDD	B19

Table 18: Pin Table in Alphabetical Order (Sheet 2 of 4)

Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
AD[23]	D16	GPIO[2]	B25	VDD	B27
AD[24]	A16	GPIO[3]	A25	VDD	H31
AD[25]	C17	HIGH_EN#	C27	VDD	J29
AD[26]	D17	IDSEL	C16	VDD	K2
AD[27]	B18	IRDY#	A12	VDD	L4
AD[28]	C18	LOW_EN#	D26	VDD	Y4
AD[29]	C19	MADR[0]	Y1	VDD	AA2
AD[3]	D8	MADR[1]	Y2	VDD	AA30
AD[30]	A20	MADR[10]	AC1	VDD	AA31
AD[31]	B20	MADR[11]	AC2	VDD	AC4
AD[4]	B7	MADR[12]	AC3	VDD	AD3
AD[5]	A7	MADR[13]	AD1	VDD	AD28
AD[6]	C8	MADR[2]	W4	VDD	AE29
AD[7]	D9	MADR[3]	Y3	VDD	AG4
AD[8]	A8	MADR[4]	AA1	VDD	AG28
AD[9]	C9	MADR[5]	AA3	VDD_REF	E4
CAS#	W3	MADR[6]	AB1	VDDP1	D5
CBE#[0]	B8	MADR[7]	AB2	VDDX	A1
CBE#[1]	C11	MADR[8]	AA4	VDDX	A31
CBE#[2]	B13	MADR[9]	AB3	VDDX	B2
CBE#[3]	B16	MDATA[0]	D2	VDDX	B30
CE#[0]	A27	MDATA[1]	D1	VDDX	C3
CE#[1]	C26	MDATA[10]	H4	VDDX	C29
CE#[2]	B26	MDATA[11]	G2	VDDX	D4
CE#[3]	A26	MDATA[12]	G1	VDDX	D7
CINT#	Y28	MDATA[13]	H3	VDDX	D10
DEVSEL#	D13	MDATA[14]	J4	VDDX	D14
DQ[0]	V29	MDATA[15]	H2	VDDX	D18
DQ[1]	V30	MDATA[16]	H1	VDDX	D22
DQ[10]	R29	MDATA[17]	J3	VDDX	D25
DQ[11]	P30	MDATA[18]	J2	VDDX	D28
DQ[12]	R28	MDATA[19]	J1	VDDX	G4
DQ[13]	P29	MDATA[2]	E3	VDDX	G28
DQ[14]	N31	MDATA[20]	K3	VDDX	K4
DQ[15]	N30	MDATA[21]	K1	VDDX	K28
DQ[16]	N29	MDATA[22]	L3	VDDX	P4
DQ[17]	M31	MDATA[23]	M4	VDDX	P28
DQ[18]	M30	MDATA[24]	L2	VDDX	V4

Table 18: Pin Table in Alphabetical Order (Sheet 3 of 4)

Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
DQ[19]	N28	MDATA[25]	L1	VDDX	V28
DQ[2]	U28	MDATA[26]	M3	VDDX	AB4
DQ[20]	M29	MDATA[27]	N4	VDDX	AB28
DQ[21]	L31	MDATA[28]	M2	VDDX	AE4
DQ[22]	L30	MDATA[29]	M1	VDDX	AE28
DQ[23]	M28	MDATA[3]	F4	VDDX	AH4
DQ[24]	L29	MDATA[30]	N3	VDDX	AH7
DQ[25]	K31	MDATA[31]	N2	VDDX	AH10
DQ[26]	K30	MDATA[32]	N1	VDDX	AH14
DQ[27]	L28	MDATA[33]	P3	VDDX	AH18
DQ[28]	K29	MDATA[34]	P2	VDDX	AH22
DQ[29]	J31	MDATA[35]	R4	VDDX	AH25
DQ[3]	U29	MDATA[36]	R3	VDDX	AH28
DQ[30]	J30	MDATA[37]	T1	VDDX	AJ3
DQ[31]	H30	MDATA[38]	T2	VDDX	AJ29
DQ[4]	T31	MDATA[39]	T3	VDDX	AK2
DQ[5]	T30	MDATA[4]	E2	VDDX	AK30
DQ[6]	T29	MDATA[40]	T4	VDDX	AL1
DQ[7]	T28	MDATA[41]	U1	VDDX	AL31
DQ[8]	R31	MDATA[42]	U2	VSS	A2
DQ[9]	R30	MDATA[43]	U3	VSS	A3
DQM	V3	MDATA[44]	V2	VSS	A14
EOP	AJ11	MDATA[45]	U4	VSS	A17
EOP32	AL5	MDATA[46]	AE1	VSS	A18
FAST_RX1	AH11	MDATA[47]	AE2	VSS	A29
FAST_RX2	AJ10	MDATA[48]	AD4	VSS	A30
FBE#[0]	AK11	MDATA[49]	AE3	VSS	B1
FBE#[1]	AL11	MDATA[5]	E1	VSS	B3
FBE#[2]	AJ12	MDATA[50]	AF1	VSS	B17
FBE#[3]	AH13	MDATA[51]	AF2	VSS	B29
FBE#[4]	AK12	MDATA[52]	AF3	VSS	B31
FBE#[5]	AL12	MDATA[53]	AG1	VSS	C1
FBE#[6]	AJ13	MDATA[54]	AG2	VSS	C2
FBE#[7]	AK13	MDATA[55]	AF4	VSS	C4
FCLK	AB30	MDATA[56]	AG3	VSS	C28
FDAT[0]	AL13	MDATA[57]	AH1	VSS	C30
FDAT[1]	AJ14	MDATA[58]	AH2	VSS	C31
FDAT[10]	AK17	MDATA[59]	AH5	VSS	D3

Table 18: Pin Table in Alphabetical Order (Sheet 4 of 4)

Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number
FDAT[11]	AJ17	MDATA[6]	F3	VSS	D29
FDAT[12]	AK18	MDATA[60]	AK4	VSS	P1
FDAT[13]	AH17	MDATA[61]	AL4	VSS	P31
FDAT[14]	AJ18	MDATA[62]	AJ5	VSS	R1
FDAT[15]	AL19	MDATA[63]	AH6	VSS	R2
FDAT[16]	AK19	MDATA[7]	F2	VSS	U30
FDAT[17]	AJ19	MDATA[8]	F1	VSS	U31
FDAT[18]	AL20	MDATA[9]	G3	VSS	V1
FDAT[19]	AK20	PAR	D12	VSS	V31
FDAT[2]	AK14	PARITY	AK5	VSS	AH3
FDAT[20]	AH19	PCI_CFN[0]	A24	VSS	AH29
FDAT[21]	AJ20	PCI_CFN[1]	C23	VSS	AJ1
FDAT[22]	AL21	PCI_CLK	D20	VSS	AJ2
FDAT[23]	AK21	PCI_IRQ#	A22	VSS	AJ4
FDAT[24]	AH20	PCI_RST#	C21	VSS	AJ28
FDAT[25]	AJ21	PERR#	A11	VSS	AJ30
FDAT[26]	AL22	PORTCTL#[0]	AA28	VSS	AJ31
FDAT[27]	AK22	PORTCTL#[1]	AB29	VSS	AK1
FDAT[28]	AH21	PORTCTL#[2]	AC31	VSS	AK3
FDAT[29]	AJ22	PORTCTL#[3]	AC30	VSS	AK15
FDAT[3]	AH15	PXTAL	B4	VSS	AK29
FDAT[30]	AL23	RAS#	W2	VSS	AK31
FDAT[31]	AK23	RDYBUS[0]	AL7	VSS	AL2
FDAT[32]	AJ23	RDYBUS[1]	AJ8	VSS	AL3
FDAT[33]	AL24	RDYBUS[2]	AH9	VSS	AL14
FDAT[34]	AK24	RDYBUS[3]	AK8	VSS	AL15
FDAT[35]	AH23	RDYBUS[4]	AL8	VSS	AL18
FDAT[36]	AJ24	RDYBUS[5]	AJ9	VSS	AL29
FDAT[37]	AL25	RDYBUS[6]	AK9	VSS	AL30
FDAT[38]	AK25	RDYBUS[7]	AL9	VSSP1	A4
FDAT[39]	AH24	RDYCTL#[0]	AK7	WE#	W1
FDAT[4]	AJ15	RDYCTL#[1]	AH8	RDYCTL#[4]	AK6
FDAT[40]	AJ25	RDYCTL#[2]	AJ7		
FDAT[41]	AL26	RDYCTL#[3]	AL6		

3.6 IX Bus Pins Function Listed by Operating Mode

Figure 7: 64-Bit Bidirectional IX Bus, 1-2 MAC Mode

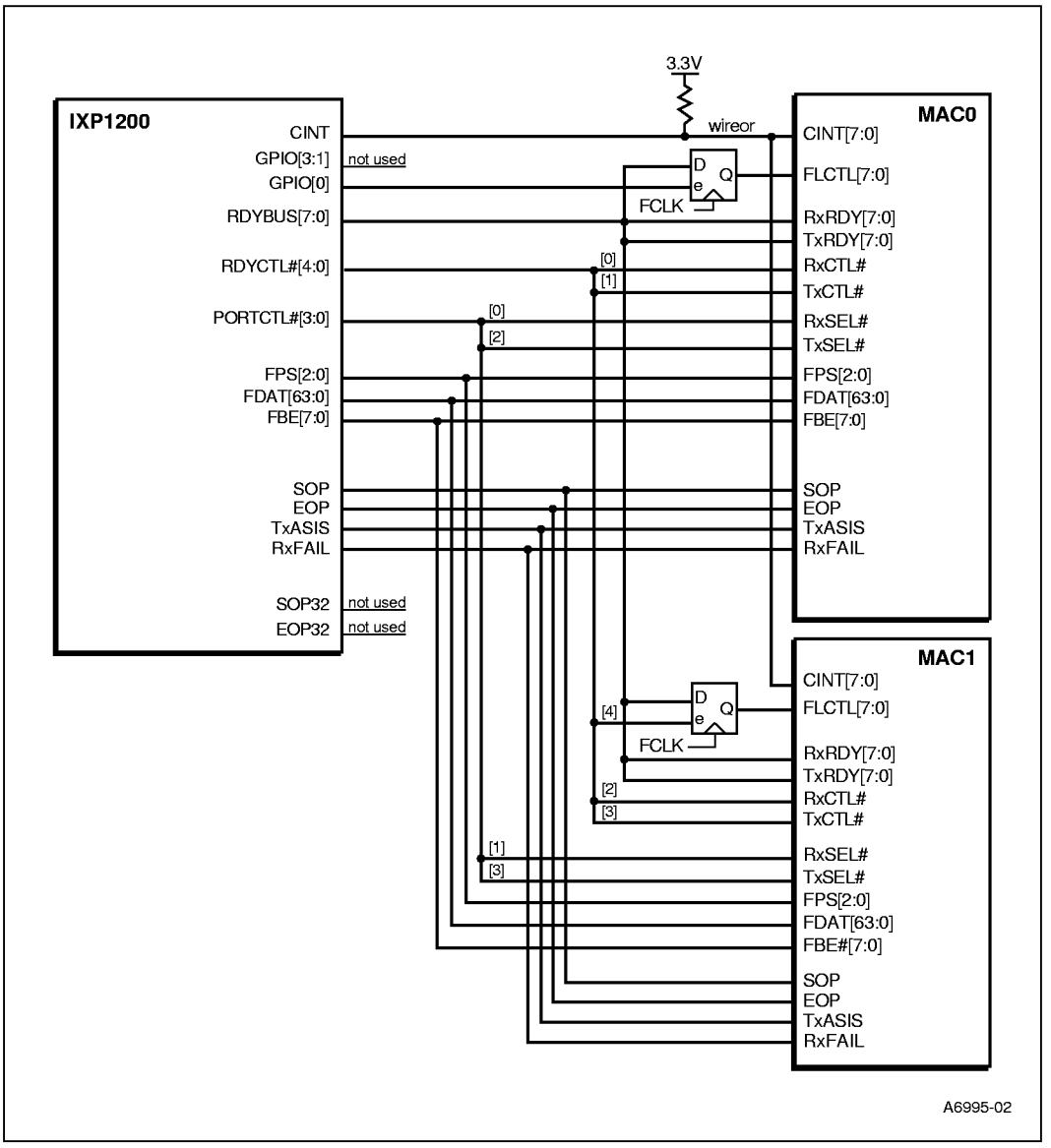


Table 19: 64-Bit Bidirectional IX Bus, 1-2 MAC Mode

Signal	Description
GPIO[3:1]	Active High input/output assigned to StrongARM® not used for MAC interface.
GPIO[0]	Active Low, output Flow-control enable for MAC 0.
RDYCTL#[3:0]	Active Low, output, enables for tx or rx ready flags.
RDYCTL#[4]	Active Low, output, flow-control enable for MAC 1.
RDYBUS[7:0]	Active Low, input/output, tx or rx ready flags.
PORTCTL#[3:0]	Active Low, output, transmit and receive mode enables.
FPS[2:0]	Active High, output port select (transmit or receive).
SOP	Active High, input/output, Start of Packet indication.
SOP_32	Output, not used, no connect.
EOP	Active High, input/output, End of Packet indication.
EOP_32	Input/output, not used, terminate through 10 KOhms to Vdd.
TK_IN	Input, not used, terminate through 10 KOhms to Vdd.
TK_OUT	Output, not used, no connect.
RXFAIL	Active High, input/output. Input - Receive Error input. Output - driven high on non-receive IX Bus cycles.
TXASIS/TXERR	Active High, output. Asserted on first transfer: 1 -Transmit using CRC in Tx FIFO. 0 -Transmit using MAC generated CRC. Asserted with EOP: 1 - Force a transmit error. 0 - Do not force a transmit error.
FBE[7:0]	Active High, byte enables for FDAT [64:0].
FDAT[64:0]	Active High, read and write data.
FAST_RX1	Active High ready input from FastPort 0, pulldown 10 KOhms to GND if not used.
FAST_RX2	Active High ready input from FastPort 1, pulldown 10 KOhms to GND if not used.

Figure 8: 64-Bit Bidirectional IX Bus, 3+ MAC Mode

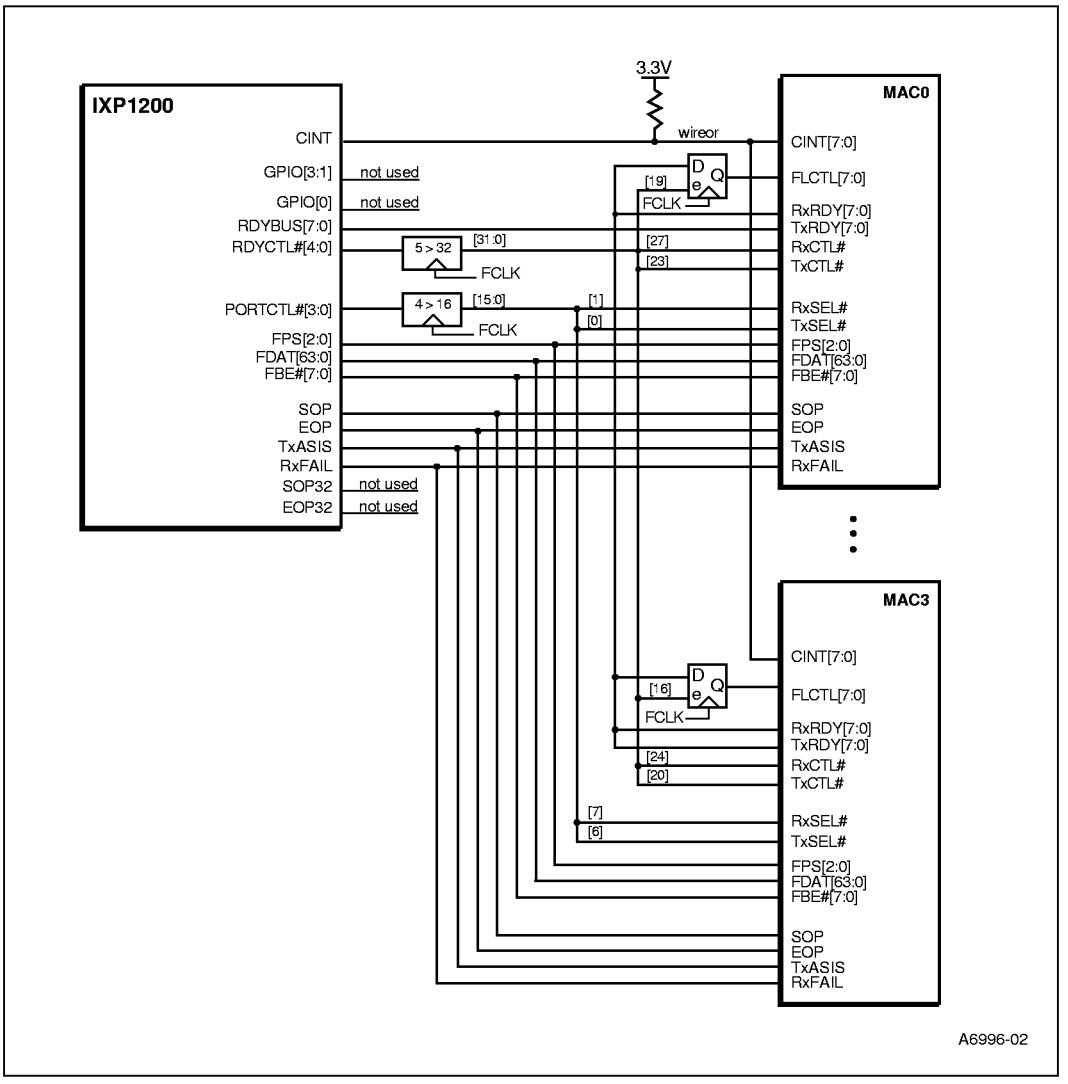


Table 20: 64-Bit Bidirectional IX Bus, 3+ MAC Mode (Shared IX Bus Operation Only in This Mode) (Sheet 1 of 2)

Signal	Description
GPIO[3:1]	Active High input/output assigned to StrongARM® not used for MAC interface.
GPIO[0]	Active High, output assigned to StrongARM® not used for MAC interface.
RDYCTL#[4:0]	Active Low, output 5 bits encoded for tx/rx ready flags, flow-control, and inter-chip communication in shared IX Bus mode. Shared IX Bus mode, Initial ReadyBus master drives RDYCTL#[4:0] and ReadyBus slave snoops.
RDYBUS[7:0]	Active High, input/output.
PORTCTL#[3:0]	Active Low, output, 4 bits encoded for transmit and receive mode select. Shared IX Bus mode - Tri-stated when bus slave.
FPS[2:0]	Active High, output, port select (transmit or receive). Shared IX Bus mode - Tri-stated when bus slave.
SOP	Active High, input/output, Start of Packet indication. Shared IX Bus mode - Tri-stated when bus slave.
SOP_32	Active High, output. Singlechip mode - not used, no connect. Shared IX Bus mode - IX Bus Request.
EOP	Active High, input/output, End of Packet indication. Shared IX Bus mode - Tri-stated when bus slave.
EOP_32	Active High, input/output. Singlechip mode - output, not used, no connect. Shared IX Bus mode - input, IX Bus Request pending.
TK_IN	Input in shared IX Bus mode. Singlechip mode - pullup through 10 KOhms to Vdd. Shared IX Bus mode - Token_Input, enables IX Bus ownership when low at reset - pulldown through 10 KOhms to GND to set as IX Bus Slave, pullup through 10 KOhms to VDD to set as Initial IX Bus Master.
TK_OUT	Active High, output. Singlechip mode - output, not used, no connect. Shared IX Bus mode - Token_Output. When high, indicates this IXP1200 Network Processor owns IX Bus as master.
RXFAIL	Active High, input/output. Input - Receive Error input. Output - driven high on non-receive cycles. Shared IX Bus mode - Tri-stated when bus slave.
TXASIS/TXERR	Active High, output. Asserted on first transfer: 1 -Transmit using CRC in Tx FIFO. 0 -Transmit using MAC generated CRC. Asserted with EOP: 1 - Force a transmit error. 0 - Do not force a transmit error. Tri-stated in shared IX Bus mode when bus slave.
FBE[7:0]	Active High, byte enables for FDAT [64:0]. Tri-stated in shared IX Bus Mode when bus slave.

Table 20: 64-Bit Bidirectional IX Bus, 3+ MAC Mode (Shared IX Bus Operation Only in This Mode) (Sheet 2 of 2)

Signal	Description
FDAT[64:0]	Active High, read and write data. Tri-stated in shared IX Bus mode when bus slave.
FAST_RX1	Active High ready input from FastPort 0, pulldown 10KOhms to GND if not used.
FAST_RX2	Active High ready input from FastPort 1, pulldown 10KOhms to GND if not used.
Shared IX Bus Operation Signals These signals are driven by the IXP1200 Network Processor IX Bus master, and are tri-stated on IXP1200 Network Processor IX Bus slave devices: PORTCTL#[3:0] FPS[2:0] FDAT[63:0] FBE#[7:0] TXASIS/TXERR RXFAIL SOP EOP	

Figure 9: 32-Bit Unidirectional IX Bus, 1-2 MAC Mode

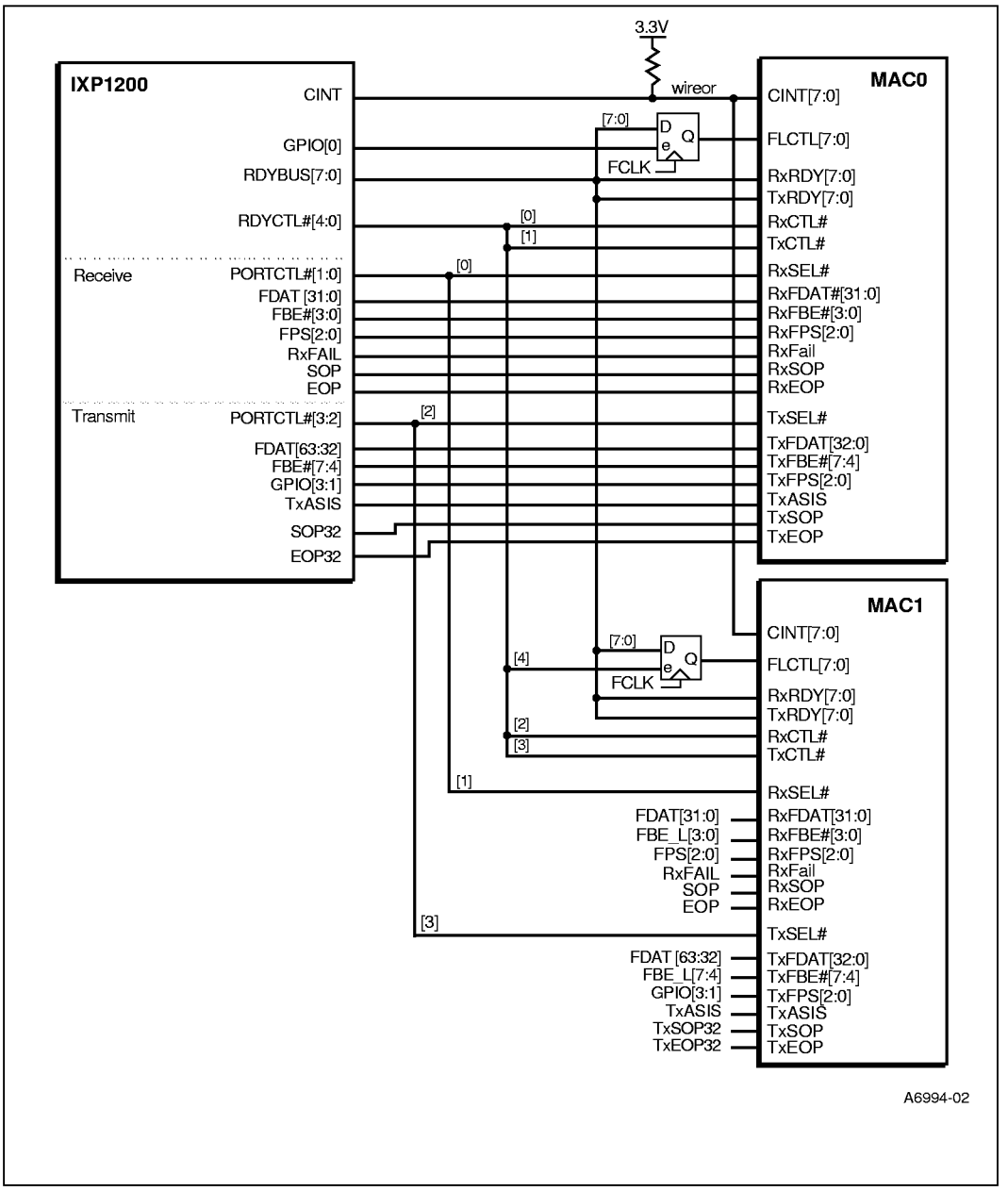


Table 21: 32-Bit Unidirectional IX Bus, 1-2 MAC Mode

Transmit Path Signals	Description
GPIO[3:1]	Active high transmit port select.
PORTCTL#[3:2]	Active Low. Transmit device select.
SOP32	Active High, output, transmit Start of Packet.
EOP32	Active High, output, transmit End of Packet.
TXASIS/TXERR	Active High, output. Asserted on first transfer: 1 -Transmit using CRC in Tx FIFO. 0 -Transmit using MAC generated CRC. Asserted with EOP: 1 - Force a transmit error. 0 - Do not force a transmit error.
FBE[7:4]	Active High, output, byte enables for FDAT [63:31].
FDAT[63:31]	Active High, output, 32-bit transmit data.
Receive Path Signals	
PORTCTL#[1:0]	Active Low, output. Receive device select.
FPS[2:0]	Active High, output. Receive port select.
SOP	Active High input, receive Start of Packet.
EOP	Active High input, receive End of Packet.
RXFAIL	Active High, input, Receive Error.
FBE[3:0]	Active High, output, byte enables for FDAT [31:0].
FDAT[31:0]	Active High, input, 32-bit receive data.
Control Signals Common to both Transmit/Receive Paths	
GPIO[0]	Active Low flow-control for MAC 0.
RDYCTL#[4]	Active Low flow-control for MAC 1.
RDYCTL#[3:0]	Active Low enables for tx or rx ready flags.
TK_IN	Input, pulldown for Initial Master initialization in this mode.
TK_OUT	Output, not used, no connect.
FAST_RX1	Active High, input, FastPort Ready, pulldown if not used.
FAST_RX2	Active High, input, FastPort Ready, pulldown if not used.

Figure 10: 32-bit Unidirectional IX Bus, 3+ MAC Mode (3-4 MACs Supported)

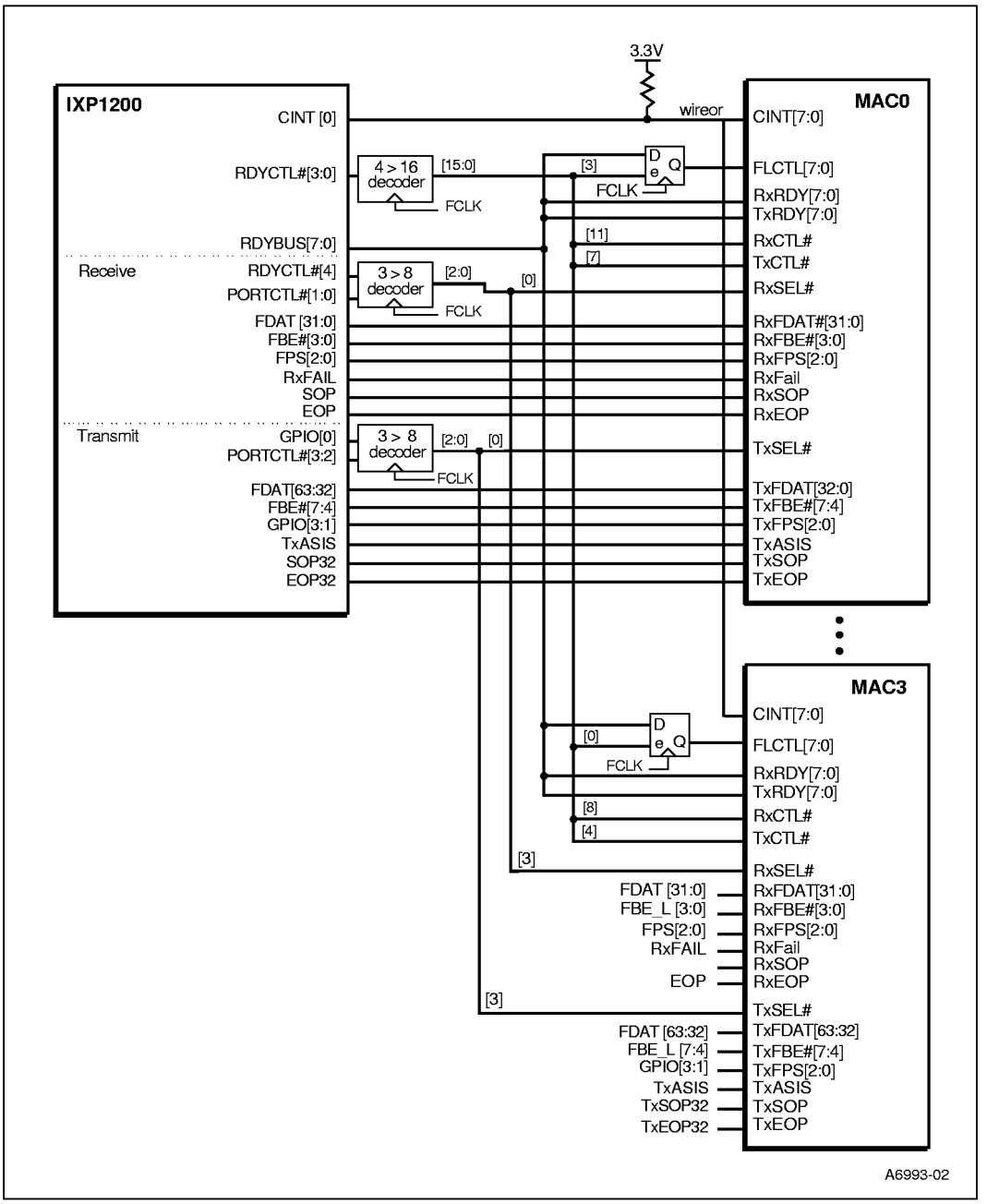


Table 22: 32-bit Unidirectional IX Bus, 3+ MAC Mode

Transmit Path Signals	Description
GPIO[3:1]	Active high transmit port select [2:0].
GPIO[0]	Active Low. Used with PortCTL#[3:2] for transmit device select via external 3-to-8 decoder.
PORTCTL#[3:2]	Active Low Used with GPIO[0] for transmit device select via external 3-to-8 decoder.

Table 22: 32-bit Unidirectional IX Bus, 3+ MAC Mode

Transmit Path Signals	Description
SOP32	Active High output, transmit Start of Packet.
EOP32	Active High output, transmit End of Packet.
TXASIS/TXERR	Active High, output. Asserted on first transfer: 1 -Transmit using CRC in Tx FIFO. 0 -Transmit using MAC generated CRC. Asserted with EOP: 1 - Force a transmit error. 0 - Do not force a transmit error.
FBE[7:4]	Active High, output, byte enables for FDAT [63:31].
FDAT[63:31]	Active High, output, 32-bit transmit data.
Receive Path Signals	
RDYCTL#[4]	Active Low. Used with PortCTL#[1:0] for transmit device select via external 3-to-8 decoder.
PORTCTL#[1:0]	Active Low, output, enable to external PORTCTL[1:0] decoder. Used with RDYCTL#[4] for receive device select via external 3-to-8 decoder.
FPS[2:0]	Active High, output. Receive port select.
SOP	Active High input, receive Start of Packet.
EOP	Active High input, receive End of Packet.
RXFAIL	Active High, input, Receive Error.
FBE[3:0]	Active High, byte enables for FDAT [31:0].
FDAT[31:0]	Active High, input, 32-bit receive data.
Control Signals Common to both Transmit/Receive Paths	
RDYCTL#[3:0]	Active Low, 4 bits encoded for tx/rx ready flags, flow-control, and inter-chip communication. Used as selects to external 4-to-16 decoder.
TK_IN	Input, pulldown for Initial Master initialization in this mode.
TK_OUT	Output, not used, no connect.
FAST_RX1	Active High, input, FastPort Ready, pulldown if not used.
FAST_RX2	Active High, input, FastPort Ready, pulldown if not used.

3.7 IX Bus Decode Table Listed by Operating Mode Type

Table 23: IX Bus Decode Table Listed by Operating Mode Type (Sheet 1 of 2)

PIN NAME	64-bit Bidirectional 1-2 MAC mode	64-bit Bidirectional 3+ MAC mode	32-bit Unidirectional 1-2 MAC mode	32-bit Unidirectional 3+ MAC mode
PORTCTL#[3:0]	1110 MAC0 RxSEL 1101 MAC1 RxSEL 1011 MAC0 TxSEL 0111 MAC1 TxSEL 1111 No Select	0000 MAC0 TxSEL 0001 MAC0 RxSEL 0010 MAC1 TxSEL 0011 MAC1 RxSEL 0100 MAC2 TxSEL 0101 MAC2 RxSEL 0110 MAC3 TxSEL 0111 MAC3 RxSEL 1000 MAC4 TxSEL 1001 MAC4 RxSEL 1010 MAC5 TxSEL 1011 MAC5 RxSEL 1100 MAC6 TxSEL 1101 MAC6 RxSEL 1110/1111 No Select	1110 MAC0 RxSel 1101 MAC1 RxSel 1011 MAC0 TxSel 0111 MAC1 TxSel 1010 MAC0 TxSel/ MAC0 RxSel 0110 MAC1 TxSel/ MAC0 RxSel 1001 MAC0 TxSel/ MAC1 RxSel 101 MAC1 TxSel/ MAC1 RxSel	If RDYCTL<4> = 0 XX00 MAC0 RxSEL XX01 MAC1 RxSEL XX10 MAC2 RxSEL XX11 MAC3 RxSEL If RDYCTL<4> = 1 No Select If GPIO<0> = 1 00XX MAC0 TxSEL 01XX MAC1 TxSEL 10XX MAC2 TxSEL 11XX MAC3 TxSEL If GPIO<0> = 0 No Select
FPS[2:0]	Rx/Tx Port Select	Rx/Tx Port Select	Rx Port Select	Rx Port Select
GPIO[3:1]	Not used	Not used	Tx Port Select	Tx Port Select
GPIO[0]	MAC0 Flw Ctl enable	Not used	MAC0 Flw Ctl enable	PORTCTL#[3:2] Tx enable (see above)
FDAT[63:32]	Rx/Tx Data	Rx/Tx Data	Tx Data	Tx Data
FDAT[31:0]	Rx/Tx Data	Rx/Tx Data	Rx Data	Rx Data
FBE#[7:4]	Rx/Tx Byte Enables	Rx/Tx Byte Enables	Tx Byte Enables	Tx Byte Enables
FBE#[3:0]	Rx/Tx Byte Enables	Rx/Tx Byte Enables	Rx Byte Enables	Rx Byte Enables
SOP	Rx/Tx SOP	Rx/Tx SOP	Rx SOP	Rx SOP
EOP	Rx/Tx EOP	Rx/Tx EOP	Rx EOP	Rx EOP
SOP32	Not used	Not used	Tx SOP	Tx SOP

Table 23: IX Bus Decode Table Listed by Operating Mode Type (Sheet 2 of 2)

PIN NAME	64-bit Bidirectional 1-2 MAC mode	64-bit Bidirectional 3+ MAC mode	32-bit Unidirectional 1-2 MAC mode	32-bit Unidirectional 3+ MAC mode
EOP32	Not used	Not used	Tx EOP	Tx EOP
RDYCTL#[4]	MAC1 Flw Ctl enable	Ready Control (see below)	MAC1 Flw Ctl enable	PORTCTL#[1:0] Rx enable (see above)
RDYCTL#[4:0]	x1111 NOP x1110 MAC0 Rx x1101 MAC0 Tx x1011 MAC1 Rx x0111 MAC1 Tx	11111 NOP 11110 GET 1 11101 SEND 1 11100 autopush 11011 MAC0 Rx 11010 MAC1 Rx 11001 MAC2 Rx 11000 MAC3 Rx 10111 MAC0 Tx 10110 MAC1 Tx 10101 MAC2 Tx 10100 MAC3 Tx 10011 MAC0 Flw Ctl enable 10010 MAC1 Flw Ctl enable 10001 MAC2 Flw Ctl enable 10000 MAC3 Flw Ctl enable 01110 GET 2 01101 SEND 2 01011 MAC4 Rx 01010 MAC5 Rx 01001 MAC6 Rx 00111 MAC4 Tx 00110 MAC5 Tx 00101 MAC6 Tx 00011 MAC4 Flw Ctl enable 00010 MAC5 Flw Ctl enable 00001 MAC6 Flw Ctl enable	x1111 NOP x1110 MAC0 Rx x1101 MAC0 Tx x1011 MAC1 Rx x0111 MAC1 Tx	x1111 NOP x1110 GET 1 x1101 SEND 1 x1100 autopush x1011 MAC0 Rx x1010 MAC1 Rx x1001 MAC2 Rx x1000 MAC3 Rx x0111 MAC0 Tx x0110 MAC1 Tx x0101 MAC2 Tx x0100 MAC3 Tx x0011 MAC0 Flw Ctl enable x0010 MAC1 Flw Ctl enable x0001 MAC2 Flw Ctl enable x0000 MAC3 Flw Ctl enable

3.8 Pin State During Reset

TBD

3.9 Pullup/Pulldown and Unused Pin, Drive Guidelines

For normal (i.e., non-test mode) operation, terminate signals as follows:

- Pullup these signals to 3.3 V: TCK, TMS, TDI.
- Pulldown these signals to Ground: SCAN_EN, TSTCLK, TCK_BYP, TRST#.

Terminate unused signals as follows:

- Pullup these signals to 3.3 V: PARITY, REQ#[1], GNT#[1], TK_IN, EOP32.
- Pulldown these signals to Ground: SACLK, FAST_RX1, FAST_RX2.

For shared IX Bus operation: Pullup PORTCTL#[3:0], FPS[2:0], and TXASIS

Drive guidelines: TBD.

SECTION 4 - ELECTRICAL SPECIFICATIONS

This chapter specifies the following electrical behavior of the IXP1200 Network Processor:

- Absolute maximum ratings.
- DC specifications.
- AC timing specifications for the following signal interfaces:
  - — PXTAL Clock input.
  - — PCI Bus Interface.
  - — FIFO Bus Interface.
  - — ReadyBus Interface.
  - — TK_OUT/TK_IN signals.
  - — SRAM interface.
  - — SDRAM Interface.
  - — Reset signals.
  - — GPIO signals.
  - — JTAG Interface.
  - — Serial Port signals.

4.1 Absolute Maximum Ratings

The IXP1200 Network Processor is specified to operate at a maximum core frequency (Fcore) of 162 MHz at a junction temperature (Tj) not to exceed 100°C. Table 24 lists the absolute maximum ratings for the IXP1200 Network Processor. These are stress ratings only; stressing the device beyond the absolute maximum ratings may cause permanent damage. Operating beyond the functional operating range (Table 25) is not recommended and extended exposure beyond the functional operating range may affect reliability.

Table 24: Absolute Maximum Ratings

Parameter	Minimum	Maximum	Comment
Junction temperature, Tj	---	100°C	
Maximum voltage applied to signal pins		3.6 V	
Supply voltage (core and PLL), VDD, VDDP1		2.1 V	2 V supply
Supply voltage (I/O), VDDX, VDDREF	---	3.6 V	3.3 V supply
Storage temperature range	-55°C	125°C	
Vdelta	0.0 V	1.6 V	

The power specifications listed below are based on the following assumptions:

- Core System Frequency (Fcore)= 162 MHz.
- FIFO Bus Frequency (FCLK) = 66 MHz.
- PCI Bus Frequency (PCI_CLK) = 66 MHz.

Table 25: Functional Operating Range

Parameter	Minimum	Maximum	Comment
Operating temperature range	0°C	55°C	
Supply voltage (core and PLL), VDD, VDDP1	1.9 V	2.1 V	+/- 5%
Supply voltage (I/O), VDDX, VDDREF	3.0 V	3.6 V	+/- 10%
Maximum Power, 2 V supply		2.7 W	(1.35 A)
Maximum Power, 3.3 V supply		2.3 W	(0.7 A)
Total Power		5.0 W	

Table 26: Thermal Specifications

Parameter	Minimum	Maximum	Comment
Junction Temperature, Tj	-	100°C	
Thermal Conductance, θja, 400 LFM airflow	8.5°C/W		Four-layer board
Thermal Conductance, θja, No airflow	12.5°C/W		Four-layer board

4.2 DC Specifications

The IXP1200 Network Processor supports two fundamental I/O buffer Types: Type 1 and Type 2. The Pin Description section defines which pins use which I/O buffer type. The driver characteristics are described in the following sections. Please note that IXP1200 Network Processor input pins are not 5 volt tolerant. Devices driving the IXP1200 Network Processor must provide 3.3 V signal levels or use level shifting buffers to provide 3.3 V compatible levels, otherwise damage to the device will result.

The Type 1 pins are 3.3 V Low Voltage TTL compatible I/O buffers. There are three versions of the Type 1 driver that differ by the maximum available driver current.

The Type 2 pins are 3.3 V PCI 2.1 compliant I/O buffers.

4.2.1 Type 1 Driver DC Specifications

Table 27 refers to pin types: I1, O1, O3, O4.

Table 27: I1, O1, O3 and O4 Pin Types

Symbol	Parameter	Condition	Minimum	Maximum
Vih	Input High Voltage		2.0 V	---
Vil	Input Low Voltage		---	0.8 V
Voh	Output High Voltage	O1: Ioh = -tbd mA O3: Ioh = -tbd mA O4: Ioh = -tbd mA Load circuit 1	2.4 V	-
Vol	Output Low Voltage	O1: Iol = +tbd mA O3: Iol = +tbd mA O4: Iol = +tbd mA Load circuit 2	---	0.4 V
Ii	Input Leakage Current1	-	- tbd µA	tbd µA
Cin	Pin Capacitance	-	5 pF	10 pF

Test Load 1 tbd

Test Load 2 tbd

4.2.1.1 Type 2 Driver DC Specifications

Table 28 refers to pin types: I2, O2.

Table 28: I2 and O2 Pin Types

Symbol	Parameter	Condition	Minimum	Maximum
Vih	Input High Voltage		0.5 x VDDX	VDD_REF + 0.5V
Vil	Input Low Voltage		---	0.3 x VDDX
Voh	Output High Voltage	Ioh = -500 uA	0.9 x VDDX	---
Vol	Output Low Voltage	Iol = 1500 uA	---	0.1 x VDDX
Ii	Input Leakage Current1	0 < Vin <VDDX	-15 uA	15 uA
Cin	Pin Capacitance		5 pF	10 pf

NOTE

In Table 27 and Table 28, currents into the chip (chip sinking) are denoted as positive(+) current. Currents from the chip (chip sourcing) are denoted as negative(-) current.

Input leakage currents include high-Z output leakage for all bidirectional buffers with tri-state outputs.

NOTE

The electrical specifications are preliminary and subject to change.

4.3 AC Specifications

4.3.1 Clock Timing Specifications

The ac specifications consist of input requirements and output responses. The input requirements consist of setup and hold times, pulse widths, and high and low times. Output responses are delays from clock to signal. The ac specifications are defined separately for each clock domain within the IXP1200 Network Processor.

For example, Figure 12 shows the ac parameter measurements for the PCI_CLK signal, and Table 30 and Table 31 specify parameter values for clock signal ac timing. See also Figure 13 for a further illustration of signal timing. Unless otherwise noted, all ac parameters are guaranteed when tested within the functional operating range of Table 25.

4.3.2 PXTAL Clock Input

Figure 11: PXTAL Clock Input

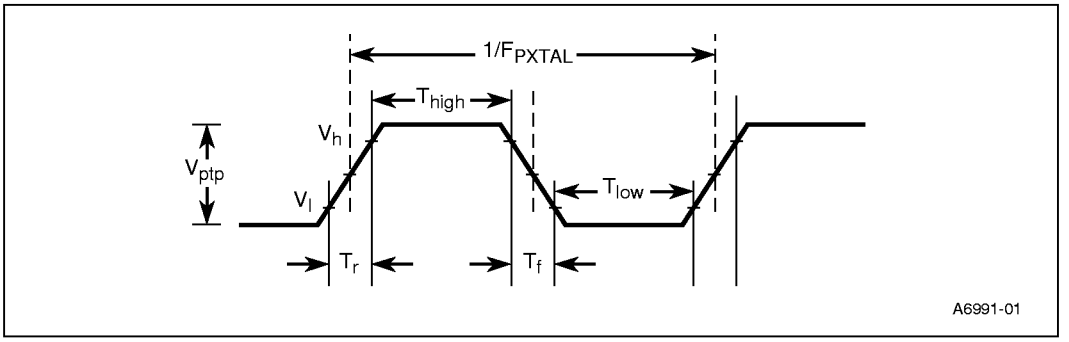


Table 29: PXTAL Clock Inputs

Symbol	Parameter	Minimum	Typical	Maximum	Unit
Fpxtal	Clock frequency	3.5795	3.6864	---	MHz
Vptp	Clock peak to peak	0.4*VDDX		---	V
Vhigh	Clock high threshold	2.0		---	V
Vlow	Clock low threshold	---		0.8	V
	Clock slew rate[1]	1		4	V/ns
Fcore	Core frequency[2]		166		MHz

1. Not tested. Guaranteed by design.
2. Core frequency (Fcore) of 162 MHz when register PLL_CFG[4:0] = 00111.

4.3.3 PXTAL Clock Oscillator Specifications

Frequency: Fpxtal ±0.01%

Stability: 100 ppm

Voltage signal level: 3.3 V

Rise/fall time: < 4 ns

Duty cycle: 40%-60%

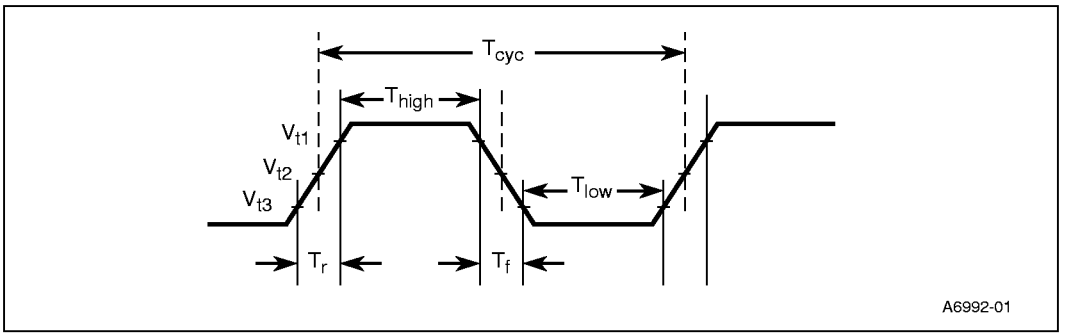
4.3.4 PCI

4.3.4.1 PCI Electrical Specification Conformance

The IXP1200 Network Processor PCI pins conform to the basic set of PCI electrical specifications in the *PCI Local Bus Specification, Revision 2.1*. See that document for a complete description of the PCI I/O protocol and pin ac specifications.

4.3.4.2 PCI Clock Signal AC Parameter Measurements

Figure 12: PCI Clock Signal AC Parameter Measurements



Vt1 = 0.5*VDDX
Vt2 = 0.4*VDDX
Vt3 = 0.3*VDDX

Table 30: 66 MHz PCI Clock Signal AC Parameters

Symbol	Parameter	Minimum	Maximum	Unit
Tcyc	PCI_CLK cycle time	15	30	ns
Thigh	PCI_CLK high time	6	---	ns
Tlow	PCI_CLK low time	6	---	ns
	PCI_CLK slew rate[1, 2]	1.5	4	V/ns

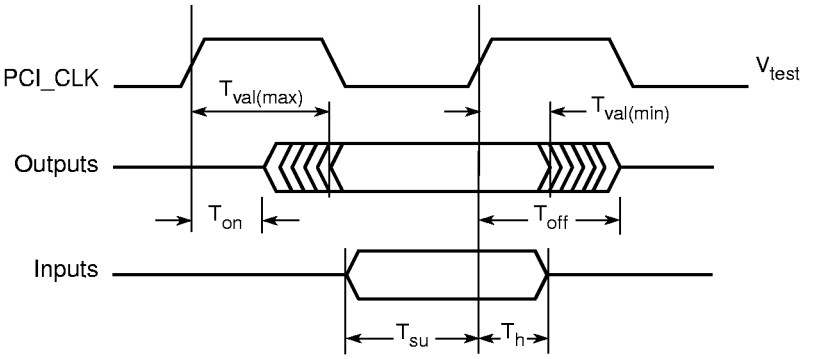
1. 0.2 VDDX to 0.6 VDDX.
2. Not tested. Guaranteed by design.

Table 31: 33 MHz PCI Clock Signal AC Parameters

Symbol	Parameter	Minimum	Maximum	Unit
Tcyc	PCI_CLK cycle time	30	∞	ns
Thigh	PCI_CLK high time	11	---	ns
Tlow	PCI_CLK low time	11	---	ns
	PCI_CLK slew rate[1 2]	1	4	V/ns

1. 0.2 VDDX to 0.6 VDDX.
2. Not tested. Guaranteed by design.

Figure 13: PCI Bus Signals



Note: V_{test} - 0.4 VDDX for 3.3 volt PCI signals

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4.3.4.3 PCI Bus Signals Timing

Table 32: 33 MHZ PCI Signal Timing

Symbol	Parameter	Minimum	Maximum	Unit
Tval	CLK to signal valid delay, bused signals	2	11	ns
Tval (point-to-point)	CLK to signal valid delay, point-to-point signals[1]	2	12	ns
Ton	Float to active delay	2	---	
Toff	Active to float delay	---	28	ns
Tsu	Input setup time to CLK, bused signals[1]	7	---	ns
Tsu (point-to-point)	Input setup time to CLK, point-to-point signals[2]	10	---	ns
Th	Input signal hold time from CLK	0	---	ns

1. Point-to-point signals are REQ#, GNT#.
2. Bused signals are AD, CBE#, PAR, PERR#, SERR#, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#

Table 33: 66 MHz PCI Signal Timing (Sheet 1 of 2)

Symbol	Parameter	Minimum	Maximum	Unit
Tval	CLK to signal valid delay, bused signals	2	6	ns
Tval (point-to-point)	CLK to signal valid delay, point-to-point signals[1]	2	6	ns
Ton	Float to active delay	2	---	
Toff	Active to float delay	---	14	ns

Table 33: 66 MHz PCI Signal Timing (Sheet 2 of 2)

Symbol	Parameter	Minimum	Maximum	Unit
Tsu	Input setup time to CLK, bused signals[2]	3	---	ns
Tsu (point-to-point)	Input setup time to CLK, point-to-point signals[1]	5	---	ns
Th	Input signal hold time from CLK	0	---	ns

1. Point-to-point signals are REQ#, GNT#.
2. Bused signals are AD, CBE#, PAR, PERR#, SERR#, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#.

4.3.5 Reset

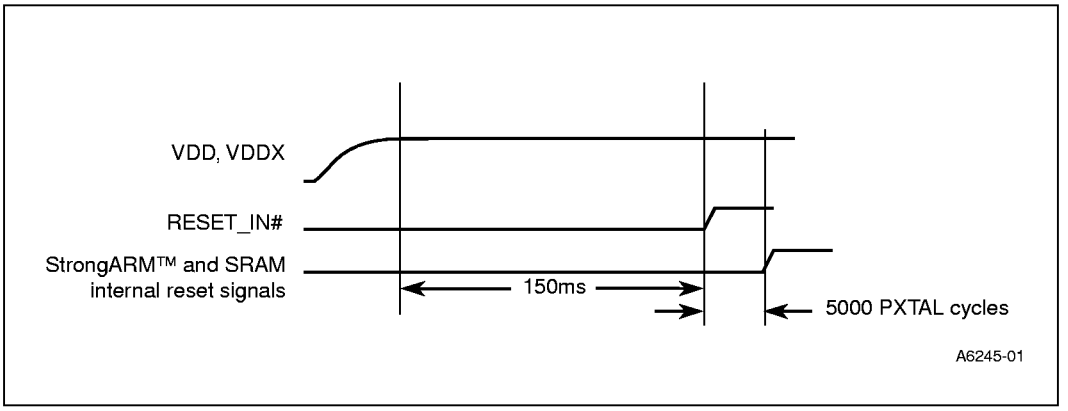
4.3.5.1 Reset Timings Specification

Table 34 shows the reset timing specifications for RESET_IN# and RESET_OUT#.

Table 34: Reset Timings Specification TBD

Symbol	Parameter	Minimum	Maximum	Unit

Figure 14: RESET_IN# Timing Diagram



4.3.6 JTAG

4.3.6.1 JTAG Timing Specifications

TBD

4.3.7 IX Bus

4.3.7.1 FCLK Signal AC Parameter Measurements

Figure 15: FCLK Signal AC Parameter Measurements

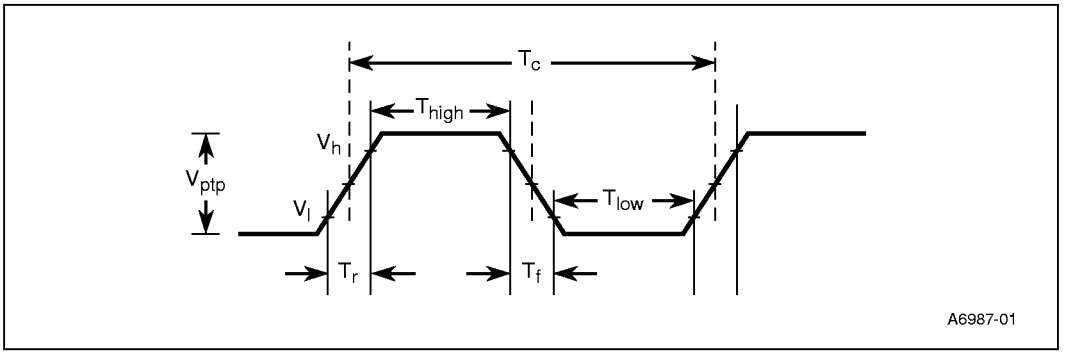


Table 35: FCLK Signal AC Parameter Measurements

Symbol	Parameter	Minimum	Maximum	Unit
Freq	Clock frequency	25 tbd	66.6	MHz
Tc	Cycle time	15	40	ns
Thigh	Clock high time	6	---	ns
Tlow	Clock low time	6	---	ns
Vptp	Clock peak to peak (0.2* VDDX to 0.6*VDDX)	0.4*VDDX	---	V
Vh	Clock high threshold	0.5*VDDX	---	V
Vl	Clock low threshold	---	0.3*VDDX	V
	Clock slew rate[1, 2]	1	4	V/ns

1. 0.2 *VDDX to 0.6 *VDDX.
2. Not tested. Guaranteed by design.

4.3.7.2 IX Bus Signals Timing

Figure 16: IX Bus Signals Timing

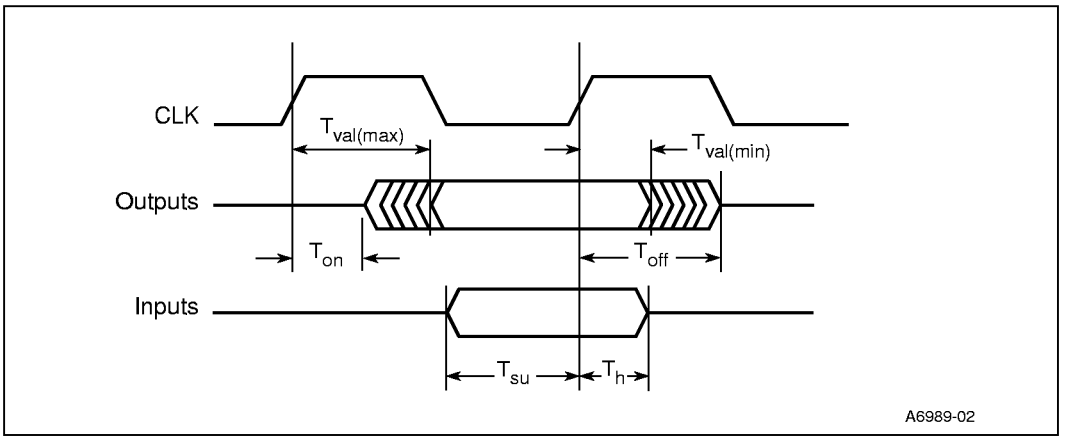


Table 36: IX Bus Signals Timing

Symbol	Parameter	Minimum	Maximum	Unit
Tval	Clock-to-signal valid delay (except RDYBUS signals)	2	6	ns
Tvalrb	Clock-to-valid delay[1], RDYBUS	2	8	ns
Tsu	Input signal valid setup time before clock	3	---	ns
Th	Input signal hold time from clock	0	---	ns
Ton	Float-to-active delay from clock	1	---	ns
Toff	Active-to-float delay from clock	---	14	ns

1. RDYCTL#[4:0] and RDYBUS[7:0] driven for two cycles.

4.3.7.3 IX Bus Protocol

The following timing diagrams show the IX Bus signal protocol for both 64-bit Bidirectional and 32-bit Unidirectional modes of operation.

Figure 17: 64-Bit Bidirectional IX Bus Timing - Consecutive Receives with EOP on 1st Data Return, No Status Transfer

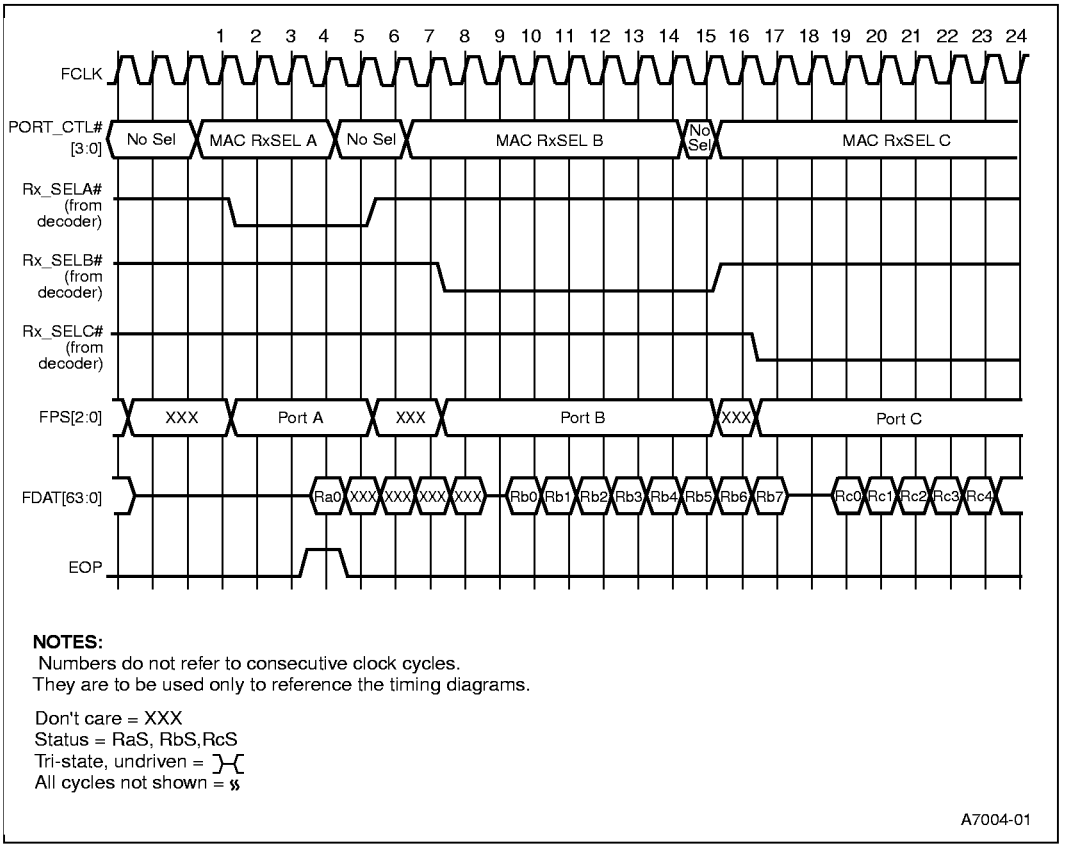
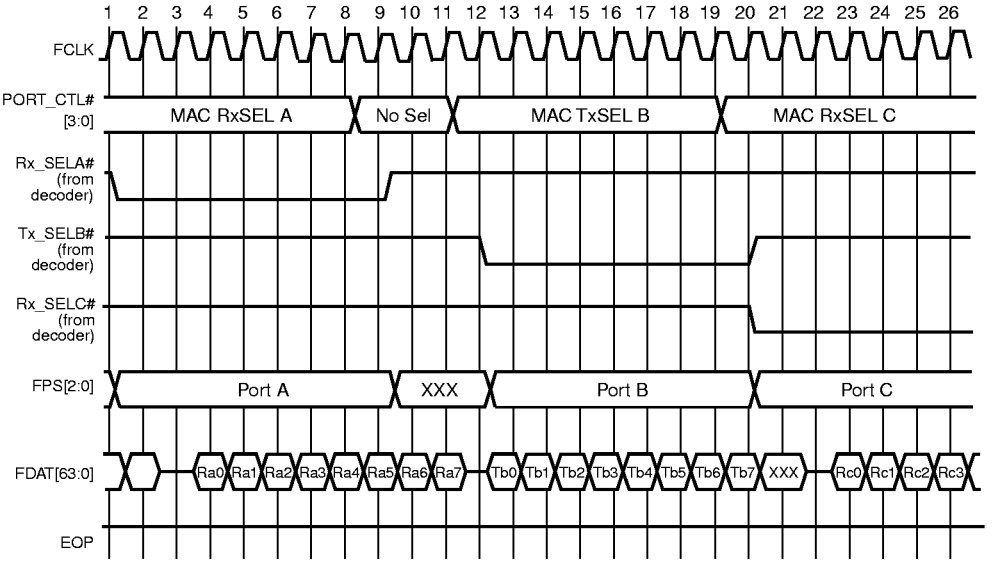


Figure 18: 64-Bit Bidirectional IX Bus Timing - Consecutive Receive and Transmit with No EOP



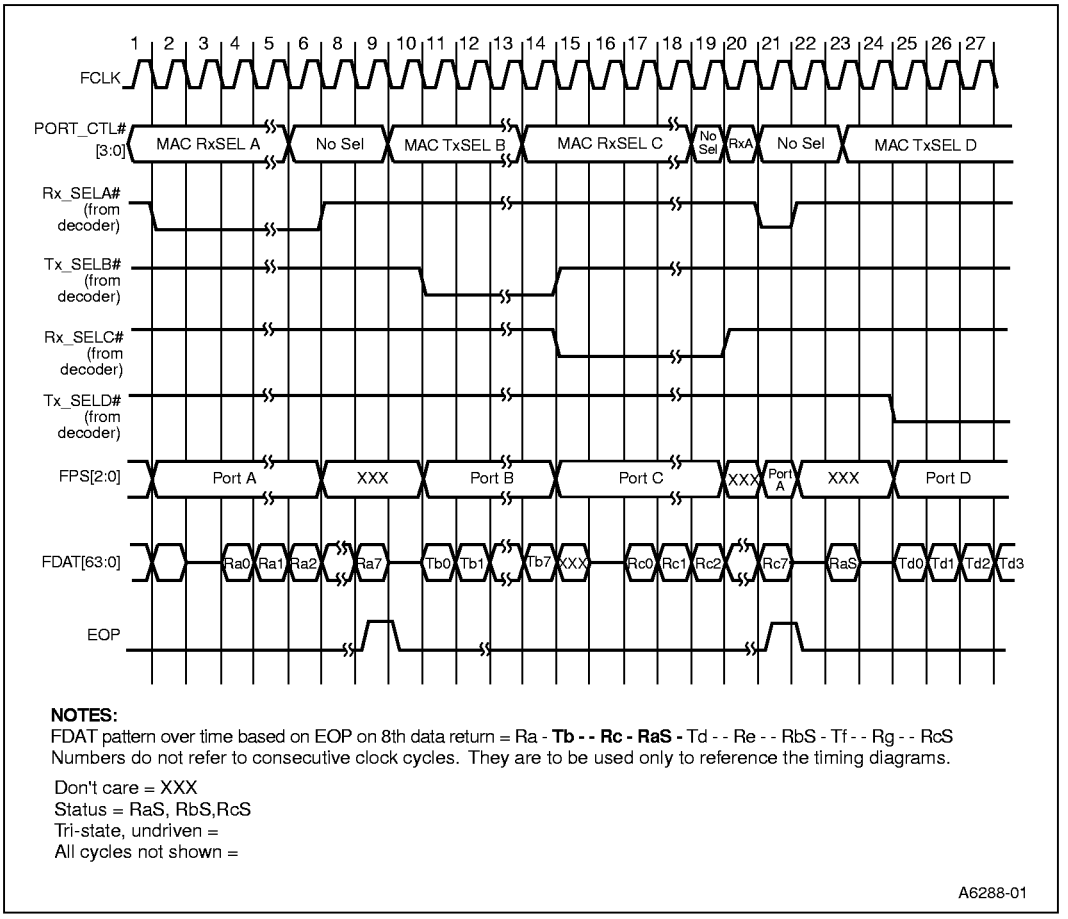
NOTES:

FDAT pattern over time based on EOP on 8th data return = Ra - **Tb - - Rc - RaS -** Td - - Re - - RbS - Tf - - Rg - - RcS
Numbers do not refer to consecutive clock cycles. They are to be used only to reference the timing diagrams.

Don't care = XXX
Status = RaS, RbS,RcS
Tri-state, undriven = }-{
All cycles not shown = ≈

A6997-01

Figure 19: 64-Bit Bidirectional IX Bus Timing - Consecutive Receive and Transmit with EOP on 8th Data Return

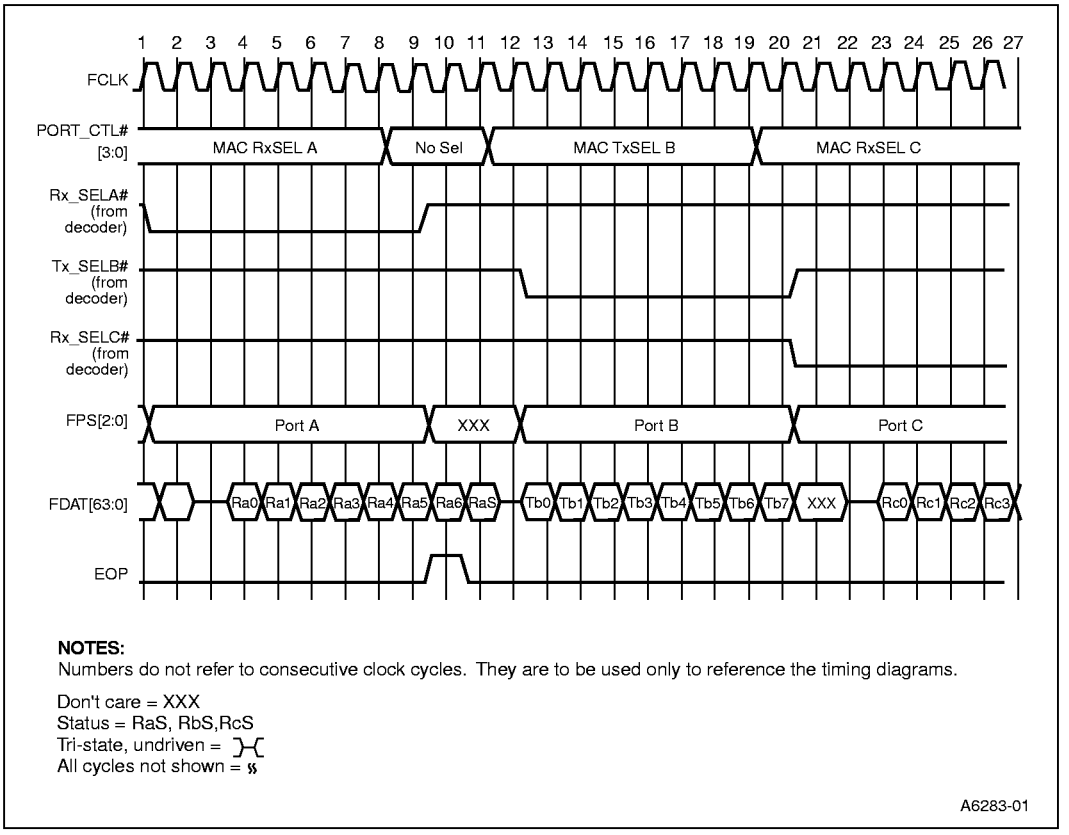


NOTES:
FDAT pattern over time based on EOP on 8th data return = Ra - **Tb - - Rc - RaS -** Td - - Re - - RbS - Tf - - Rg - - RcS
Numbers do not refer to consecutive clock cycles. They are to be used only to reference the timing diagrams.

Don't care = XXX
Status = RaS, RbS,RcS
Tri-state, undriven =
All cycles not shown =

A6288-01

Figure 20: 64-Bit Bidirectional IX Bus Timing - Consecutive Receive and Transmit with EOP on 7th Data Return

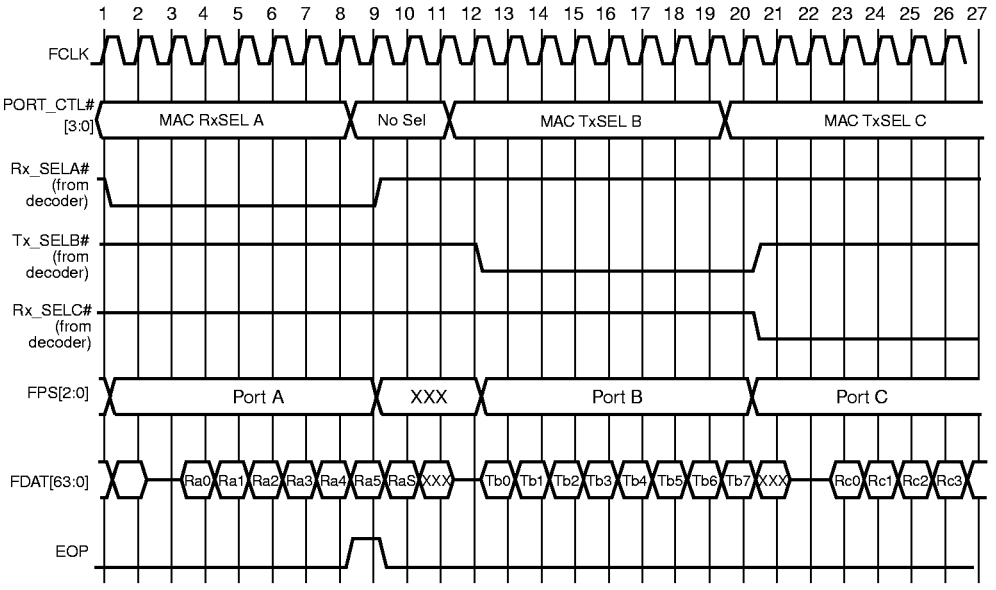


NOTES:
Numbers do not refer to consecutive clock cycles. They are to be used only to reference the timing diagrams.

Don't care = XXX
Status = RaS, RbS,RcS
Tri-state, undriven = }-{
All cycles not shown = ≈

A6283-01

Figure 21: 64-Bit Bidirectional IX Bus Timing - Consecutive Receive and Transmit with EOP on 6th Data Return

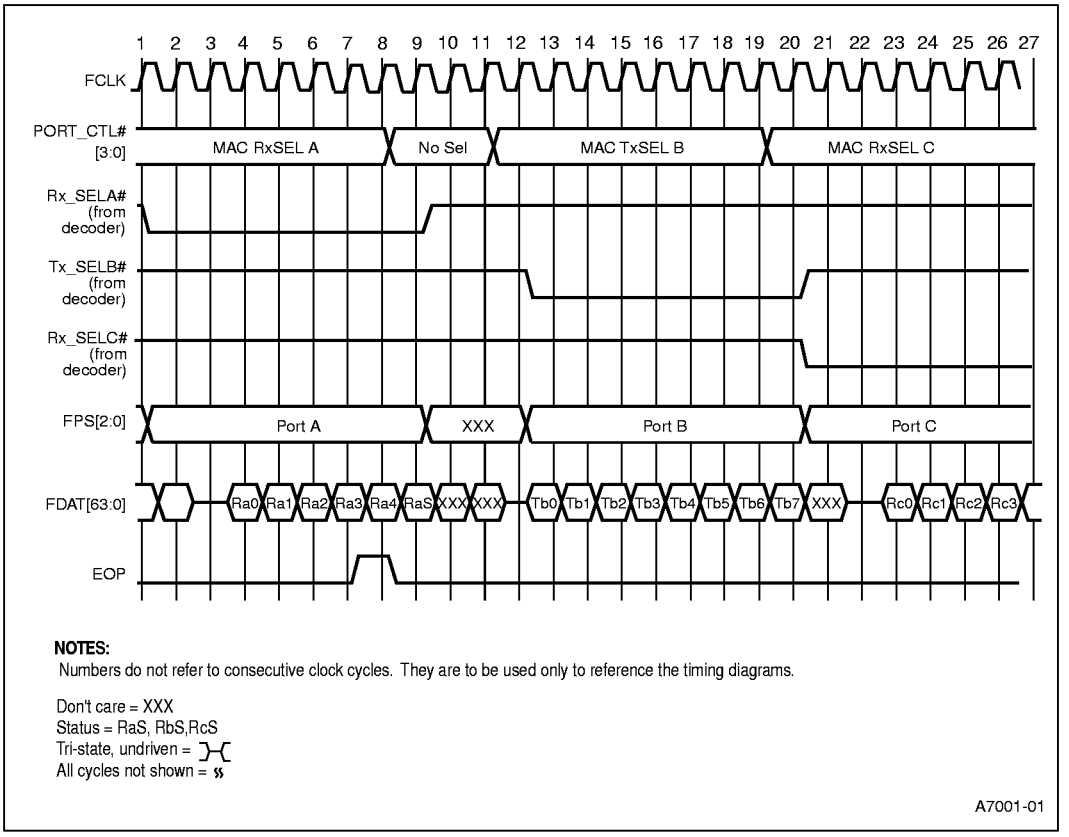


NOTES:
Numbers do not refer to consecutive clock cycles. They are to be used only to reference the timing diagrams.

Don't care = XXX
Status = RaS, RbS,RcS
Tri-state, undriven = ><
All cycles not shown = ≈

A6289-02

Figure 22: 64-Bit Bidirectional IX Bus Timing - Consecutive Receive and Transmit with EOP on 5th Data Return

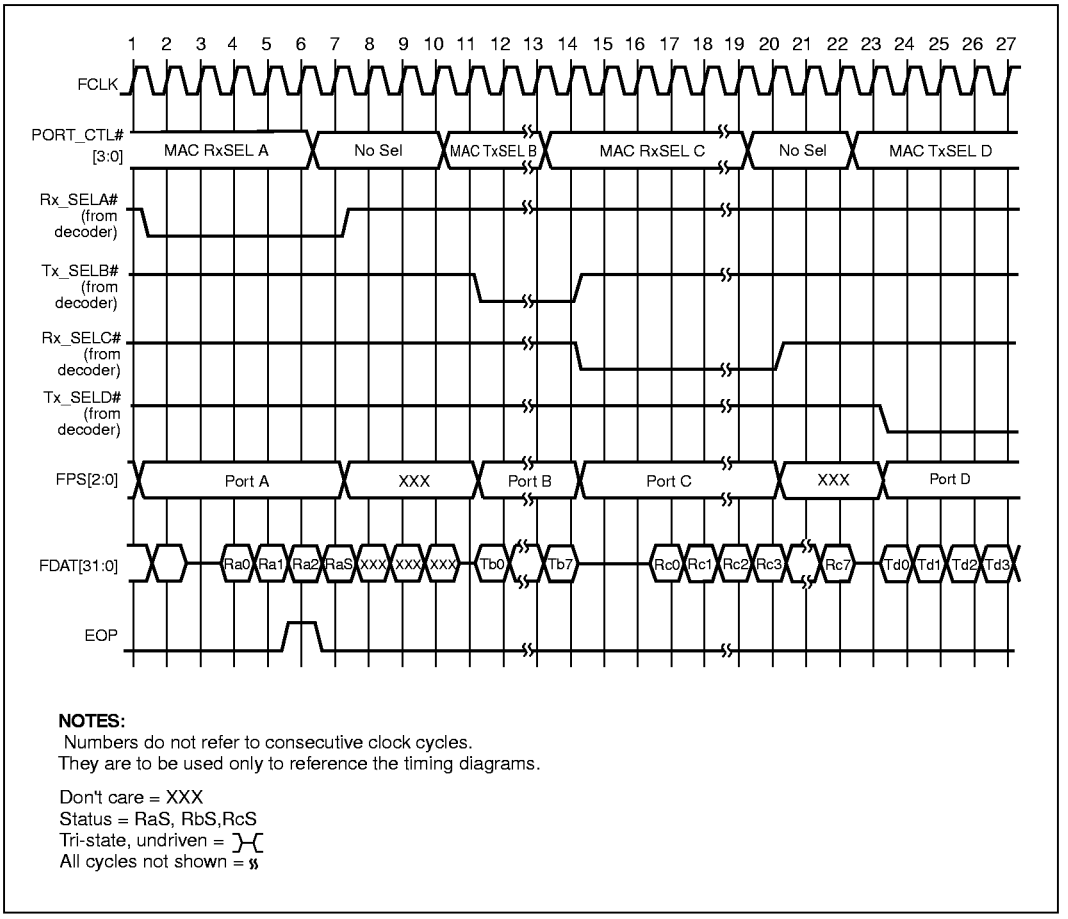


NOTES:
Numbers do not refer to consecutive clock cycles. They are to be used only to reference the timing diagrams.

Don't care = XXX
Status = RaS, RbS,RcS
Tri-state, undriven = }-{
All cycles not shown = ≈

A7001-01

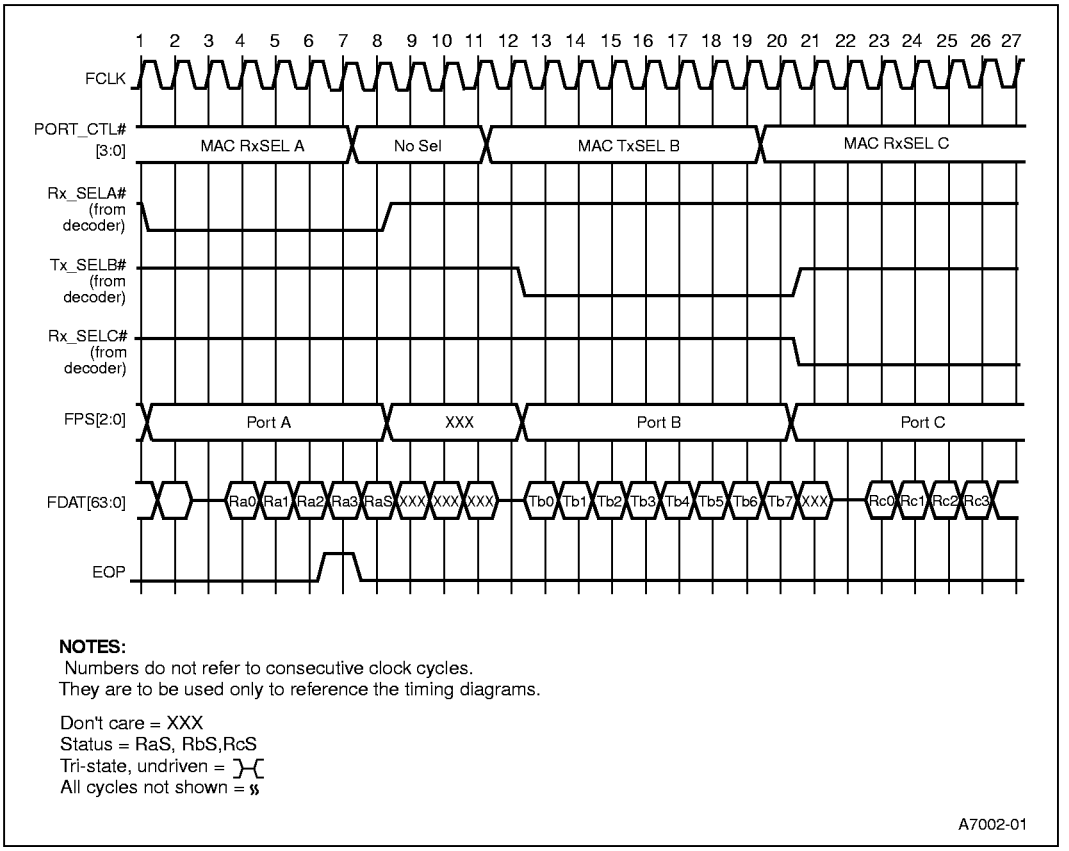
Figure 23: 64-Bit Bidirectional IX Bus Timing - Consecutive Receive and Transmit with EOP on 1st through 3rd Data Return (3rd Data Return Shown)



NOTES:
Numbers do not refer to consecutive clock cycles.
They are to be used only to reference the timing diagrams.

Don't care = XXX
Status = RaS, RbS,RcS
Tri-state, undriven = }-{
All cycles not shown = ≈

Figure 24: 64-Bit Bidirectional IX Bus Timing - Consecutive Receive and Transmit with EOP on 4th Data Return

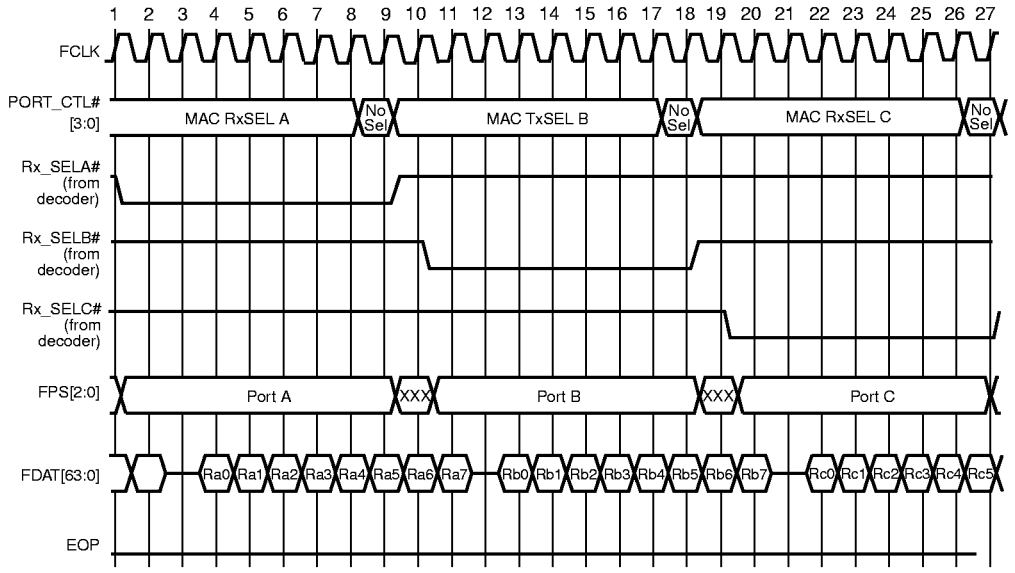


NOTES:
Numbers do not refer to consecutive clock cycles.
They are to be used only to reference the timing diagrams.

Don't care = XXX
Status = RaS, RbS,RcS
Tri-state, undriven = }-{
All cycles not shown = ≈

A7002-01

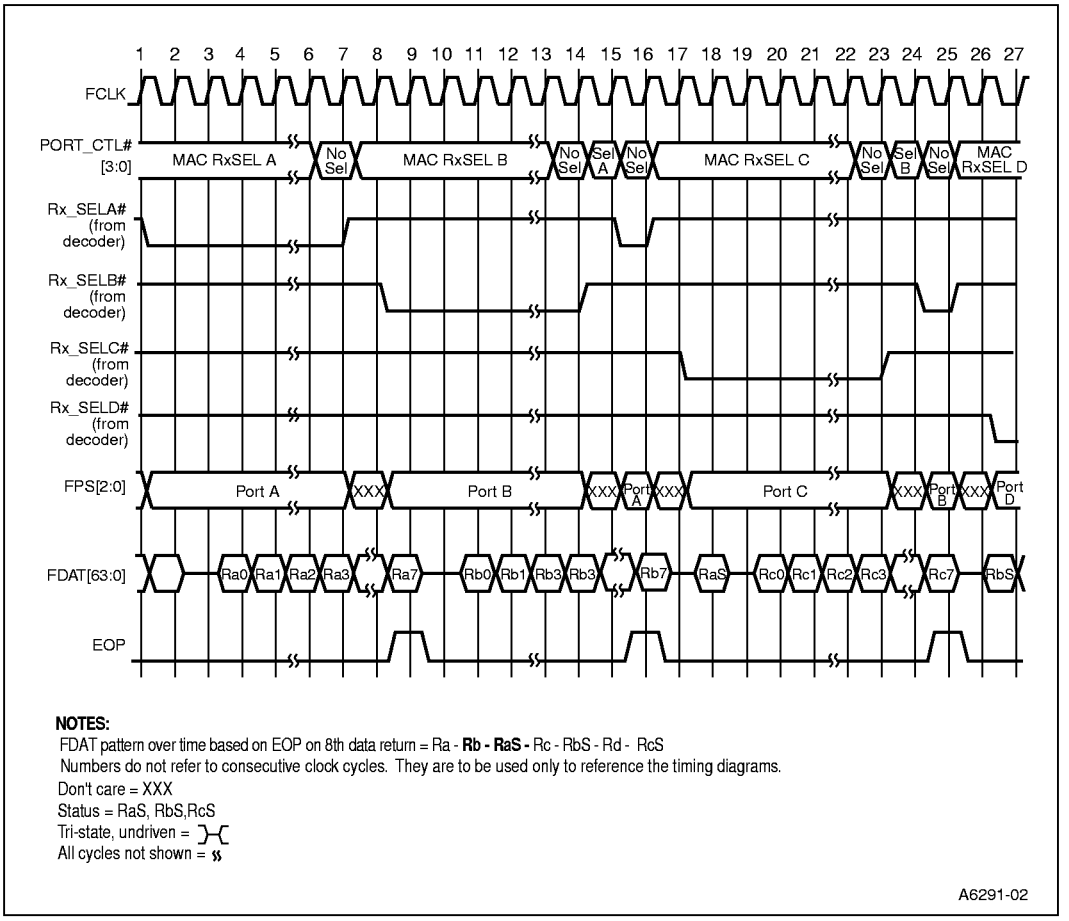
Figure 25: 64-Bit Bidirectional IX Bus Timing - Consecutive Receives with No EOP



NOTES:
FDAT pattern over time based on EOP on 8th data return = Ra - **Rb - RaS -** Rc - RbS - Rd - RcS
Numbers do not refer to consecutive clock cycles. They are to be used only to reference the timing diagrams.
Don't care = XXX
Status = RaS, RbS,RcS
Tri-state, undriven =
All cycles not shown =

A7003-01

Figure 26: 64-Bit Bidirectional IX Bus Timing - Consecutive Receives with EOP on 8th Data Return



NOTES:

FDAT pattern over time based on EOP on 8th data return = Ra - **Rb - RaS -** Rc - RbS - Rd - RcS

Numbers do not refer to consecutive clock cycles. They are to be used only to reference the timing diagrams.

Don't care = XXX

Status = RaS, RbS,RcS

Tri-state, undriven = }-{

All cycles not shown = ≈

A6291-02

Figure 27: 64-Bit Bidirectional IX Bus Timing - Consecutive Receives with EOP on 7th Data Return

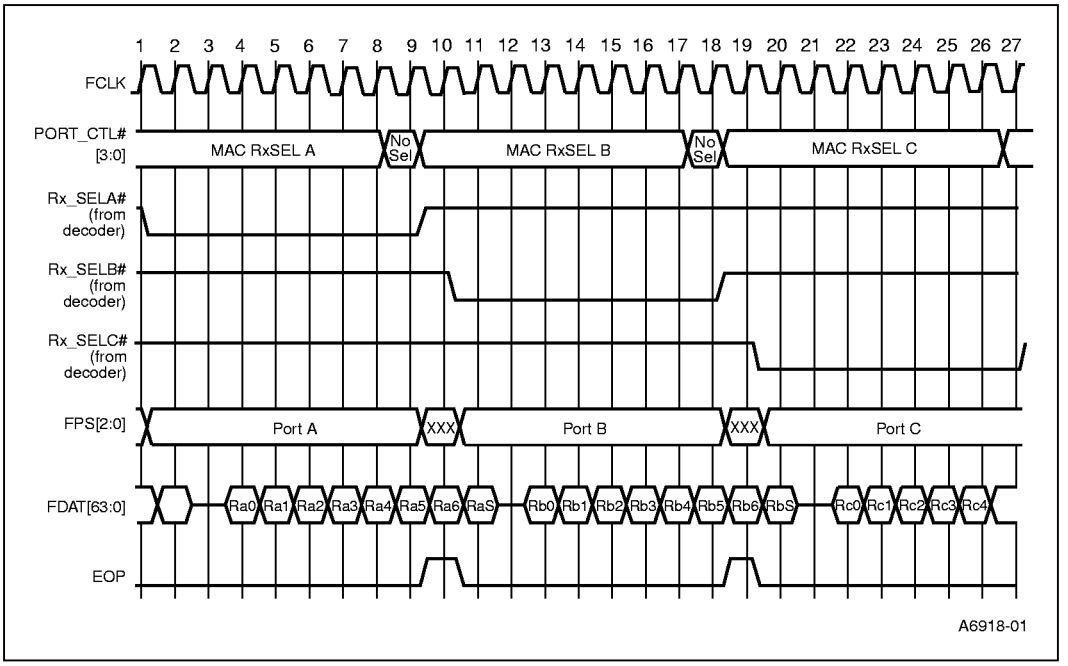
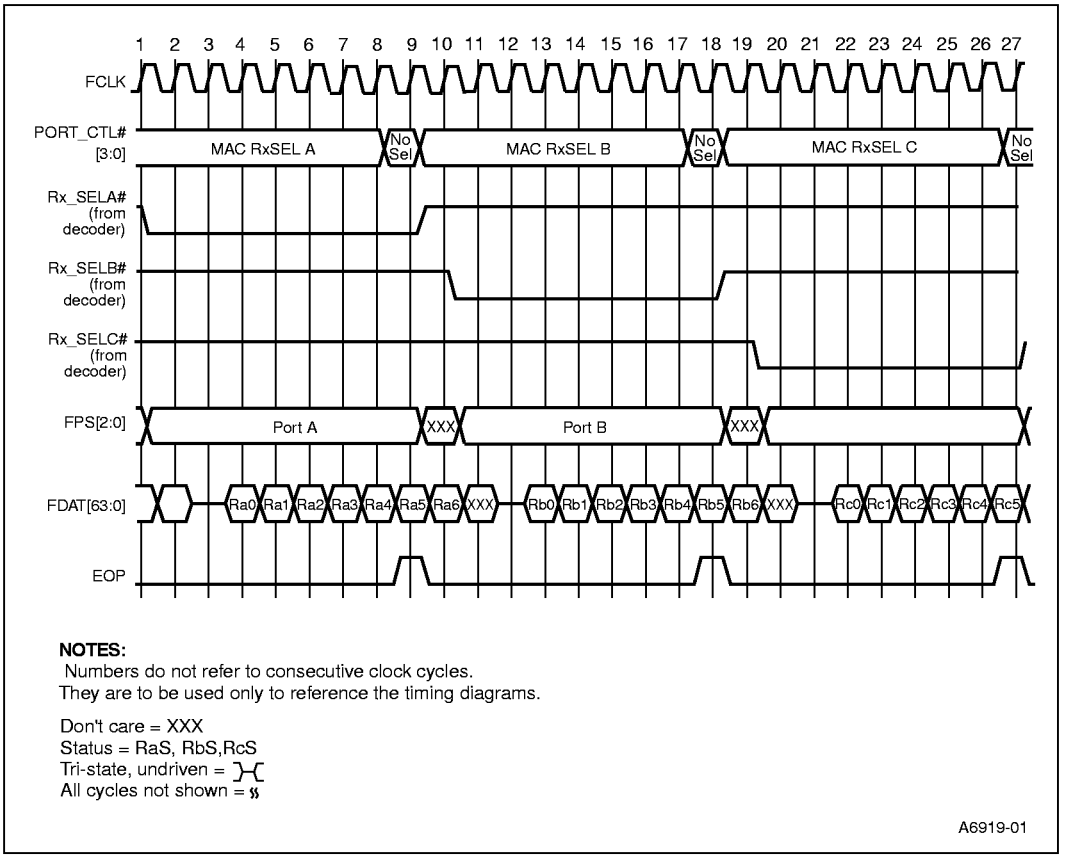


Figure 28: 64-Bit Bidirectional IX Bus Timing - Consecutive Receives with EOP on 6th Data Return

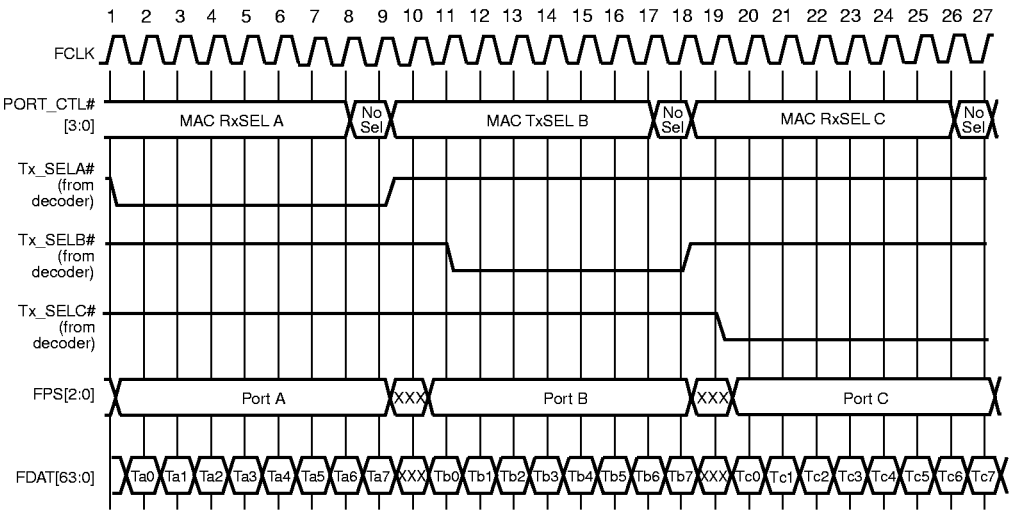


NOTES:
Numbers do not refer to consecutive clock cycles.
They are to be used only to reference the timing diagrams.

Don't care = XXX
Status = RaS, RbS,RcS
Tri-state, undriven = }-{
All cycles not shown = ≈

A6919-01

Figure 29: 64-Bit Bidirectional IX Bus Timing - Consecutive Transmits

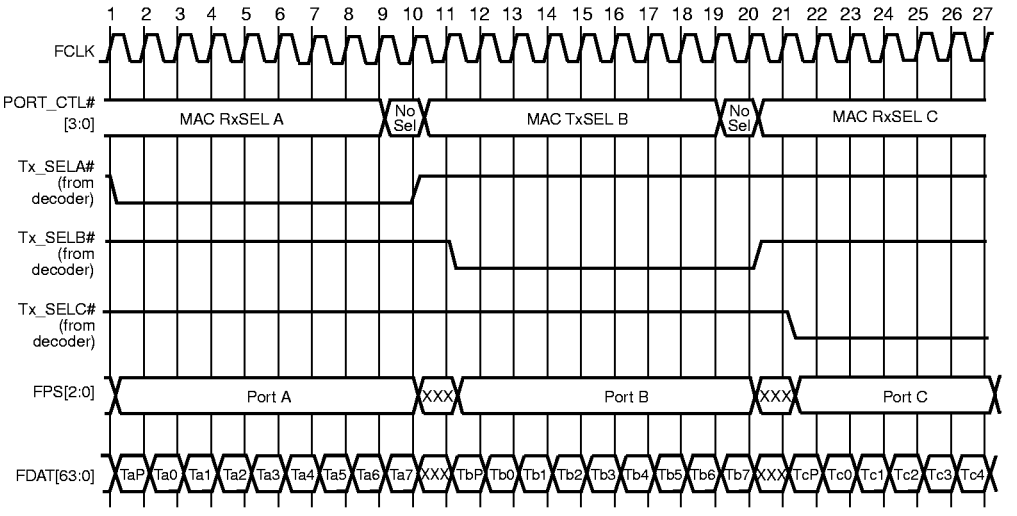


NOTES:
Numbers do not refer to consecutive clock cycles. They are to be used only to reference the timing diagrams.

Don't care = XXX
Status = RaS, RbS,RcS
Tri-state, undriven = }-{
All cycles not shown = ≈

A6286-01

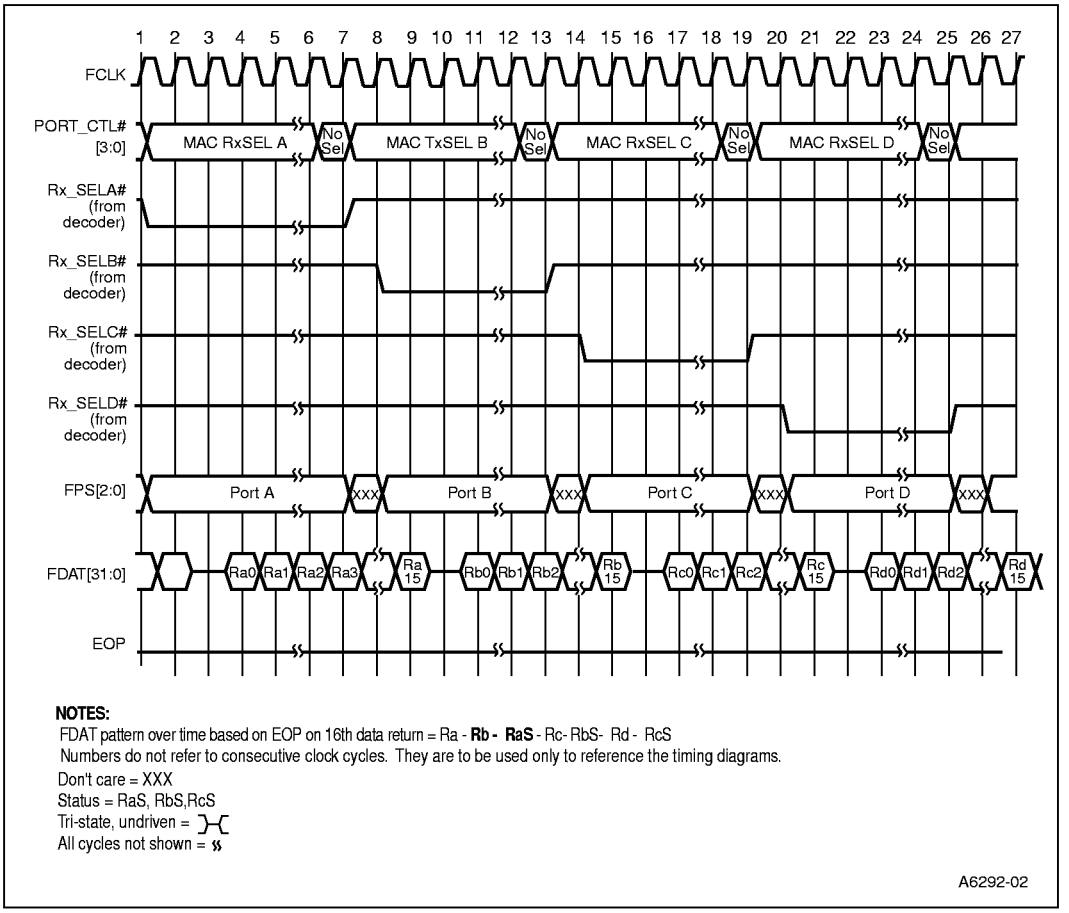
Figure 30: 64-Bit Bidirectional IX Bus Timing - Consecutive Transmits with Prepend



NOTES:
Numbers do not refer to consecutive clock cycles. They are to be used only to reference the timing diagrams.
Don't care = XXX
Status = RaS, RbS,RcS
Tri-state, undriven = }-{
All cycles not shown = ≈

A6287-01

Figure 31: 32-Bit Unidirectional IX Bus Timing - Consecutive Receives with No EOP



NOTES:

FDAT pattern over time based on EOP on 16th data return = Ra - **Rb - RaS** - Rc- RbS- Rd - RcS

Numbers do not refer to consecutive clock cycles. They are to be used only to reference the timing diagrams.

Don't care = XXX

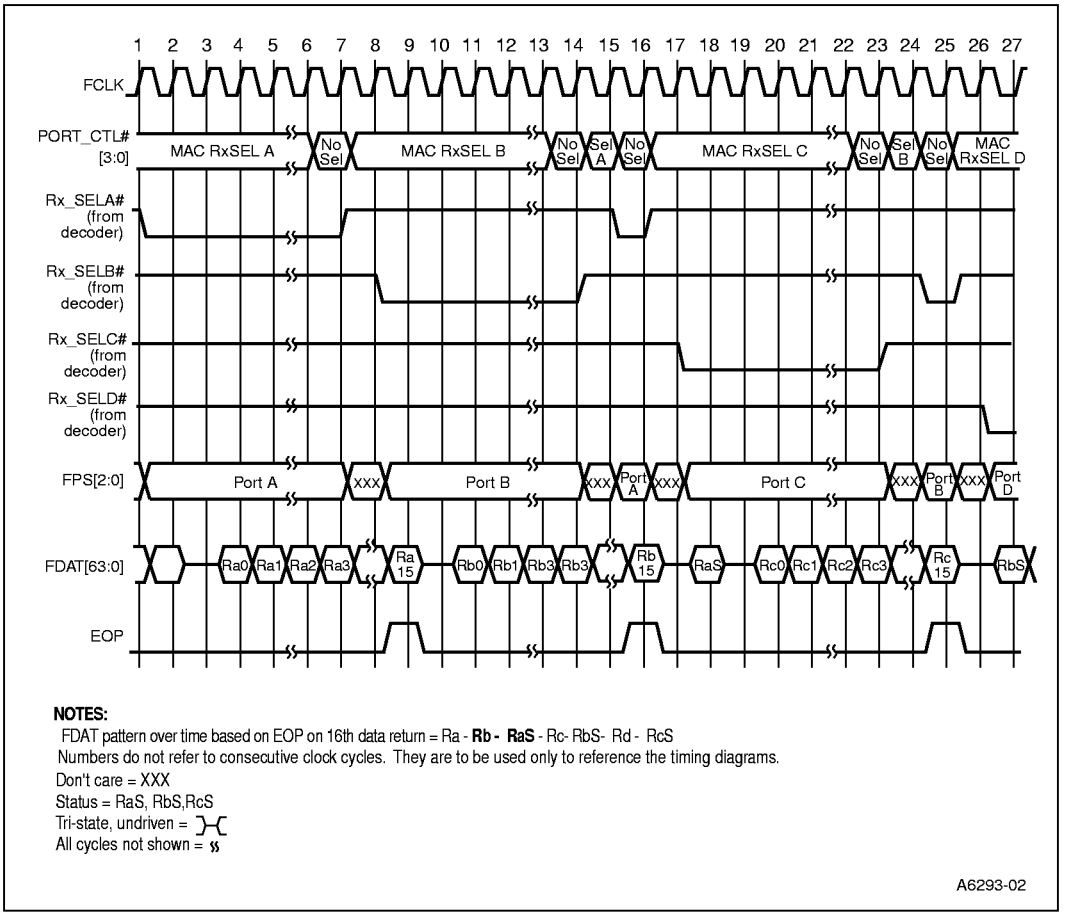
Status = RaS, RbS,RcS

Tri-state, undriven =

All cycles not shown =

A6292-02

Figure 32: 32-Bit Unidirectional IX Bus Timing - Consecutive Receives with EOP on 16th Data Return



NOTES:

FDAT pattern over time based on EOP on 16th data return = Ra - **Rb - RaS** - Rc- RbS- Rd - RcS

Numbers do not refer to consecutive clock cycles. They are to be used only to reference the timing diagrams.

Don't care = XXX

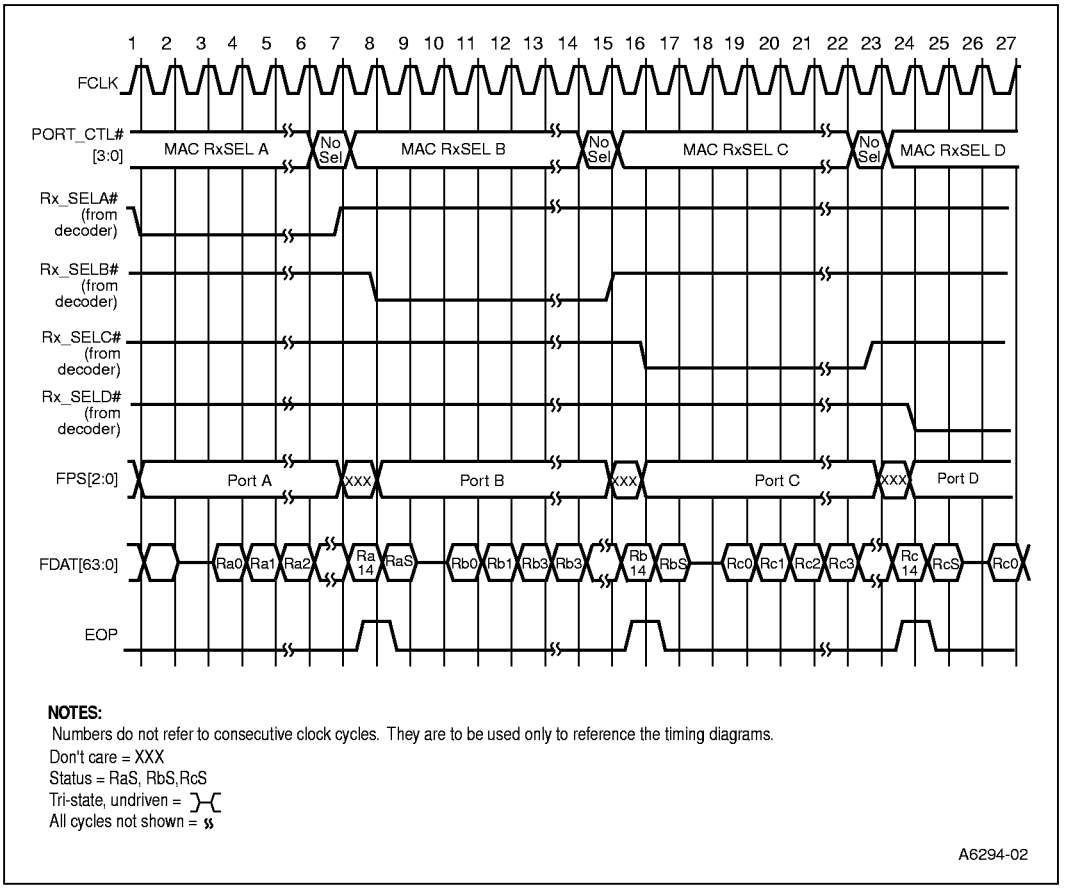
Status = RaS, RbS,RcS

Tri-state, undriven =)-(

All cycles not shown = ≈

A6293-02

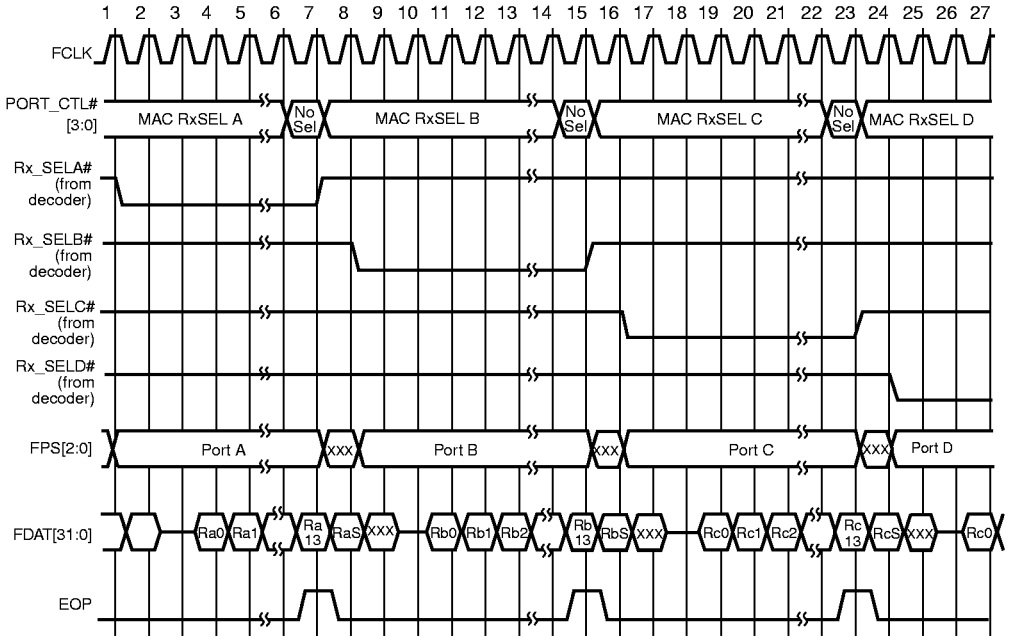
Figure 33: 32-Bit Unidirectional IX Bus Timing - Receive with EOP on 15th Data Return



NOTES:
Numbers do not refer to consecutive clock cycles. They are to be used only to reference the timing diagrams.
Don't care = XXX
Status = RaS, RbS,RcS
Tri-state, undriven = }-{
All cycles not shown = ≈

A6294-02

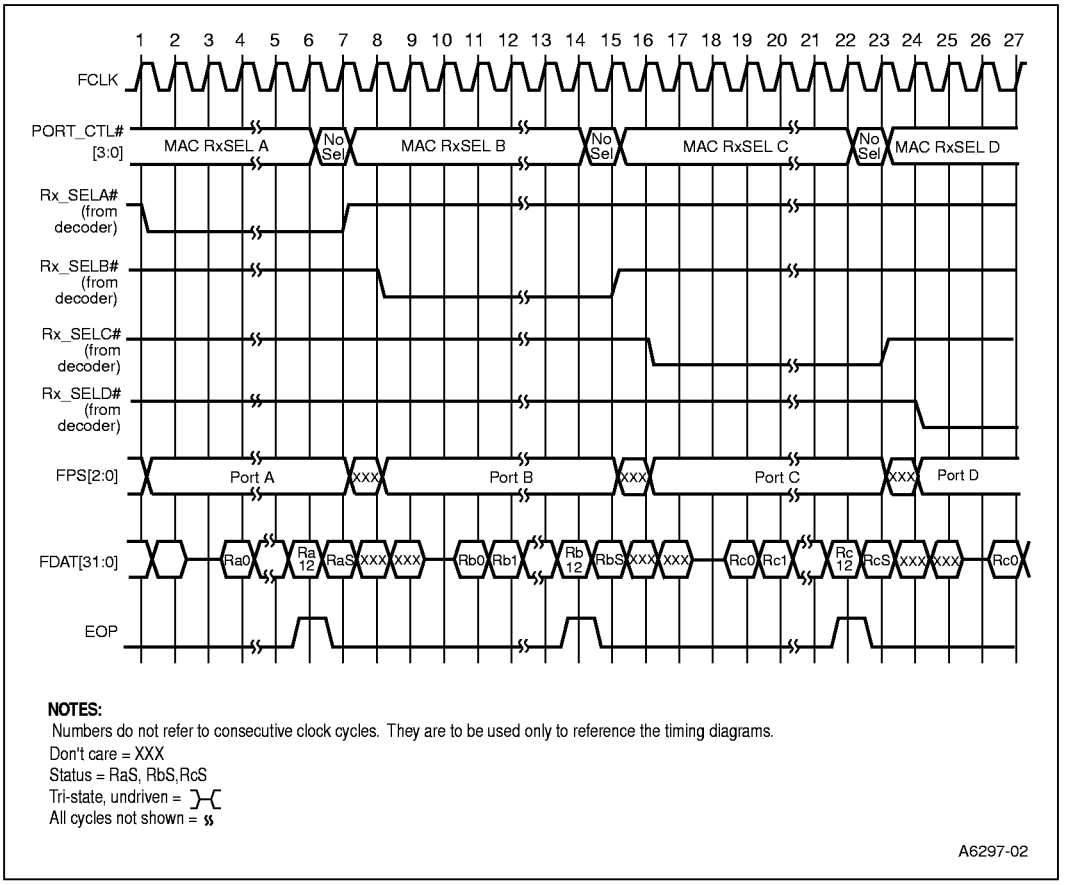
Figure 34: 32-Bit Unidirectional IX Bus Timing - Receive with EOP on 14th Data Return



NOTES:
Numbers do not refer to consecutive clock cycles. They are to be used only to reference the timing diagrams.
Don't care = XXX
Status = RaS, RbS,RcS
Tri-state, undriven =
All cycles not shown =

A6296-02

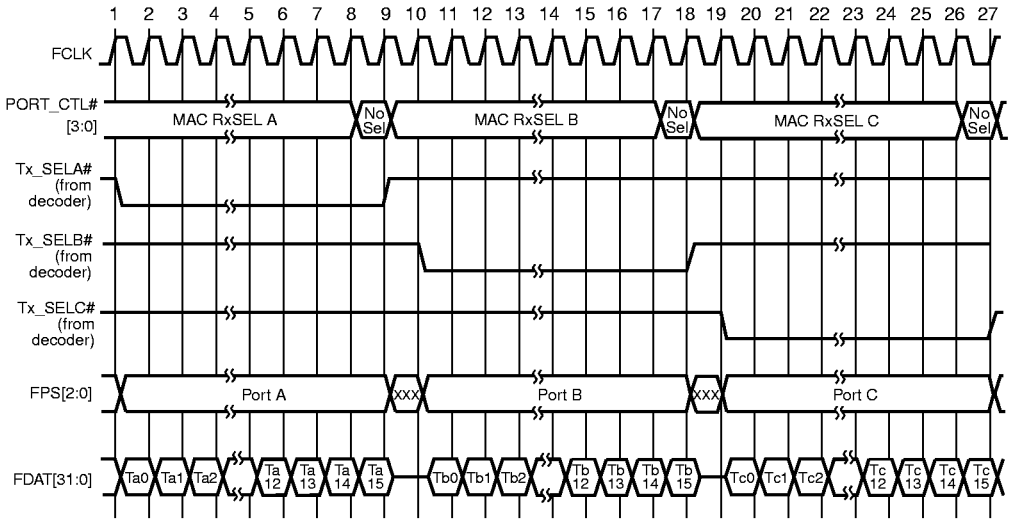
Figure 35: 32-Bit Unidirectional IX Bus Timing - Consecutive Receives with EOP on 1st Through 13th Data Return (13th Data Return Shown)



NOTES:
Numbers do not refer to consecutive clock cycles. They are to be used only to reference the timing diagrams.
Don't care = XXX
Status = RaS, RbS,RcS
Tri-state, undriven = ⟩⟨
All cycles not shown = ≋

A6297-02

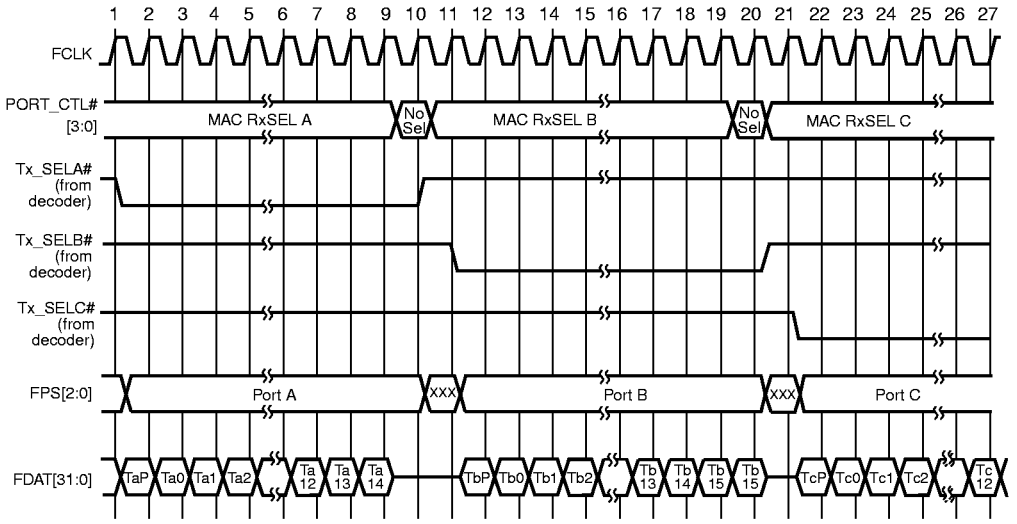
Figure 36: 32-Bit Unidirectional IX Bus Timing - Consecutive Transmits



NOTES:
Numbers do not refer to consecutive clock cycles. They are to be used only to reference the timing diagrams.
Don't care = XXX
Status = RaS, RbS,RcS
Tri-state, undriven = }-{
All cycles not shown = ≈

A6298-01

Figure 37: 32-Bit Unidirectional IX Bus Timing - Consecutive Transmits with Prepend



NOTES:
Numbers do not refer to consecutive clock cycles. They are to be used only to reference the timing diagrams.
Don't care = XXX
Status = RaS, RbS,RcS
Tri-state, undriven = }-{
All cycles not shown = ≈

A6299-01

4.3.7.4 RDYBus

Figure 38: Consecutive Fetch Ready Flags, 1-2 MACs (with No External Registered Decoder) - RDYBUS_TEMPLATE_CTL[10]=1

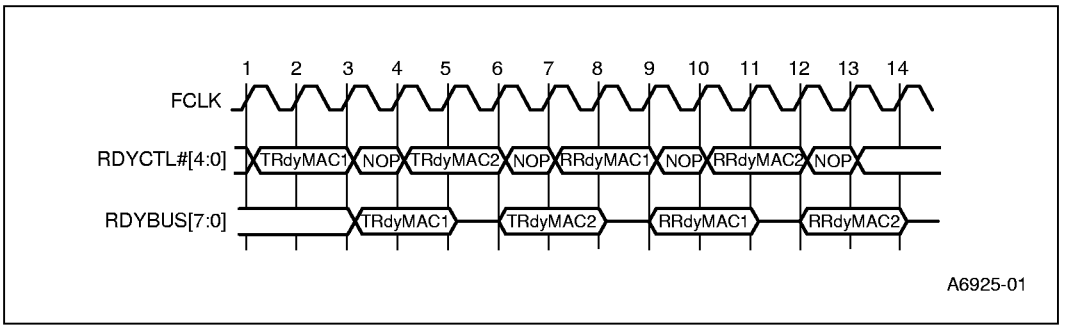


Figure 39: Consecutive Fetch Ready Flags, 3+ MACs (with External Decoder) - RDYBUS_TEMPLATE_CTL[10]=0

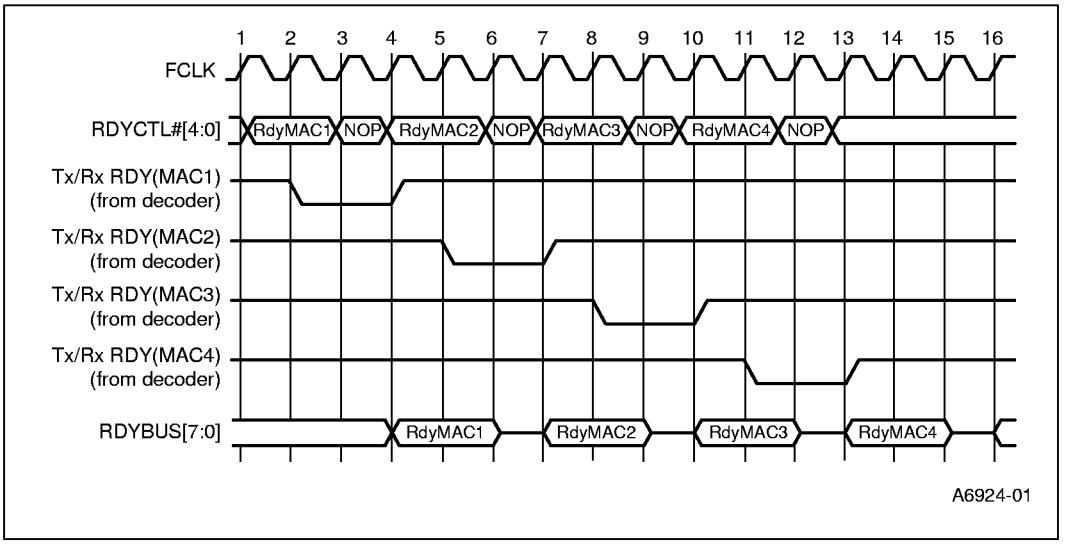


Figure 40: Fetch Ready Flags, Get/Send Commands, 1-2 MACs (with No External Registered Decoder) - RDYBUS_TEMPLATE_CTL[10]=1

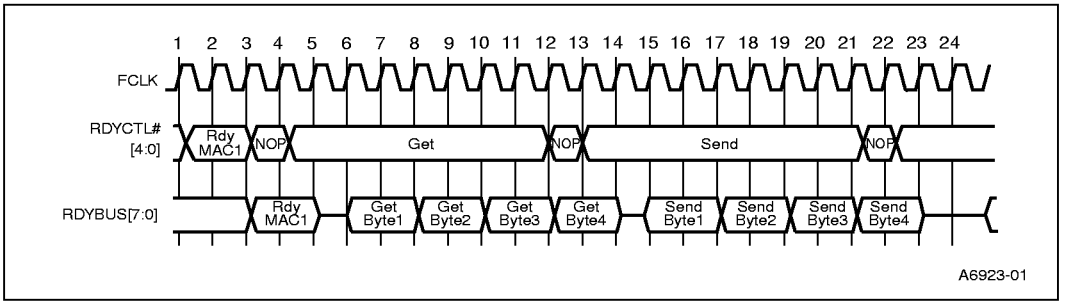


Figure 41: Fetch Ready Flags, Get/Send Commands, 3+ MACs (with No External Registered Decoder) - RDYBUS_TEMPLATE_CTL[10]=0

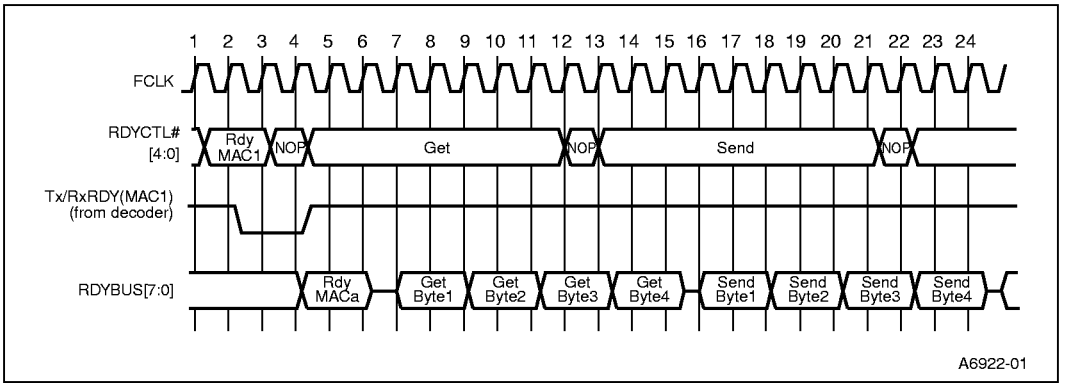


Figure 42: Ready Bus Control Timing, Fetch Ready Flags - Flow Control - Fetch Ready Flags, 1-2 MACs (with No External Registered Decoder) - RDYBUS_TEMPLATE_CTL[10]=1

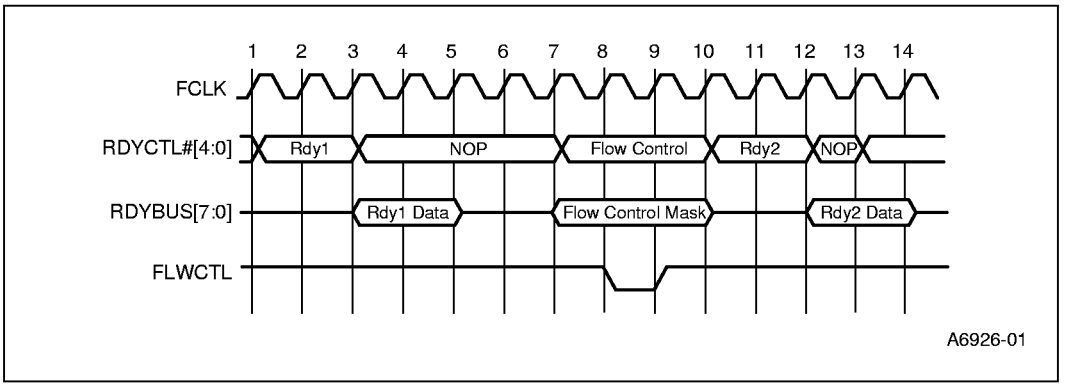
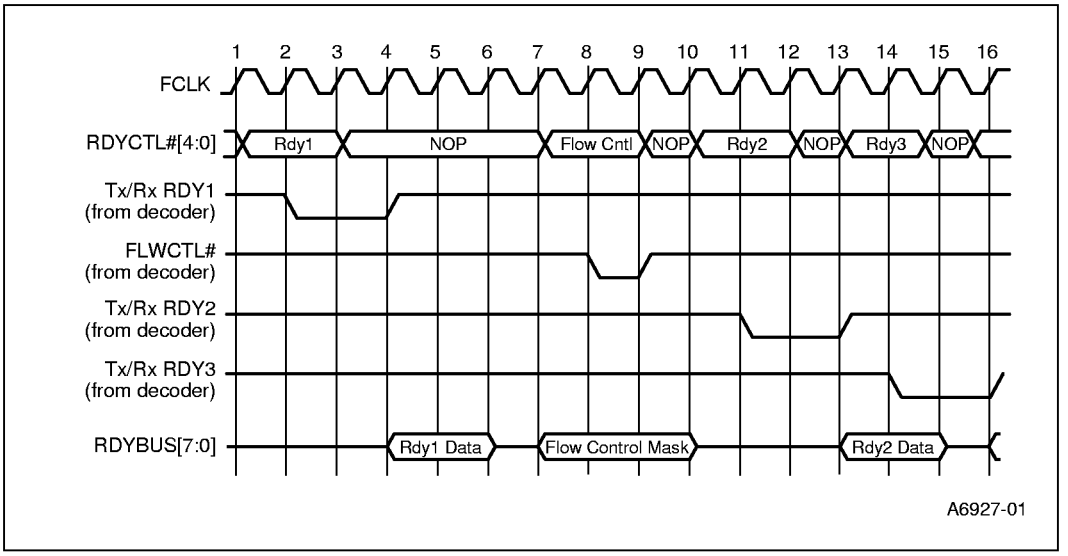


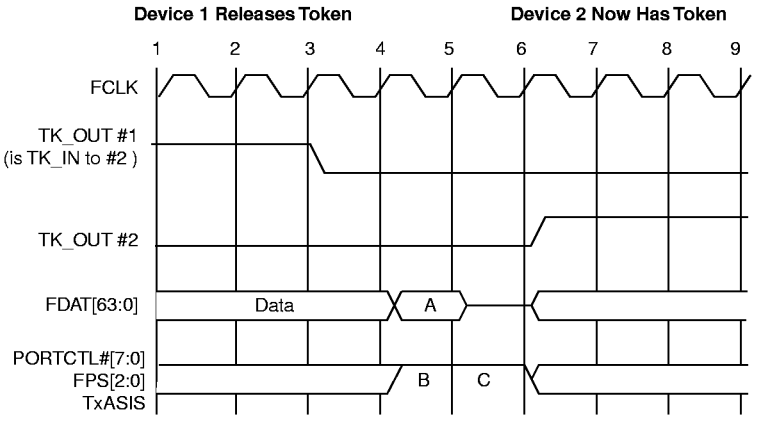
Figure 43: Ready Bus Control Timing, Fetch Ready Flags - Flow Control - Fetch Ready Flags, 1-2 MACs (with No External Registered Decoder) - RDYBUS_TEMPLATE_CTL[10]=0



4.3.7.5 TK_IN/TK_OUT

The following timing diagrams show the transition from one IX Bus owner to another. Note that prior to giving up the bus, the PORTCTL[4:0] signals are driven high which will not select any ports. Then the signal is tri-stated and held up with weak pull-up resistors.

Figure 44: IX Bus Ownership Passing



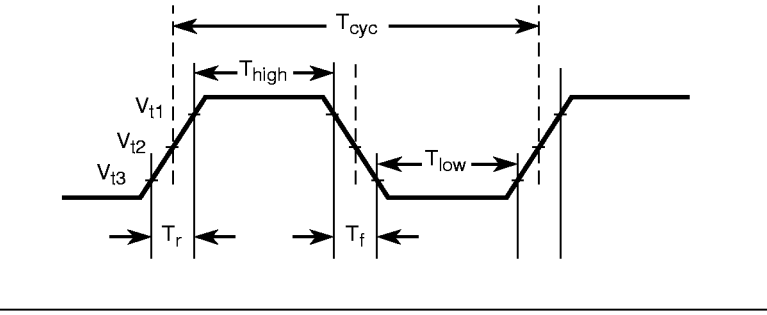
Notes:
A = Driven by the IPX1200 Network Processor #1 if the transfer is a Tx, not driven if the transfer is a Rx.
B = Driven high for one cycle by the IXP1200 #2 (no port is selected) then tristated.
C = Weak external pull-up resistors will be required on PORTCTL#[7:0], FPS[2:0] and TxASIS.

A7005-01

4.3.8 SRAM Interface

4.3.8.1 SRAM SCLK Signal AC Parameter Measurements

Figure 45: SRAM SCLK Signal AC Parameter Measurements



A6992-01

Vt1 = 0.5*VDDX
Vt2 = 0.4*VDDX
Vt3 = 0.3*VDDX

Table 37: SRAM SCLK Signal AC Parameter Measurements

Symbol	Parameter	Minimum	Maximum	Unit
Freq	Clock frequency	tbd	0.5*Fcore	MHz
Tc	Cycle time	12	tbd	ns
Thigh	Clock high time	5	---	ns
Tlow	Clock low time	5	---	ns
Voh	Output high voltage	2.4	---	V
Vol	Output low voltage	---	0.4	V
Tr, Tf	SCLK rise/fall time[1]	0.5	1	ns

1. Not tested. Guaranteed by design.

4.3.8.2 SRAM Bus Signal Timing

Figure 46: SRAM Bus Signal Timing

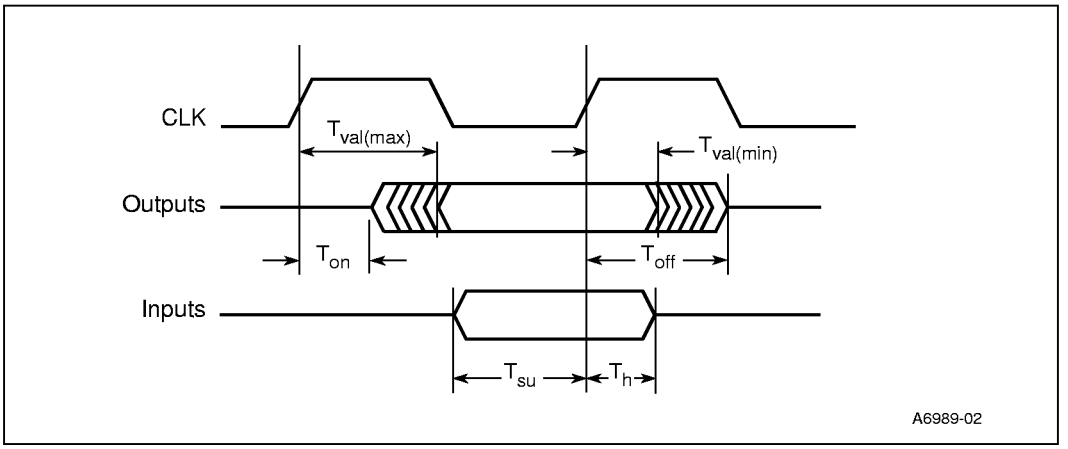


Table 38: SRAM Bus Signal Timing

Symbol	Parameter	Minimum	Maximum	Unit
Tval	Clock-to-signal valid delay	2	6	ns
Tsu	Input signal valid setup time before clock	3.5 (Flowthru SRAMs) 7.5 (Pipelined SRAMs)	---	ns
Th	Input signal hold time from clock	1	---	ns
Ton	Float-to-active delay from clock	1	---	ns
Toff	Active-to-float delay from clock	---	10	ns

4.3.8.3 SRAM Bus - SRAM Signal Protocol and Timing

Figure 47: Pipelined SRAM Read Burst of Eight

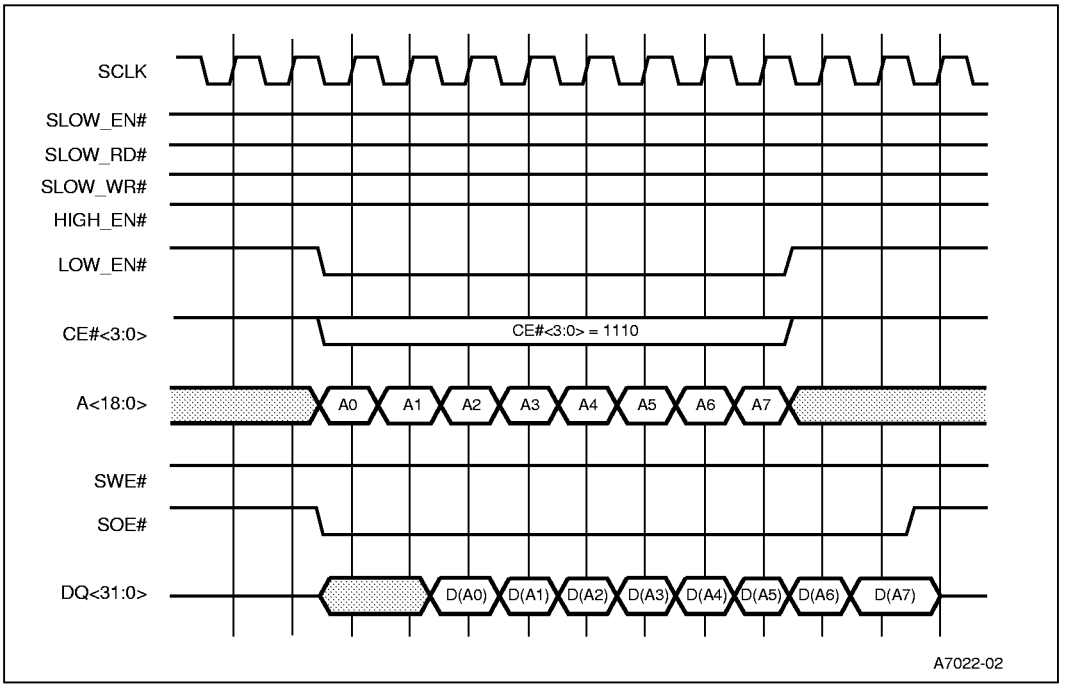


Figure 48: Pipelined SRAM Write Burst of 8 DWords

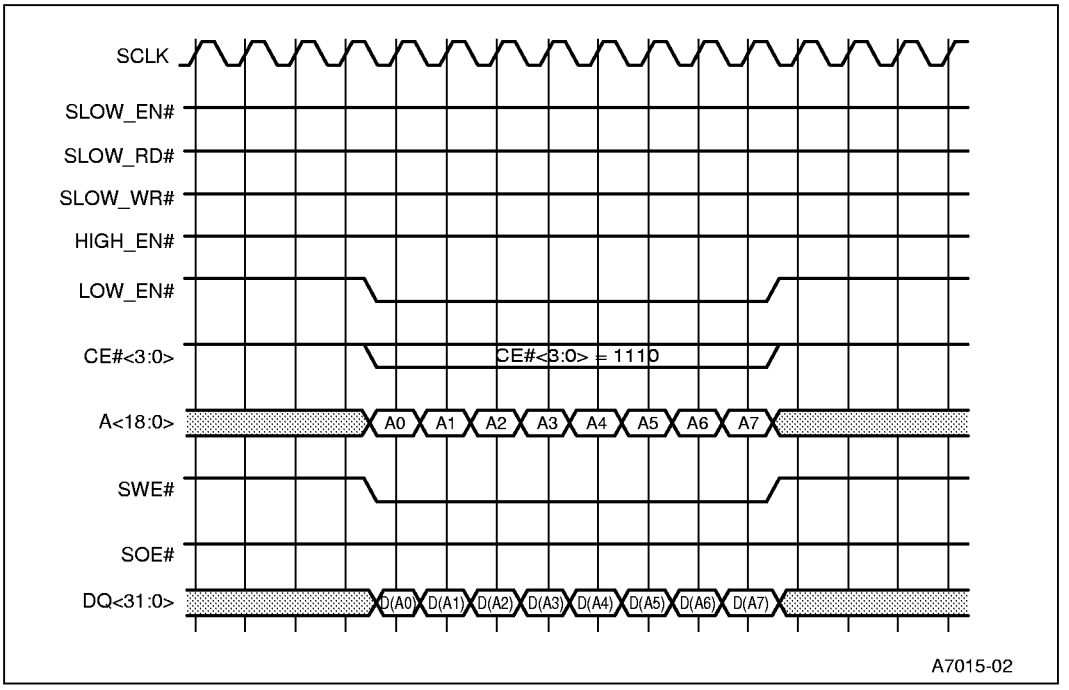
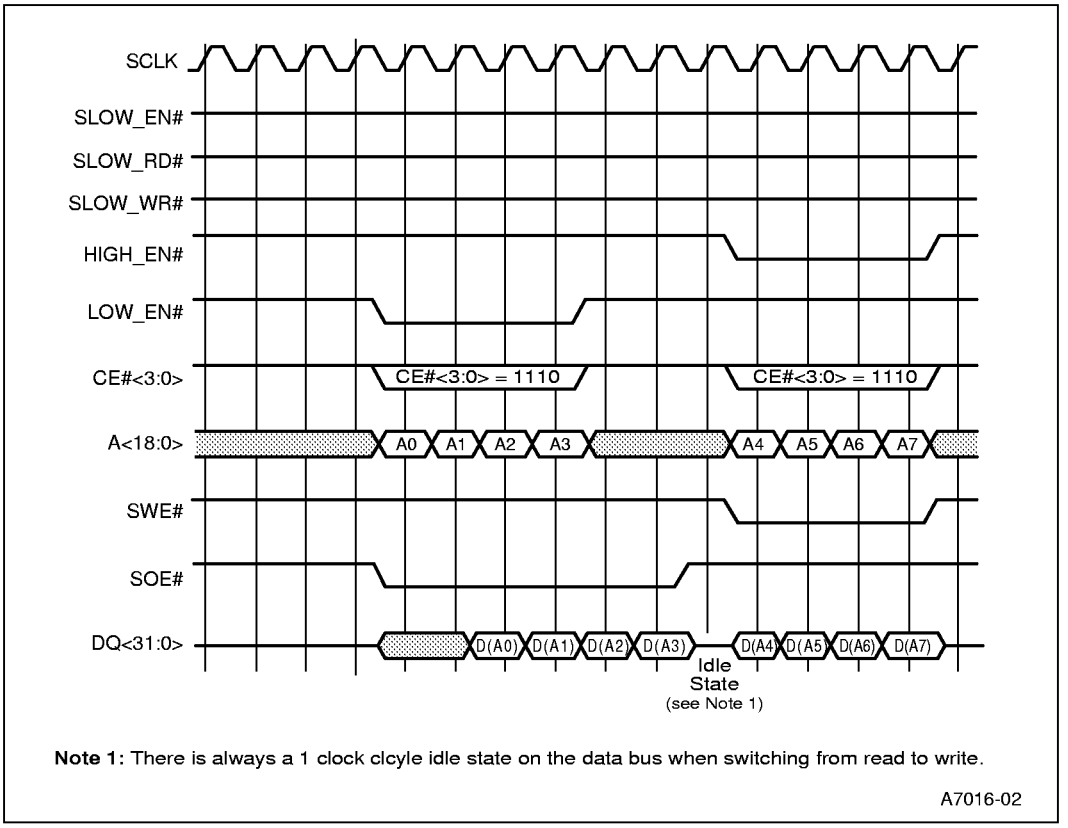


Figure 49: Pipelined SRAM Read Burst of Four From Bank 0 Followed by Write Burst of Four From Bank 8



Note 1: There is always a 1 clock clcyle idle state on the data bus when switching from read to write.

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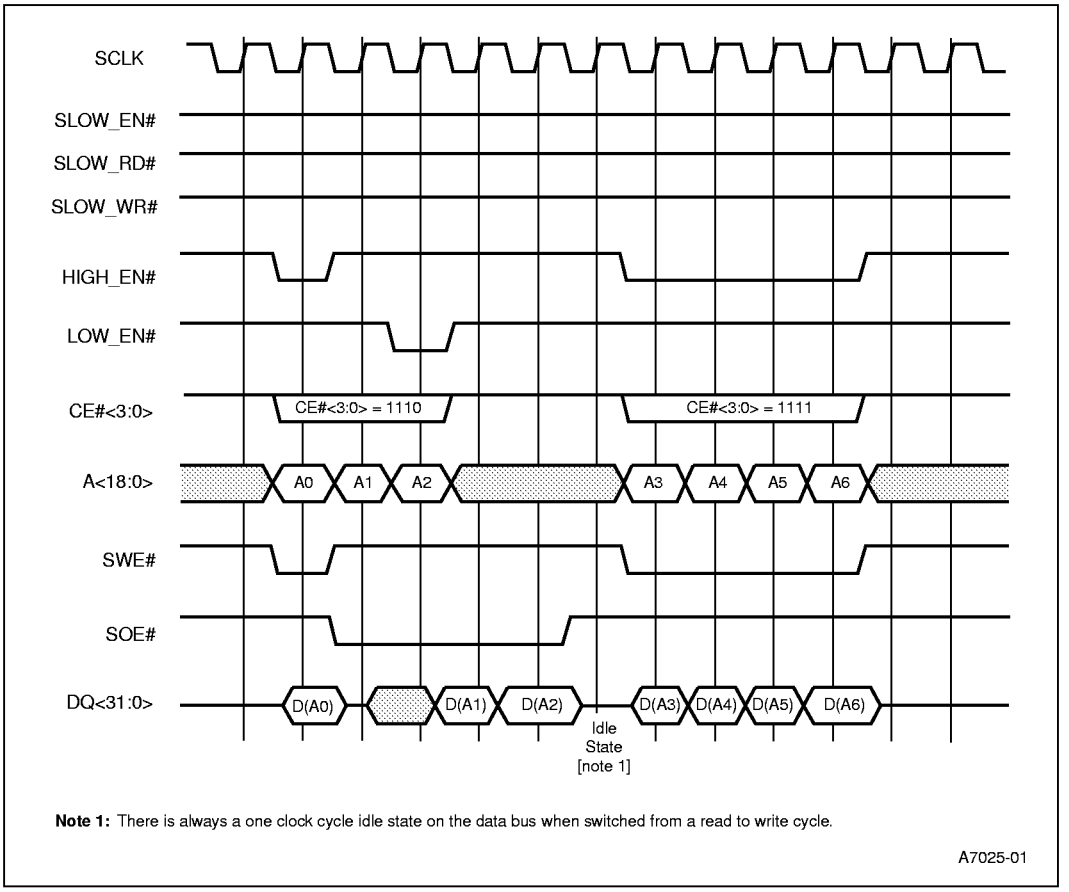
Figure 50: Pipelined SRAM DWord Write Followed by 2 DWord Burst Read Followed by 4 DWord Burst Write



Note 1: There is always a one clock cycle idle state on the data bus when switched from a read to write cycle.

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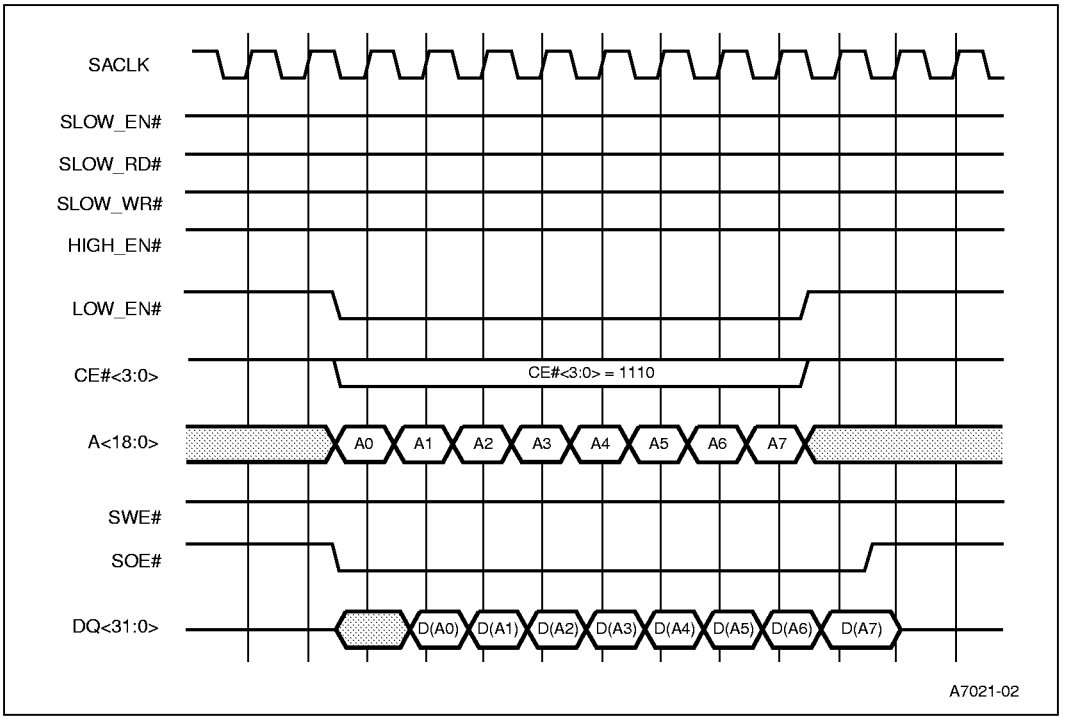
Figure 51: Flowthrough SRAM Read Burst of Eight



4.3.8.4 SRAM Bus - BootROM and SlowPort Timings

Timing for the BootROM and SlowPort areas are programmable through the SRAM configuration registers described in the *IXP1200 Network Processor Programmer's Reference Manual*. The designer should refer to this manual to understand restrictions in selecting timing values. Each timing illustration shows the appropriate register settings to generate the timing shown.

4.3.8.5 SRAM Bus - BootRom Signal Protocol and Timing

Figure 52: BootROM Read

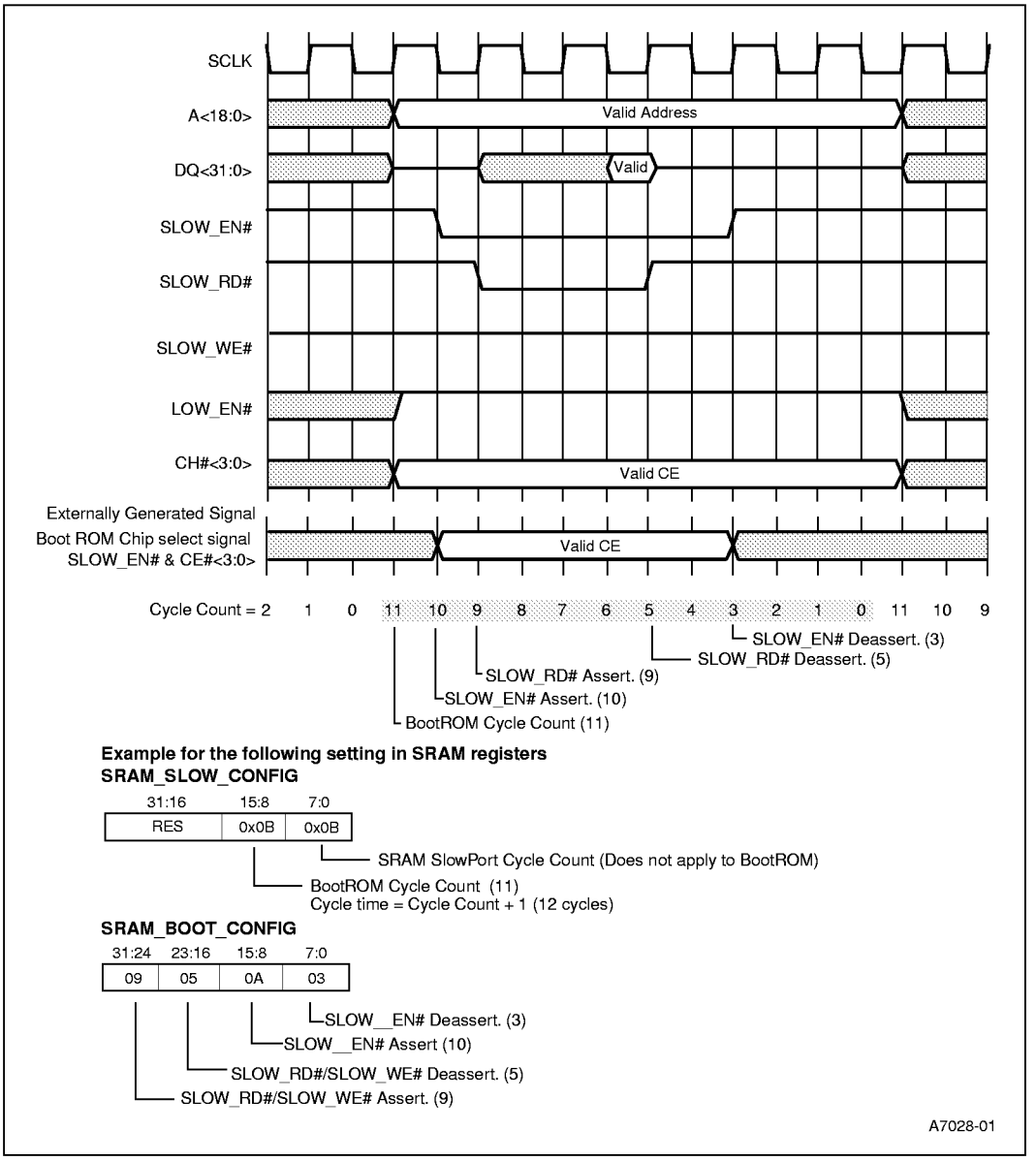


Figure 53: BootROM Write

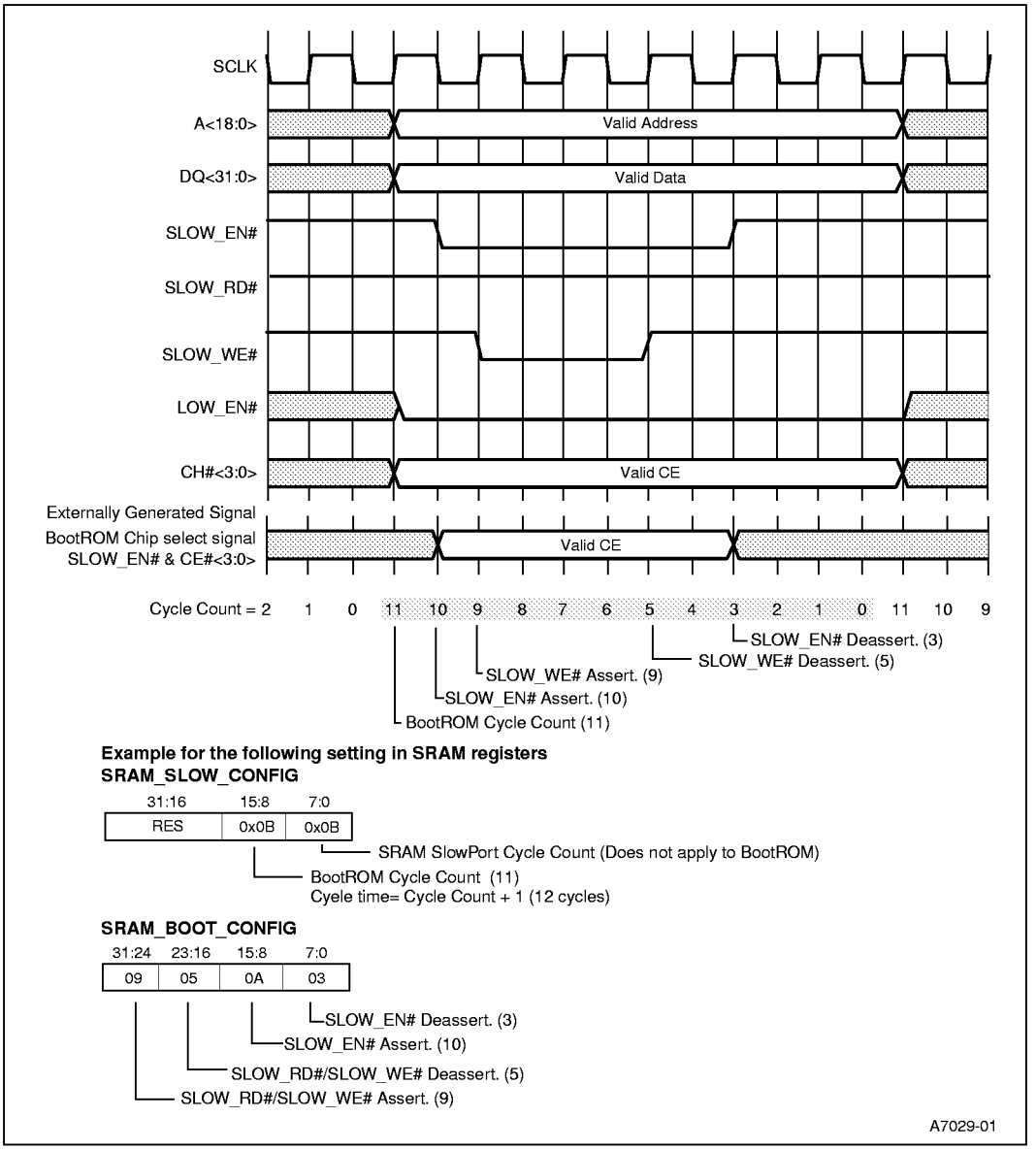
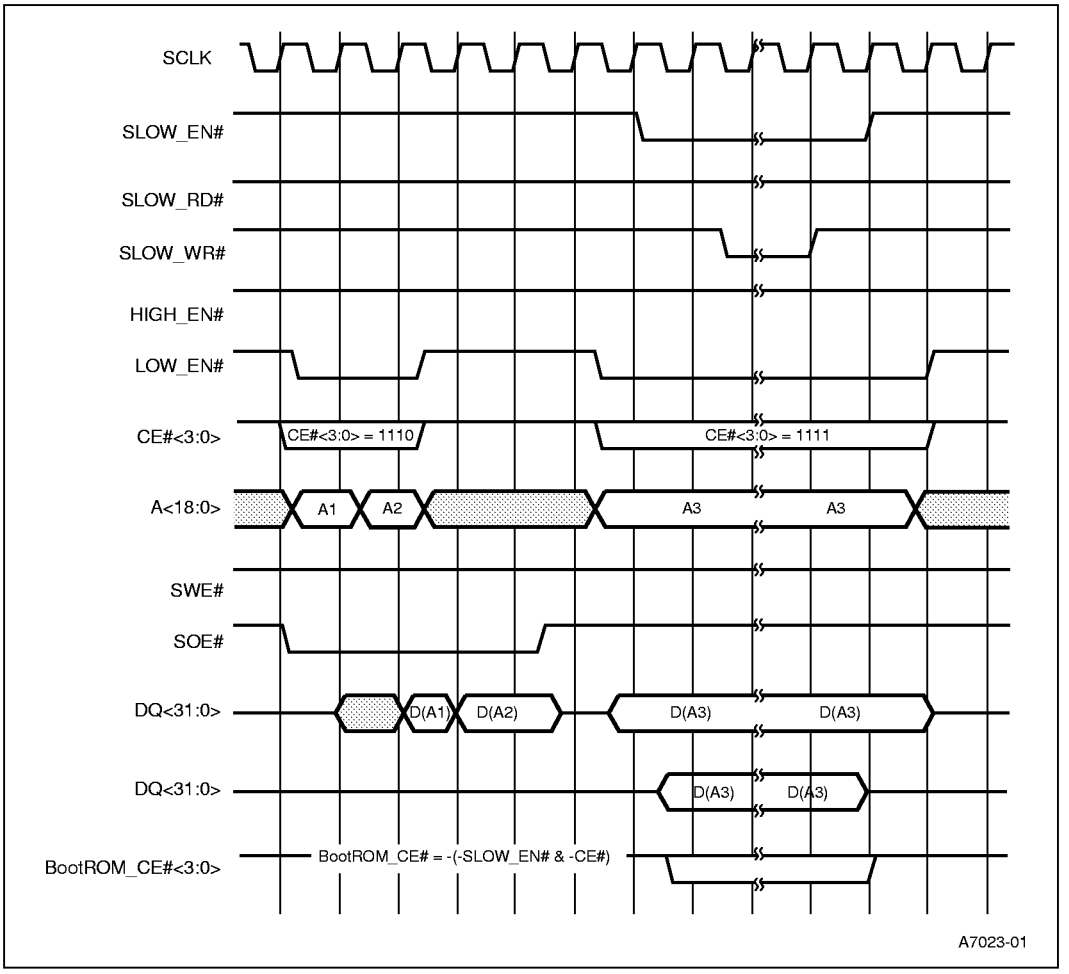


Figure 54: Pipelined SRAM Two DWord Burst Read Followed by BootROM Write



4.3.8.6 SRAM Bus - Slow-Port Device Signal Protocol and Timing

Figure 55: SRAM SlowPort Read

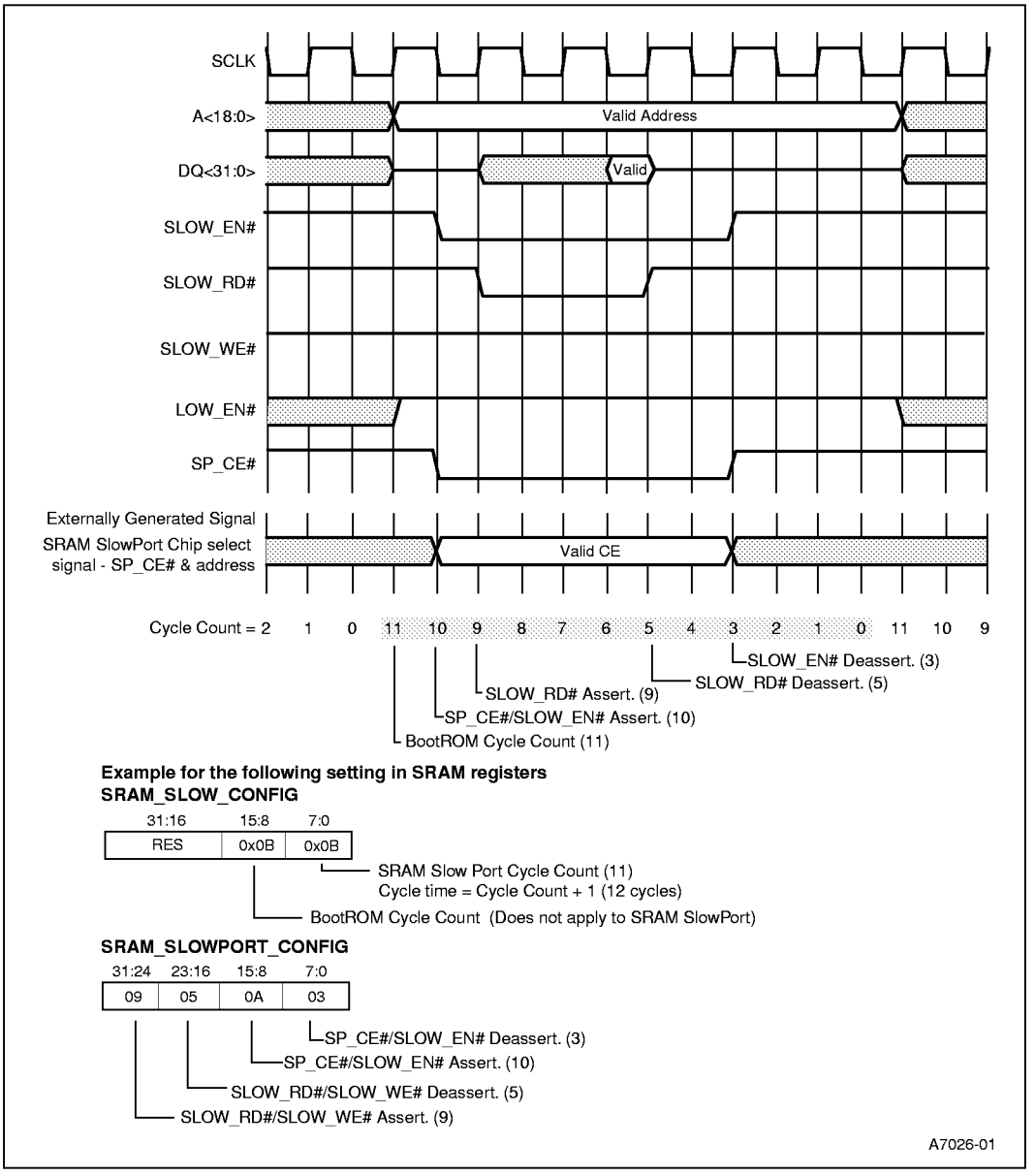


Figure 56: SRAM SlowPort Write

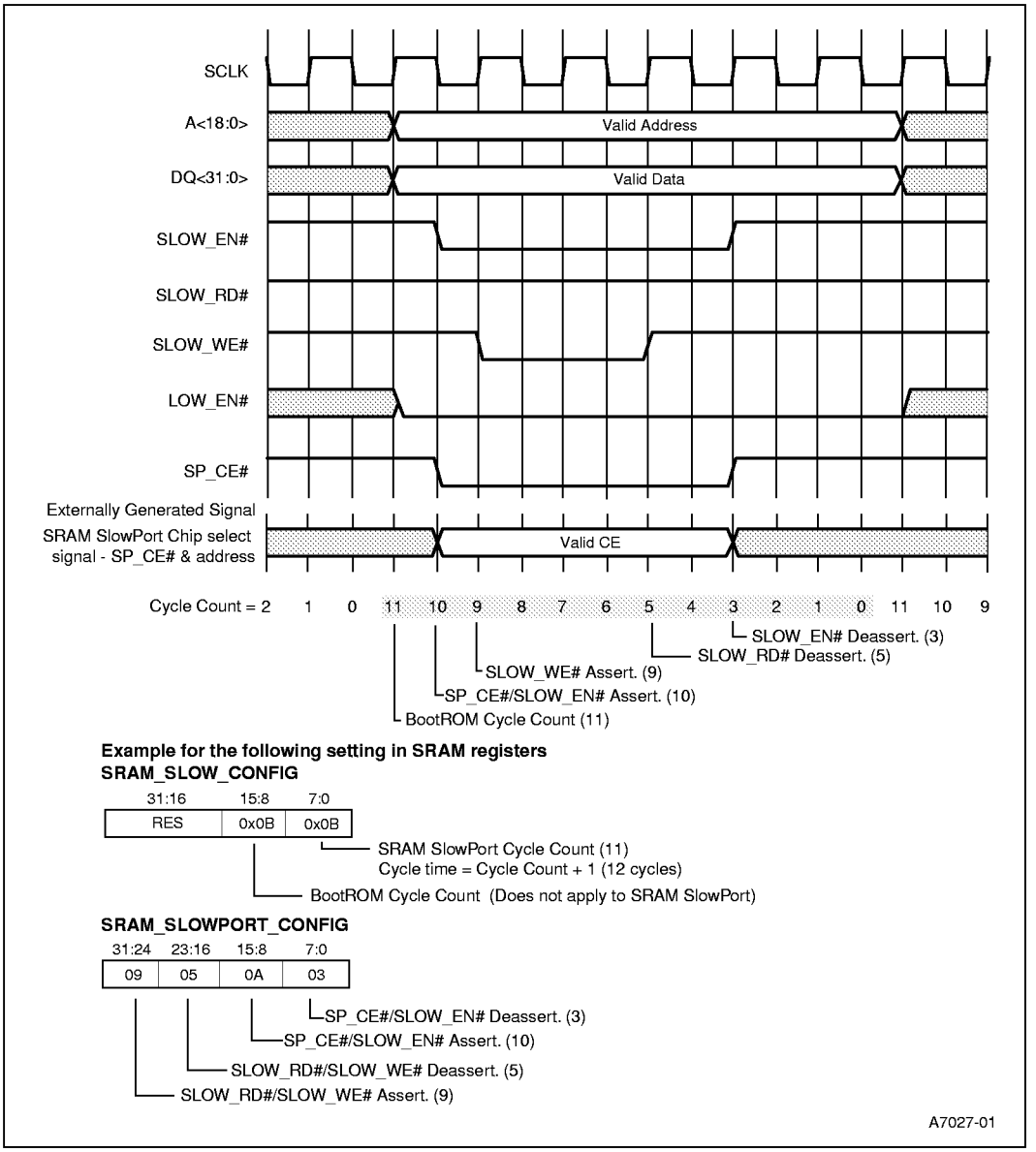
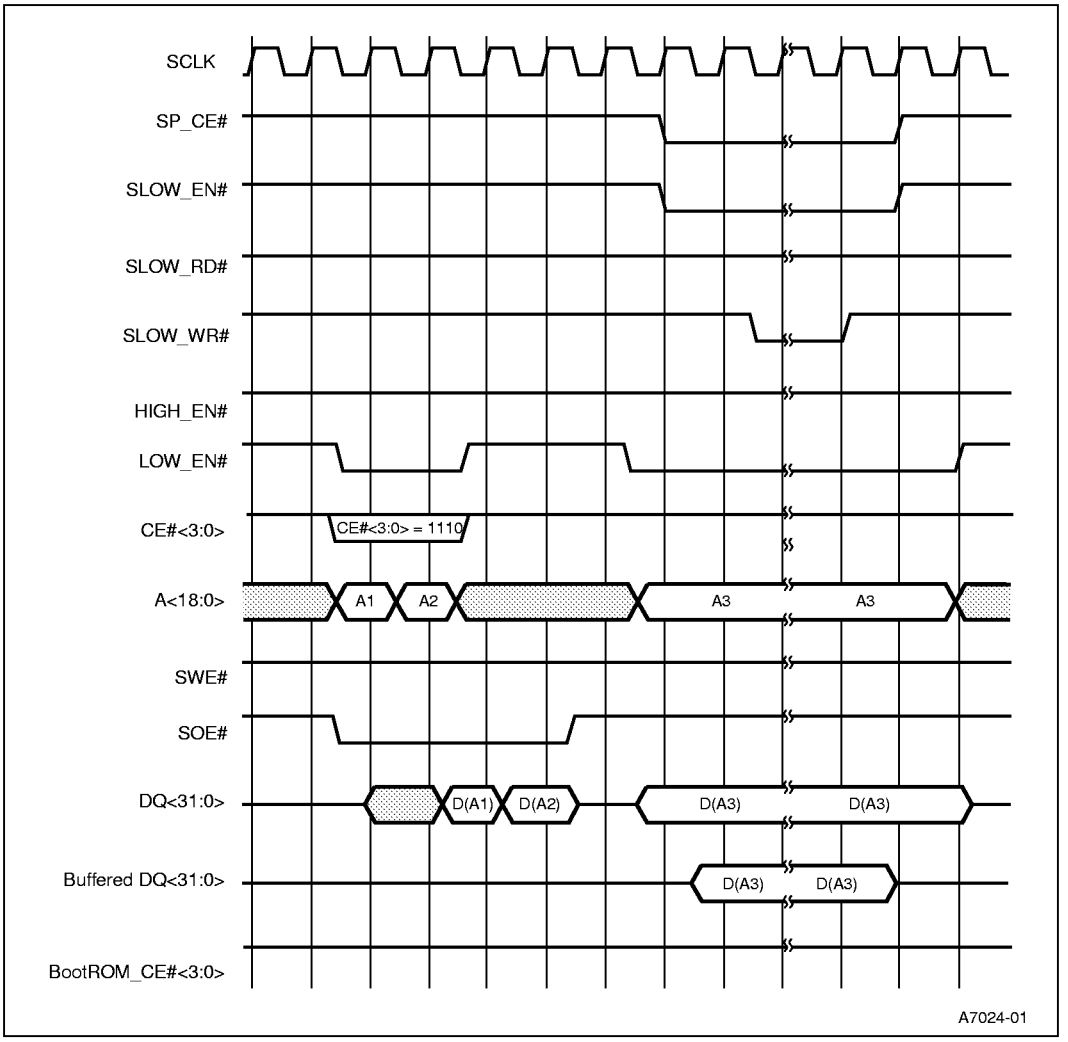


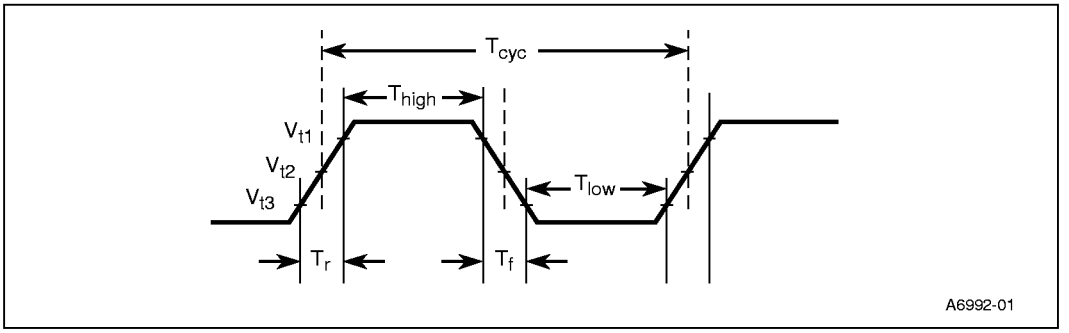
Figure 57: Pipelined SRAM 2 Dword Burst Read Followed By SlowPort Write



4.3.9 SDRAM Interface

4.3.9.1 SDCLK AC Parameter Measurements

Figure 58: SDCLK AC Timing Diagram



Vt1 = 0.5*VDDX
Vt2 = 0.4*VDDX
Vt3 = 0.3*VDDX

Table 39: SDCLK AC Parameter Measurements

Symbol	Parameter	Minimum	Maximum	Unit
Freq	Clock frequency	tbd	0.5*Fcore	MHz
Tcyc	Cycle time	12	tbd	ns
Th	Clock high time	5	---	ns
Tl	Clock low time	5	---	ns
Voh	Output high voltage	2.4	---	V
Vl	Output low voltage	---	0.4	V
Tr, Tf	SDCLK rise/fall time[1]	0.5	1	ns

1. Not tested. Guaranteed by design.

4.3.9.2 SDRAM Bus Signal Timing

Figure 59: SDRAM Bus Signal Timing

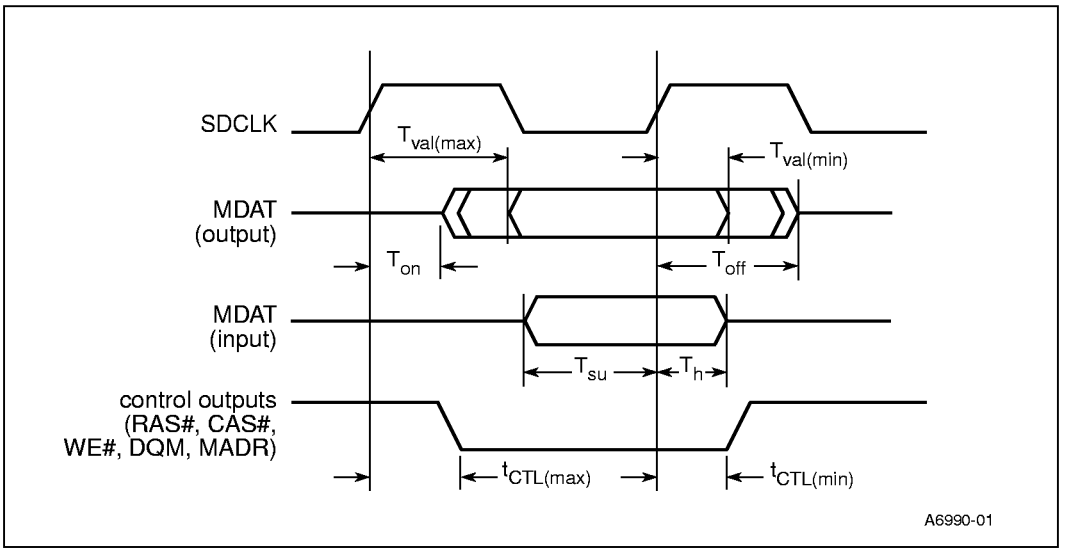
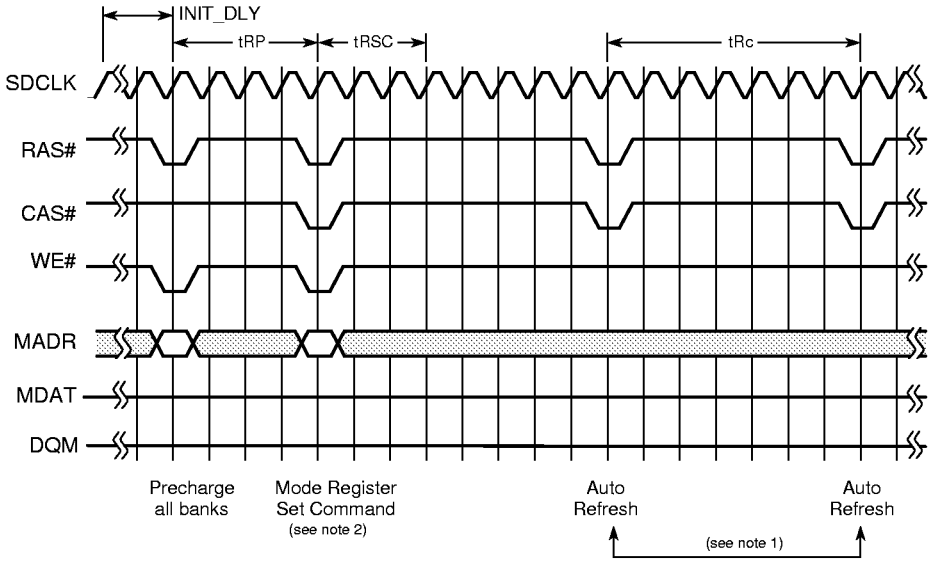


Table 40: SDRAM Bus Signal Timing Parameters

Symbol	Parameter	Minimum	Maximum	Unit
Tval	Clock-to-data output valid delay	1	4.5	ns
Tsu	Input data setup time before clock	0.5 * Tcyc	---	ns
Th	Input data hold time from clock	1	---	ns
Ton	Float-to-active data delay from clock	1	---	ns
Toff	Data Active-to-float delay from clock	---	10	ns
tCTL	Clock to control output low valid delay	4	9	ns

4.3.9.3 SDRAM Signal Protocol

Figure 60: SDRAM Initialization Sequence



Notes:
1. Number of total initialization phase refresh cycles programmed as INIT_RFRSH value in register SDRAM_MEMINIT.
2. Burst length and CAS latency values programmed as BURSTL value in register SDRAM_MEMCTL0 emitted in this cycle.
3. INIT_DLY, tRSC values programmed into register SDRAM_MEMINIT.
4. tRP, tRC values programmed into register SDRAM_MEMCTL1
5. tRSC is minimum SDRAM programmable register value. In actual use, refresh cycles will not occur immediately after tRSC cycles due to SDRAM unit internal pipeline delays.

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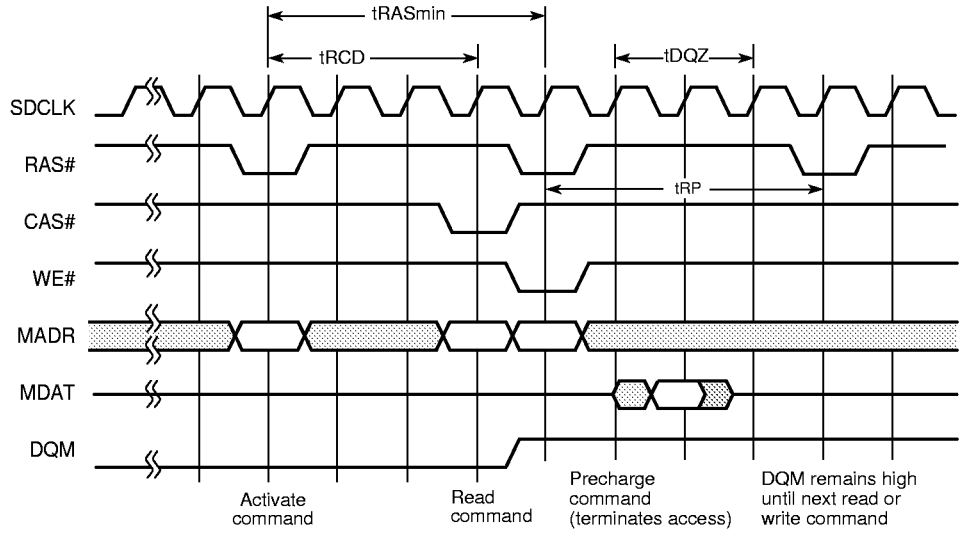
Figure 61: SDRAM Read Cycle



Notes:
1. Parameters tRWT, tDPL, tDQZ, tRC, tRRD, tRCD, tRASmin, and tRP programmed into register SDRAM_MEMCTL1
2. CAS Latency value (CASL) = 3 programmed in SDRAM_MEMCTL0

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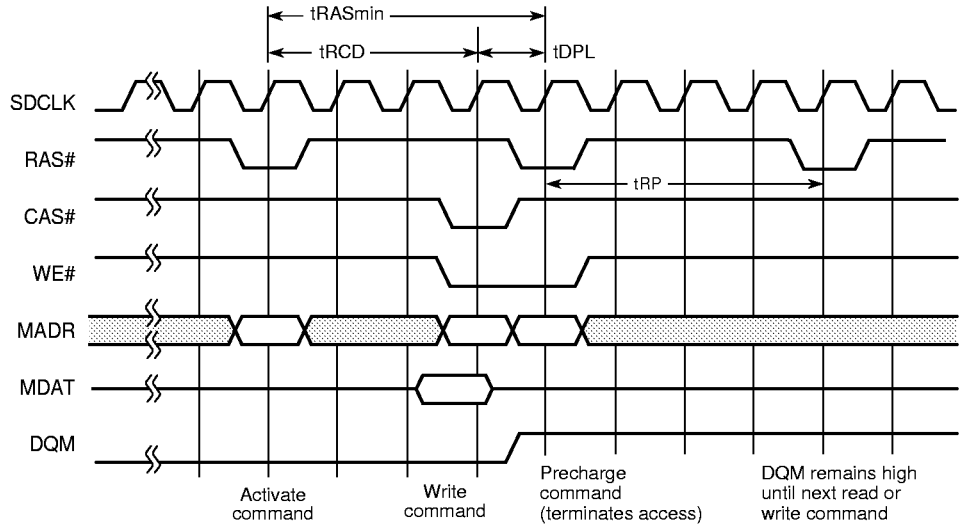
Figure 62: SDRAM Write Cycle



Notes:
1. Parameters tRWT, tDPL, tDQZ, tRC, tRRD, tRCD, tRASmin, and tRP programmed into register SDRAM_MEMCTL1
2. CAS Latency value (CASL) = 3 programmed in SDRAM_MEMCTL0

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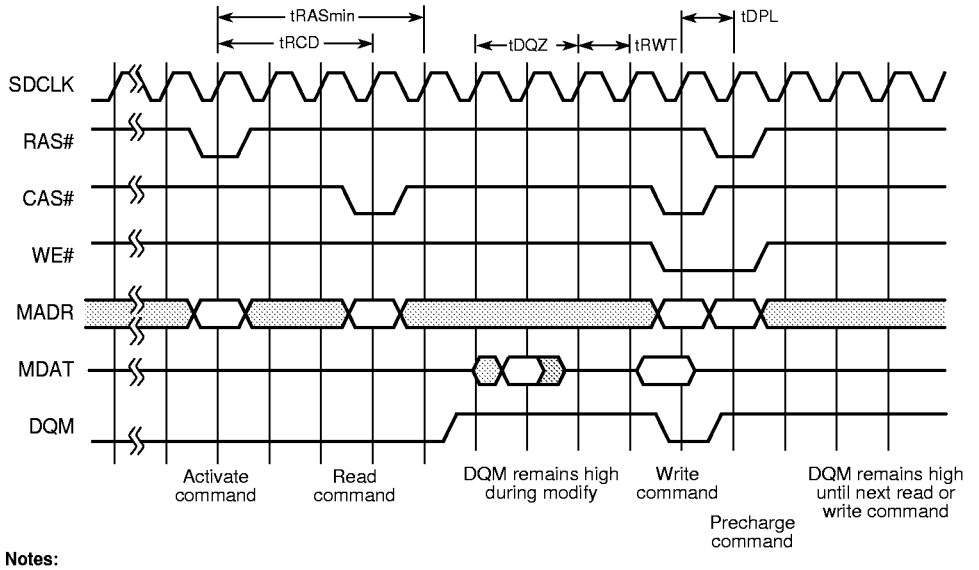
Figure 63: SDRAM Read-Modify-Write Cycle



Notes:
1. Parameters tRWT, tDPL, tDQZ, tRC, tRRD, tRCD, tRASmin, and tRP programmed into register SDRAM_MEMCTL1
2. CAS Latency value (CASL) = 3 programmed in SDRAM_MEMCTL0

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4.4 Asynchronous Signal Timing Descriptions

RESET_IN must remain asserted for 150 ms after VDD and VDDX are stable to properly reset the IXP1200 Network Processor.

RESET_OUT is asserted for all types of reset (hard, watchdog, and software) and appears on the pin asynchronously to all clocks.

TRST# TBD.

GPIO<3:0> are read and written under software control. When writing a value to these pins, the pins transition approximately 20 ns after the write is performed. When reading these pins, the signal is first synchronized to the internal clock and must be valid for at least 20 ns before it is visible to a processor read.

TXD, RXD are asynchronous relative to any device outside the IXP1200 Network Processor.

SECTION 5 - MECHANICAL SPECIFICATIONS

5.1 Package Dimensions

The IXP1200 Network Processor is contained in a 432-
BGA package, as shown in the following illustrations.

Figure 64: IXP1200 Network Processor Part Marking (TBD)

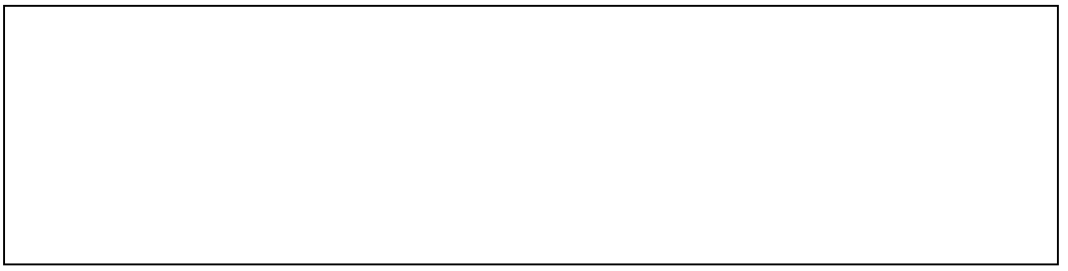


Figure 65: 432-BGA Package - Bottom View

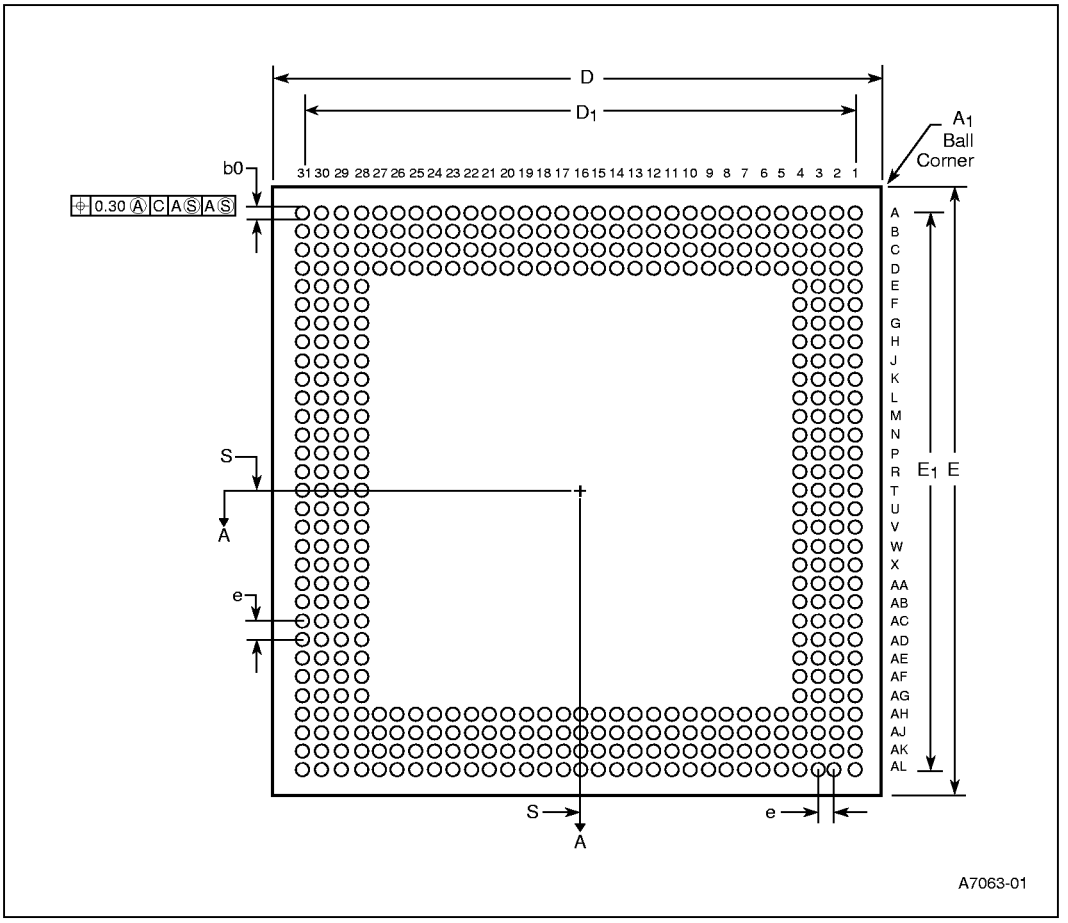


Figure 66: IXP1200 Network Processor Side View

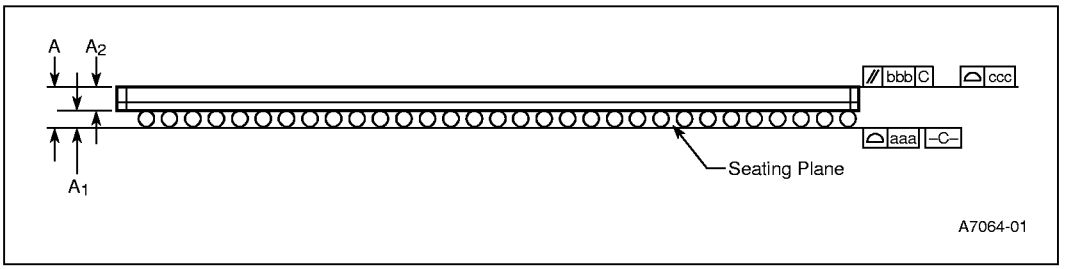
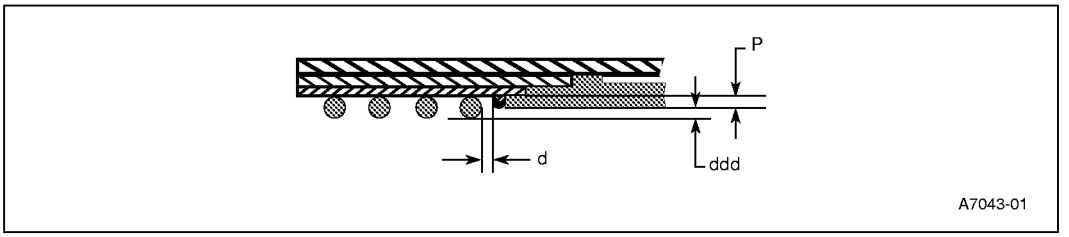


Figure 67: IXP1200 Network Processor A-A Section View



5.2 IXP1200 Network Processor Package Dimensions (mm)

Table 41: IXP1200 Network Processor Package Dimensions (mm)

Symbol	Definition	Minimum	Nominal	Maximum
A	Overall thickness	1.41	1.54	1.67
A_1	Ball height	0.56	0.63	0.70
A_2	Body thickness	0.85	0.91	0.97
D	Body size	39.90	40.00	40.10
D_1	Ball footprint	38.00	38.10	38.20
E	Body size	39.90	40.00	40.10
E_1	Ball footprint	38.00	38.10	38.20
b	Ball diameter	0.60	0.75	0.90
aaa	Coplanarity	--	--	0.15
bbb	Parallel	--	--	0.15
ccc	Top flatness	--	--	0.20
ddd [8]	Seating plane clearance	0.15	0.33	0.50
P	Encapsulation height	0.20	0.30	0.35
S	Solder ball placement	--	--	0.00
M, N	Ball matrix	--	31 x 31	--
M1[7]	Number of rows deep	--	4	--

Table 41: IXP1200 Network Processor Package Dimensions (mm) – continued

Symbol	Definition	Minimum	Nominal	Maximum
d	Minimum distance, encap to balls	--	0.6	--
e	Ball pitch	--	1.27	--

NOTES:
1. All dimensions and tolerances conform to ANSI Y1.45M-1982.
2. Dimension “b” is measured at the maximum solder ball diameter parallel to primary datum “c”.
3. Primary datum “c” and seating plane are defined by the spherical crowns of the solder balls.
4. Pin A1 I.D. marked by ink.
5. Shape at corner, single form.
6. All dimensions are in millimeters.
7. Number of rows in from edge to center.
8. Height from ball seating plane to plane of encapsulant.
9. S is measured with respect to -A- and -B- and defines the position of the center solder ball in the outer row. When there is an odd number of solder balls in the outer row, S=0.000; when there is an even number of solder balls in the outer row, the value S=e/2. S can be either 0.000 or e/2 for each variation.
10. The dimension from the outer edge of the resin dam to the edge of the innermost row of the solder ball pads is to be a minimum of 0.50 mm.

5.3 Package Pin Layout with Power and Ground

Figure 68: IXP1200 Network Processor Package Pin Layout with Power and Ground