Obsolescence Notice

ZARLINK SEMICONDUCTOR

This product is obsolete.

This information is available for your convenience only.

For more information on Zarlink's obsolete products and replacement product lists, please visit

http://products.zarlink.com/obsolete_products/

ISO-CMOS ST-BUS™ Family **MT8926**

ZARLINK SEMICONDUCTOR™

T1 Performance Monitoring Adjunct Circuit (PMAC)

Data Sheet

DS5718 Issue 3 July 1993

Features

- ANSI T1.403 and T1.408 Performance Monitoring and Maintenance Functions
- Operates in conjunction with Mitel's T1/ESF framer circuits (MT8976/77 and MH89760B)
- D3/D4 (SF), and ESF modes of operation
- One and two second timers
- Supports bit-oriented and message-oriented data transfer over the Facility Data Link (FDL)
- ESF and D3/D4 Yellow Alarms, Alarm Indication Signal and Loss of Signal Indication
- Framing Error, CRC Error and Bipolar Violation Error counters
- Alarm interrupts and counter overflow interrupts

Applications

- T1 line performance data collection
- CSU performance monitoring
- ISDN Primary Rate maintenance controller

Ordering Information

MT8926AE	28 Pin Plastic DIP
MT8926AP	28 Pin PLCC

-40°C to +85°C

Description

The MT8926 Performance Monitoring Adjunct Circuit (PMAC) interworks with Mitel's MT8976/77 and MH89760B to provide performance monitoring data, alarms and T1 maintenance features.

It meets the performance monitoring and maintenance requirements of ANSI T1.403 and T1.408, and also supports Channel Service Unit (CSU) requirements.

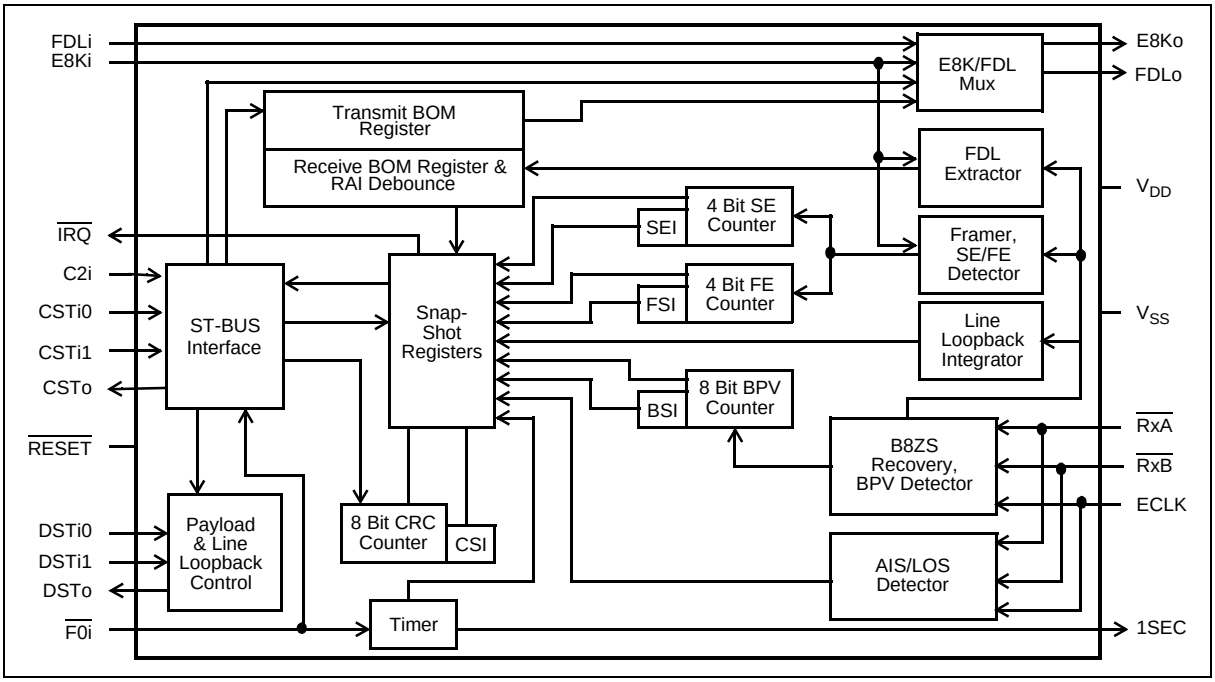


Figure 1 - Functional Block Diagram

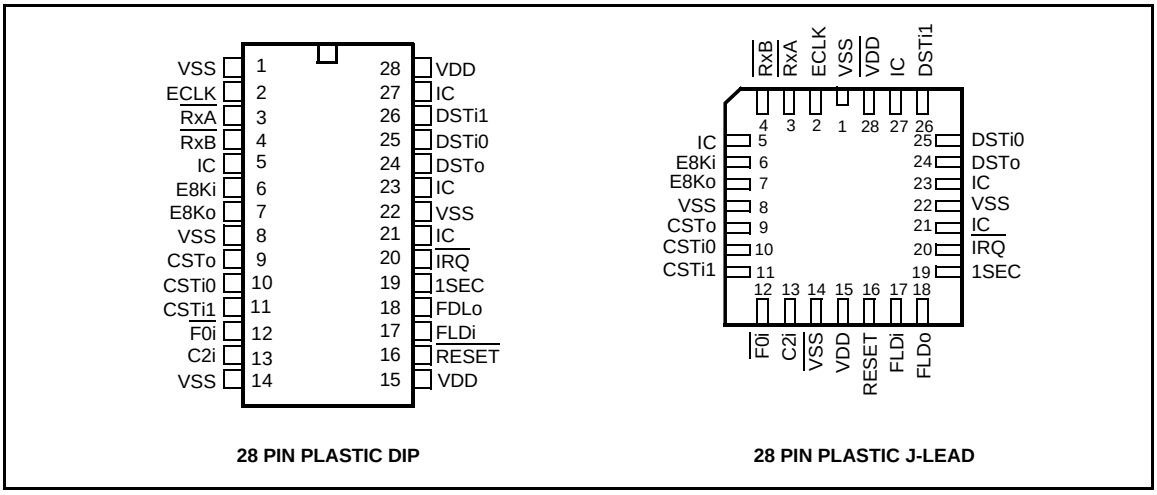


Figure 2 - Pin Connections

Pin Description Table

Pin #	Name	Description
1	V_{SS}	**System Ground.**
2	ECLK	**Extracted Clock Input**. A 1.544 MHz clock derived from the received data. This signal is used to clock in the data on pins RxA and RxB. See Figure 11 on page 26 for timing information.
3	$\overline{RxA}$	**Receive A Input**. A unipolar active low signal decoded from the received T1 signal. See Figure 11 on page 26 for timing information.
4	$\overline{RxB}$	**Receive B Input.** A unipolar active low signal decoded from the received T1 signal. See Figure 11 on page 26 for timing information.
5	IC	**Internal Connection.** Must be tied to V_{SS} for normal operation.
6	E8Ki	**Extracted 8 kHz Input.** A low going pulse on this input is used by the PMAC to locate the framing bit in the received signal. The device uses this information to detect errors in the received framing bits. Connect to E8Ko of the MT8976/77. See Figure 12 on page 27 for timing information.
7	E8Ko	**8 kHz clock output.** The 8 kHz signal input at E8Ki is output on this pin when bit 2 (8KEn) of the PMAC Control Word is set. The output is pulled high when 8KEn is reset. See Figure 12 on page 27 for timing information.
8	V_{SS}	**System Ground.**
9	CSTo	**Control ST-BUS Output.** The data that enters the PMAC on CSTi0 will exit the device on this pin. Data derived by the PMAC will be inserted into specific channels of this output stream. See Figure 13 on page 28 and Figure 14 on page 28 for timing information and Figure 5 on page 8 for channel allocation.
10	CSTi0	**Control ST-BUS Input 0.** Accepts the serial ST-BUS stream output on CSTo of the MT8976/77. The data that enters the PMAC on this pin exits the device on CSTo. The contents of specific CSTi0 channels is replaced by data derived by the PMAC. See Figure 13 on page 28 and Figure 14 on page 28 for timing information and Figure 4 on page 6 for channel allocation.
11	CSTi1	**Control ST-BUS Input 1.** Channel 11 of this ST-BUS input stream is used to control specific features in the device (Table 14 on page 16). Channel 7 is used for the transmit bit-oriented message (Table 13 on page 15), and channel 15 is used to control loopback functions (Table 4 on page 9). See Figure 13 on page 28 for timing information and Figure 3 on page 5 for channel allocation.
12	$\overline{F0i}$	**Frame Pulse Input.** This input accepts an 8 kHz signal, which is used to delineate the ST-BUS frame boundary. See Figure 15 on page 29 for timing information.
13	C2i	**2.048 MHz Clock Input.** This input accepts a 2.048 MHz clock signal, which is used to clock ST-BUS control and data streams into and out of the PMAC. See Figure 13 on page 28 and Figure 14 on page 28 for timing information.
14	V_{SS}	**System Ground.**
15	V_{DD}	**Supply Voltage Input (+5 V).**
16	$\overline{RESET}$	**$\overline{RESET}$ Input.** Must be high for normal operation. When low, the functions of the MT8926 will be suspended.
17	FDLi	**Facility Data Link Input.** This input accepts a 4 kbit/sec. facility data link transmit signal, which is routed back out transparently on FDLo if message-oriented signal transmission is enabled (i.e., PMAC Control Word bit 0, FDLEn, is low). This signal is not clocked into the PMAC. If bit-oriented messaging is enabled (FDLEn high), data on this input will not be routed to FDLo (see pin 18, FDLo, below).

Pin Description Table (continued)

Pin #	Name	Description
18	FDLo	**Facility Data Link Output**. When bit-oriented messaging is enabled (i.e., PMAC Control Word bit 0, FDLEn, is high), data in the Transmit BOM register will be appended to a 1111 1111 (FF) flag and clocked out of the device at this output. The output timing for this signal is shown in Figure 18 on page 30. When bit-oriented messaging is disabled (FDLEn low), data received at the FDLi pin is routed back out transparently on this pin (it is not re-timed). See Figure 19 on page 30 for timing information.
19	1SEC	**1 Second Output.** A one second timing signal derived from the ST-BUS $\overline{F0i}$ signal is output on this pin. The output is low for 0.5 seconds and high for 0.5 seconds. It can be used as an interrupt source to generate T1.403 message-oriented performance reports. See Figure 16 on page 29 for timing information.
20	$\overline{IRQ}$	**Interrupt Request Output.** An open drain output that is to be externally connected to V_{DD} through a pull-up resistor. The PMAC will pull this pin low to assert an interrupt request. Interrupting events and their groupings are described in Table 16 on page 19 and Table 17 on page 20. $\overline{IRQ}$ is released by making bit 1 (Interrupt Acknowledge - INTA) of the PMAC Control Word low. Once INTA is set, all interrupting signals of a particular group must be inactive before the next interrupt of that group can assert $\overline{IRQ}$. See Figure 17 on page 30 for functional timing information.
21	IC	**Internal Connection.** Must be left open for normal operation.
22	V_{SS}	**System Ground.**
23	IC	**Internal Connection.** Must be left open for normal operation.
24	DSTo	**Data ST-BUS Output.** A 2.048 MBit/sec. serial output stream, which contains the 24 PCM or data channels to be transmitted on the T1 trunk. This data stream is multiplexed from either input DSTi0 (Normal Mode) or input DSTi1 (Payload Loopback Mode). The selection of either the Normal or Payload Loopback mode is made through the Loopback Control Word. This output should be connected to DSTi of the MT8976/77. When the loopback control word is set for line loopback code generation, the 24 PCM channels will contain the line loopback activate or deactivate code stream. See Figure 14 on page 28 for timing information.
25	DSTi0	**Data ST-BUS Input 0.** A 2.048 MBit/sec. serial input stream, which contains the 24 PCM or data channels to be transmitted on the T1 trunk in Normal Mode. This input should be connected to the system side output stream.
26	DSTi1	**Data ST-BUS Input 1.** A 2.048 MBit/sec. serial input stream, which contains the 24 PCM or data channels to be transmitted on the T1 trunk in Payload Loopback Mode. This input should be connected to DSTo of the MT8976/77.
27	IC	**Internal Connection.** Must be tied to V_{SS} for normal operation.
28	V_{DD}	**Supply Voltage Input (+5 V).**

1.0 Functional Description

The MT8926 Performance Monitoring Adjunct Circuit (PMAC) is designed to enable a MT8976/77 based T1 interface to gather performance data and perform maintenance functions as per ANSI T1.403 and T1.408. Performance data collection includes CRC errors, severely errored framing events, frame synchronization-bit errors, line code violations, and controlled slips. Maintenance functions include the detection of alarms, SF line loopback code generation and detection, ESF payload loopback, as well as the transport of bit-oriented and message-oriented signals over the Facility Data Link (FDL).

The control and status data of the MT8926 is transported over spare channels of the existing MT8976/77 ST-BUS streams. Therefore, no new ST-BUS streams are required to upgrade with the PMAC.

The PMAC has an on-board framer that uses the received signal and extracted 8 kHz clock to achieve synchronization. The result of this frame alignment is logically ANDed with the SYN bit of the MT8976/77 CSTo stream to give FECV (see Table 5 on page 10). This will ensure that the PMAC can only declare synchronization after the framer is synchronized. The MT8926 will align to SF or ESF framing without user selection.

An interrupt (IRQ output) system is also provided to reduce the requirement to monitor ST-BUS channels continuously for exception conditions. Interrupt sources are divided into group one (G1) for service affecting events and group two (G2) for counter overflows.

A timer has been included to allow scheduling of T1.403/408 message-oriented performance reports for transmission over the facility data link. This timer provides a two second output (register accessed) and a one second output pin.

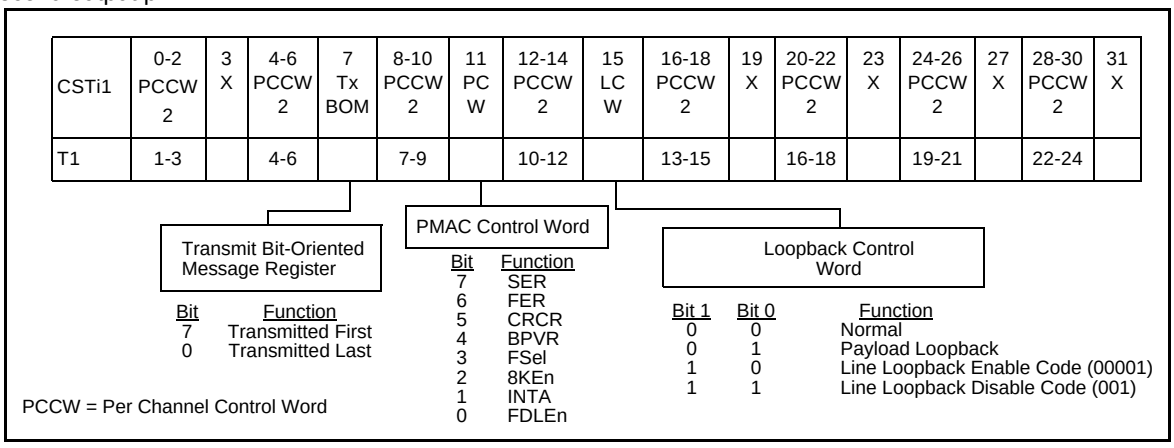


Figure 3 - CSTi1 Channel Allocation Versus T1 Channels

Two eight bit counters with overflow bits and resets (resets counter and overflow bit) are provided to record line code violations (BPV) and CRC errors. The BPV counter will not count B8ZS encoding violations. When either overflow bit goes high it will generate a group two (G2) interrupt.

Two four bit counters are used to record framing error events (FE) and severely errored framing events (SE). The FE counter has an overflow indication bit and can be cleared (resets counter and overflow bit) by the user. Its overflow bit will generate a group two (G2) interrupt when it goes high. A G2 interrupt will also be issued whenever the SE counter is incremented.

The alarms that the PMAC monitors are alternate SF yellow alarm (i.e., twelfth SF framing bit =1, ALRM), ESF facility data link yellow alarm (RAI), loss of signal (i.e., reception of 128 or more consecutive zeros), and alarm indication signal (AIS, blue alarm or all ones alarm). Therefore, the MT8926/MT8976/77 combination supports a comprehensive alarm package.

The PMAC alarm registers and counters are updated as the corresponding events occur. Once per frame (8000

times a second) the state of these registers and counters is recorded in a set of snap-shot registers. This data in the snap-shot registers is then inserted into the appropriate bit positions of the ST-BUS status stream CSTo.

FDL bit-oriented messages can be communicated via the PMAC transmit and receive bit-oriented message registers. The user gains access to these registers through the ST-BUS control streams. Valid bit-oriented messages consist of a series of repeating 16 bit code words of the form: 11111111 0XXXXXX0, where XXXXXX is the message content. The PMAC will automatically append the prefix byte 11111111 to the transmit message and remove it from the receive message. It will also indicate the reception of a valid message. When bit-oriented messages are not being transported, message-oriented facility data link signals, assembled by an external HDLC controller (i.e., MT8952), can be passed through the PMAC to the MT8976/77 for transmission.

The PMAC can implement an ESF payload loopback by routing the MT8976/77 DSTo stream to the MT8976/77 DSTi input (see Figure 6 on page 8). The payload loopback is controlled through the loopback control word, Channel 15 of CSTi1 (see Figure 3 on page 5). When the payload loopback is disabled, data entering the PMAC's DSTi0 pin is transferred to the PMAC DSTo. DSTo of the PMAC should be connected to the DSTi pin of the MT8976/77 framer.

1.1 PMAC - Framer Interworking

The MT8926 PMAC is designed to function with the MT8976/77 T1 framer. Figure 9 on page 21 illustrates a typical application and the connections involved in realizing this interface. Both the PMAC and framer receive the extracted clock and data from the T1 line interface. This allows the MT8926 to perform B8ZS recovery and BPV detection, as well as SF or ESF synchronization, framing error detection, facility data link extraction, and line loopback code detection.

Some of the CSTi1 channels that are not used to control the MT8976/77 are used to control the PMAC, therefore, CSTi1 will connect to both devices. Figure 3 on page 5 shows the channels of CSTi1 that carry the MT8976/77 Per Channel Control Words, as well as the MT8926 control data. C2i and $\overline{F0i}$ supply timing references for both devices.

The CSTo stream of the MT8976/77 framer enters the PMAC on CSTi0 (see Figure 4 on page 6). The PMAC adds its performance data to form the CSTo stream of the PMAC. Figure 5 on page 8 shows the channels and status bits that the PMAC has added to CSTo. E8Ko of the framer will also pass through the PMAC, E8Ki to E8Ko, under control of CSTi1.

CSTi0 MT8976/77 CSTo	0-2 PCSW	3 PSW	4-6 PCSW	7 X	8-10 PCSW	11 X	12-14 PCSW	15 MSW1	16-18 PCWS	19 X	20-22 PCSW	23 X	24-26 PCSW	27 X	24-26 PCSW	31 MSW2
T1	1-3		4-6		7-9		10-12		13-15		16-18		19-21		22-24	

PCSW = Per Channel Status Word
PSW = Phase Status Word
MSW = Master Status Word

Figure 4 - MT8926 CSTi0 (MT8976/77 CSTo) Channel Allocation Versus T1 Channels

It should be noted that the PMAC will replace some of the data of MT8976/77 Master Status Words 1 and 2. This is outlined in Table 1 on page 7 and Table 2 on page 7.

Bit	MT8976/77 CSTo	MT8926 CSTo
7	YLALR	YLALR
6	MIMIC	MIMIC
5	ERR	ALRM
4	ESFYLW	RAI
3	MFSYNC	MFSYNC
2	BPV	LOS
1	SLIP	SLIP
0	SYN	SYN

Table 1 - Master Status Word 1 Data Substitution

Bit	MT8976/77 CSTo	MT8926 CSTo
7	BlAlm	BlAlm
6	FrCnt	FrCnt
5	Xst	Xst
4	BPVCnt	SEI
3	BPVCnt	FSI
2	CRCCNT	CSI
1	CRCCNT	BSI
0	CRCCNT	AIS

Table 2 - Master Status Word 2 Data Substitution

The MT8926 can be programmed to either pass data through from FDLi to FDLo and on to the MT8976/77 input TxFDL, or insert bit-oriented messages into the FDL via the transmit bit-oriented message register, channel 7 of CSTi1. This function is under control of the FDLEn bit of the PMAC Control Word. See Application section Figure 9 on page 21 for FDL connections.

Channel 15 of CSTi1, the Loopback Control Word, is used to control the line loopback code generation and payload loopback functions of the PMAC. This is done by internally connecting the MT8926 DSTo to either a line loopback enable code generator, a line loopback disable code generator, DSTi0 or DSTi1. Figure 6 on page 8 illustrates the connections required to support these functions. The DSTo of the framer connects to DSTi1 of the PMAC and to the receive side of the system. This allows the PMAC to perform a payload loopback by internally connecting DSTi1 to DSTo. In normal operation, transmit data will flow from DSTi0 to DSTo of the PMAC to DSTi of the MT8976/77.

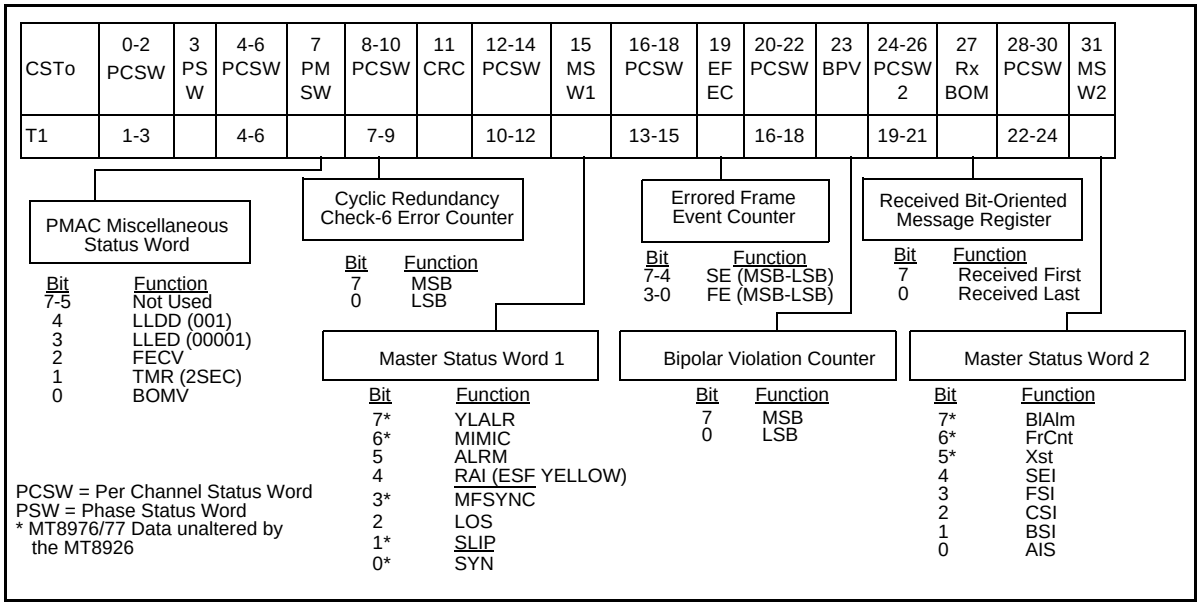


Figure 5 - CSTo Channel Allocation Versus T1 Channels

1.2 PMAC $\overline{\text{RESET}}$

The MT8926 functions may be suspended by making the $\overline{\text{RESET}}$ input low ($\overline{\text{RESET}}$ must be high for normal operation). In the reset state, data entering the PMAC on FDLi, DSTi0 and CSTi0 will pass through unaltered to FDLo, DSTo and CSTo respectively. E8Ko will be high, $\overline{\text{IRQ}}$ will be high impedance and the 1SEC output (and TMR bit) will be low.

After the MT8976/77 has acquired frame synchroni-zation and $\overline{\text{RESET}}$ returns high, the MT8926 will require two superframes to acquire synchronization and two ST-BUS frames to align to the ST-BUS. $\overline{\text{RESET}}$ can be used to prevent DS1 interface interrupts from occurring during system initialization. It should be noted that when the MT8926 is acquiring synchronization the CRC and BPV counters may record errors.

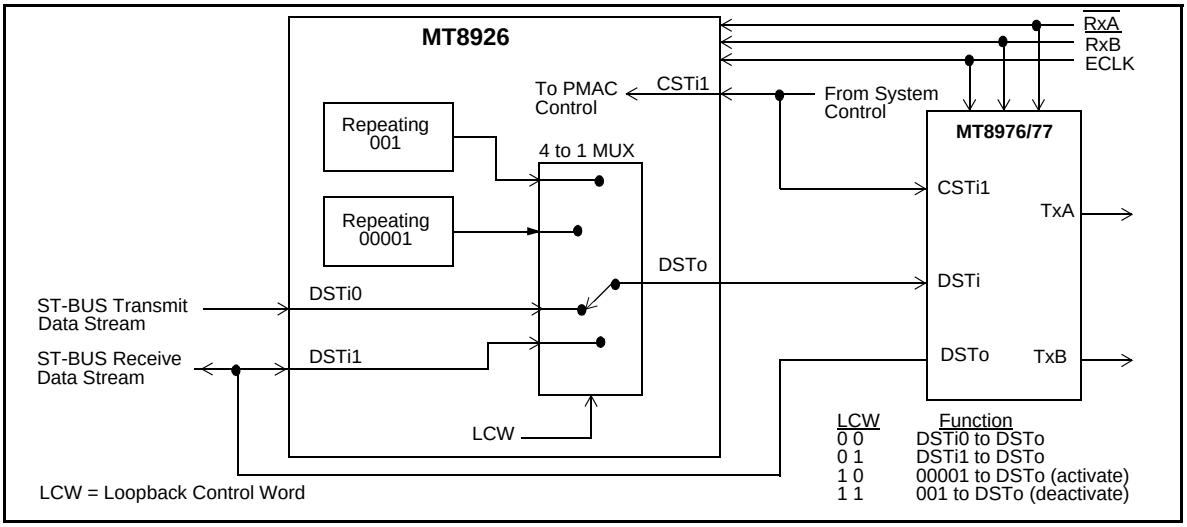


Figure 6 - Payload and Line Loopback Operation

Bit	Name	Description
7-6	YLALR & MIMIC	These bits (Yellow Alarm Indication and Mimic) contain information from the MT8976/77 that is unaltered by the MT8926. See Master Status Word 1 of the MT8976/77 data sheet.
5	ALRM	Alarm. This bit will be set if the MT8926 detects a 1 in the F_S bit position of the twelfth frame of an SF superframe (alternate yellow alarm indication). ALRM will be low when the F_S bit is 0. When receiving an ESF signal or if bit 3 (FSEL) of the PMAC Control Word (CSTi1 Channel 11) is low, the ALRM bit will always be low.
4	RAI	Remote Alarm Indication (also known as ESF Yellow Alarm). This bit is set if an RAI code word (repeating hex FF00 pattern) is received on the ESF facility data link. This code must be correctly detected in seven out of 10 messages. RAI will be reset if more than three of 10 messages are in error. When receiving an SF signal, this bit will always be low.
3	$\overline{\text{MFSYNC}}$	This bit (Multiframe Synchronization) contains information from the MT8976 that is unaltered by the MT8926. See Master Status Word 1 of the MT8976 data sheet.
2	LOS	Loss of Signal. This bit will go high when the MT8926 detects 128 or more consecutive zeros in the line signal. It will be reset after the device detects a 12.5% ones density (48 ones in two or less frames) in the received signal.
1-0	SLIP & $\overline{\text{SYN}}$	These bits (Slip Indication and Synchronization) contain information from the MT8976/77 that is unaltered by the MT8926. See Master Status Word 1 of the MT8976/77 data sheet.

Table 3 - Master Status Word 1 (CSTo Channel 15)

Bit 1	Bit 0	Description
0	0	Normal operation. The transmit data applied to DSTi0 will pass through the PMAC, and be output on DSTo.
0	1	Payload Loopback mode. Connect as per Figure 6 on page 8. The received data on DSTo of the MT8976/77 is routed through the PMAC to the DSTi input of the MT8976/77.
1	0	Transmit Line Loopback Enable. Connect as per Figure 6 on page 8. DSTo of the PMAC will be internally connected to an SF line loopback enable code generator. That is, a repeating 00001 code is placed in the 24 T1 channels of DSTo, so it may be transmitted by the framer.
1	1	Transmit Line Loopback Disable. Connect as per Figure 6 on page 8. DSTo of the PMAC will be internally connected to an SF line loopback disable code generator. That is, a repeating 001 code is placed in the 24 T1 channels of DSTo, so it may be transmitted by the framer.

Table 4 - Loopback Control Word (CSTi1 Channel 15)

Note: Bits 2 to 7 of the Loopback Control Word are not used

1.3 ALRM (SF Yellow Alarm)

The MT8926 will recognize the sixth F_S bit of an SF superframe as an alternate Yellow Alarm indicator, if FSel of the PMAC Control Word is high. That is, when this F_S bit is high/low, the ALRM bit of Master Status Word 1 will be high/low (see Table 3 on page 9). When an ESF signal is being received or when FSel is low, ALRM will always be low.

A low to high transition of the ALRM bit will initiate a group one (G1) interrupt.

1.4 Remote Alarm Indication (RAI)

The PMAC will decode the bit-oriented priority codeword 11111111 00000000 received on the FDL as a Remote Alarm Indication (RAI or Yellow Alarm) signal as per T1.403/408. See the section on MT8926 FDL message transfer. This 16 bit pattern must be detected in seven out of 10 codewords in order for the RAI bit of Master Status Word 1 (CSTo channel 15 bit 4) to go high (see Table 3 on page 9). If more than three out of 10 codewords are in error, then RAI will remain low.

A low to high transition of the RAI bit will initiate a group one (G1) interrupt. See the section on interrupts for the control of the RAI interrupt.

1.5 Loss of Signal Indication (LOS)

The LOS bit of Master Status Word 1, Table 3 on page 9, will be high if the MT8926 receives 128 or more consecutive zeros from the T1 interface. LOS will return low when a ones density of 12.5% has been achieved (approximately 48 ones is received in two or less frames).

1.6 Payload Loopback

The payload of a T1 signal consists of the 192 data bits of each frame and excludes the framing bit (the first bit of 193). Therefore, a T1.403 or T1.408 ESF payload loopback extracts the payload of a receive T1 signal and transmits it back to the originator with new framing bits. This allows the transport of maintenance and performance data over the facility data link while the payload loopback is activated. The CRC-6 multiframe alignment remainder will not be looped around, but will function normally (i.e., calculated for each direction of transmission).

The MT8926 PMAC can perform a payload loopback by muxing the data received on the MT8976/77's DSTo to DSTi of the MT8976/77. This is controlled by the MT8926 Loopback Control Word (CSTi1 channel 15, see Table 4 on page 9).

Figure 6 on page 8 illustrates the MT8926 payload loopback connections. The ST-BUS transmit stream (normally connected to DSTi of the MT8976/77) will connect to DSTi0 of the MT8926. The DSTo stream of the MT8976/77 will connect to DSTi1 of the MT8926 and to the ST-BUS receive stream. DSTo of the MT8926 will connect to DSTi of the MT8976/77.

Bit	Name	Description
7-5	---	Not Used.
4	LLDD	Line Loopback Disable Detect. This bit is set when a repeating 001 pattern (either framed or unframed) is detected in the received T1 signal for at least five frames. In order to comply with T1.403, the user's operating system will ensure that this code is present for at least five seconds before deactivating the SF line loopback (MT8976/77 Remote Loopback). The MT8926 will detect this repeating bit pattern even in the presence of a BER of 3 errors in 1000 bits.
3	LLED	Line Loopback Enable Detect. This bit is set when a repeating 00001 pattern (either framed or unframed) is detected in the received T1 signal for at least five frames. In order to comply with T1.403, the user's operating system will ensure that this code is present for at least five seconds before activating the SF line loopback (MT8976/77 Remote Loopback). The MT8926 will detect this repeating bit pattern even in the presence of a BER of 3 errors in 1000 bits.

Table 5 - PMAC Miscellaneous Status Word (CSTo Channel 7)

Bit	Name	Description
2	FECV	Framing Error Count Validation. This bit is set when the MT8926 has synchronized to a framed T1 signal. The framing error count is frozen if this bit is not set. Synchronization (FECV=1) is reported when the MT8926 detects two consecutive superframes with correct framing bits, and bit 0 in CSTi0 channel 15 (SYN) is zero. When receiving an SF signal, both F_S and F_T bits are examined if bit 3 (FSel) in the PMAC Control word is set. In this case the sixth F_S bit is not examined when checking for framing bits. If bit FSel is reset, then only F_T bits are examined. Loss of synchronization (FECV=0) is reported when either two out of four errors have been detected in the received framing bit position (SF F_T bits or ESF FPS bits) or if bit 0 in CSTi0 channel 15 (SYN) is set indicating the MT8976/77 has lost synchronization.
1	TMR	Two Second Timer. This bit changes state once per second.
0	BOMV	Bit-Oriented Message Validation. This bit will be set when a valid bit-oriented message is present in the receive BOM register (Table 12 on page 15, CSTo, channel 27). It is reset when a valid message is not being received. A valid bit-oriented message has the form 111111110XXXXXX0, where XXXXXX contains the message information.

Table 5 - PMAC Miscellaneous Status Word (CSTo Channel 7) (continued)

1.7 Line Loopback Codes

T1.403 defines SF mode line loopback activate and deactivate codes. These codes are either a framed or un-framed repeating bit sequence of 00001 for activation or 001 for deactivation. The standard goes on to say that these codes will persist for five seconds or more before the loopback action is taken.

The MT8926 will generate line loopback activate and de-activate codes. These functions are controlled by the Loopback Control Word of CSTi1 channel 15 (see Table 4 on page 9). The connections illustrated in Figure 6 on page 8 must be implemented for this feature to function.

The MT8926 will also detect both framed and un-framed line loopback activate and de-activate codes even in the presence of a BER of 3 errors in 1000 bits. See the PMAC Miscellaneous Status Word, Table 5 on page 10, CSTo channel 7 bit 3 Line Loopback Enable Detect (LLED) and bit 4 Line Loopback Disable Detect (LLDD). The line loopback of T1.403 is equivalent to the remote loopback function of the MT8976/77 (see MT8976/77 data sheet, Master Control Word 2). Therefore, the user will monitor the LLED and LLDD bits to ensure that they persist for a minimum of five seconds. Then the line loopback can be either activated or de-activated using the MT8976/77 Remote Loopback function.

1.8 PMAC Synchronization

The MT8926 has its own frame synchronization mechanism, which uses the received signal ($\overline{\text{RxA}}$ and $\overline{\text{RxB}}$) and E8Ki to achieve SF and ESF frame and superframe alignment. Further, the PMAC monitors the SYN bit of the MT8976/77 (CSTo channel 15 bit 0) and will not declare synchronization until it is clear. When SYN is low and the MT8926 framer is properly aligned for two superframes, the PMAC will declare synchronization by making the Frame Error Count Validation bit (FECV) high. If this criteria is not met, FECV will be low.

The PMAC will use the received F_T and F_S bits, F_T bits only or FPS bits to acquire synchronization. The receive F_T or FPS bits are used to determine the out-of-synchronization state (see Table 5 on page 10).

1.9 Timer Outputs

The PMAC has two timer outputs, 1SEC pin and CSTo TMR bit, which are derived from the 8 kHz ST-BUS frame pulse F0i. These signals have been implemented to provide the interface controller with a timing reference for the transmission of T1.403/408 message-oriented performance data over the FDL. See the Application section for an explanation of T1.403/408 FDL Message Transfer.

The 1SEC output (pin 19) changes state once every half second, and therefore, has a period of one second. The relationship between the 1SEC output and the frame pulse F0i is shown in Figure 16 on page 29.

TMR is bit one of the PMAC Miscellaneous Status Word (CSTo channel 7, see Table 5 on page 10). It changes state once per second on the rising edge of the 1SEC output, and thus, has a two second period. Therefore, TMR will change state 62 C2i clock cycles (or ST-BUS bit times) after the frame pulse that immediately precedes the rising edge of the 1SEC output.

1.10 Framing Error Event Counters

The MT8926 has two four bit counters, the Framing Error Counter (FE) and the Severely Errored Framing Event Counter (SE). The FE counter will be incremented each time a single framing error in the T1 signal is received. The SE counter will be incremented by the reception of a T1 framing pattern with an error rate that is greater than or equal to two out of six bits. See Table 8 on page 13 for errored frame event counter details.

Frame #	F_T	F_S
1	1	
2		0
3	0	
4		0
5	1	
6		1
7	0	
8		1
9	1	
10		1
11	0	
12		0

Table 6 - D3/D4 or SF Frame Pattern

Table 6 on page 12 illustrates the Terminal Framing bits (F_T) and Signalling Framing bits (F_S) of the SF or D3/D4 framing pattern. Refer to Table 18 on page 22 for the ESF framing pattern.

Framing Select	SF (F_T)	SF (F_S)	ESF (FPS)
FSel=0	101010	XXXXXX	XXXXXX
FSel=1	101010	00111X	001011

Table 7 - Framing Bits which Affect the SE and FE Counters

Table 7 on page 12 illustrates which framing bits are included in the framing error calculations in SF and ESF modes with the Framing Pattern Selection bit (FSel), CSTi1 channel 11 bit 3, high and low. Bits marked "1" or "0" are counted, bits marked "X" are excluded.

When an SF signal is being received and FSel is low the counters are incremented by F_T framing bit error events. FSel must be high for the extended superframe FPS bits or both SF F_T and F_S bits to be included. It should be noted that the twelfth SF framing bit (the sixth F_S framing bit) is excluded because it can be used as an SF alternate yellow alarm. The ALRM bit of the Master Status Word 1 (CSTo channel 15 bit 5) will be high if the received alternate yellow alarm bit is high. The ALRM bit will always be low if FSel is low.

The FE and SE counters will wrap around to 0000 after reaching a terminal count of 1111. When the FE counter wraps around the Framing Error Saturation Indication bit (FSI) will be set, Table 11 on page 14, and a G2 interrupt will be asserted. The Severely Errored Framing Event Indication bit (SEI), Table 11 on page 14, will be set when the SE counter is incremented. This will also assert a G2 interrupt. These counters are frozen when the PMAC or MT8976/77 has lost synchronization (i.e., CSTo Channel 7 bit 2, FECV = 0).

The SE and FE counters, as well as the SEI and FSI bits are cleared by a high-to-low transition of bit 7, SE Counter Reset (SER), and bit 6, FE Counter Reset (FER), of the PMAC Control Word channel 11 CSTi1.

1.11 BPV and CRC-6 Error Counters

The MT8926 has two eight bit counters, the Bipolar Violation Counter (BPV), Table 10 on page 14, and the CRC-6 Framing Error Counter (CRC), Table 9 on page 14. The BPV counter is incremented each time a non-B8ZS bipolar code violation is received on the T1 interface. The PMAC performs B8ZS recovery of the receive data before BPVs are detected. The CRC-6 Framing Error Counter is incremented when the least significant bit of the MT8976/77 CRC error counter is incremented.

The BPV and CRC counters will wrap around to 00000000 after reaching a terminal count of 11111111. When the BPV counter wraps around the BPV Saturation Indication bit (BSI) will be set, Table 11 on page 14, and a G2 interrupt will be asserted. Similarly, when the CRC counter wraps around the CRC Saturation Indication bit (CSI) will be set and a G2 interrupt will be asserted.

Bit	Name	Description
7-4	SE	Severely Errored Framing Event. This four bit counter is incremented when the MT8926 detects two out of six framing bit errors. It will wrap around after reaching terminal count and can be reset by toggling bit 7 of the PMAC Control Word (Table 14 on page 16, CSTi1 channel 11) from high to low. When receiving a SF T1 signal, both F_S and F_T bit errors are counted if bit 3 in the PMAC Control Word is set high. If this bit is set low, only errors in the F_T bits will be counted. When both F_S and F_T bit errors are counted, F_S bit 6 (in the twelfth frame in an SF superframe) is not examined for errors because it can be used to indicate a Yellow alarm.
3-0	FE	Framing Error Count. This four bit counter is incremented when a framing bit error is detected. When receiving a SF T1 signal, both F_S and F_T bit errors are counted if bit 3 in the PMAC Control Word is set high. If this bit is set low, only errors in the F_T bits will be counted. When both F_S and F_T bit errors are counted, F_S bit 6 (in the twelfth frame in an SF superframe) is not examined for errors because it can be used to indicate a Yellow alarm. The counter shall wrap around after reaching terminal count and can be reset by toggling bit 6 in the PMAC Control Word (Table 14 on page 16, CSTi1 channel 11) from high to low.

Table 8 - Framing Error and Severely Errored Framing Event Counters (CSTo Channel 19)

Bit	Name	Description
7-0	CRC	CRC Error Counter. This is an 8 bit counter, which is incremented when the LSB of the MT8976/77 CRC counter toggles. The CRC error counter will wrap around after reaching terminal count (i.e., 11111111 to 00000000). This will also set bit 2 (CSI) of master status word 2. CRC is reset when bit 5 in the PMAC Control Word is toggled from high to low. This counter is invalid when a SF mode T1 signal is being received.

Table 9 - CRC-6 Error Counter (CSTo Channel 11)

Bit	Name	Description
7-0	BPV	Bipolar Violation Counter. This is an 8 bit counter, which is incremented when a line code violation is detected by the MT8926. The counter will wrap around upon reaching terminal count (11111111 to 00000000). This will also set bit 1 (BSI) of master status word 2. BPV is reset when bit 4 in the PMAC Control Word is toggled from high to low.

Table 10 - Bipolar Violation Counter (CSTo Channel 23)

Bit	Name	Description
7-5	BlAlm, FrCnt & Xst	These bits (Blue Alarm, Frame Count and External Status) contain information from the MT8976/77 that is unaltered by the MT8926. See Master Status Word 2 of the MT8976/77 data sheet.
4	SEI	Severely Errored Framing Event Indication. This bit goes high when the SE counter is incremented (i.e., when the LSB of the SE counter toggles). It goes low when bit 7 (SER) of the PMAC Control Word (Table 14 on page 16, CSTi1 channel 11) is changed from high to low. It can also be cleared by a low on the INTA bit of the PMAC Control Word and will remain clear as long as the INTA bit is low.
3	FSI	Framing Error Counter Saturation Indication. This bit is set when the FE counter overflows its terminal count (i.e., 1111 to 0000). It will be reset low when bit 6 (FER) of the PMAC Control Word (Table 14 on page 16, CSTi1 channel 11) is changed from high to low.
2	CSI	CRC Error Counter Saturation Indication. This bit is set when the CRC counter overflows its terminal count (i.e., 11111111 to 00000000). It will be reset when bit 5 (CRCR) of the PMAC Control Word (Table 14 on page 16, CSTi1 channel 11) is changed from high to low. Valid for ESF only.
1	BSI	Bipolar Violation Counter Saturation Indication. This bit is set when the BPV counter overflows its terminal count (11111111 to 00000000). It will be reset when bit 4 (BPVR) of the PMAC Control Word (Table 14 on page 16, CSTi1 channel 11) is changed from high to low.
0	AIS	Alarm Indication Signal. This bit is set when the MT8976/77 has lost synchronization and less than three zeros are detected in any 250 microsecond interval. It is reset when three or more zeros are detected in a 250 microsecond interval or when synchronization is regained.

Table 11 - Master Status Word 2 (CSTo Channel 31)

Bit	Name	Description
7-0	RxBOM	Received Bit-Oriented Message. This register contains the eight least significant bits of the ESF bit oriented message codeword. The contents of this register is valid when a bit-oriented message codeword is received by the MT8926 in the facility data link bit positions of consecutive extended superframes. A valid codeword will have the form 111111110XXXXXX0. The most significant eight bits (FF sequence) are received first. The register will contain the eight bits following the 11111111 sequence, which are 0XXXXXX0. When a valid codeword is detected, bit zero of the PMAC Miscellaneous Status Register is set.

Table 12 - Receive Bit-Oriented Message Register (CSTo Channel 27)

Bit	Name	Description
7-0	TxBOM	Transmit Bit-Oriented Message. The contents of this register will be appended to an FF flag to form a bit-oriented codeword, and clocked out on FDLo when bit zero in the PMAC Control Word is set high. The MT8926 will continue to clock this message out until bit 0 in the Control word is reset. The order of transmission is Bit 7 first. Bits 7 and 0 should be zero for a code word to be valid.

Table 13 - Transmit Bit-Oriented Message Register (CSTi1 Channel 7)

The BPV and CRC counters, as well as the BSI and CSI bits, are cleared by a high-to-low transition of bit 4, BPV Counter Reset (BPVR), and bit 5, CRC Counter Reset (CRCR), of the PMAC Control Word channel 11 CSTi1, Table 14 on page 16.

1.12 Alarm Indication Signal (AIS)

An AIS or Blue alarm is an all ones signal that can be transmitted from the network side to the terminal equipment side of an interface or from the terminal equipment side to the network side of an interface. In the first case, it indicates that the T1 signal from the network may be lost, and the timing that the terminal equipment derives from the received AIS may not be from the network. In the second case, it indicates that data from the terminal equipment side of an interface has been lost and AIS is being transmitted in its place.

The MT8926 will detect an AIS alarm and indicate its presence by making the AIS bit of Master Status Word 2 (Table 11 on page 14, CSTo channel 31 bit 0) high. This state occurs when the MT8976/77 has lost synchronization and less than three zeros are detected in any 250 microsecond interval. The AIS bit will go low when either of these conditions is no longer true.

1.13 MT8926 FDL Message Transfer

The MT8926 will support the transfer of FDL bit-oriented messages in a format that is consistent with T1.403 and T1.408. A BOM is transmitted by loading the message into the PMAC Transmit Bit-Oriented Message Register (TxBOM), Table 13 on page 15, CSTi1 Channel 7. This data has the form 0XXXXXX0, where XXXXXX is the content of the T1.403/408 message. When FDLEn (bit zero of the PMAC Control Word, Table 14 on page 16) is made high, the BOM is transmitted on the FDL preceded by 11111111. The start of the bit-oriented message is not synchronous with FDLEn going high. Therefore, to ensure a message is sent a minimum of n times, the message must be transmitted for 32n + 32 ST-BUS frames.

Valid codewords that are received on the FDL are loaded into the Receive Bit-Oriented Message Register (RxBOM, see Table 12 on page 15). A codeword is valid if it fits the 11111111 0XXXXXX0 form, however, only the 0XXXXXX0 portion of the message will appear in the RxBOM register. When a valid codeword has been received

the BOMV bit of the PMAC Miscellaneous Status Word (Table 5 on page 10, CSTo channel 7 bit 0) will be high. If the next received codeword is not valid, the BOMV bit will become zero and the RxBOM register will retain its most recent valid message.

The MT8926 will support LAPD message-oriented performance reporting when it is combined with an HDLC controller such as the MT8952. See Figure 7 on page 17 for FDL operation. The performance monitoring data that makes up the LAPD message is derived by the combination of MT8976/77 T1 framer and MT8926 PMAC, and is available on CSTo. This data can then be assembled into a LAPD message and presented to the MT8952 HDLC controller for transmission over the FDL on a one second basis as per T1.403/408 (see Figure 10 on page 24). FDLEn of the PMAC Control Word (CSTi1 channel 11 bit 0) must be low to allow transmission of a performance report from the HDLC controller through pins FDLi and FDLo of the MT8926 to the TxFDL input of the MT8976/77. The 1SEC output pin or the two second TMR bit of the Miscellaneous Status Word (CSTo channel 7 bit 0) are derived from the ST-BUS timing and can be used to initiate the transmission of these messages.

Bit	Name	Description
7	SER	SE Counter Reset. Toggling this bit from high to low will reset the severely errored framing event counter (SE counter, CSTo channel 19 bits 7-4) and event indicator (SEI bit, CSTo channel 31 bit 4).
6	FER	FE Counter Reset. Toggling this bit from high to low will reset the framing error counter (FE counter, CSTo channel 19 bits 3-0) and saturation indicator (FEI bit, CSTo channel 31 bit 3).
5	CRCR	CRC Counter Reset. Toggling this bit from high to low will reset the eight bit CRC error counter (CRC, CSTo channel 11) and saturation indicator (CSI bit, CSTo channel 31 bit 2)
4	BPVR	BPV Counter Reset. Toggling this bit from high to low will reset the eight bit BPV counter (BPV, CSTo channel 23) and saturation indicator (BSI bit, CSTo channel 31 bit 1).
3	FSel	Framing Pattern Select. With FSel = 1 and an SF signal detected, both F_S and F_T errors are considered by the FE and SE counters. The user must set this bit high in ESF mode. With FSel = 0 and an SF signal detected, only errors in F_T bits are considered by the FE and SE counters.
2	8KEn	8 KHz Output Enabled. When 8KEn = 1, the E8Ko output will be enabled. That is, the signal input at E8Ki will be output on E8Ko. See Figure 12 on page 27 for timing. When 8KEn = 0, the E8Ko output will be high.
1	INTA	Interrupt Acknowledge. When INTA = 1 the MT8926 interrupts are armed or have been triggered (see Table 15 on page 18). Once INTA is set all interrupting signals of a group must be inactive before another interrupt of that group can assert the $\overline{IRQ}$ output (active low). See Pin Description, pin 20. When this bit is low the $\overline{IRQ}$ output state will be high impedance. $\overline{IRQ}$ will remain in this state as long as INTA remains low or there are no interrupting events (Table 16 on page 19 Table 17 on page 20).

Table 14 - C Control Word (CSTi1 Channel 11)

Bit	Name	Description
0	FDLEn	Facility Data Link Enable. FDLEn = 1 enables transmission of the facility data link bit-oriented messages on FDLo. The BOM byte is stored in the TxBOM register (Table 13 on page 15, CSTi1 Channel 7). See Figure 7 on page 17 for illustration. When FDLEn = 0, the data received on FDLi is multiplexed back out of the MT8926 on FDLo. See Figure 19 on page 30 for timing.

Table 14 - C Control Word (CSTi1 Channel 11) (continued)

When the MT8926 is synchronized to an SF T1 signal, its receive FDL functions are disabled. BOMV of the PMAC Miscellaneous Status Register and RAI of Master Status Word 1 will be zero.

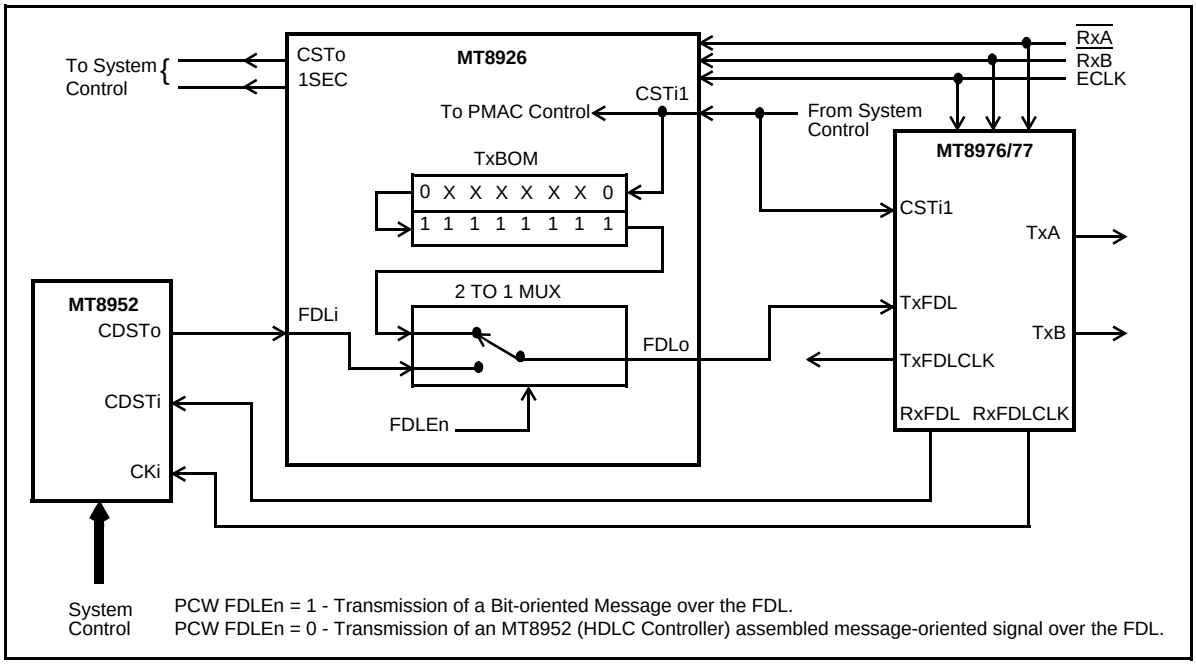


Figure 7 - T1.403/408 FDL Message Transmission

1.14 8 kHz Control

Figure 9 on page 21 illustrates a typical MT8976/77 - MT8926 application. This diagram shows E8Ko (an 8 kHz output aligned with the received framing bit) of the T1 framer connected to E8Ki of the PMAC. The PMAC uses this signal for frame alignment, therefore, the 8kHSel (Master Control Word 1) of the MT8976/77 must be active for the framer - PMAC combination to function properly, even if the interface is in master mode. See the MT8976/77 data sheet.

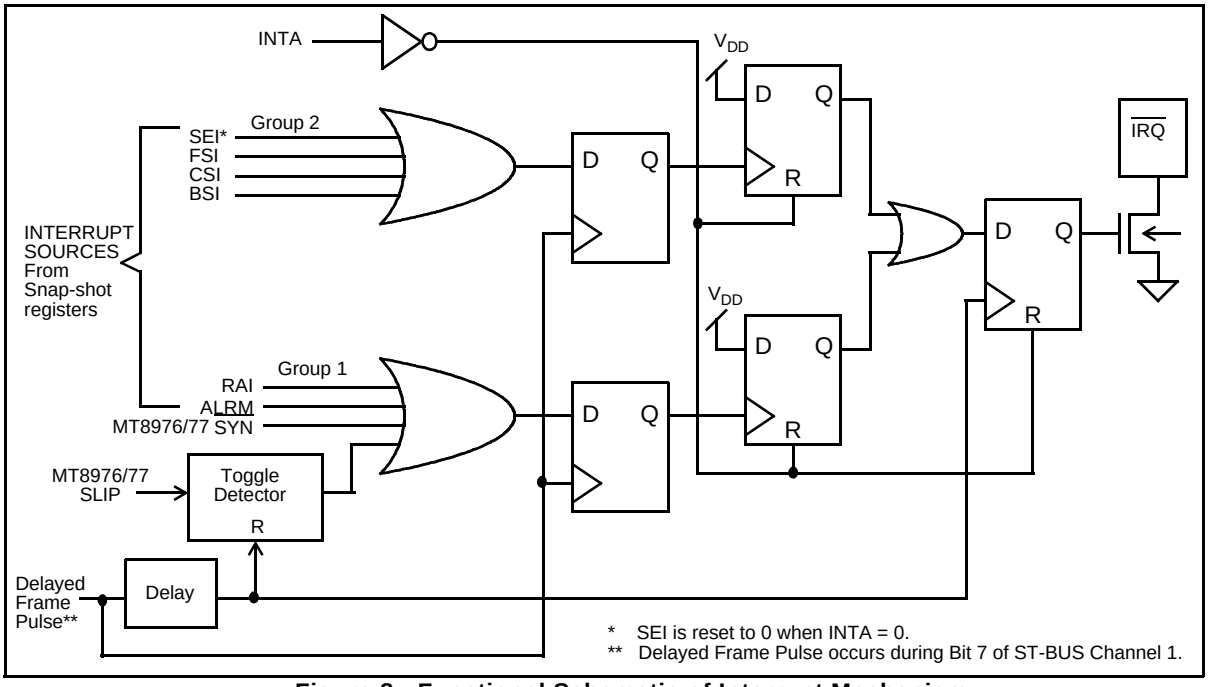


Figure 8 - Functional Schematic of Interrupt Mechanism

In slave or loop-timed operation 8KEn of the PMAC Control Word (Table 14 on page 16, CSTi1 channel 11 bit 2) will be high, which will pass the signal on E8Ki through to E8Ko. In Master mode or if loop-timing is acquired from another interface, 8KEn must be low, which will make E8Ko high.

1.15 Interrupts

The MT8926 interrupts originate from eight sources, which are divided into two groups. Group one (G1) contains ALRM (SF Yellow Alarm), RAI (ESF Yellow Alarm), SLIP and SYN - all except SLIP must be cleared by some means external to the MT8926. Group two (G2) contains SEI, FSI, CSI, and BSI - these can be cleared via the MT8926. See Table 16 on page 19 Table 17 on page 20 for further information.

The interrupting mechanism is controlled by the interrupt acknowledge bit (INTA) of the PMAC control word (Table 14 on page 16). The status of the interrupts is output on IRQ. This will allow the three valid states described in Table 15 on page 18.

State	INTA Bit	$\overline{IRQ}$ Output
Cleared	0	High Impedance
Armed	1	High Impedance
Triggered	1	0

Table 15 - Interrupt States

In the Cleared state (INTA = 0) interrupt sources are ignored and $\overline{IRQ}$ will always be high impedance. If the interrupts are not being used, then INTA should remain in the Cleared state. When the MT8926 is in the Armed state and an interrupt occurs, it will go to the Triggered state ($\overline{IRQ}$ = 0).

When a G1 interrupt occurs and $\overline{IRQ}$ goes low (Triggered), no other G1 or G2 interrupts will affect $\overline{IRQ}$. If $\overline{IRQ}$ is then Cleared and re-Armed, only an active G2 interrupt can Trigger $\overline{IRQ}$ low unless the G1 interrupt has been removed. That is, both the MT8926 interrupt mechanism and the interrupting source of a group must be cleared before a further interrupt of that group can cause $\overline{IRQ}$ to go low. The only exception to this is SEI, which can be

cleared by INTA (see Table 11 on page 14).

A PMAC interrupting signal is either a low-to-high transition or a change in state (SLIP), therefore, for $\overline{IRQ}$ to go low the MT8926 must be Armed before the initiating edge occurs. In the case where all interrupts are quiescent and then an interrupt becomes active, while the MT8926 is in its Clear state, $\overline{IRQ}$ will remain in a high impedance condition. This is true even if the MT8926 is then put in the Armed state and the interrupt persists (see Figure 8 on page 18).

It should be noted that when an SF mode T1 signal is being received the MT8926 CRC error counter will be incremented once every two superframes (24 frames or 3 msec.). This is because SF mode T1 has no CRC bits. Therefore, the CRC circuitry of the MT8976/77 will compare the calculated CRC remainder with the received FS bits, which will result in a mismatch. This will increment the MT8976/77 and MT8926 CRC error counters.

The MT8926 CRC error counter will count to 255 and then overflow to zero, which will cause an interrupt ($\overline{IRQ}$). Therefore, when an SF mode T1 signal is being received an interrupt will be asserted every 256 X 3 msec. = 768 msec. This can be avoided by clearing the CRC error counter before it overflows. A change of state of the 1SEC output (once every 0.5 seconds) can be used to trigger a high-to-low transition of the CRCR bit (CSTi1 channel 11 bit 5, PMAC Control Word). This will ensure the CRC error counter never overflows.

Signal‡	**To Trigger interrupt ($\overline{IRQ}$ low)**	**To Clear and Arm interrupt ($\overline{IRQ}$ high impedance)**
ALRM	ALRM bit low to high AND other G1 interrupts quiescent AND $\overline{IRQ}$ high impedance.	The INTA bit of the PMAC Control Word (CSTi1 channel 11 bit 1) should be made low to clear the interrupt mechanism ($\overline{IRQ}$ high impedance). All G1 interrupts must be quiescent and then INTA must be made high before a further interrupt can be generated from G1. See MT8976/77 data sheet master status word 1 for information on the SLIP and $\overline{SYN}$ bits.
RAI	RAI bit low to high AND other G1 interrupts quiescent and $\overline{IRQ}$ high impedance.	
SLIP	CSTi0/CSTo Channel 15 Bit 1 (SLIP) changes state AND other G1 interrupts quiescent AND $\overline{IRQ}$ high impedance.	
$\overline{SYN}$†	CSTi0/CSTo Channel 15 Bit 0 ($\overline{SYN}$) low to high AND other G1 interrupts inactive AND $\overline{IRQ}$ high impedance.	

‡ G1 interrupts are cleared when $\overline{SYN}$, ALRM, and RAI = 0.
† The SYN interrupt indicates that a LOS or a AIS condition may exist.
Note: AND denotes a logical and.

Table 16 - Group One (G1) Interrupt Activation and Clearing

1.16 SLIP and $\overline{SYN}$ Interrupts

The MT8976 SLIP and $\overline{SYN}$ status bits are passed to the PMAC via the MT8976/77 CSTo to PMAC CSTi0 connection. A MT8926 interrupt will be initiated when the SLIP bit of the framer changes state. This is the only interrupt source that does not have to be cleared before another interrupt of that group can make $\overline{IRQ}$ go low. Therefore, when $\overline{IRQ}$ is returned to a high impedance condition after a SLIP interrupt and all other G1 interrupts are quiescent, any G1 interrupt can make $\overline{IRQ}$ to go low.

A Low-to-High transition of the MT8976/77 $\overline{SYN}$ bit will initiate a PMAC interrupt. This loss of synchronization situation may indicate that a loss of signal condition (LOS) exists or that an all ones (AIS or Blue Alarm) is being received. Therefore, the $\overline{SYN}$ interrupt service routine should check the state of the AIS and LOS bits of CSTo.

Signal‡	To Trigger interrupt ($\overline{\text{IRQ}}$ low)	To Clear and Arm interrupt ($\overline{\text{IRQ}}$ high impedance)
SEI	SEI bit low to high AND other G2 interrupts quiescent AND $\overline{\text{IRQ}}$ high impedance.	The INTA bit of the PMAC Control Word (CSTi1 channel 11 bit 1) should be made low to clear the interrupt mechanism ($\overline{\text{IRQ}}$ high impedance). All G2 interrupts must be clear and INTA must be high before a further interrupt can be generated from G2. The SEI bit will remain clear as long as the INTA bit is low. SEI can also be cleared (low) by toggling SER (CSTi1 channel 11 bit 7) from high to low. FSI is cleared (low) by toggling FER (CSTi1 channel 11 bit 6) from high to low. CSI is cleared (low) by toggling CRCR (CSTi1 channel 11 bit 5) from high to low. Valid for ESF only. BSI is cleared (low) by toggling BPVR (CSTi1 channel 11 bit 4) from high to low.
FSI	FSI bit low to high AND other G2 interrupts quiescent AND $\overline{\text{IRQ}}$ high impedance.	
CSI	CSI bit low to high AND other G2 interrupts quiescent AND $\overline{\text{IRQ}}$ high impedance.	
BSI	BSI bit low to high AND other G2 interrupts quiescent AND $\overline{\text{IRQ}}$ high impedance.	

‡ G2 interrupts are cleared when SEI, FSI, CSI and BSI = 0.
Note: AND denotes a logical and.

Table 17 - Group Two (G2) Interrupt Activation and Clearing

2.0 Applications

Figure 9 on page 21 illustrates a typical application of a MT8926 PMAC. T1 data is transmitted and received using a generic Line Interface Unit (LIU). The LIU passes the received data and extracted clock to both the MT8926 and MT8976. E8Ko (MT8976) is derived from E1.5i by dividing it by 193 and aligning the result with the receive framing. E8Ko (MT8976) connects to E8Ki (MT8926), and is used by the MT8926 for frame alignment. E8Ko (MT8926) is connected to C8Kb of the MT8941. In MT8941 normal mode, C8Kb is the reference clock for the ST-BUS and transmit signals (F0, C4 and C2). This 8 kHz output can be turned off (output high) at the MT8926 so the MT8941 reference clock can be derived from another interface. The intrinsic jitter (typical 0.07 UI) and jitter attenuation of the MT8941 will meet T1.408 requirements (see MT8941 data sheet).

Control of the MT8926 is accomplished over the CSTi1 ST-BUS stream, which is shared by the MT8926 and MT8976. Status data (Performance Monitoring Information) is inserted into the MT8976 CSTo stream by the MT8926 and is output on its CSTo stream. This CSTo stream data is routed through the MT8980 switch, in message mode, to the microprocessor. The microprocessor will assemble the information section of the T1.403/T1.408 message-oriented signal and pass it to the MT8952 HDLC controller for transmission over the facility data link. The MT8952 must be in external timing mode and will be clocked by the RxFDLCLK output to the MT8976. The assembly and transmission of the message-oriented signal is under control of the 1SEC output of the MT8926.

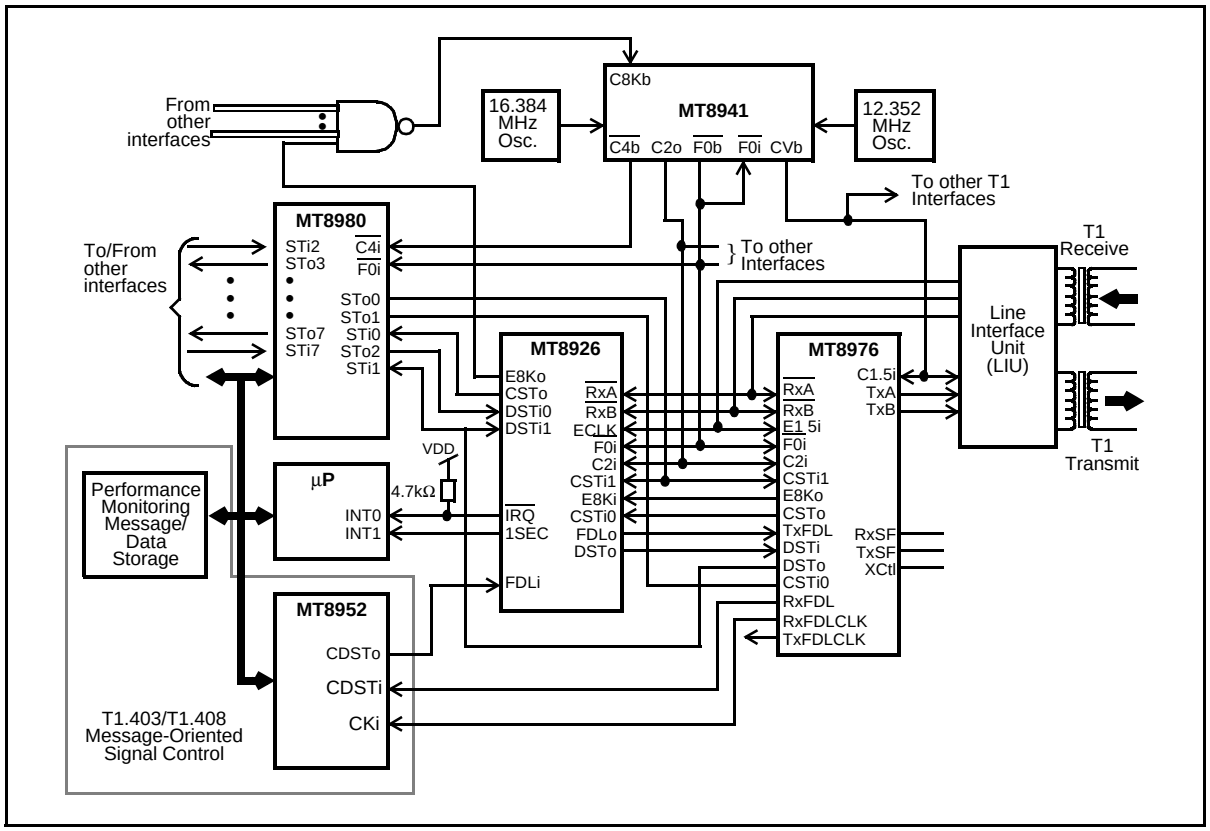


Figure 9 - Typical T1.403/T1.408 Application

Bit-oriented messages are also transmitted and received via MT8980 message mode access to the CSTi1 and CSTo streams. The MT8926 will receive bit-oriented messages from the receive T1 line (i.e., RxA and RxB). Both bit-oriented and message-oriented signals are transmitted over the MT8926 FDLo to MT8976 TxFDL link.

Payload loopback is performed by internally connecting DSTi1 to DSTo of the MT8926 (under control of the CSTi1 stream), instead of the normal connection of DSTi0 to DSTo (see Figure 6 on page 8).

$\overline{IRQ}$ is an open drain interrupt output that will signal the microprocessor when an exception condition occurs (see Figure 8 on page 18). Exception conditions are counter overflows and alarms. Interrupts are reset via the PMAC Control Word of the CSTi1 control stream.

2.1 T1.403/408 FDL Message Transfer Overview

ANSI standards T1.403 and T1.408 define an ESF mode Facility Data Link (FDL), which is used to transport performance information and control signals across a T1 link. The FDL channel is formed from the framing bit position of every second frame, and therefore, has a 4 KBit/sec. bandwidth. See Table 18 on page 22 for the ESF Framing Pattern.

FRAME #	FPS	FDL	CRC
1		X	
2			CB1
3		X	
4	0		
5		X	
6			CB2
7		X	
8	0		
9		X	
10			CB3
11		X	
12	1		
13		X	
14			CB4
15		X	
16	0		
17		X	
18			CB5
19		X	
20	1		
21		X	
22			CB6
23		X	
24	1		

Table 18 - ESF Frame Pattern

The following two FDL message formats are defined in T1.403/408:

1) Bit-oriented, which are repeated 16 bit patterns or codeword messages, and

2) Message-oriented performance reports, which are LAPD protocol messages.

Bit-oriented messages (BOMs) are preemptive, and therefore, override other FDL communications. Each message consists of a 16 bit codeword of the form 11111111 0XXXXXX0. Therefore, there are 64 unique codewords or messages defined by XXXXXX. Refer to T1.403 or T1.408 for a list of messages and message restrictions.

BOMs are further divided into priority messages, and command and response messages. Priority messages indicate the existence of a service-affecting failure, and are repeated until the condition that caused the message is removed. These BOMs are transmitted for at least one second, but may be interrupted as often as once per second, for a

maximum of 100 msec. This is to accommodate the periodic transmission of message-oriented performance reports.

Command and response messages are used to perform various functions, which include the following:

1) line and payload loopback control,

2) protection switch control,

3) synchronization control,

4) reserved for network use, and

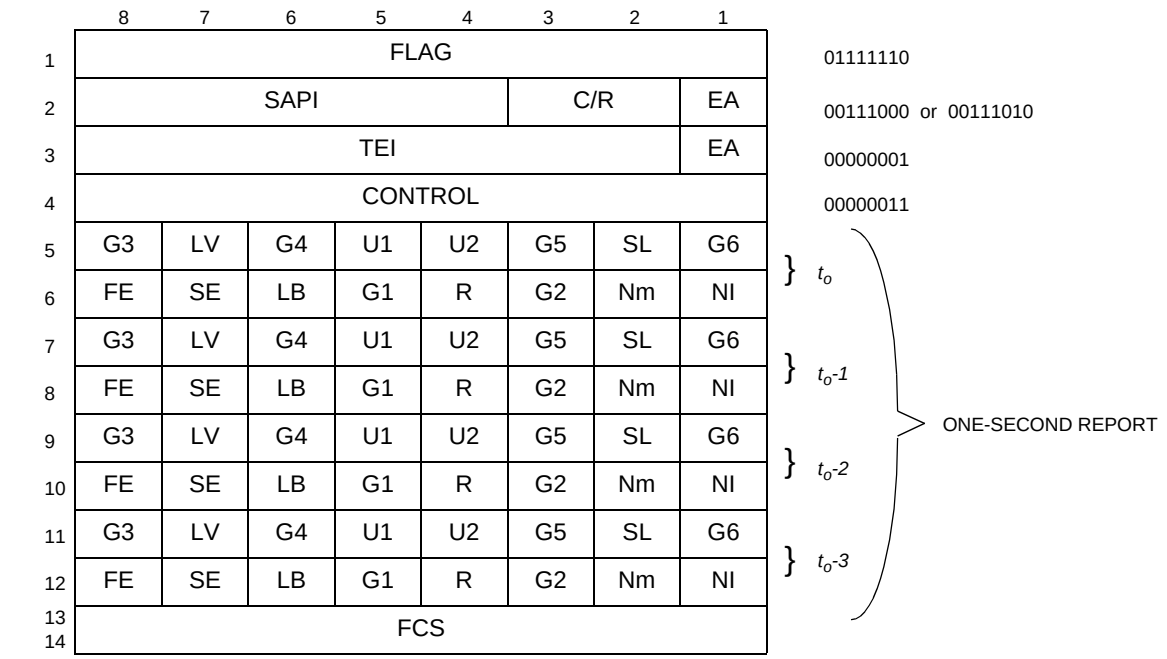
5) unassigned.

Each message consists of a 16 bit codeword of the form 11111111 0XXXXXX0, which is repeated at least 10 times.

The LAPD message-oriented performance reports are sent across the FDL once per second using the bit-assigned message structure of Figure 10 on page 24. Each report contains performance data for each second of the previous four seconds.

When data for the next one second interval t_{0+1} is gathered, it will take the place of t_0 data of the last message. The t_0 data will move to the t_{0-1} position, the t_{0-1} data will move to the t_{0-2} position, the t_{0-2} data will move to the t_{0-3} position, and the data of t_{0-3} will be discarded. Refer to T1.403 or T1.408 for a more complete definition of this protocol.

User defined Operations, Administration and Maintenance (OA&M), terminal-to-network and terminal-to-terminal communications may also pass over the FDL.



ADDRESS	INTERPRETATION
00111000	SAPI = 14, C/R = 0 (CI) EA = 0
00111010	SAPI = 14 C/R = 1 (Carrier) EA = 0
00000001	TEI = 0, EA = 1

CONTROL	INTERPRETATION
00000011	Unacknowledged Information Transfer

ONE-SECOND REPORT	INTERPRETATION
G1 = 1	CRC Error Event = 1
G2 = 1	1<CRC Error Event ≤ 5
G3 = 1	5<CRC Error Event ≤ 10
G4 = 1	10<CRC Error Event ≤ 100
G5 = 1	100<CRC Error Event ≤ 319
G6 = 1	CRC Error Event ≥ 320
SE = 1	Severely-Errored Framing Event ≥ (FE shall = 0)
FE = 1	Frame Synchronization Bit Error Event ≥ 1 (SE shall = 0)
LV = 1	Line Code Violation Event ≥ 1
SL = 1	Slip Event ≥ 1
LB = 1	Payload Loopback Activated
U1, U2 = 0	Under study for synchronization
R = 0	Reserved (Default value is 0)
NmNI = 00, 01, 10, 11	One second report modulo 4 counter

FCS	INTERPRETATION
Variable	CRC 16 Frame Check Sequence

Figure 10 - Message-Oriented Performance Report Structure (from T1.403 and T1.408)

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Power Supplies with respect to V_{SS}	V_{DD}	-0.3	7	V
2	Voltage on any pin other than supplies		V_{SS}-0.3	V_{DD}+0.3	V
3	Current at any pin other than supplies			40	mA
4	Storage Temperature	T_{ST}	-40	125	°C
5	Continuous Power Dissipation	P_D		500	mW

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Operating Temperature	T_{OP}	-40		85	°C	
2	Power Supplies	V_{DD}	4.5	5.0	5.5	V	
3	Input High Voltage	V_{IH}	2.4		V_{DD}	V	Noise margin = 150 mV
4	Input Low Voltage	V_{IL}	V_{SS}		0.4	V	Noise margin = 400 mV

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - Clocked operation over recommended temperature ranges and power supply voltages.

	Parameters	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Supply Current	I_{DD}			5	mA	Outputs Unloaded
2	Input High Voltage	V_{IH}	2.25		V_{DD}	V	
3	Input Low Voltage	V_{IL}	V_{SS}		0.8	V	
4	Input Leakage Current	I_{IL}			±10	µA	Digital Inputs V_{IN}=0 to V_{DD}
5	Output High Current	I_{OH}	8			mA	V_{OH}=2.4V
6	Output Low Current	I_{OL}	8			mA	V_{OL}=0.4V

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Capacitance

	Parameters	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Input Pin Capacitance	C_I		10		pF	
2	Output Pin Capacitance	C_O		10		pF	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
† Timing is over recommended temperature ranges and power supply voltages.

AC Electrical Characteristics† - DS1 Link Timing (Figure 11)

	Parameters	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Receive Data Setup Time	t_{RS}	0			ns	
2	Receive Data Hold Time	t_{RH}	30			ns	
3	Extracted Clock Width	t_{ECW}	250	324		ns	
4	Extracted 1.5 MHz Clock Period	$t_{P1.5}$	500	649		ns	

† Timing is over recommended temperature & power supply voltage ranges.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

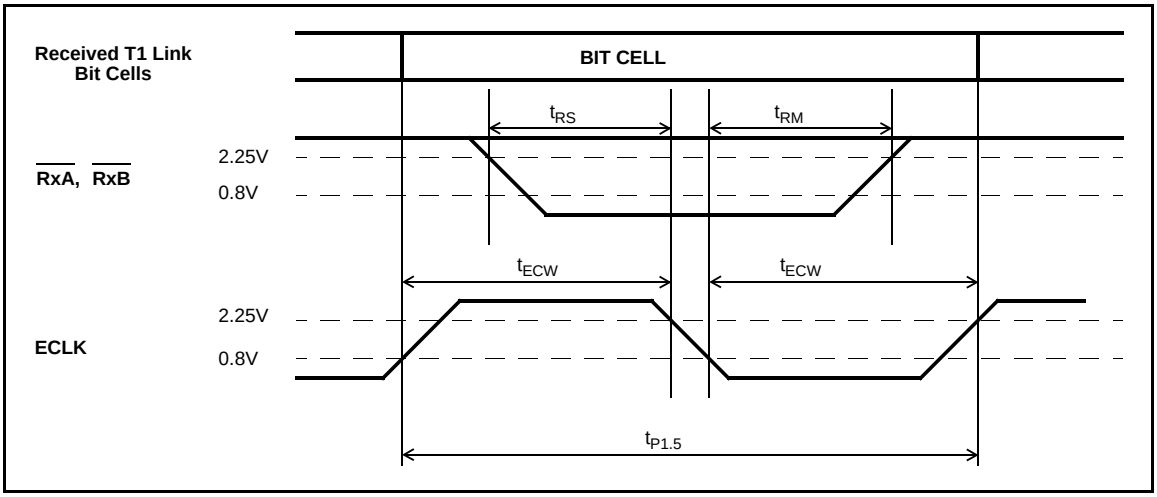


Figure 11 - Receive T1 Link Timing

AC Electrical Characteristics† - 8 kHz Timing (Figures 12)

	Parameters	Sym	Min	Typ‡	Max	Units	Test Conditions
1	8kHz Propogation Delay	t_{8PD}			20	ns	50 pF load
2	8kHz Setup Time	t_{8S}	45			ns	
3	8kHz Input Low	t_{8IL}	0.065	78		µs	
4	8kHz Input High	t_{8IH}		47		µs	

† Timing is over recommended temperature & power supply voltage ranges.
Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

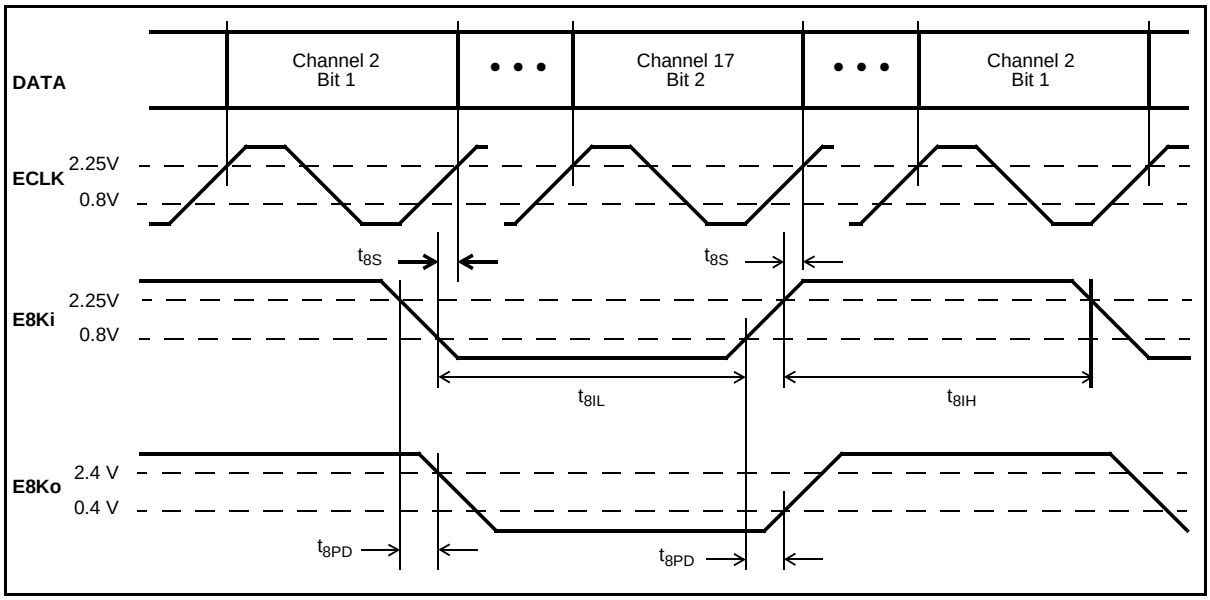


Figure 12 - 8kHz Extracted Framing Signal

AC Electrical Characteristics† - 2048 kBit/s ST-BUS Streams (Figures 13 and 14)

	Parameters	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Clock to Output Delay ¿	t_{COD}			125	ns	150 pF load
2	ST-BUS Setup Time	t_{STS}	15			ns	
3	ST-BUS Hold Time	t_{STH}	50			ns	
4	Serial Output Delay¡	t_{SOD}			35 15 40	ns	150 pF load CSTo 50 pF load CSTo 150 pF load DSTo

† Timing is over recommended temperature & power supply voltage ranges.

‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Note¿ - The PMAC is overwriting some of the bits received on CSTi0, and transmitting the aggregate on CSTo. Line loopback codes are being transmitted on DSTo.

Note¡ - The ST-BUS stream being received on CSTi0 is not being overwritten, but passes through the PMAC unaltered. DSTi0 and DSTi1 are not overwritten, but passes through the PMAC unaltered to the DSTo output.

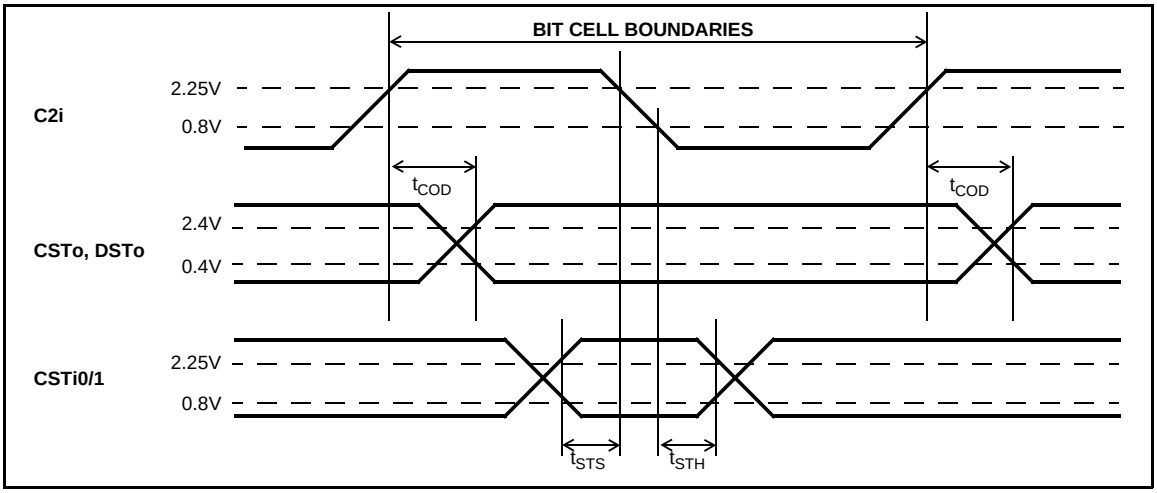


Figure 13 - ST-BUS Timing - CSTo/DSTo Altered by PMAC

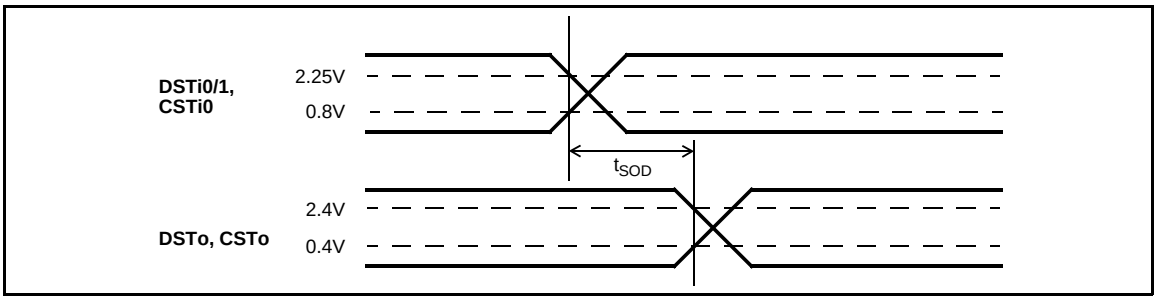


Figure 14 - T-BUS Timing - CSTo/DSTo Unaltered by PMAC

AC Electrical Characteristics† - Clock and Frame Pulse Timing (Figure 15)

	Parameters	Sym	Min	Typ‡	Max	Units	Test Conditions
1	C2i Clock Period	t_{2P}	400	488	600	ns	
2	C2i Clock Width High or Low	t_{2W}	200	244	300	ns	
3	Frame Pulse Setup Time	t_{FPS}	50			ns	
4	Frame Pulse Width High	t_{FPH}	50			ns	
5	Frame Pulse Width Low	t_{FPL}	50			ns	

† Timing is over recommended temperature & power supply voltage ranges.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

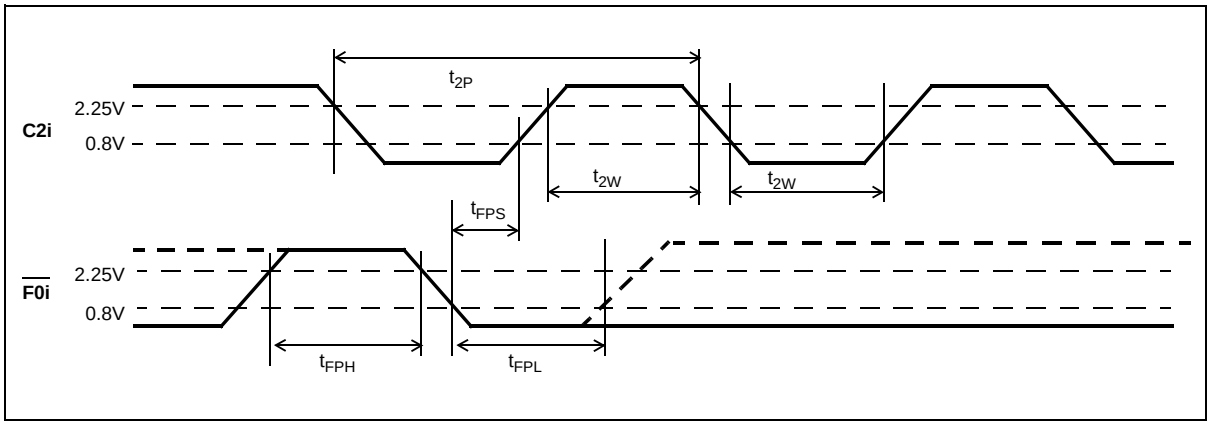


Figure 15 - T-BUS Clock and Frame Pulse Timing

AC Electrical Characteristics† - 1SEC Output Timing (Figure 16)

	Parameters	Sym	Min	Typ‡	Max	Units	Test Conditions
1	1SEC Output Delay	t_{1SD}			95	ns	150 pF load

† Timing is over recommended temperature & power supply voltage ranges.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

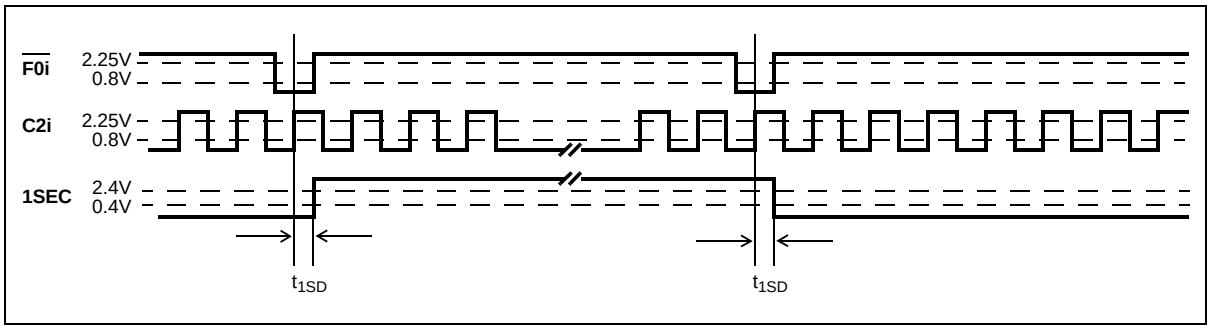
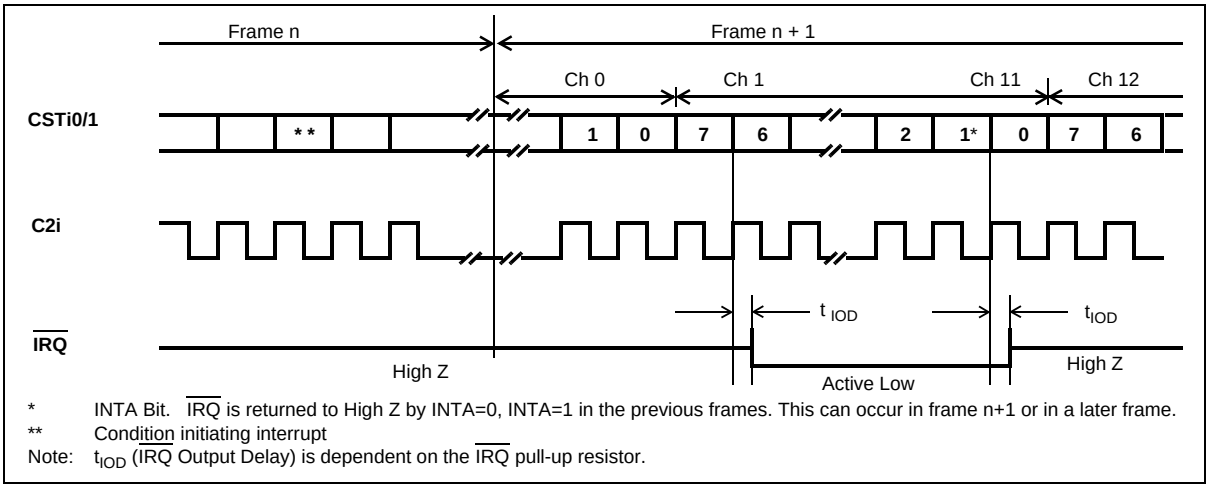


Figure 16 - 1SEC Timing



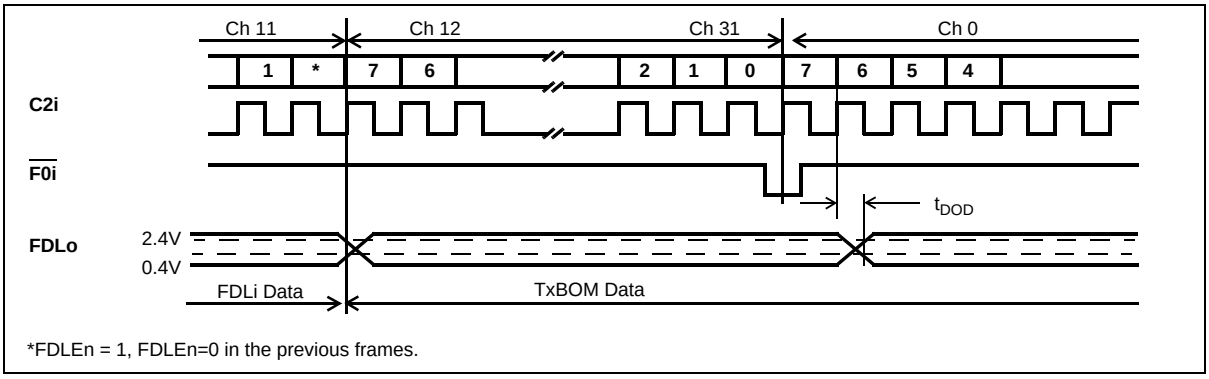
* INTA Bit. $\overline{IRQ}$ is returned to High Z by INTA=0, INTA=1 in the previous frames. This can occur in frame n+1 or in a later frame.
** Condition initiating interrupt
Note: t_{IOD} ($\overline{IRQ}$ Output Delay) is dependent on the $\overline{IRQ}$ pull-up resistor.

Figure 17 - Interrupt Functional Timing

AC Electrical Characteristics† - Facility Data Link Timing (Figures 18 and 19)

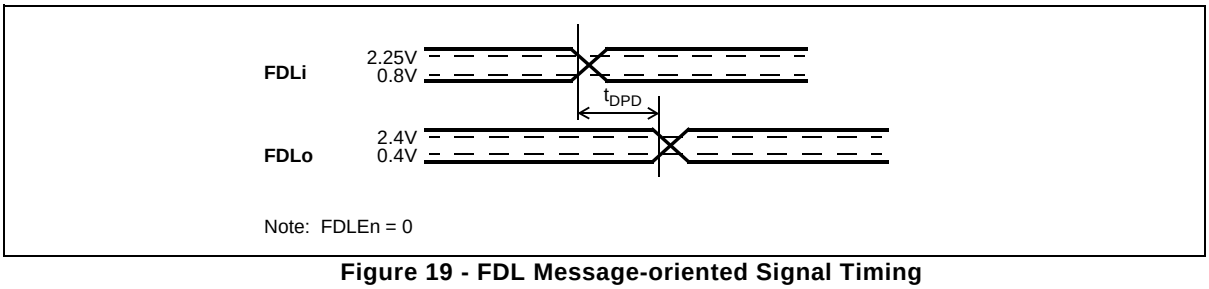
	Parameters	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Data Link Output Delay	t_{DOD}			45	ns	150 pF load
2	Data Link Propagation Delay	t_{DPD}			40	ns	150 pF load

† Timing is over recommended temperature & power supply voltage ranges.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.



*FDLEn = 1, FDLEn=0 in the previous frames.

Figure 18 - FDL Bit-oriented Message Timing



Note: FDLEn = 0

Figure 19 - FDL Message-oriented Signal Timing

Appendix

Control and Status Register Summary

7	6	5	4	3	2	1	0
Debounce 1 Disabled 0 Enabled	**TSPZCS** 1 Disabled 0 Enabled	**B8ZS** 1 B8ZS 0 Jammed Bit	**8KHSel** 1 Disabled 0 Enabled	**XCtl** 1 Set High 0 Cleared	**ESFYLW** 1 Enabled 0 Disabled	**Robbed Bit** 1 Disabled 0 Enabled	**YLALR** 1 Enabled 0 Disabled

Master Control Word 1 (Channel 15, CSTi0)

RMLOOP 1 Enabled 0 Disabled	**DGLOOP** 1 Enabled 0 Disabled	**ALL 1's** 1 Enabled 0 Disabled	**ESF/D4** 1 ESF 0 D3/D4	**Reframe** Device Reframes on High to Low Transition	**SLC-96** 1 Enabled 0 Disabled	**CRC/MIMIC** See Note 1	**Maint.** 1 4/12 0 2/4

Master Control Word 2 (Channel 31, CSTi0)

UNUSED - KEEP AT 0	**Polarity** 1 No Inversion 0 Inversion	**Loop** 1 Ch. looped back 0 Normal	**Data** 1 Enabled 0 Disabled

Per Channel Control Words (All Channels on CSTi0 Except Channels 3, 7, 11, 15, 19, 23, 27 and 31)

Transmitted First	TxBOM	Transmitted Last

Transmit Bit-Oriented Message Register (Channel 7, CSTi1)

SER High-to-Low Reset	**FER** High-to-Low Reset	**CRCR** High-to-Low Reset	**BPVR** High-to-Low Reset	**FSel** 1 F_S, F_T, FPS 0 F_T only	**8KEn** 1 Enabled 0 Disabled	**INTA** 1 Enabled 0 Disabled/ Clear	**FDLEn** 1 TxBOM-to-FDL 0 FDLi-to-FDLo

PMAC Control Word (Channel 11, CSTi1)

UNUSED	00 Normal 01 Payload 10 LL Enable 11 LL Disable

Loopback Control Word (Channel 15, CSTi1)

UNUSED - KEEP AT 0	**A** Txt. Sig. Bit	**B** Txt. Sig. Bit	**C** Txt. Sig. Bit	**D** Txt. Sig. Bit

Per Channel Control Words (All Channels on CSTi1 Except Channels 3, 7, 11, 15, 19, 23, 27 and 31)

CHANNEL COUNT	BIT COUNT

Phase Status Word (Channel 3, CSTo)

Appendix (continued)

Control and Status Register Summary

7	6	5	4	3	2	1	0
UNUSED			**LLDD** 1 Detected 0 Not Detected	**LLED** 1 Detected 0 Not Detected	**FECV** 1 In-Sync 0 Out-of-Sync	**TMR** Changes State once per second	**BOMV** 1 Valid 0 Invalid

PMAC Miscellaneous Status Word (Channel 7, CSTo)

CRC ERROR COUNT

Cyclic Redundancy Check-6 Error Counter (Channel 11, CSTo)

YLALR 1 Detected 0 Normal	**MIMIC** 1 Detected 0 Not Detected	**ALRM** 1 Detected 0 Not Detected	**RAI** 1 Detected 0 Not Detected	**$\overline{\text{MFSYNC}}$** 1 Not Detected 0 Detected	**LOS** 1 Detected 0 Normal	**SLIP** Changes State when Slip Performed	**$\overline{\text{SYN}}$** 1 Out-of-Sync. 0 In-Sync

Master Status Word 1 (Channel 15, CSTo)

SEVERELY ERRORED FRAMING EVENT COUNTER (SE)	FRAMING ERROR COUNTER (FE)

Severely Errored Framing Event and Error Counters (Channel 19, CSTo)

BPV ERROR COUNT

Bipolar Violation Error Counter (Channel 23, CSTo)

Received First	RxBOM	Received Last

Receive Bit-Oriented Message Register (Channel 27, CSTo)

BlAlm 1 Detected 0 Not Detected	**FrCnt** Frame Count	**XSt** 1 XSt High 0 XSt Low	**SEI** 1 SE Toggles 0 SER High-to-Low	**FSI** 1 FE F-to-0 0 FEF High-to-Low	**CSI** 1 CRC FF-to-00 0 CRCR High-to-Low	**BSI** 1 BPV FF-to-00 0 BPVR High-to-Low	**AIS** 1 Detected 0 Not Detected

Master Status Word 2 (Channel 31, CSTo)

UNUSED	**A** Rec'd. Sig. Bit	**B** Rec'd. Sig. Bit	**C** Rec'd. Sig. Bit	**D** Rec'd. Sig. Bit

Per Channel Status Word (All Channels on CSTo Except Channels 3, 7, 11, 15, 19, 23, 27, 31)

Note 1: In ESF mode:
1: CRC calc. ignored during Sync.
0: CRC checked for Sync.
In D3/D4 mode:
1: Sync. to first correct S-bit pattern.
0: Will not Sync. if Mimic detected.

For more information about all Zarlink products
visit our Web Site at

www.zarlink.com

TECHNICAL DOCUMENTATION - NOT FOR RESALE