40V COMPLEMENTARY PAIR ENHANCEMENT MODE MOSFET

Product Summary

Device	$V_{(BR)DSS}$	$R_{DS(on)}$ max	I_D max (A) T_A = 25°C (Notes 3 & 5)
Q1	40V	25mΩ @ V_{GS}= 10V	7.5
		40mΩ @ V_{GS}= 4.5V	6.2
Q2	-40V	25mΩ @ V_{GS}= -10V	-7.3
		45mΩ @ V_{GS}= -4.5V	-5.7

Features and Benefits

- Matched N & P $R_{DS(on)}$ - Minimizes power losses
- Fast switching – Minimizes switching losses
- Dual device – Reduces PCB area
- **"Green" component and RoHS compliant (Note 1)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

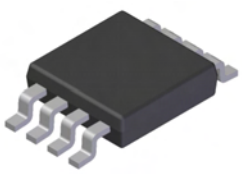
- Case: SO-8
- Case Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0 (Note 1)
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Matte Tin annealed over Copper lead frame. Solderable per MIL-STD-202, Method 208
- Weight: 0.074 grams (approximate)

Description and Applications

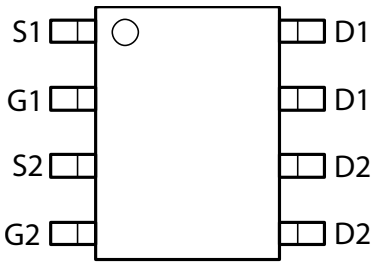
This MOSFET has been designed to ensure that $R_{DS(on)}$ of N and P channel FET are matched to minimize losses in both arms of the bridge. The DMC4040SSD is optimized for use in 3 phases brushless DC motor circuits (BLDC), CCFL backlighting.

- 3 phases BLDC motor
- CCFL backlighting

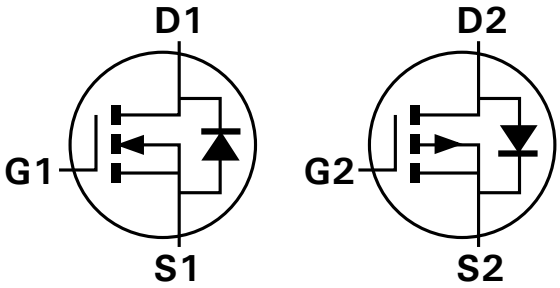
SO-8



Top View



Top View



Q1 N-Channel

Q2 P-Channel

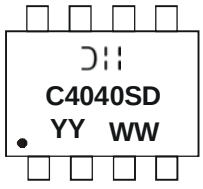
Equivalent Circuit

Ordering Information (Note 1)

Product	Marking	Reel size (inches)	Tape width (mm)	Quantity per reel
DMC4040SSD-13	C4040SD	13	12	2,500

Note: 1. Diodes, Inc. defines “Green” products as those which are RoHS compliant and contain no halogens or antimony compounds; further information about Diodes Inc.’s “Green” Policy can be found on our website. For packaging details, go to our website.

Marking Information



= Manufacturer’s Marking
C4040SD = Product Type Marking Code
YYWW = Date Code Marking
YY = Year (ex: 10 = 2010)
WW = Week (01 - 53)

Maximum Ratings @T_A = 25°C unless otherwise specified

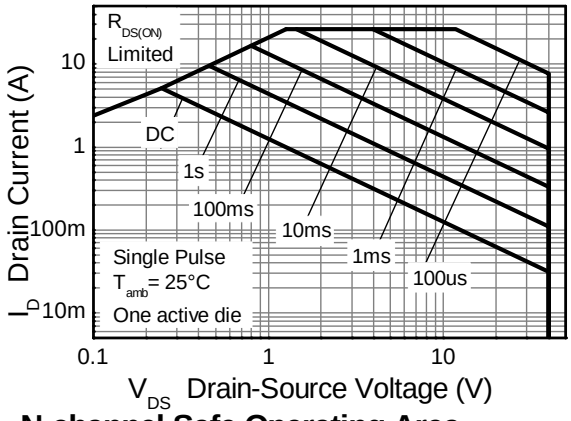
Characteristic			Symbol	N-Channel - Q1	P-Channel - Q2	Unit
Drain-Source Voltage			V_{DSS}	40	-40	V
Gate-Source Voltage			V_{GSS}	±20	±20	
Continuous Drain Current	V_{GS} = 10V	(Notes 3 & 5)	I_D	7.5	-7.5	A
		T_A = 70°C (Notes 3 & 5)		5.8	-5.8	
		(Notes 2 & 5)		5.7	-5.7	
		(Notes 2 & 6)		6.8	-6.8	
Pulsed Drain Current	V_{GS} = 10V	(Notes 4 & 5)	I_{DM}	29.0	-29.0	
Continuous Source Current (Body diode)		(Notes 3 & 5)	I_S	3.0	-3.0	
Pulsed Source Current (Body diode)		(Notes 4 & 5)	I_{SM}	29.0	-29.0	

Thermal Characteristics @T_A = 25°C unless otherwise specified

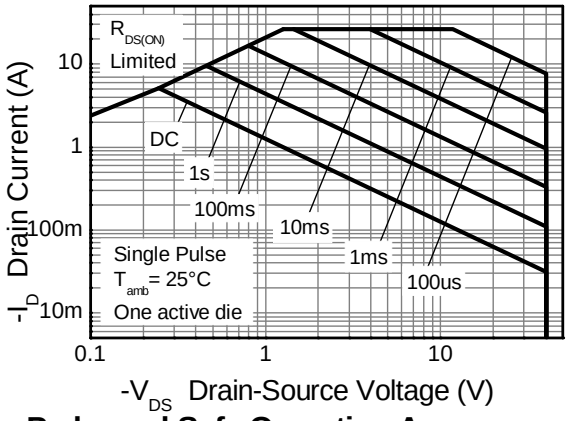
Characteristic		Symbol	N-Channel - Q1 / P-Channel - Q2	Unit
Power Dissipation Linear Derating Factor	(Notes 2 & 5)	P_D	1.25 10	W mW/°C
	(Notes 2 & 6)		1.8 14.3	
	(Notes 3 & 5)		2.14 17.2	
Thermal Resistance, Junction to Ambient	(Notes 2 & 5)	$R_{\theta JA}$	100	°C/W
	(Notes 2 & 6)		70	
	(Notes 3 & 5)		58	
Thermal Resistance, Junction to Lead	(Notes 5 & 7)	$R_{\theta JL}$	51	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Notes:
2. For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
3. Same as note (2), except the device is measured at t ≤ 10 sec.
4. Same as note (2), except the device is pulsed with D = 0.02 and pulse width 300µs.
5. For a dual device with one active die.
6. For a device with two active die running at equal power.
7. Thermal resistance from junction to solder-point (at the end of the drain lead).

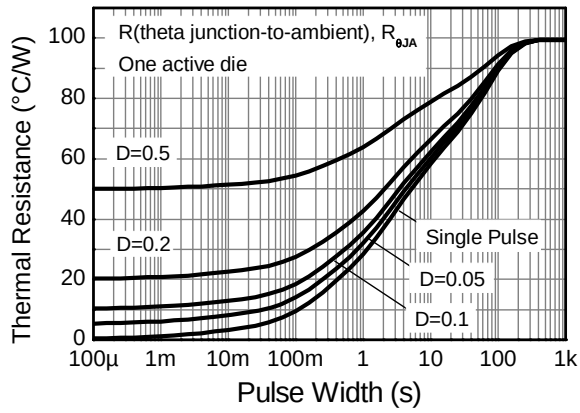
Thermal Characteristics



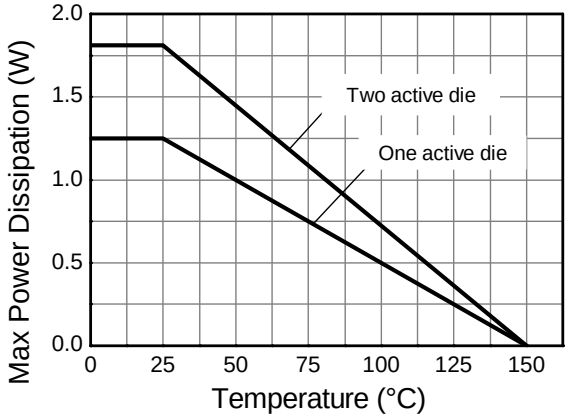
N-channel Safe Operating Area



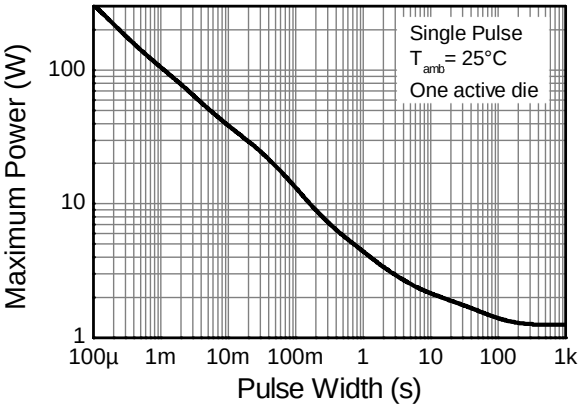
P-channel Safe Operating Area



Transient Thermal Impedance



Derating Curve



Pulse Power Dissipation

Electrical Characteristics – Q1 N-CHANNEL @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	40	—	—	V	I_D = 250μA, V_{GS}= 0V
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1.0	μA	V_{DS}= 40V, V_{GS}= 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS}= ±20V, V_{DS}= 0V
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(th)}$	0.8	1.3	1.8	V	I_D= 250μA, V_{DS}= V_{GS}
Static Drain-Source On-Resistance (Note 8)	$R_{DS\ (ON)}$	—	0.013	0.025	Ω	V_{GS}= 10V, I_D= 3A
			0.028	0.040		V_{GS}= 4.5V, I_D= 3A
Forward Transconductance (Notes 8 & 9)	g_{fs}	—	12.6	—	S	V_{DS}= 5V, I_D= 3A
Diode Forward Voltage (Note 8)	V_{SD}	—	0.7	1.0	V	I_S= 1A, V_{GS}= 0V
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	1790	—	pF	V_{DS}= 20V, V_{GS}= 0V f= 1MHz
Output Capacitance	C_{oss}	—	160	—		
Reverse Transfer Capacitance	C_{rss}	—	120	—		
Gate Resistance	R_g	—	1.03	—	Ω	V_{DS}= 0V, V_{GS}= 0V, f= 1MHz
Total Gate Charge (Note 10)	Q_g	—	16.0	—	nC	V_{GS}= 4.5V; V_{DS}= 20V, I_D= 3A
Total Gate Charge (Note 10)	Q_g	—	37.6	—		V_{GS}= 10V; V_{DS}= 20V, I_D= 3A
Gate-Source Charge (Note 10)	Q_{gs}	—	7.8	—		
Gate-Drain Charge (Note 10)	Q_{gd}	—	6.6	—		
Turn-On Delay Time (Note 10)	$t_{D(on)}$	—	8.1	—	ns	V_{DD}= 20V, V_{GS}= 10V I_D= 3A
Turn-On Rise Time (Note 10)	t_r	—	15.1	—		
Turn-Off Delay Time (Note 10)	$t_{D(off)}$	—	24.3	—		
Turn-Off Fall Time (Note 10)	t_f	—	5.3	—		

Notes: 8. Measured under pulsed conditions. Pulse width ≤ 300μs; duty cycle ≤ 2%
9. For design aid only, not subject to production testing.
10. Switching characteristics are independent of operating junction temperatures.

Typical Characteristics – Q1 N-Channel

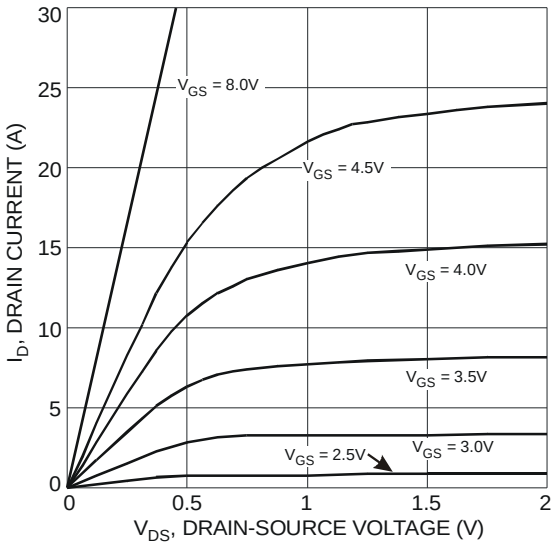


Fig. 1 Typical Output Characteristic

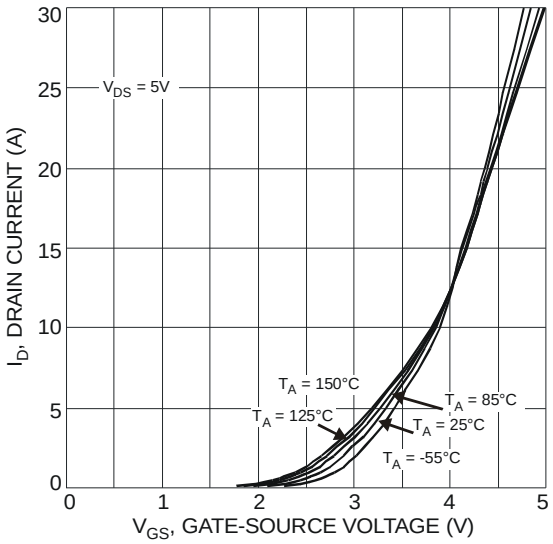


Fig. 2 Typical Transfer Characteristic

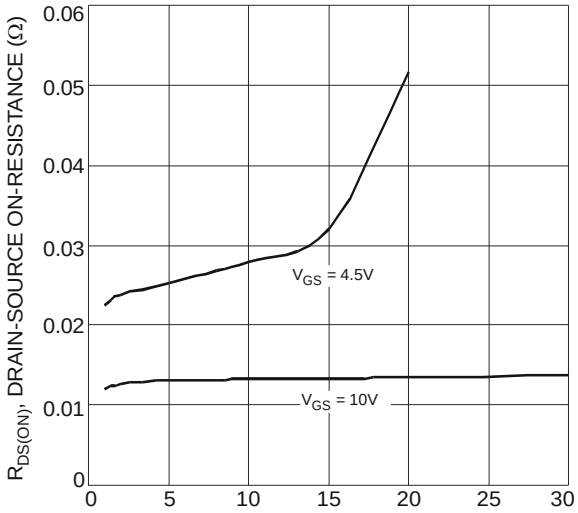


Fig. 3 Typical On-Resistance
vs. Drain Current and Gate Voltage

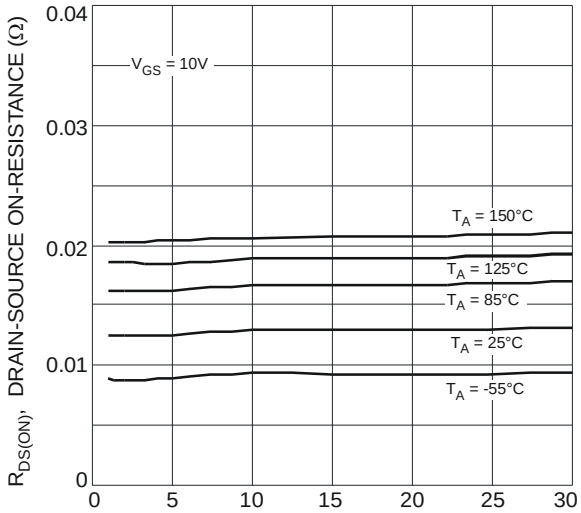


Fig. 4 Typical On-Resistance
vs. Drain Current and Temperature

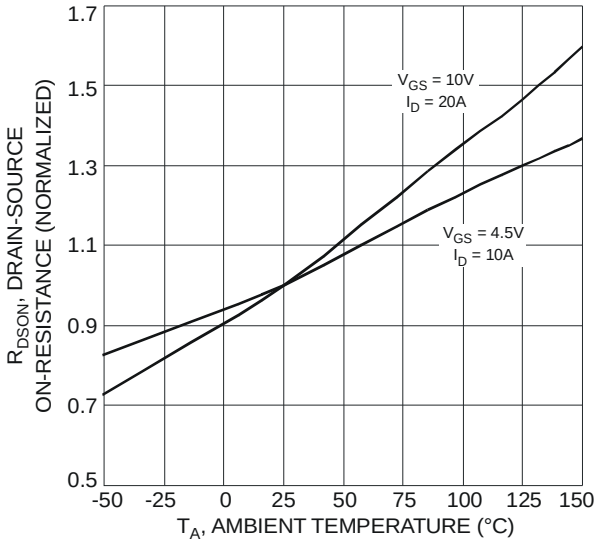


Fig. 5 On-Resistance Variation with Temperature

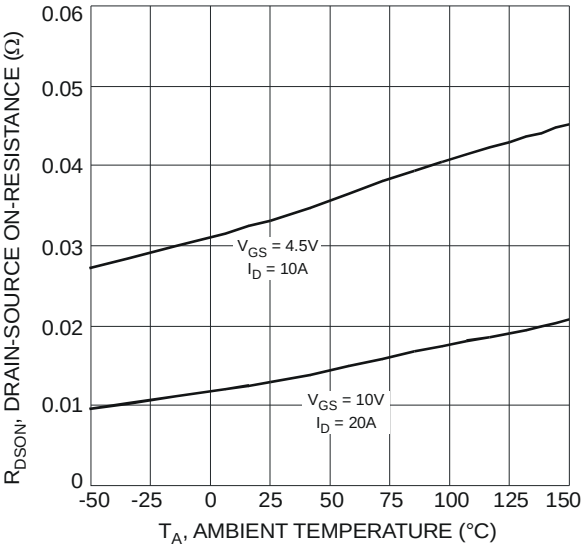


Fig. 6 On-Resistance Variation with Temperature

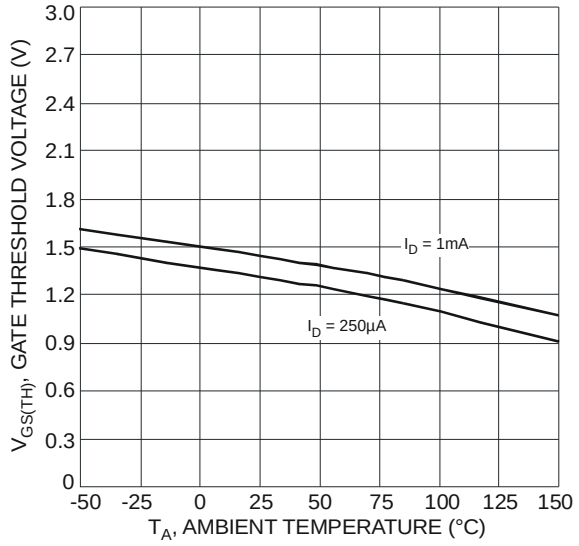


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

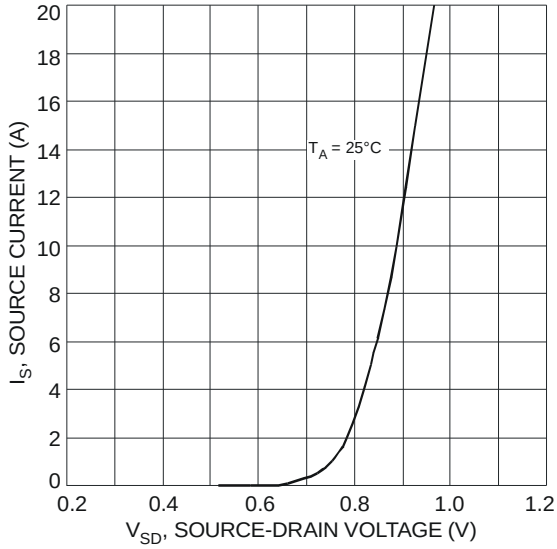


Fig. 8 Diode Forward Voltage vs. Current

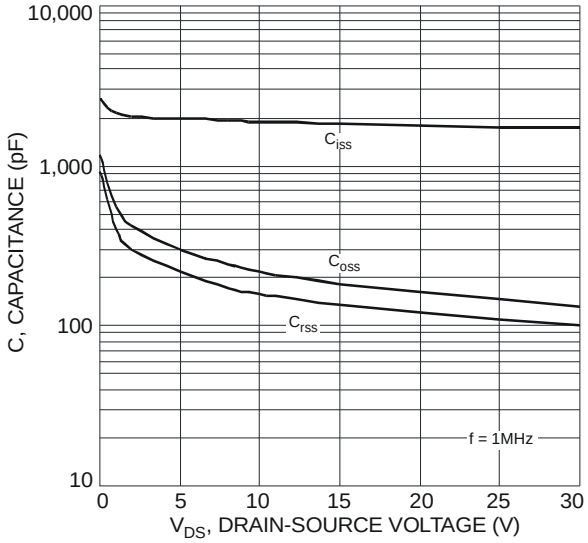


Fig. 9 Typical Total Capacitance

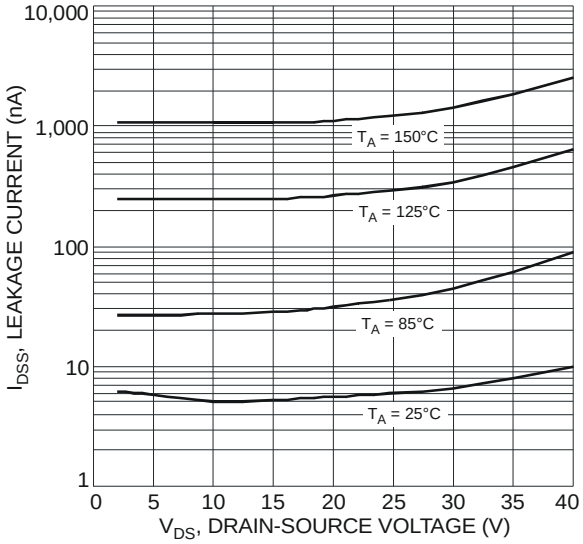


Fig. 10 Typical Leakage Current
vs. Drain-Source Voltage

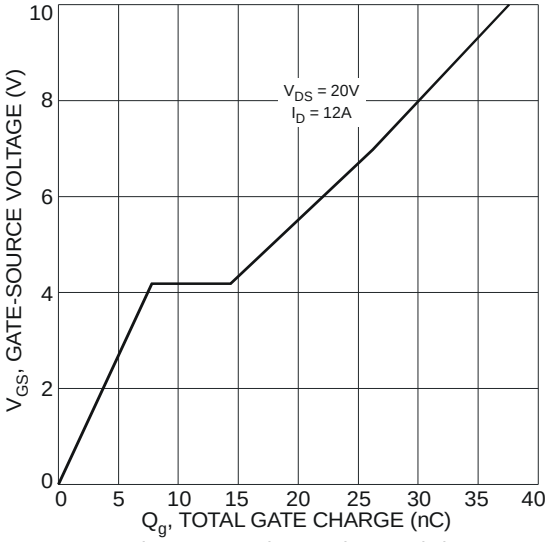


Fig. 11 Gate-Charge Characteristics

Electrical Characteristics – Q2 P-CHANNEL @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	-40	–	–	V	I_D = -250μA, V_{GS} = 0V
Zero Gate Voltage Drain Current	I_{DSS}	–	–	-1.0	μA	V_{DS} = -40V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	–	–	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(th)}$	-0.8	-1.3	-1.8	V	I_D = -250μA, V_{DS} = V_{GS}
Static Drain-Source On-Resistance (Note 11)	$R_{DS(on)}$	–	0.018	0.025	Ω	V_{GS} = -10V, I_D = -3A
			0.030	0.045		V_{GS} = -4.5V, I_D = -3A
Forward Transconductance (Notes 11 & 12)	g_{fs}	–	16.6	–	S	V_{DS} = -5V, I_D = -3A
Diode Forward Voltage (Note 11)	V_{SD}	–	-0.7	-1.0	V	I_S = -1A, V_{GS} = 0V
DYNAMIC CHARACTERISTICS (Note 12)						
Input Capacitance	C_{iss}	–	1643	–	pF	V_{DS} = -20V, V_{GS} = 0V f = 1MHz
Output Capacitance	C_{oss}	–	179	–		
Reverse Transfer Capacitance	C_{rss}	–	128	–		
Gate Resistance	R_g	—	6.43	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (Note 13)	Q_g	–	14.0	–	nC	V_{GS} = -4.5V; V_{DS} = -20V, I_D = -3A
Total Gate Charge (Note 13)	Q_g	–	33.7	–		V_{GS} = -10V; V_{DS} = -20V, I_D = -3A
Gate-Source Charge (Note 13)	Q_{gs}	–	5.5	–		
Gate-Drain Charge (Note 13)	Q_{gd}	–	7.3	–		
Turn-On Delay Time (Note 13)	$t_{D(on)}$	–	6.9	–	ns	V_{DD} = -20V, V_{GS} = -10V I_D = -3A
Turn-On Rise Time (Note 13)	t_r	–	14.7	–		
Turn-Off Delay Time (Note 13)	$t_{D(off)}$	–	53.7	–		
Turn-Off Fall Time (Note 13)	t_f	–	30.9	–		

Notes: 11.Measured under pulsed conditions. Pulse width ≤ 300μs; duty cycle ≤ 2%
12. For design aid only, not subject to production testing.
13. Switching characteristics are independent of operating junction temperatures.

Typical Characteristics – Q2 P-Channel

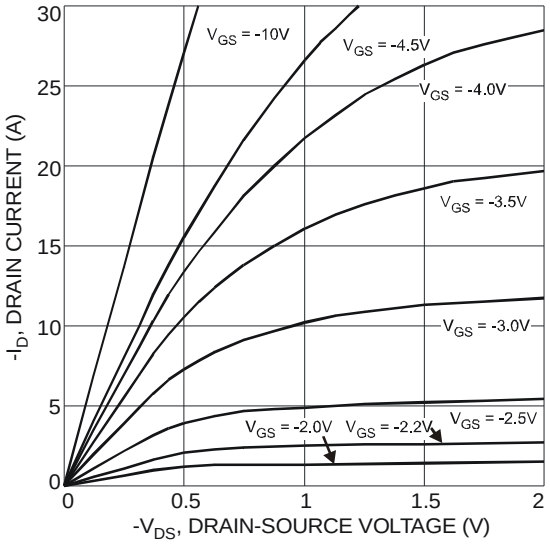


Fig. 12 Typical Output Characteristic

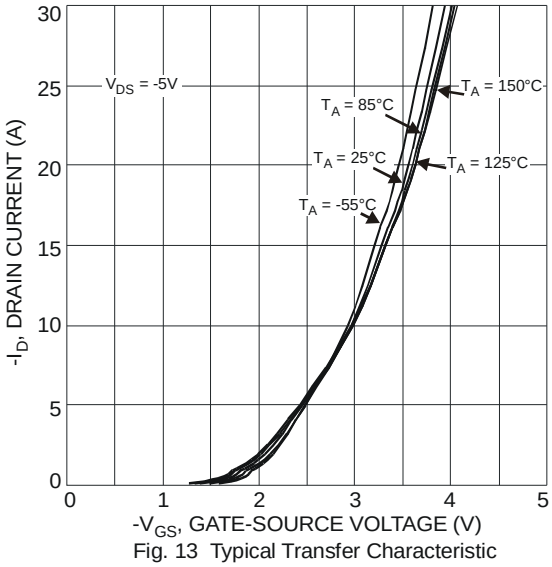


Fig. 13 Typical Transfer Characteristic

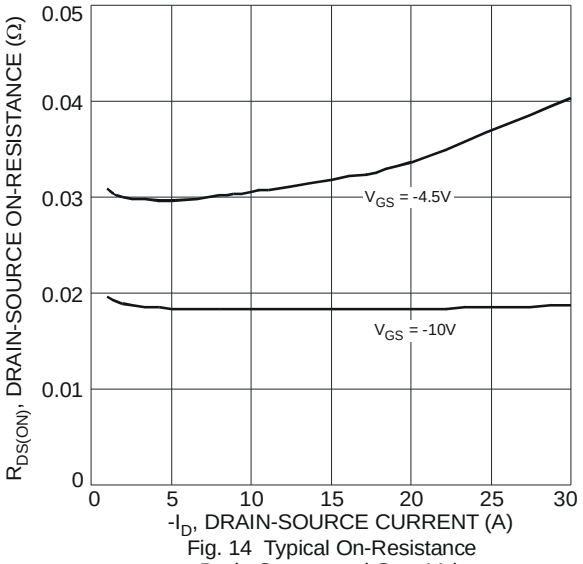


Fig. 14 Typical On-Resistance
vs. Drain Current and Gate Voltage

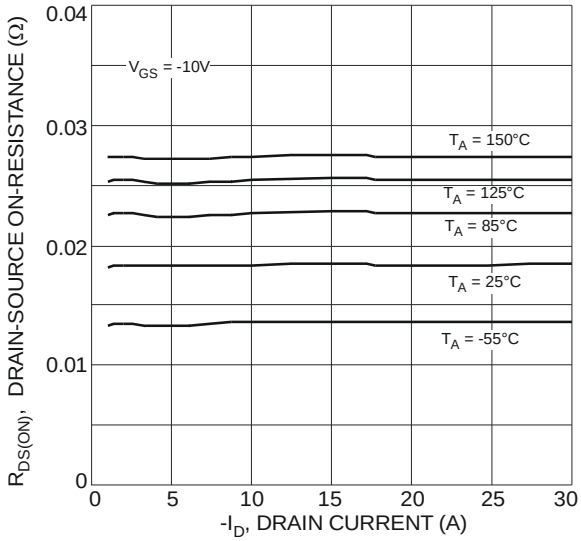


Fig. 15 Typical On-Resistance
vs. Drain Current and Temperature

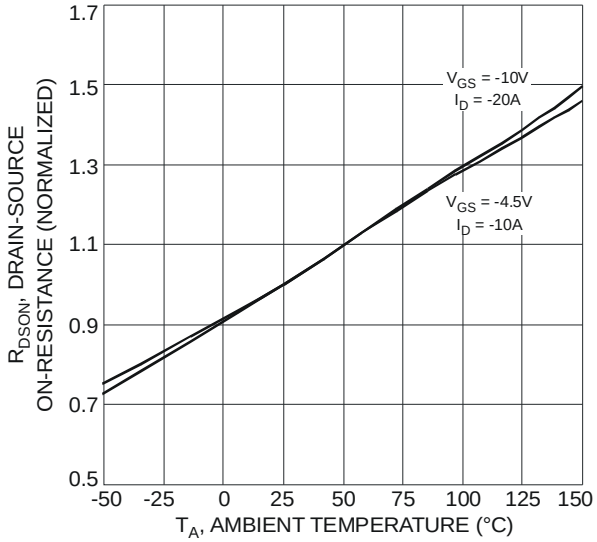


Fig. 16 On-Resistance Variation with Temperature

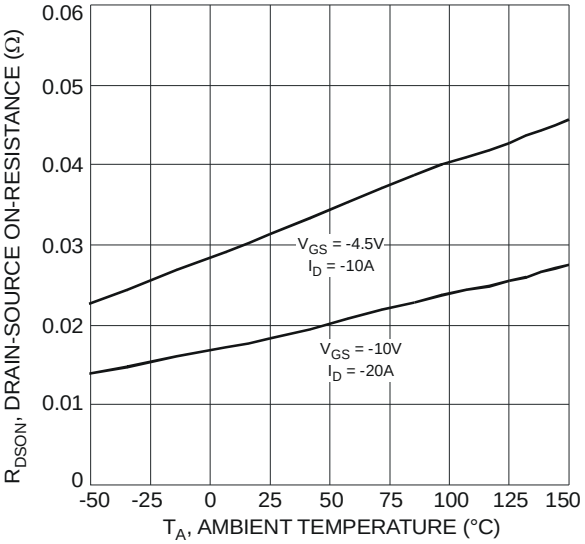


Fig. 17 On-Resistance Variation with Temperature

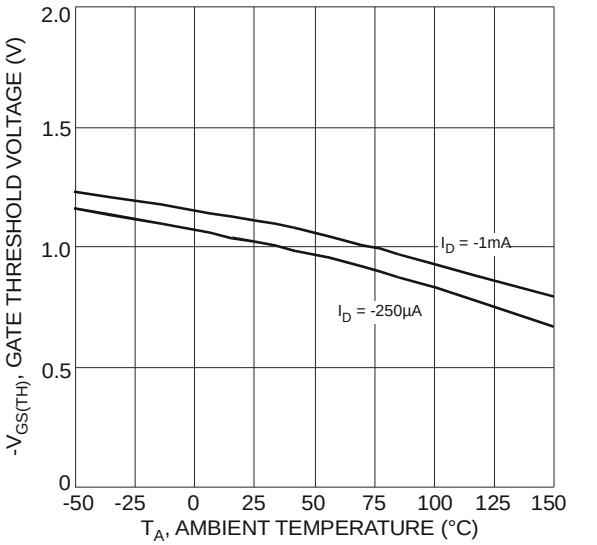


Fig. 18 Gate Threshold Variation vs. Ambient Temperature

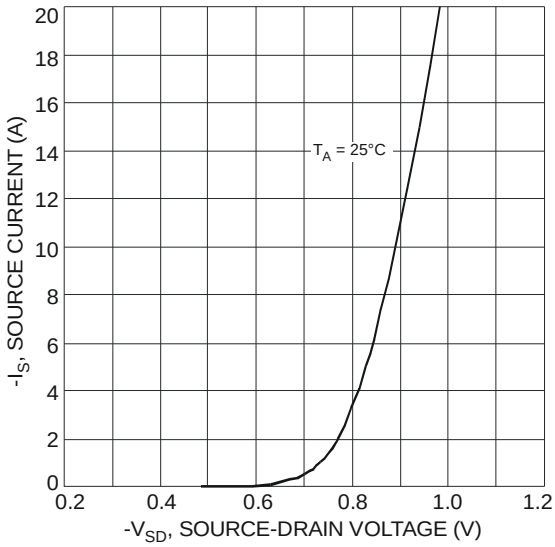


Fig. 19 Diode Forward Voltage vs. Current

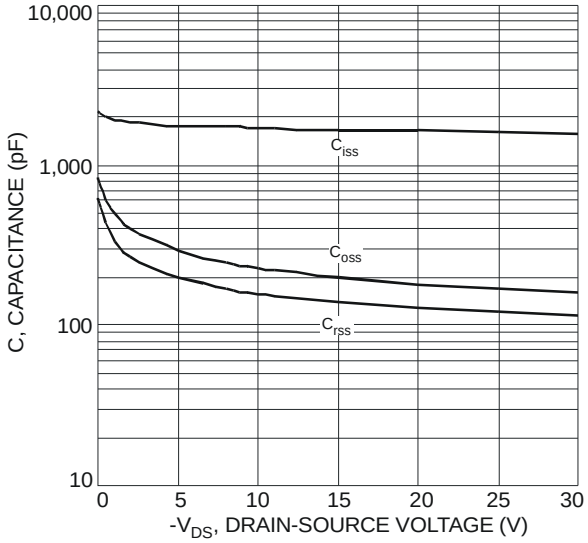


Fig. 20 Typical Total Capacitance

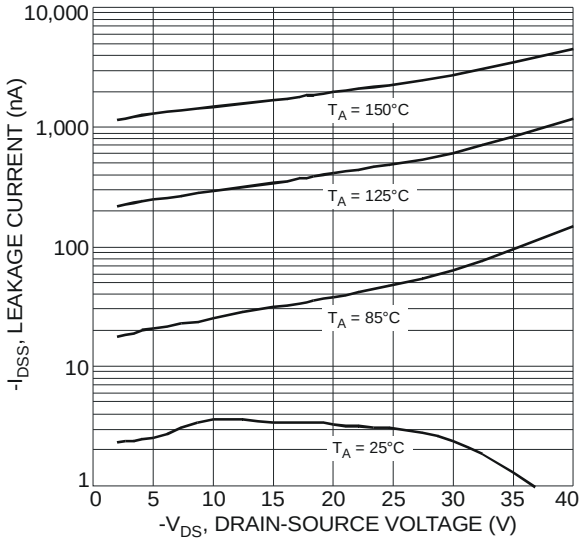


Fig. 21 Typical Leakage Current
vs. Drain-Source Voltage

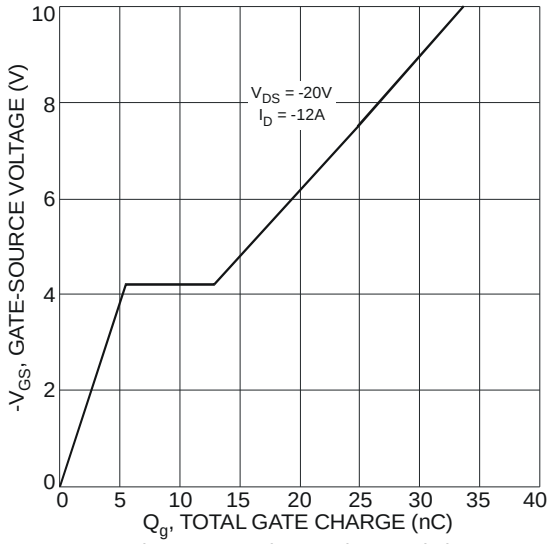
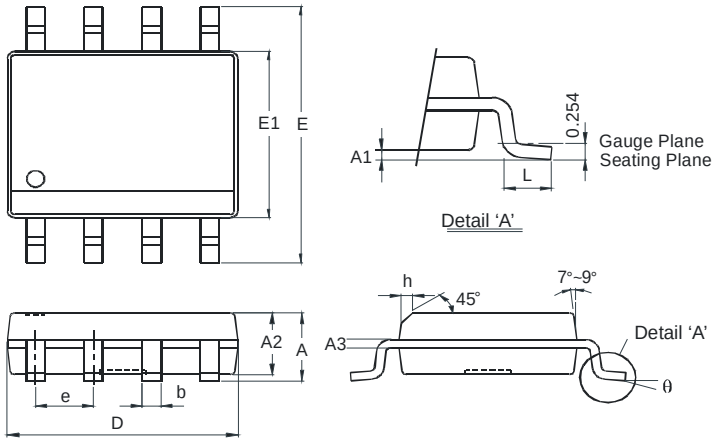


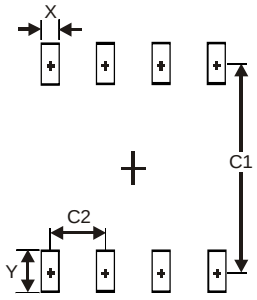
Fig. 22 Gate-Charge Characteristics

Package Outline Dimensions



SO-8		
Dim	**Min**	**Max**
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

Suggested Pad Layout



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

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2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

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