SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

MULTIFREQUENCY AND AUTO-ADAPTATIVE APPLICATIONS WITH TDA9102C

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SUMMARY **Page**

In the following pages, we examine how to design variable frequency applications with TDA9102C. The design rules will be applied to the calculation of a self-contained, autoadaptive application with characteristics as below :

- Horizontal frequency 30....90kHz
- Vertical frequency 40....120Hz, constant oscillator amplitude
- Sync signals : TTL levels, positive or negative
- Vertical S-correction independent of frequency
- DC adjustment of Horizontal phase and Vertical scanning amplitude.

Further to the TDA9102C, one TTL X-OR, one quad op-amp and three small signal transistors are used.

In the description, reference will be made to the TDA 9102C Application Note by F. GRILLI, simply quoted as "AN540 Application Note".

I - HORIZONTAL OSCILLATOR

I.1 - Programming the Horizontal Open Loop Frequency

As explained in page 10 of "AN540 Application Note", when the first phase-locked loop PLL1 is open, the horizontal frequency is proportional to the current sunk from Pin 1 :

Open-loop Free-running frequency

$$f_0 = \frac{0.375 \cdot I_1}{C17 \cdot \Delta V}$$

C17 : Capacitor on Pin 2

ΔV = 4V typ. (in standard application, oscillation takes place between 2.5V and 6.5V)

The main sources of discrepancy versus ideal law are two :

- a parasitic bias current (about 2.5µA) which adds to current sunk from Pin 1.
- the time θ needed for comparators to switch from "charge" to "discharge" and back, which is about 0.5µs.

First cause will be made negligible by choosing a high value for I_1 (not exceeding 1.5mA for max frequency). Second cause represents +3% on period for 64kHz, +4.5% for 90kHz. If necessary, this can be compensated by introducing a resistor in series with the oscillator capacitor, as will be seen in § I-4-2.

I.1.1 - Frequency-to-current Converter

If the phase-locked loop PLL1 of TDA 9102C were able to lock in the whole range 25 to 90kHz, it would have a chance to lock on half the sync frequency f_H : to avoid this problem,it is necessary to limit the holding range of PLL1 to less than ± 50% and to preprogram the oscillation frequency by sinking from Pin 1 a current roughly proportionnal to sync frequency ; then PLL1 performs fine tuning.

A simple and sufficiently precise ($f_H \rightarrow I$) converter was designed, using the constant amplitude pulse on Pin 5, triggered by the horizontal sync pulse. (See schematic Figure 6). For every pulse, capacitor C29 is fastly charged to a constant voltage, then discharged in an exponential way through R41. Taking the average value of the resulting periodic waveform provides a voltage proportional to frequency. This is done by the filter R42 - C30. Same voltage will be found on R44, thanks to T2 controlled by an op-amp.: consequently R44 will conduct a current proportional to frequency, sinking from Pin 1 either through T2 or through R45.

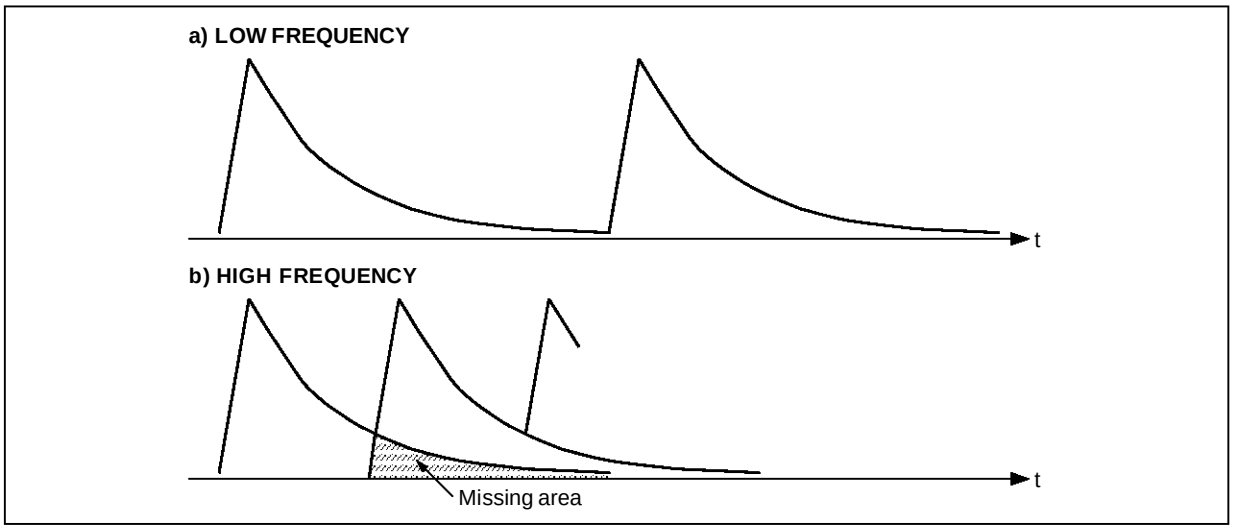
When no sync pulse is present, T2 will not conduct; at that moment, the current sunk from Pin 1 will be determined by R44 - R45 in series. This corresponds to the no-sync free-running frequency.

The above analysis is valid only if C29 is completely discharged when next pulse occurs. This in fact is not the case in the present design : The result is that, compared to low frequencies, the late part of the integrated waveform is missing at high frequencies : (Figure 1).

This, combined with the effect described in § 1, leads to a less than linear ($I_1 \rightarrow f_0$) characteristic at high frequencies (see Figure 3).

The way to compensate for this and other second-order effects will be examined in § I.4.2.

Figure 1



I.1.2 - Programming Precision

The precision of this converter may be evaluated as follows :

- Peak voltage on C29 5%
- Resistors (2) 2%
- Oscillator thresholds 4%
- Capacitors (2) $2 \cdot X\%$

Since unprecision, not including capacitors and non linearity, is already $\pm$ 11%, it is advisable to adopt capacitors with 2% precision in order to maintain the necessary adjustment to a reasonable amount.

I.2 - PLL1 Holding and Capture Range

PLL1 maintains the oscillator locked by injecting positive or negative current from Pin 3 to Pin 1 and thus correcting any difference between f_H and f_0. The capture range is narrower than or equal to holding range.

The way PLL1 works is explained on page 4 of "AN540 Application Note" and summarized below : Each incoming sync pulse triggers an internal sync pulse, of which the duration t_5 is dependant on the value of capacitor on Pin 5, C21.
During t_5, a comparator will activate a 4mA sink or source current (depending on the phase error to be recovered); this current, once filtered, is injected into Pin 1 for correction purpose.

Hence the maximum DC correction current available amounts to : $t_5 \cdot f_0 \cdot 4 \cdot 10^{-3}$

The ratio of this DC current to the DC programming current sunk from Pin 1 gives the relative hold frequency range. Since the programming current is proportional to frequency, therefore this ratio is constant : The hold frequency range is a constant fraction of programmed frequency :

$$\frac{\Delta f}{f_0} = t_5 \cdot f_0 \cdot 4 \cdot 10^{-3} \cdot \frac{0.375}{f_0 \cdot C17 \cdot \Delta V} = 0.375 \cdot \frac{t_5}{C17}$$

For instance, with C17 = 1nF and t_5 = 1µs, the relative holding range will be 37.5%.

The above analysis is valid only if voltage on Pin 3 is not clamped, since possible excursion on this pin is 3.5 $\pm$ 2V. When clamping occurs, the possible amount of correction depends on R24 : from Equation 1,

$$\Delta f_0 = \frac{0.375}{C17 \cdot \Delta V} \cdot \frac{2}{R24} = \frac{0.375}{2 \cdot C17 \cdot 24}$$

In present design, the holding range (limited by clamping at high frequencies) has been chosen to be higher than desired capture range at 90kHz ; it remains constant for lower frequencies, till limitation by t_5 occurs in the low end of the range. Limiting the holding range improves the capture behaviour.

I.3 - Miscellaneous

Though the suggestions below were not used in present design, they might prove helpful in other cases.

I.3.1 - Programming Duty Factor

When using a single bipolar transistor as horizontal power switch, it can be necessary to increase the duty factor at high frequencies, because the transistor desaturation time, which amounts to 1.5...4µs, occupies a more and more important fraction of the period (duty factor is defined as the ratio of time during which the transistor base is driven LOW, to total period). This was not found necessary in the present design, which is intended to control a compound (Bipolar + MOS) power switch with desaturation time around 1µs.

Nevertheless, herebelow is described a method to increase the duty factor.

For that purpose, connect a resistor R54 in series with the oscillator capacitor, C17.

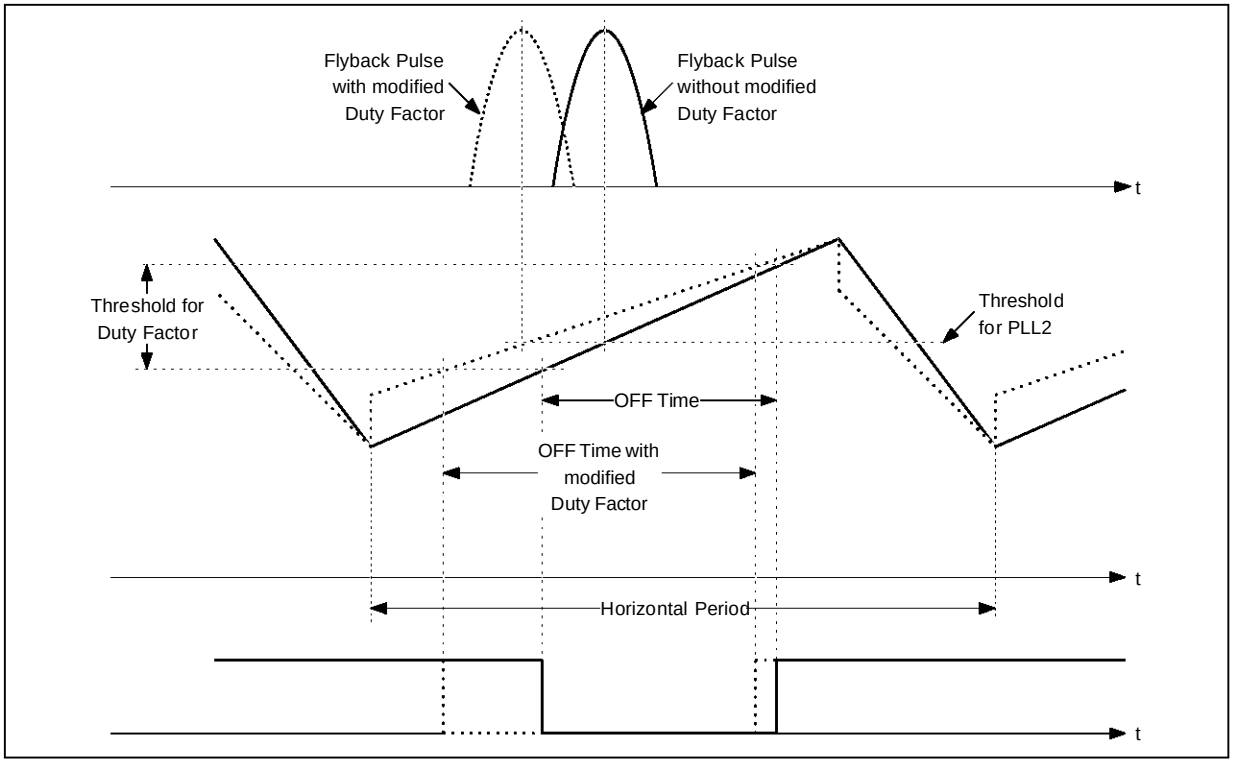
R54 will be crossed by the charge and discharge currents ; the corresponding voltage drops will reduce the ramp voltage amplitude, while the two thresholds which determine duty factor keep the same interval (Figure 2).

By this method, duty factor will remain near to 41% in the low frequency range and progressively increase at high frequencies.

Nevertheless, it is advisable not to overcome 50 %, since this could impair the locking capability of PLL1.

A secondary effect is that in the formula of § 1, ΔV, rather than keeping constant, will decrease when more current is sunk from Pin 1 : Consequently, the oscillation frequency will increase more than proportionally to current in Pin 1, as regards the high frequency range. This will more or less compensate the less than proportional characteristic of ($f_H \rightarrow I$) converter described in § I.1.1, as will be seen in the Calculations Section.

Figure 2



I.3.2 - Shifting the Phase Reference

In standard applications, PLL 2 will maintain the flyback pulse centered on that moment when the oscillator sawtooth crosses the 4.5V level (see Figure 2). When R54 is used, this moment occurs earlier within the period, allowing lowered adjustment margin for fly-back pulse phase.

Some margin may be recovered by injecting a current into Pin 9 ; this will give an offset to PLL2 and some point of the fly-back pulse, earlier than its middle, will now coincide with the 4.5V crossing. The flyback pulse can be delayed this way by not more than half its duration.

Since the sink and source currents of PLL2 on Pin 9 are in the mA range, substantially less than 1mA (average) should be injected for the duration of flyback pulse, or a DC current with same mean value.

The former method is preferred since it provides constant delay versus frequency (injecting DC current makes the delay increase when frequency decreases with the risk of exceeding the allowed value). It can be implemented with a diode and high value resistor from flyback pulse to Pin 9.

The phase control of PLL2 is not implemented on the demoboard.

I.4 - Calculations

I.4.1 - Frequency-to-current Converter

Every occurring sync pulse triggers the rise of Pin 5 voltage , up to a threshold normally equal to 6V.

In fact, because of a comparator delay, the threshold will overstep this level by an amount proportional to the reverse of t_5. If we choose $t_5 = 1\mu s$ (see § I-4), which corresponds to C21 = 27pF, the peak voltage will be 7V.

On C29 will be found a peak voltage 0.7V lower, that is $V_P = 6.3V$

Then C29 will discharge exponentially into R41 till next sync pulse (see Figure 1). Consequently, if $t_H = \frac{1}{f_0}$ is the horizontal period, the average voltage on C29 will be :

$$V_m = \frac{V_P}{t_H}\left[\frac{t_5}{2} + \int_0^{t_H - t_5} \exp\left(\frac{-t}{R41 \cdot C29}\right) dt\right]$$

$$= \frac{V_P}{t_H}\left[\frac{t_5}{2} + R41 \cdot C29\left(1 - \exp\left(-\frac{t_H - t_5}{R41 \cdot C29}\right)\right)\right]$$

The exponential term is responsible for the less than linear response at high frequencies. It can be neglected for a rule-of-thumb calculation or in the low-frequency range.

In present case, our aim is to obtain on R44 a voltage in the range of 2.5V at 90kHz, so as to leave sufficient overhead to the collector of T2 (Voltage on Pin 1 is 3.5V). A time constant R41 · C29 = 3µs is convenient (less than one third of the shortest period), for instance

C29 = 680 pF (choice)

$$R41 = \frac{3 \cdot 10^{-6}}{0.68 \cdot 10^{-9}} = 4.41k\Omega$$

will provide from (2) :

$$V_m = \frac{6.3}{11.1}\left[\, 0.5 + 3\left(1 - e^{-\frac{10.1}{3}}\right)\right] = 1.945V \text{ at } 90kHz$$

where the exponential term is responsible for -3% deviation at 90kHz, compared to linear law.

The filter values are not critical : R42 = 1MΩ, and C30 = 47nF are convenient. Modifying C30 will change the rate at which horizontal frequency can change when receiving a new standard.

R43 = 1MΩ is placed in series with op-amp inverting input to compensate its input bias current. For stability reasons it is decoupled by C31.

I.4.2 - Oscillator

According to § I.1, C17 should be chosen in such way that I_1 be near to 1mA for the highest frequency ; equation (1) gives

$$C17 \leq \frac{0.375 \cdot 10^{-3}}{90 \cdot 10^{3} \cdot 4} = 1.04nF$$

C17 = 1nF is adopted.

- Correction of Deviation from Linear Law
  Equation (1) may be written as follows :

$$\frac{1}{f_0} = \frac{C17 \cdot \Delta V}{0.375 \cdot I_1}$$

  In fact, it was indicated that a delay θ was necessary for the comparators to switch from charge to discharge and back, so that a more precise equation is

$$\frac{1}{f_0} = \frac{C17 \cdot \Delta V}{0.375 \cdot I_1} + \theta \quad \theta \approx 0.5\mu s$$

  When R54 is connected in series with C17, it introduces a supplementary voltage drop equal to $0.5 \cdot I_1 \cdot R54$ during charge phase, and $1.5 \cdot I_1 \cdot R54$ during discharge phase.
  As a result, ΔV is reduced by an amount $2 \cdot I_1 \cdot R54$ and new oscillation frequency is given by

$$\frac{1}{f_0} = \frac{C17 \cdot (\Delta V - 2 \cdot I_1 \cdot R54)}{0.375 \cdot I_1} + \theta$$

$$\text{or } \frac{I_1}{f_0} = \frac{C17 \cdot \Delta V}{0.375} \cdot \frac{1}{1 + f_0\left(\frac{2 \cdot R54 \cdot C17}{0.375} - \theta\right)}$$

  Consequently, the relation between I_1 and f_O will be perfectly linear if

$$R_{54} = \frac{0.375}{2} \cdot \frac{\theta}{C17}$$

  (This compensation technique is also used in the Vertical section, see § II.1)

  In present case, this would lead to R54 = 94Ω. A higher value, 150Ω, was adopted in order to compensate also for the 3% shortfall of the ($f_H \rightarrow I$) converter at high frequencies (see § I.1.1).

- Now we can determine the value of I_1 at 90kHz :

$$I_1 = f_0 \cdot \frac{C17 \cdot \Delta V}{0.375} \cdot \frac{1}{1 + f_0\left(\frac{2 \cdot R54 \cdot C17}{0.375} - \theta\right)}$$

$$= 0.96 \cdot 10^{-3} \cdot \frac{1}{1 + 0.027}$$

$$= 0.935mA$$

  Since V_m was calculated to be 1.945V at that frequency, then

$$R44 = \frac{1.945}{0.935} = 2.08k\Omega$$

  R44 will consist of a fixed resistor of 1.82kΩ in series with a 500Ω variable resistor P7, in order to allow for ±12% adjustment, to cope with the unprecision of the ($f_H \rightarrow I_1 \rightarrow f_0$) converter. This potentiometer will be set so as to obtain 3.5V on Pin 3 of the TDA9102C with 80kHz horizontal sync signal.
  All components influencing the ($f_H \rightarrow I_1 \rightarrow f_0$) converter slope : C21, C29, R41, R44, C17 will be precision ones.

- No-sync free-running frequency
  It is determined by R44 and R45 in series, according to the formula in § V.1 of "AN540 Application Note" ; it must be lower than the lowest frequency in the range : in present case

$$R44 + R45 \geq \frac{1}{3.0476 \cdot 31.4 \cdot 10^{3} \cdot 10^{-9}}$$

$$= 10.45k\Omega$$

  As safety margin, we need 5% for the precision of factor K_0 = 3.0476, 2% for C17, then

$$R44 + R45 > 11.2k\Omega$$

  Taking into account the lowest value of R44 (1.82kΩ)

$$R45 = 9.53k\Omega \pm 1\%$$

I.4.3 - PLL1 Holding and Capture Range

- The value of R24 is chosen so as to provide room for sufficient capture range ; from § I.2, R24 = 20kΩ ensures a holding range of 9.4kHz at high frequencies, larger than the 7kHz capture range.
- Time constant C18 · R23 influences the PLL in two ways :
  It controls the capture range of the loop.
  It ensures the stability of the loop, once locked at the sync frequency (critical for low frequencies).
  Capture range and instability frequency remain roughly proportional. The value chosen for C18 (2.2nF) ensures a capture range 7kHz at 90kHz (few dependant of frequency) and stability at frequencies higher than 25kHz.
- The capture range is influenced by the horizontal phase setting : when shifting the display to the right (that is, when V_{10} is low), capture range will shift towards low frequencies by some 4kHz and reversedly. In order to maintain a fixed capture range, a resistor R56 was connected between Pins 1 and 10; its effect is to shift f_0 (and the capture range which remains centered on it) to higher values when V_{10} goes lower.
  Since center value of V_{10} is 2.5V and voltage on Pin 1 is 3.5V, R57 was connected between Pins 1 and 19 in order that no neat current be injected into Pin 1 in these conditions.
  Refering again to Equation 1, R56 = 43kΩ will provide a frequency shift

$$\Delta f = \frac{0.375}{C17 \cdot \Delta V} \frac{2}{43 \cdot 10^3} = 4.36kHz$$

  for a 2V variation on Pin 10. The 23.3µA sunk by R56 for center setting will be compensated if R57 = 141kΩ.

Global performances of ($f_H \rightarrow V_m \rightarrow f_0$) converter and PLL are depicted in Figure 3. The diagram scale is not sufficient to separate the $f_H \rightarrow V_m$ and $V_m \rightarrow f_0$ characteristics, which differ by less than 1kHz once P7 is adjusted.

II - VERTICAL OSCILLATOR

II.1 - Programming the Vertical Frequency

The law which governs vertical frequency may be found in page 11 of "AN540 Application Note" :

$$f_V = \frac{I_{12}}{\Delta V \cdot C16}$$

where $\Delta V = 6.8 - 2 = 4.8V$ (free-running)
$\Delta V = 6 - 2 = 4V$ (ideal sync running)

There are two main sources of discrepancy between real frequency and ideal law :

- a parasitic internal bias current (about 1.5µA) which adds to current sunk from Pin 12; in order to make its influence negligible, a high value should be chosen for I_{12} (not exceeding 200µA in order to avoid saturation problems at high temperature);
- the response time of comparators used to switch from "charge" to "discharge".

The influence of first factor can be neglected (0.75% frequency offset if I_{12} = 200µA); second factor should be examined in detail.

When voltage on oscillator capacitor C16 reaches the upper threshold, a very fast discharge is triggered. The discharge time to 2V is between 10 and 22µs if C16 = 0.22µF, which corresponds to a discharge current between 48 and 106mA. When the lower threshold (2V) is reached, the comparator will trigger a new charge phase only after 0.5µs, during which the discharge will continue with the same rate. Consequently the apparent lower threshold will be less than 2V by an amount 0.5/10 to 0.5/22 of 4V (variable from circuit to circuit) (see Figure 4).

This cause of imprecision will be miminized if a high value is chosen for C16, because discharge rate will decrease. Inserting a low-value resistor R58 in series with C16 (1.2Ω for 0.39nF; proportional to 1/C16) will compensate most of the unprecision. The explanation may be found in § I.4.2.

On the other hand, the discharge time by itself has but low influence on total period (in the range of 0.1 - 0.2%).

Figure 3

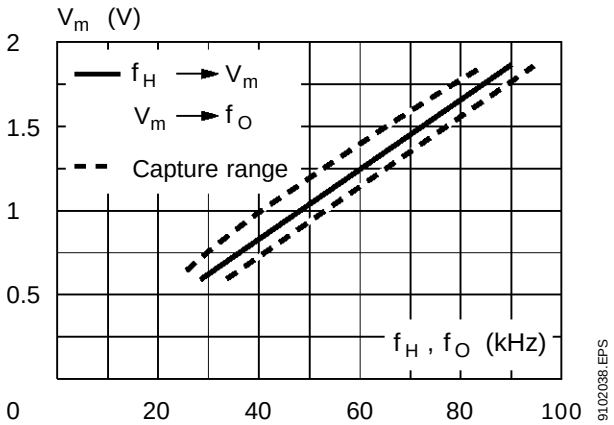
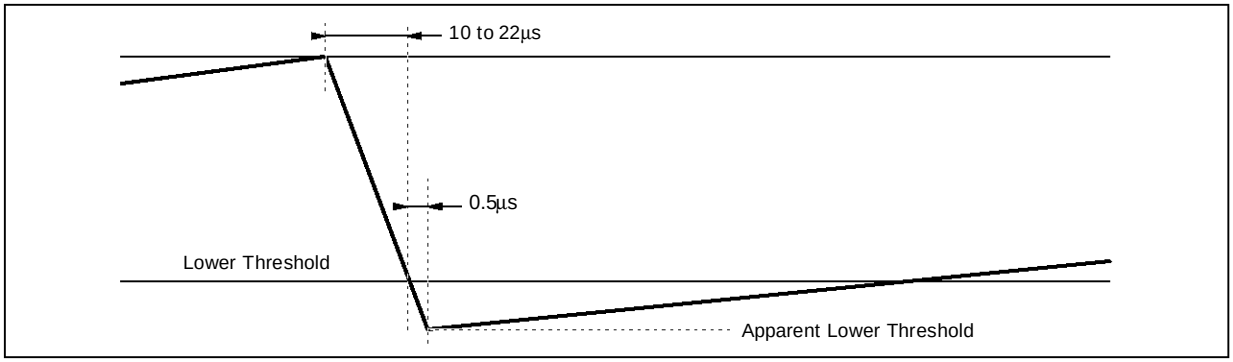


Figure 4



II.2 - Frequency-to-current Converter

As usual, it consists of a monostable triggered by every sync pulse, and a filter which delivers the mean value of the monostable output pulse : the filtered voltage is proportional to sync frequency.

The negative-going vertical sync pulse available at the output of X-OR gate is used to discharge capacitor C22 down to 0.7V; then it will charge again through R30 with time constant C22 · R30. An op-amp compares the capacitor voltage with a fixed voltage from bridge R31 - R32. A constant-width pulse is available on the op-amp output : it is filtered by R35, C25, R36, C26. R35 is chosen high-valued, so that the op-amp can drive it down to almost 0V. A double RC filter was chosen, in order that settling time be low, notwithstanding the high filtering ratio required (imperfect filtering would be visible on the CRT).

II.3 - Frequency Programmation

Transistor T3, combined with an op-amp, is connected in such a way that its emitter voltage keep strictly equal to the filtered voltage, representative of frequency.

This way, the current through R47, which is finally sunk from Pin 12, is proportional to frequency.

R46 is added in order to set the free-running frequency when no sync pulse is present. In that case, T3 does not conduct and current sunk from Pin 12 is fixed by R46 and R47 in series.

II.4 - S - correction

In TDA9102C, the vertical S-correction is obtained by adding to the current sunk from Pin 2 an M-shaped current from Pin 18 (see page 7 of "AN540 Application Note").
Because Pin 12 currents are integrated by C16, the S-correction obtained is proportional to the reverse of vertical frequency.
Since the S-correction amplitude is DC controllable through Pin 17, controlling it with a voltage increasing with frequency will provide constant S-correction versus frequency. Nevertheless, since the amplitude of S-correction is proportional to (V_{17} - 1.5V), the resistor bridge R39 - R40 is introduced, in such a way that V_{17} be equal to 1.5V for null frequency. Once this proportional control established, R20 has to be fitted so as to obtain convenient correction on the screen.

II.5 - Automatic control of oscillator amplitude

The optimal oscillator amplitude is 4V (from 2 to 6V): this corresponds to the center of holding range and provides symetrical S-correction (see page 6 and 16 of "AN540 Application Note"). Since the lower threshold is constant (2V), simply maintaining the mean value of oscillator ramp to 4V will keep the oscillation between 2V and 6V levels .For that purpose, taking advantage of the fact that the mean value of oscillation is transmitted to Pin 15, a resistor bridge R52 - R53 reduces the Pin 15 voltage by a ratio 3.5/4; then the reduced voltage is filtered; this way, if the oscillation amplitude is correct, a DC voltage of 3.5V (equal to Pin 12 voltage) will be found at filter output. An op-amp measures any difference between Pin 12 voltage and filter output voltage, and injects into Pin 12 through R48 a current in such direction to correct the shift.
The capability to adjust amplitude on Pin 15 through DC voltage on Pin 16 is not impaired by this system. In particular, the different amplitudes corresponding to the various VGA modes may be programmed by switching the DC voltage on Pin 16, depending on the sign of sync pulses.
Diodes D4 and D5 are provided to avoid that op-amp inject such high current (thus reducing the oscillation frequency) that the oscillator might synchronize on half the sync frequency. There is no danger in the other direction. D4 is a low-voltage signal Schottky diode.

II.6 - Calculations

II.6.1 - $f_V \rightarrow I_{12}$ converter

- If maximum frequency is 120Hz, 0.39µF is a convenient value for C16 : the corresponding programmation current (free-running) is :
  $I_2 = C16 \cdot \Delta V \cdot 120 = 187.2\mu A$ (less than 200µA).
  This value is preferred to 0.22µF, as explained in § II.1
- Evaluation of the precision of $f_V \rightarrow I$ converter

C22	:	± 5%
R30 R31 R32 R47	:	± 4%
C16	:	± 5%
Total precision about		± 15%

- Programmation resistors
  T3 must not be saturated, even for highest frequency and maximum $f_V \rightarrow I$ converter deviation : ≈ 2.5V on its emitter at 120Hz provides sufficient overhead (Voltage on Pin 12 is 3.5 V).
  Consequently

$$R47 = \frac{2.5}{0.39 \cdot 10^{-6} \cdot 4 \cdot 110} \approx 13.4k\Omega$$

  Choosing 13kΩ, the voltage becomes 2.44V.
  R46 + R47 must be chosen for min frequency without sync to be lower than 40Hz even with min value of C16 and with max voltage 3.8V on Pin 12. Nevertheless, the calculation should take into account the current injected by op-amp into Pin 12 (which will be calculated later to be 36µA). For this calculation, amplitude is 4.8V instead of 4V.

$$\frac{1}{R46 + R47} \leq \frac{0.39 \cdot 10^{-6} \cdot 4.8 \cdot 40}{1.05 \cdot 3.8} + \frac{36 \cdot 10^{-6}}{3.8}$$
$$= 28.24 \cdot 10^{-3}\Omega^{-1}$$

  $R46 + R47 \geq 35.4k\Omega$, $R46 = 22.1k\Omega$
- $f_V \rightarrow I$ converter must provide 2.44V on its output for 120Hz.
  Since the voltage excursion at monostable output is from 0 to (12-1.6) = 10.4V, the pulse duty factor must be $\frac{2.44}{10.4}$ at 120Hz.
  This gives the time at which the voltage on C22 will cross the threshold, according to exponential law :

$$\frac{V}{V_0} = \exp\left(\frac{-t}{R30 \cdot C22}\right) \text{ with } \begin{cases} V_0 = 12 - 0.7 = 11.3V \\ V = 12 \cdot \frac{430}{430 + 220} \\ \quad = 7.94V \\ t = \frac{2.44}{10.4 \cdot 120} \\ \quad = 1.96\ ms \end{cases}$$

$$\frac{t}{R30 \cdot C22} = \text{Log}\frac{V_0}{V}$$

$$R30 = \frac{t}{C22\,\text{Log}\frac{V_0}{V}} = \frac{2.44}{10.4 \cdot 120 \cdot 10^{-7} \cdot \text{Log}\frac{11.3}{7.94}}$$
$$= 55.4k\Omega$$

II.6.2 - Automatic gain control

- Loop gain :
  At a given frequency, corresponding to some value of I_{12}, the variation of mean output voltage is half the variation of output amplitudes, so that

$$\Delta V_{OUT} = \frac{1}{2} V_{OUT\ P-P} \cdot \frac{\Delta I_{12}}{I_{12}}$$

  This is amplified by op-amp and injected in Pin 12 through R48 ; consequently, loop gain is

$$A = \frac{3.5}{4} \frac{1}{2} \frac{V_{OUT\,P-P}}{I_{12}} \frac{G}{R48}$$

  where G is the op-amp gain and gain of 1 is assumed between Pins 13 and 15.
  This gain depends on I_{12} and hence on frequency; G was fixed to $1 + \frac{R49}{R50} \approx 31$ in order to have A = 11 in worst case (120 Hz). This way, the initial offset of $f_V \rightarrow I$ converter will be reduced by factor A in closed loop.
- Limitation when sync is absent :
  When no sync pulse is received, the oscillator reaches 6.8V as peak voltage, which will cause control loop to inject maximum current in Pin 12. Without limitation, the oscillator would stop.
  Current injected in Pin 12 comes through R48, R50 and R51 - D4, the latter being about 2µA. Diode D4 (a signal Schottky) limits the voltage on positive (and also negative) input of op-amp to some 150mV. Diode D5 limits the output voltage to some 400mV above inputs. Hence, a current

$$\frac{0.15}{R50} + \frac{0.15 + 0.4}{R48} + 2\mu A = 36\mu A$$

  will be injected in pin 12 and substract from current sunk by R46, R47.
- Limitation when sync is present :
  At any frequency, the AGC system must be able to recover the possible offset of $f_V \rightarrow I$ converter, (more than 15%), but it must not allow locking on half the sync frequency.
  Since the max current from CAG is constant, 15% at 120Hz means $\frac{15 \times 120}{40}$ = 45% at 40Hz
  Locking to double frequency means, in the worst case, increasing current by 85%.
  At 40Hz, the CAG system must provide not less than 45%, not more than 85% extra current.
  The current injected into Pin 12 : $\frac{V_{D5}}{R48}$ = 27.8µA is 45% of programmation current and fulfills the requirements.

III - SYNC SYSTEM

The board can synchronize on positive- or negative-going fronts on H and V sync inputs. A quite well-known system based on X-OR gates is used in order to deliver the negative transitions necessary for TDA9102C.

In order to maintain TTL compatibility, a TTL X-OR IC is used. Consequently, the R.C. filters which store the mean value of sync signal include 330Ω resistors, able to drive the inputs to LOW. The sync inputs of TDA9102C itself have thresholds of 1.4V, compatible with other logic families.

In addition, wiring R37 and C27 will allow to synchronise on composite TTL sync arriving on Horizontal input, provided Vertical input takes a high state when left free. If this facility is not needed, gate input should be connected to 5V instead of R37, C27.

The logic is normally fed from already present 5V supply; on this board a TO92 - 7805 was included.

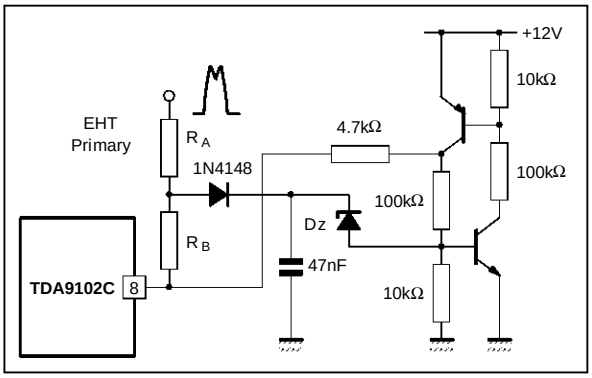
IV - X-RAY PROTECTION

A possible schematic for X-ray protection is given in Figure 5. It uses a thyristor made from two TO92 transistors.

The zener and resistor bridge must be selected in accordance with the desired threshold on EHT transformer winding.

This function is not included on the demoboard.

Figure 5



V - DEMOBOARD

The self adaptative function was implemented on a demoboard, intended to complete the standard TDA9102C demoboard.

It can also be connected to an already existing TDA9102C application in order to make it self-adaptative. It must be kept in mind that this evaluation board, connected with flying wires, is more sensitive to parasitics than the final layout will be.

The complete schematic (modified demoboard of TDA9102C + self adaptative function) is shown in Figure 6 and the printed circuit of self-adaptative function in Figure 7.

Figure 6

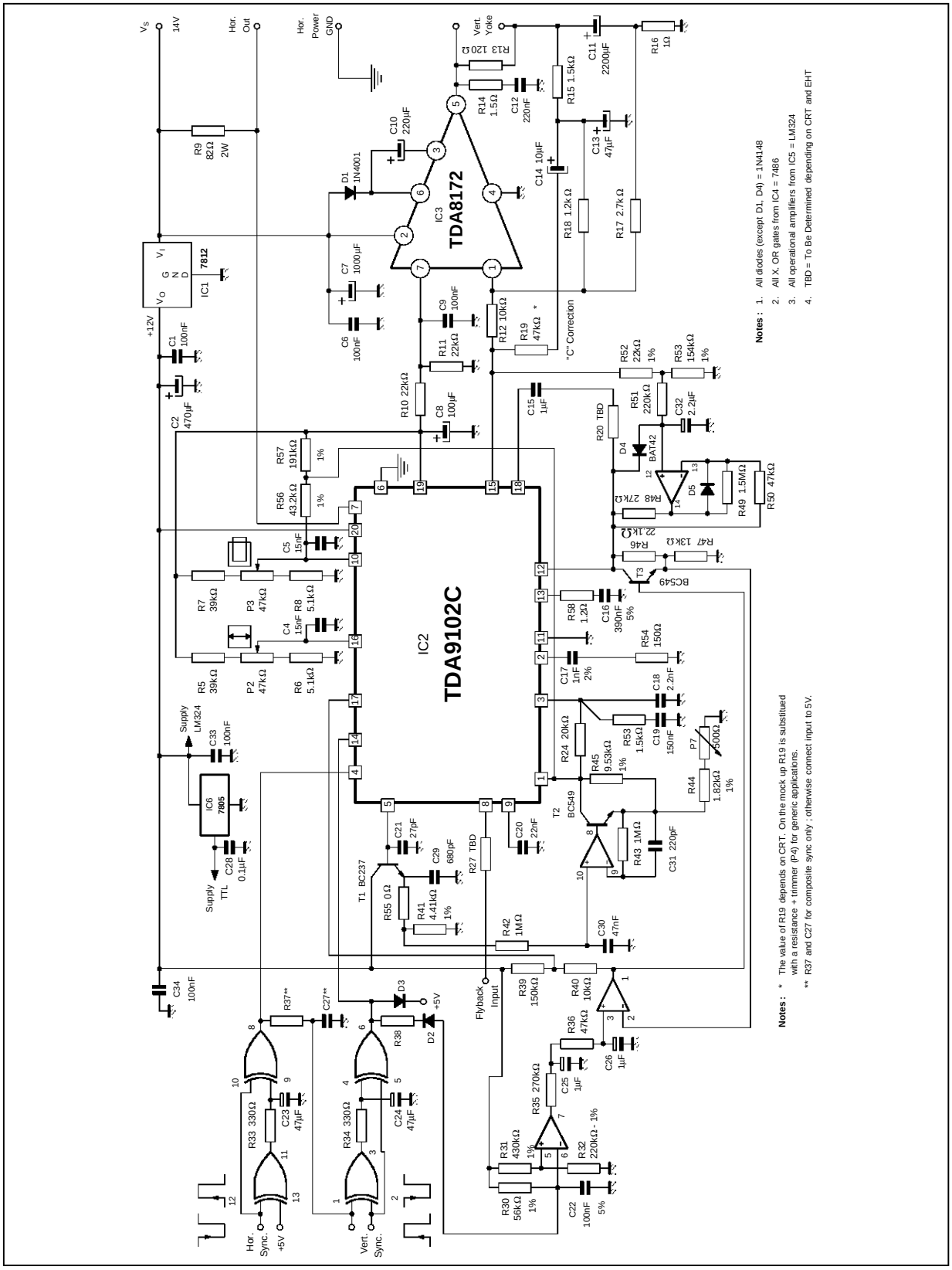

TDA9102C
IC2
TDA8172
IC3
7812
IC1
TBC549
IC6
7805
Vs
14V
Hor. Out
Hor. Power GND
Vert. Yoke
+12V
Supply LM324
Supply TTL
Flyback Input
Hor. Sync.
Vert. Sync.
+5V
"C" Correction
Notes : 1. All diodes (except D1, D4) = 1N4148
2. All X. OR gates from IC4 = 7486
3. All operational amplifiers from IC5 = LM324
4. TBD = To Be Determined depending on CRT and EHT
Notes : * The value of R19 depends on CRT. On the mock up R19 is substitued with a resistance + trimmer (P4) for generic applications.
** R37 and C27 for composite sync only ; otherwise connect input to 5V.
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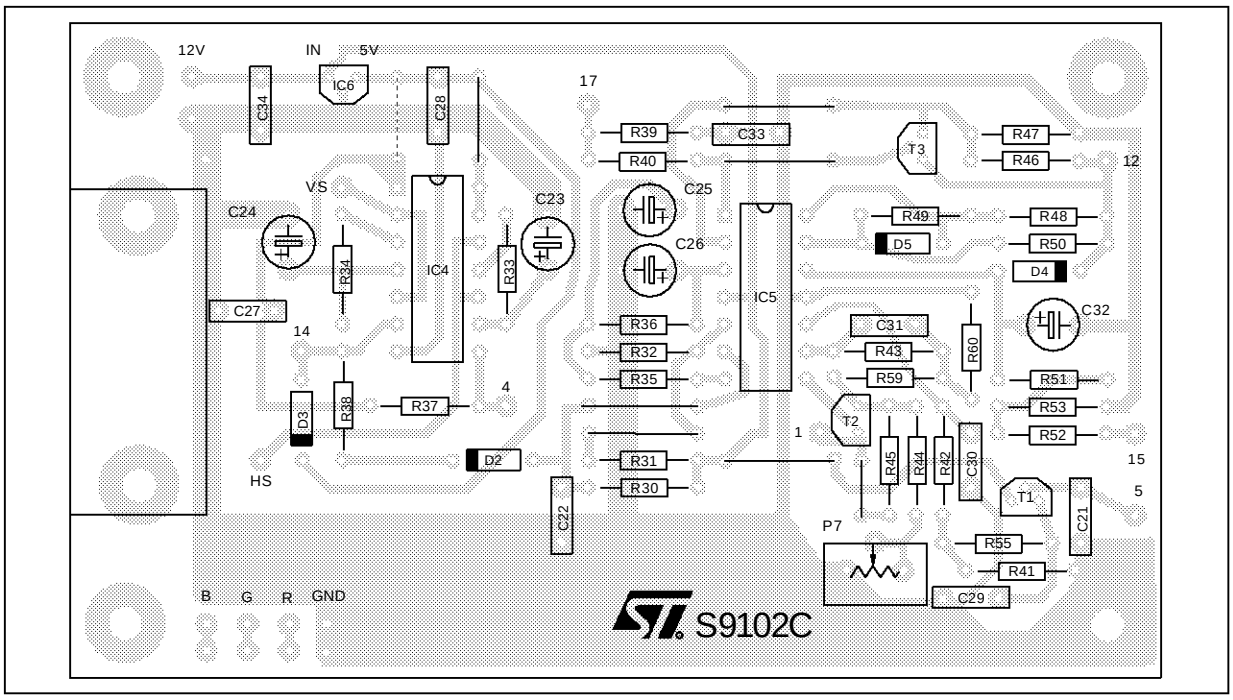
Figure 7



LIST OF COMPONENTS
Resistors

Comp.	Value
R5	39kΩ
R6	5.1kΩ
R7	39kΩ
R8	5.1kΩ
R9	82Ω 2W
R10	22kΩ
R11	22kΩ
R12	10kΩ
R13	120Ω
R14	1.5Ω
R15	1.5kΩ
R16	1Ω
R17	2.7kΩ
R18	1.2kΩ
R19	TBD
R20	TBD
R23	1.5kΩ

Comp.	Value
R24	20kΩ
R27	TBD
R30	56kΩ 1%
R31	430kΩ 1%
R32	220kΩ 1%
R33	330Ω
R34	330Ω
R35	270kΩ
R36	47kΩ
R37	TBD
R38	0Ω
R39	150kΩ
R40	10kΩ
R41	4.41kΩ 1%
R42	1MΩ
R43	1MΩ
R44	1.82kΩ 1%

Comp.	Value
R45	9.53kΩ 1%
R46	22.1kΩ
R47	13kΩ 1%
R48	27kΩ
R49	1.5MΩ
R50	47kΩ
R51	220kΩ
R52	22kΩ 1%
R53	154kΩ 1%
R54	150Ω
R55	0Ω
R56	43.2kΩ 1%
R57	191kΩ 1%
R58	1.2Ω
R59	0Ω
R60	-

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Potentiometers

Comp.	Value
P2, P3	47kΩ

Comp.	Value
P7	500Ω

Comp.	Value

Capacitors

Comp.	Value
C1	100nF
C2	470µF
C4	15nF
C5	15nF
C6	100nF
C7	1000µF
C8	100µF
C9	100nF
C10	220µF
C11	2200µF
C12	220nF

Comp.	Value
C13	47µF
C14	10µF
C15	1µF unpolarized
C16	390nF 5%
C17	1nF 2%
C18	2.2nF
C19	150nF
C20	22nF
C21	27pF 5%
C22	100nF 5%
C23	47µF

Comp.	Value
C24	47µF
C25	1µF
C26	1µF
C27	TBD
C28	100nF
C29	680pF 2%
C30	47nF
C31	220pF
C32	2.2µF
C33	100nF
C34	100nF

Diodes

Comp.	Value
D1	1N4001 (100V 1A)

Comp.	Value
D2,D3,D5	1N4148

Comp.	Value
D4	BAT42 (Signal Schottky)

Transistors

Comp.	Value
T1	BC237

Comp.	Value
T2, T3	BC549C (gain 420..800)

Comp.	Value

Circuits

Comp.	Value
IC1	L7812CV
IC2	TDA9102C

Comp.	Value
IC3	TDA8172
IC4	7486 TTL XOR

Comp.	Value
IC5	7805 (TO92)
IC6	LM324

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