TC1232

Microprocessor Monitor

Features

- Precision Voltage Monitor
  - Adjustable +4.5V or +4.75V
- Reset Pulse Width – 250 msec minimum
- No External Components
- Adjustable Watchdog Timer
  - 150 msec, 600 msec or 1.2 sec
- Debounced Manual Reset Input for External Override

Applications

- Computers
- Controllers
- Intelligent Instruments
- Automotive Systems
- Critical µP Power Monitoring

General Description

The TC1232 is a fully-integrated processor supervisor that provides three important functions to safeguard processor sanity: precision power on/off reset control, watchdog timer and external reset override.

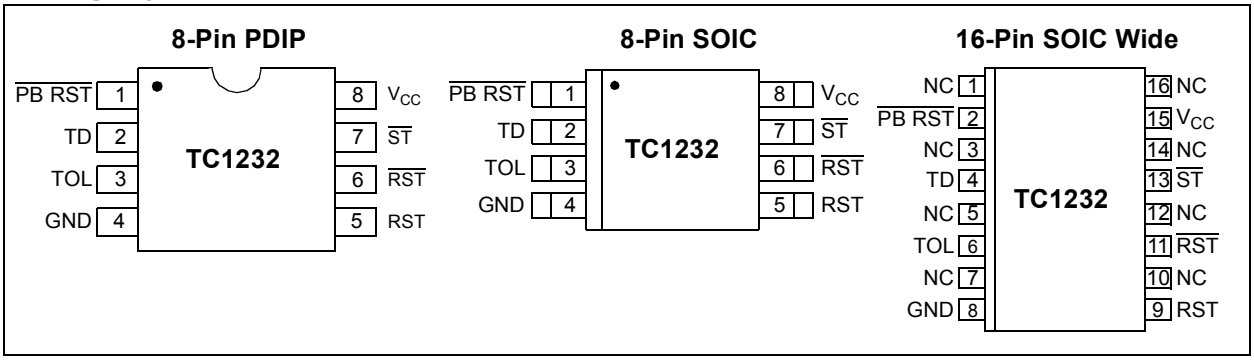
On power-up, the TC1232 holds the processor in the reset state for a minimum of 250 msec after V_{CC} is within tolerance to ensure a stable system start-up.

Microprocessor sanity is monitored by the on-board watchdog circuit. The microprocessor must provide a periodic low-going signal on the $\overline{ST}$ input. Should the processor fail to supply this signal within the selected time-out period (150 msec, 600 msec or 1200 msec), an out-of-control processor is indicated and the TC1232 issues a processor reset as a result.

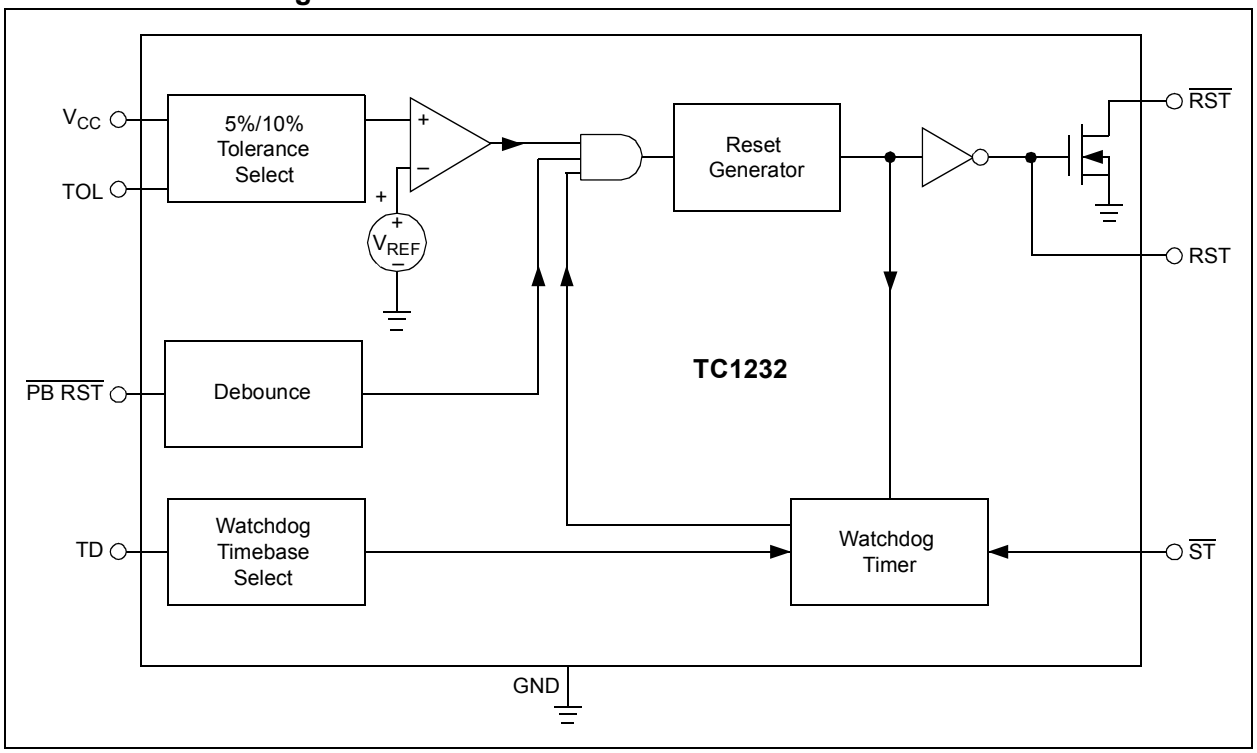
The outputs of the TC1232 are immediately driven active when the PB input is brought low by an external push-button switch or other electronic signal. When connected to a push-button switch, the TC1232 provides contact debounce.

The TC1232 is packaged in a space-saving 8-Pin PDIP or SOIC package and a 16-Pin SOIC (Wide) package and requires no external components.

Package Types



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Voltage on Any Pin (With Respect to GND)
..... -0.3V to +5.8V

Operating Temperature Range

C-Version ..... 0°C to +70°C
E-Version ..... -40°C to +85°C

Storage Temperature Range ..... -65°C to +150°C

† Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, $T_A = T_{MIN}$ to T_{MAX}; V_{CC} = +4.5V to 5.5V.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
$\overline{ST}$ and $\overline{PB\ RST}$ Input High Level	V_{IH}	2.0	—	V_{CC} +0.3	V	**Note 1**
$\overline{ST}$ and $\overline{PB\ RST}$ Input Low Level	V_{IL}	-0.3	—	+0.8	V	
Input Leakage $\overline{ST}$, TOL	I_L	-1.0	—	+1.0	µA	
Output Current RST	I_{OH}	-1.0	-12	—	mA	V_{OH} = 2.4V
Current RST, $\overline{RST}$	I_{OL}	2.0	10	—	mA	V_{OL} = 0.4V
Operating Current	I_{CC}	—	50	200	µA	**Note 2**
V_{CC} 5% Trip Point	V_{CCTP}	4.50	4.62	4.74	V	TOL = GND **(Note 3)**
V_{CC} 10% Trip Point	V_{CCTP}	4.25	4.37	4.49	V	TOL = V_{CC} **(Note 3)**
Capacitance Electrical Characteristics: Unless otherwise noted, T_A = +25°C. **(Note 4)**						
Input Capacitance $\overline{ST}$, TOL	C_{IN}	—	—	5	pF	
Output Capacitance RST, $\overline{RST}$	C_{OUT}	—	—	7	pF	
AC Electrical Characteristics: Unless otherwise noted, $T_A = T_{MIN}$ to T_{MAX}; V_{CC} = +5V to ±10%.						
$\overline{PB\ RST}$	t_{PB}	20	—	—	msec	**Figure 3-3 (Note 5)**
$\overline{PB\ RST}$ Delay	t_{PBD}	1	4	20	msec	**Figure 3-3**
Reset Active Time	t_{RST}	250	610	1000	msec	
$\overline{ST}$ Pulse Width	t_{ST}	20	—	—	nsec	**Figure 3-4**
$\overline{ST}$ Time-out Period	t_{TD}	62.5	150	250	msec	TD Pin = 0V, **Figure 3-4**
		250	600	1000	msec	TD Pin = Open, **Figure 3-4**
		500	1200	2000	msec	TD Pin = V_{CC}, **Figure 3-4**
V_{CC} Fall Time	t_F	10	—	—	µsec	**Figure 3-5**, **(Note 4)**
V_{CC} Rise Time	t_R	0	—	—	µsec	**Figure 3-6**, **(Note 4)**
V_{CC} Detect to RST High and $\overline{RST}$ Low	t_{RPD}	—	—	100	nsec	**Figure 3-7**, V_{CC} Falling
V_{CC} Detect to RST High and $\overline{RST}$ Open	t_{RPU}	250	610	1000	msec	**Figure 3-8**, V_{CC} Rising, **(Note 6)**

Note 1: $\overline{PB\ RST}$ is internally pulled up to Vcc with an internal impedance of typically 40 kΩ.
2: Measured with outputs open.
3: All voltages referenced to GND.
4: Ensured by design.
5: $\overline{PB\ RST}$ must be held low for a minimum of 20 msec to ensure a reset.
6: t_R = 5 µsec.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin No. (8-pin PDIP, SOIC)	Pin No. (16-pin SOIC)	Symbol	Function
1	2	$\overline{\text{PB RST}}$	Push-button Reset Input. A debounced active-low input that ignores pulses less than 1 msec in duration and is ensured to recognize inputs of 20 msec or greater.
2	4	TD	Time Delay Set. The watchdog time-out select input (t_{TD} = 150 msec for TD = 0V, t_{TD} = 600 msec for TD = open, t_{TD} = 1.2 sec for TD = V_{CC}).
3	6	TOL	Tolerance Input. Connect to GND for 5% tolerance or to V_{CC} for 10% tolerance.
4	8	GND	Ground.
5	9	RST	Reset Output (Active-High) – goes active: 1. If V_{CC} falls below the selected reset voltage threshold. 2. If $\overline{\text{PB RST}}$ is forced low. 3. If $\overline{\text{ST}}$ is not strobed within the minimum time-out period. 4. During power-up
6	$\overline{11}$	$\overline{\text{RST}}$	Reset output (active-low, open-drain) – see RST.
7	$\overline{13}$	$\overline{\text{ST}}$	Strobe input. Input for watchdog timer.
8	15	V_{CC}	The +5V power-supply input.
—	1,3,5,7,10,12,16	NC	No internal connection.

3.0 DETAILED DESCRIPTION

3.1 Power Monitor

The TC1232 provides the function of warning the processor of a power failure. When V_{CC} is detected as being below the voltage levels defined by the TOL pin, the TC1232's comparator outputs the RST and $\overline{RST}$ signals to a logic level that warns the system of an out-of-tolerance power supply. The RST and $\overline{RST}$ signals switch at a threshold value of 4.5V if TOL is tied to V_{CC} and at a value of 4.75 volts if TOL is grounded. The RST and $\overline{RST}$ signals are held active for a minimum of 250 msec to ensure that the power supply voltage has been stabilized.

3.2 Push-Button Reset Input

The debounced manual reset input ($\overline{PB\ RST}$) manually forces the reset outputs into their active states. Once $\overline{PB\ RST}$ has been low for a time t_{PBD} (the push-button delay time) the reset outputs go active. The reset outputs remain in their active states for a minimum of 250 msec after $\overline{PB\ RST}$ rises above V_{IH} (Figure 3-3).

A mechanical push-button or active logic signal can drive the $\overline{PB\ RST}$ input. The debounced input ignores input pulses less than 1 msec and ecognizes pulses of 20 msec or greater. No external pull-up resistor is required because the $\overline{PB\ RST}$ input has an internal pull-up to V_{CC} of approximately 100 µA.

3.3 Watchdog Timer

When the $\overline{ST}$ input is not stimulated for a preset time period, the watchdog timer function forces RST and $\overline{RST}$ signals to the active state. The preset time period is determined by the $\overline{TD}$ inputs to be 150 msec with TD connected to ground, 600 msec with TD floating, or 1200 msec with TD connected to V_{CC} (typical). The watchdog timer starts timing-out from the set time period as soon as RST and $\overline{RST}$ are inactive. If a high-to-low transition occurs on the ST input pin prior to time-out, the watchdog timer is reset and begins to time-out again. If the watchdog timer is allowed to time-out, then the RST and $\overline{RST}$ signals are driven to the active state for 250 msec minimum (Figure 3-2).

The software routine that strobes $\overline{ST}$ is critical. The code must be in a section of software that is executed frequently enough so the time between toggles is less than the watchdog time-out period. One common technique controls the µP I/O line from two sections of the program. The software might set the I/O line high while operating in the foreground mode and set it low while in the background or interrupt mode. If both modes do not execute correctly, the watchdog timer issues reset pulses.

3.4 Supply Monitor Noise Sensitivity

The TC1232 is optimized for fast response to negative-going changes in V_{DD}. Systems with an inordinate amount of electrical noise on V_{DD} (such as systems using relays) may require a 0.01 µF or 0.1 µF bypass capacitor to reduce detection sensitivity. This capacitor should be installed as close to the TC1232 as possible to keep the capacitor lead length short.

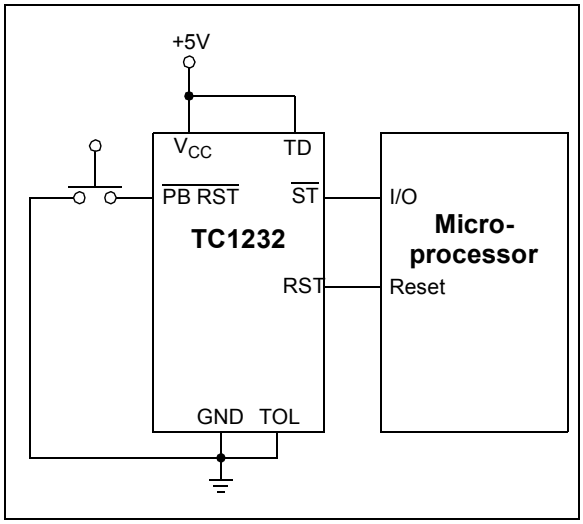


FIGURE 3-1: *Push-Button Reset.*

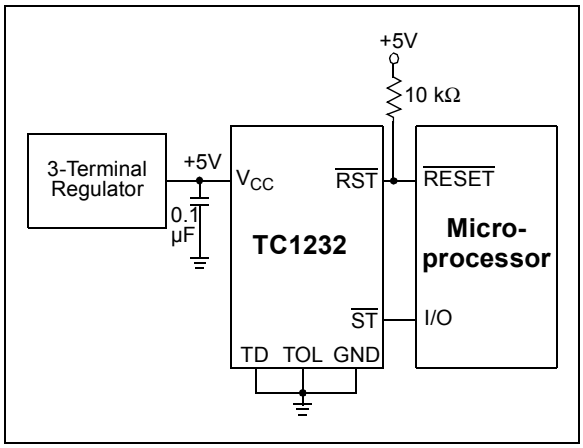
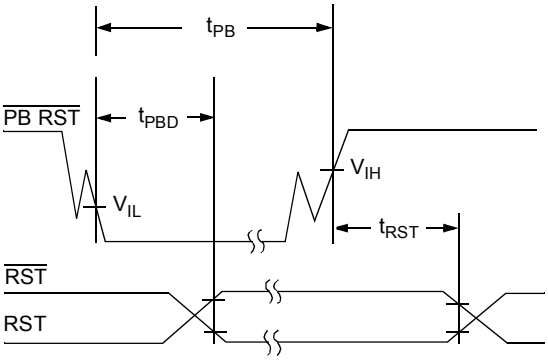
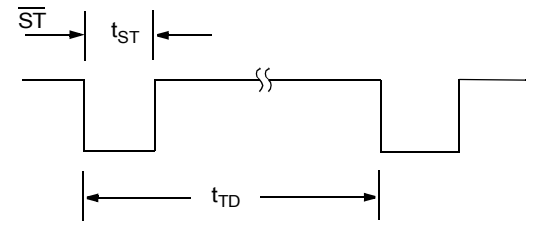


FIGURE 3-2: *Watchdog Timer.*



The debounced $\overline{PB\ RST}$ input ignores input pulses less than 1 msec and is designed to recognize pulses of 20 msec or greater.

FIGURE 3-3: *Push-Button Reset – $\overline{PB\ RST}$ Input.*



Note: t_{TD} is the maximum elapsed time between $\overline{ST}$ high-to-low transitions ($\overline{ST}$ is activated by falling edges only) which will keep the watchdog timer from forcing the reset outputs active for a time of t_{RST}. I_{TD} is a function of the voltage at the TD pin, as tabulated below:

Condition	Min	I_{TD} Typ	Max
TD pin = 0V	62.5 ms	150 ms	250 ms
TD pin = Open	250 ms	600 ms	1000 ms
TD pin = V_{CC}	500 ms	1200 ms	2000 ms

FIGURE 3-4: *Strobe Input.*

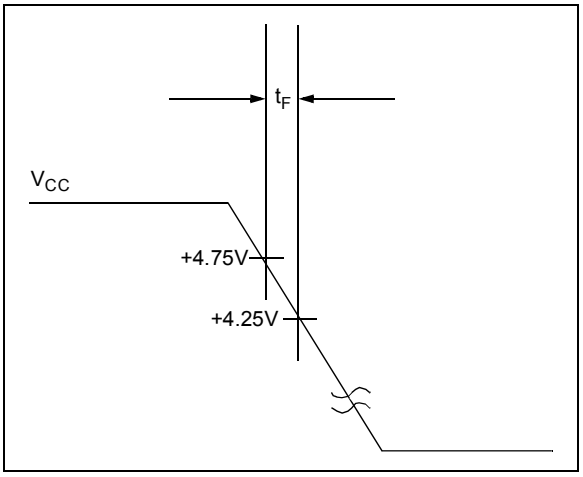


FIGURE 3-5: *Power-Down Slew Rate.*

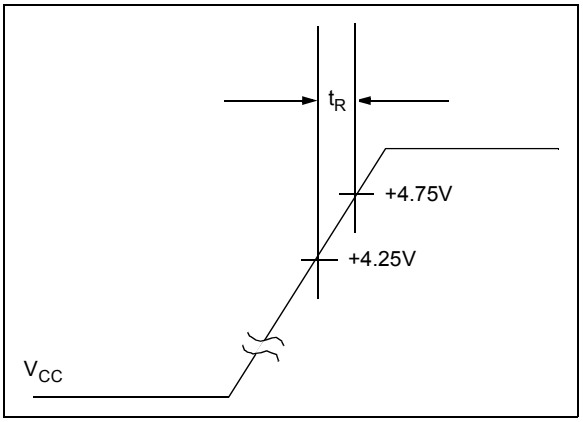


FIGURE 3-6: *Power-up Slew Rate.*

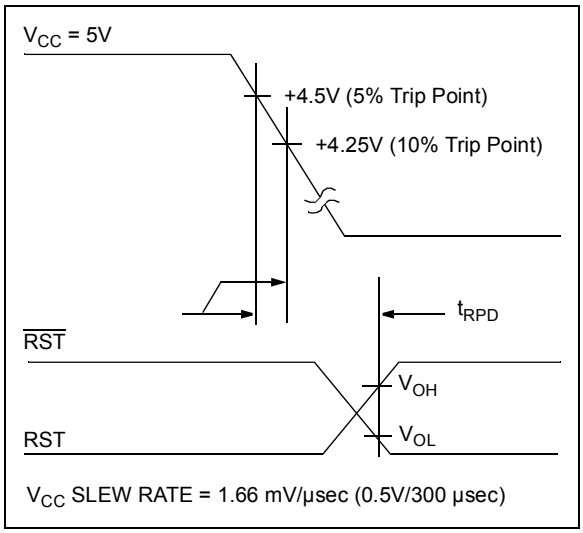


FIGURE 3-7: *V_{cc} Detect Reset Output Delay (Power-Down).*

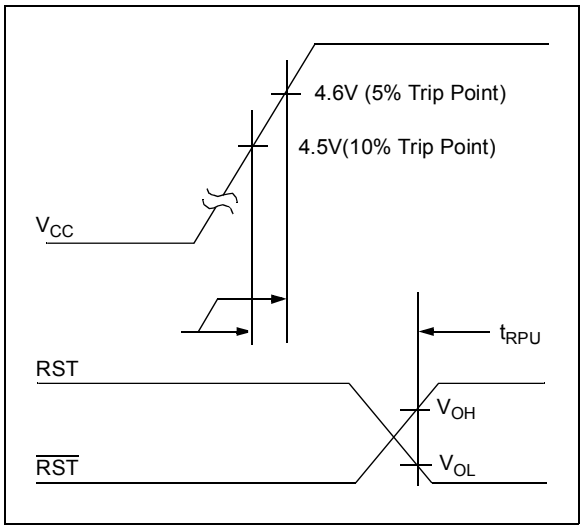
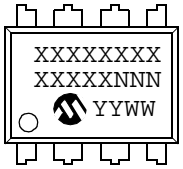


FIGURE 3-8: *V_{cc} Detect Reset Output Delay (Power-Up).*

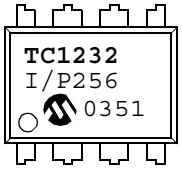
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

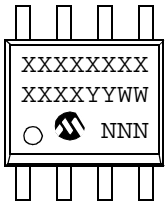
8-Lead PDIP (300 mil)



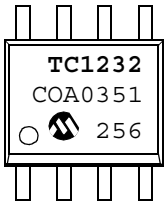
Example:



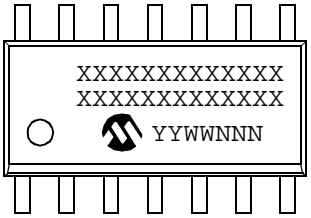
8-Lead SOIC (150 mil)



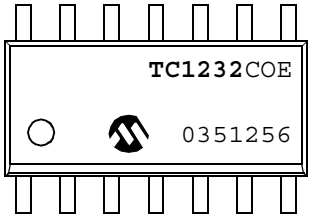
Example:



16-Lead SOIC (150 mil)



Example:

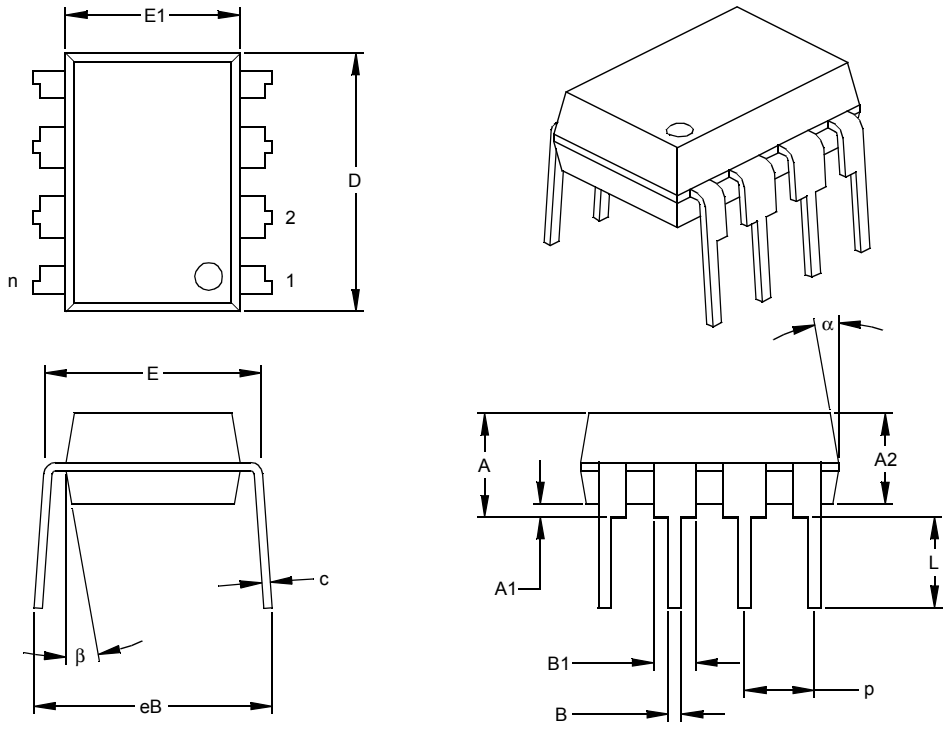


Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

***** Standard OTP marking consists of Microchip part number, year code, week code, and traceability code.

8-Lead Plastic Dual In-line (PA) – 300 mil (PDIP)

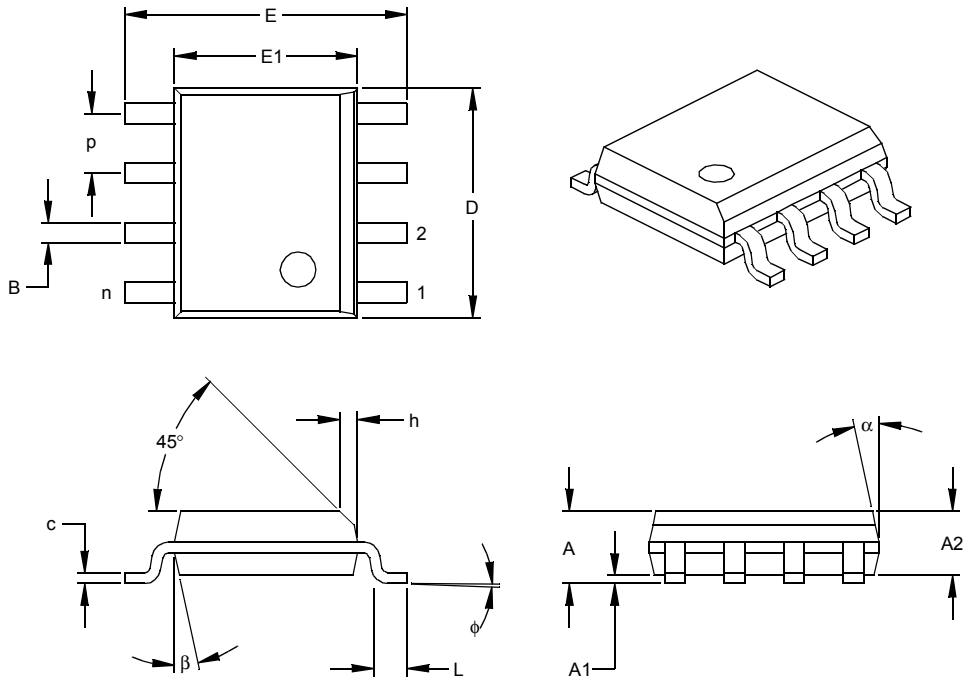


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (OA) – Narrow, 150 mil (SOIC)

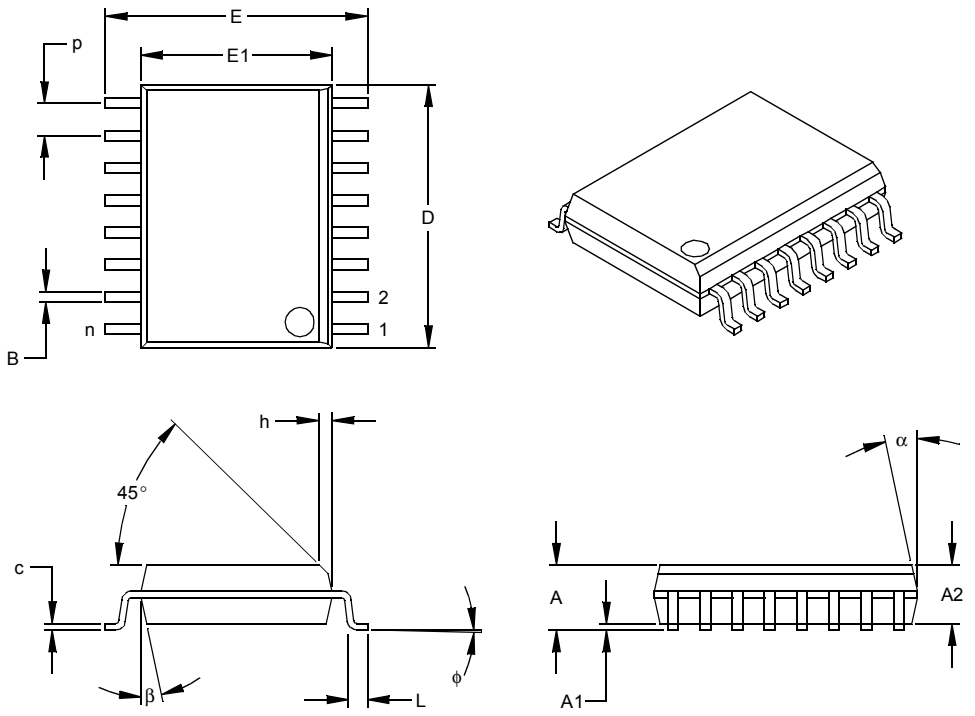


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

16-Lead Plastic Small Outline (OE) – Wide, 300 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		16			16	
Pitch	p		.050			1.27	
Overall Height	A	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.398	.406	.413	10.10	10.30	10.49
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.009	.011	.013	0.23	0.28	0.33
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-013
Drawing No. C04-102

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	TC1232:	Microprocessor Monitor
Temperature Range:	C =	0°C to +70°C
	E =	-40°C to +85°C
Package:	PA =	Plastic DIP (300 mil Body), 8-lead
	OA =	Plastic SOIC, (150 mil Body), 8-lead
	OA713 =	Plastic SOIC, (150 mil Body), 8-lead Tape and Reel
	OE =	Plastic SOIC (300 mil Body), 16-lead
	OE713 =	Plastic SOIC (300 mil Body), 16-lead Tape and Reel

Examples:

a) TC1232COA: 0°C to +70°C, 8L-SOIC
b) TC1232COA713: 0°C to +70°C, 8L-SOIC, Tape and Reel
c) TC1232COE: 0°C to +70°C, 16L-SOIC
d) TC1232COE713: 0°C to +70°C, 16L-SOIC, Tape and Reel
e) TC1232CPA: 0°C to +70°C, 8L-PDIP
f) TC1232EOA: -40°C to +85°C, 8L-SOIC
g) TC1232EOA713: -40°C to +85°C, 8L-SOIC, Tape and Reel
h) TC1232EOE: -40°C to +85°C, 16L-SOIC
i) TC1232EOE713: -40°C to +85°C, 16L-SOIC, Tape and Reel
j) TC1232EPA: -40°C to +85°C, 8L-PDIP

Sales and Support

Data Sheets
Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

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NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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03/25/03