MC34280

Power Supply & Management IC for Handheld Electronic Products

The MC34280 is a power supply integrated circuit which provides two boost regulated outputs and some power management supervisory functions. Both regulators apply Pulse–Frequency–Modulation (PFM). The main step–up regulator output can be externally adjusted from 2.7V to 5V. An internal synchronous rectifier is used to ensure high efficiency (achieve 87%). The auxiliary regulator with a built–in power transistor can be configured to produce a wide range of positive voltage (can be used for LCD contrast voltage). This voltage can be adjusted from +5V to +25V by an external potentiometer; or by a microprocessor, digitally through a 6–bit internal DAC.

The MC34280 has been designed for battery powered hand–held products. With the low start–up voltage from 1V and the low quiescent current (typical 35 μA); the MC34280 is best suited to operate from 1 to 2 AA/ AAA cell. Moreover, supervisory functions such as low battery detection, CPU power–on reset, and back–up battery control, are also included in the chip. It makes the MC34280 the best one–chip power management solution for applications such as electronic organizers and PDAs.

FEATURES:

- Low Input Voltage, 1V up
- Low Quiescent Current in Standby Mode: 35μA typical
- PFM and Synchronous Rectification to ensure high efficiency (87% @200mA Load)
- Adjustable Main Output: nominal 3.3V @ 200mA max, with 1.8V input
- Auxiliary Output Voltage can be digitally controlled by microprocessor
- Auxiliary Output Voltage:
  +5V @ 25mA max, with 1.8V input
  +25V @ 15mA max, with 1.8V input
- Current Limit Protection
- Power–ON Reset Signal with Programmable Delay
- Battery Low Detection
- Lithium Battery Back–up
- 32–Pin LQFP Package

APPLICATIONS:

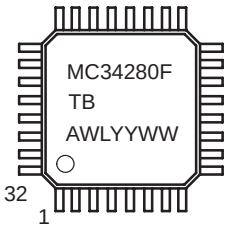
- Digital Organizer and Dictionary
- Personal Digital Assistance (PDA)
- Dual Output Power Supply (For MPU, Logic, Memory, LCD)
- Handheld Battery Powered Device (1–2 AA/AAA cell)

ON Semiconductor

http://onsemi.com

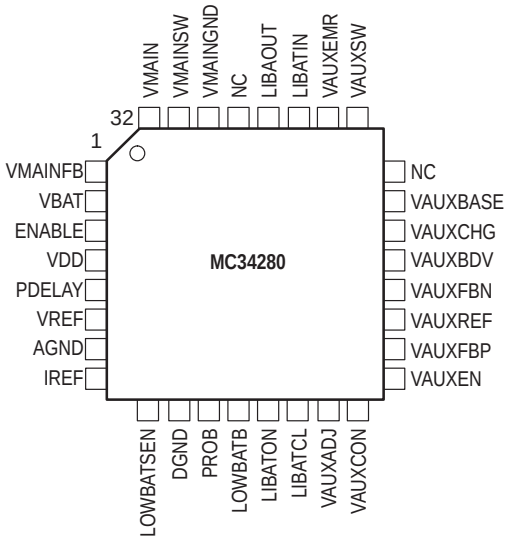
32–LEAD LQFP
FTB SUFFIX
CASE 873A

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

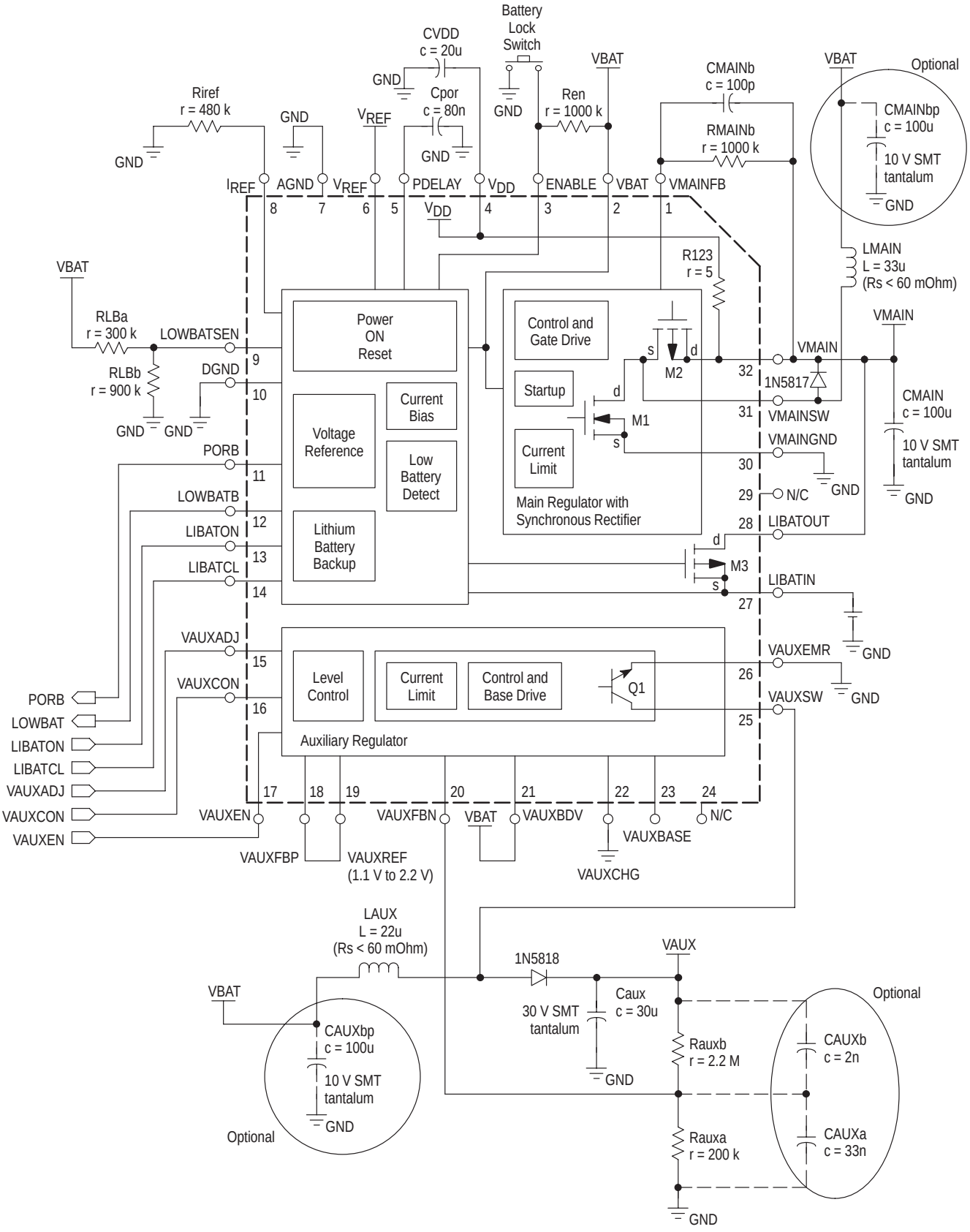
PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping
MC34280FTB	LQFP	250 Units/Tray
MC34280FTBR2	LQFP	1800 Tape & Reel

Figure 1. Typical Application Block Diagram



TIMING DIAGRAMS

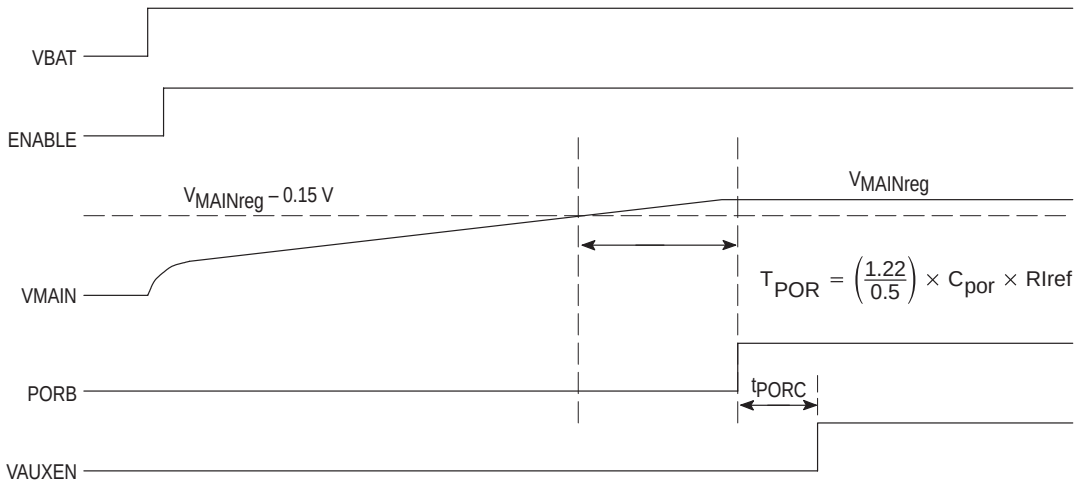


Figure 2. Startup Timing

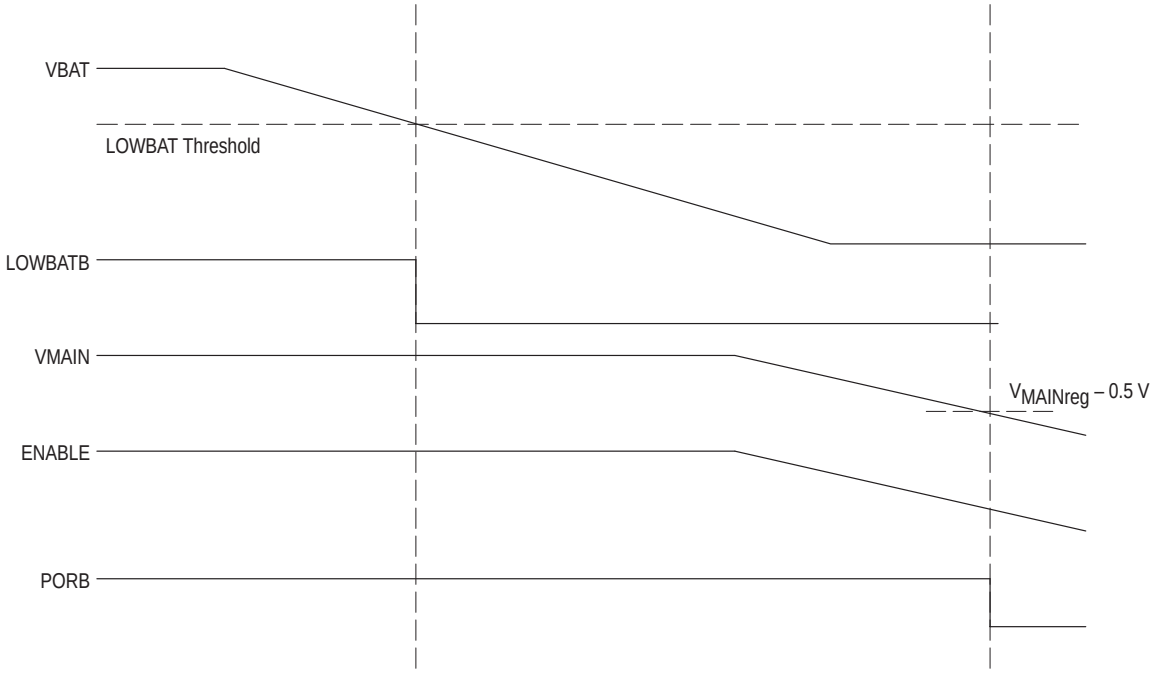


Figure 3. Power Down Timing

TIMING DIAGRAMS (Con't)

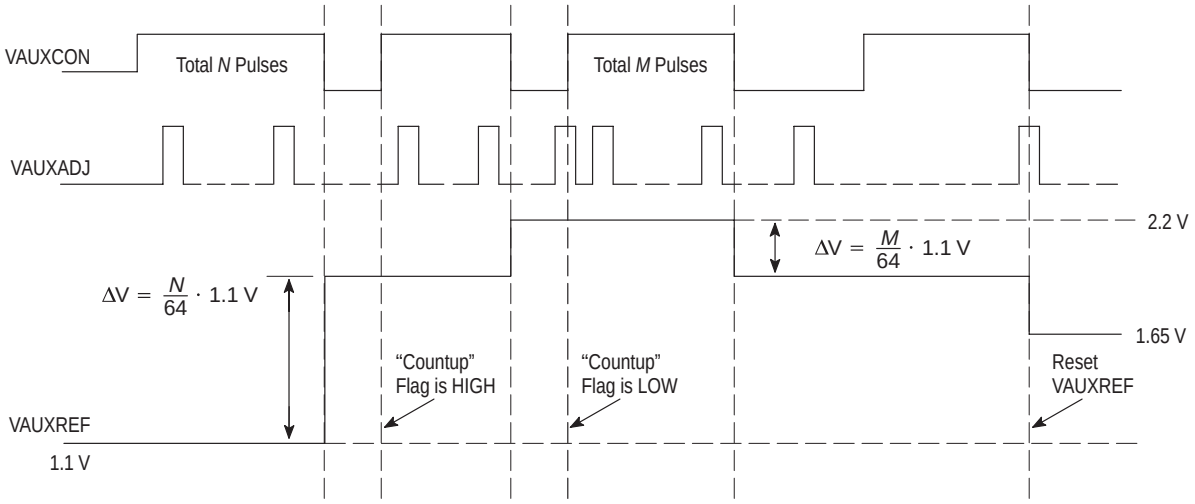


Figure 4. Auxiliary Regulator Voltage Control

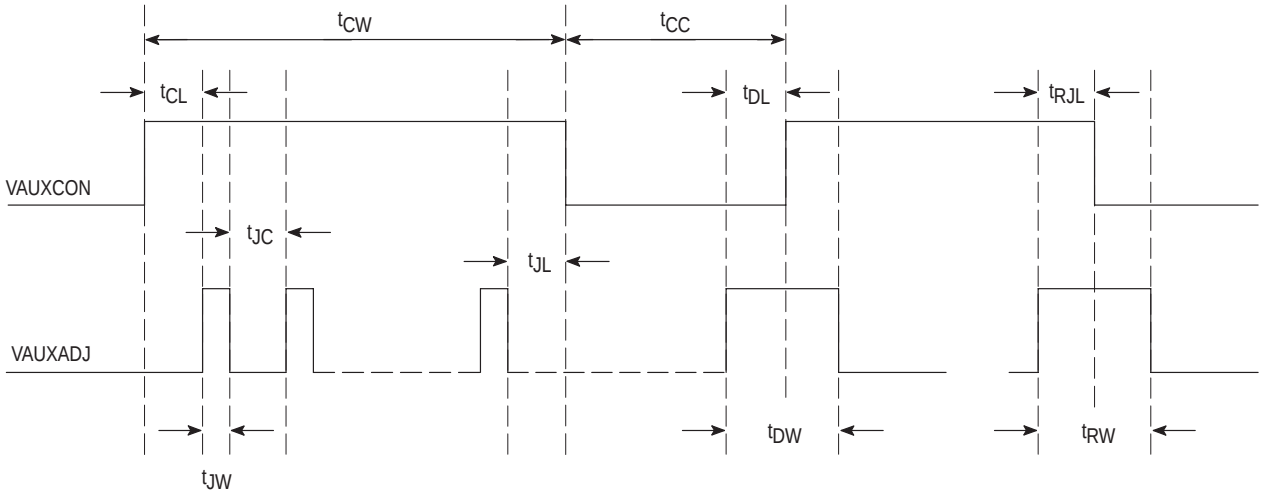


Figure 5. Auxiliary Regulator Voltage Control Timing

PIN FUNCTION DESCRIPTION

Pin No.	Function	Type/Direction	Description
1	VMAINFB	Analog / Input	Feedback pin for VMAIN
2	VBAT	Power	Main battery supply
3	ENABLE	CMOS / Input	Chip enable, Active high, ENABLE activates VMAIN after battery plug in, ENABLE is inactive after VMAIN is on
4	VDD	Analog / Output	Connect to decoupling capacitor for internal logic supply
5	PDELAY	Analog / Input	Capacitor connection for defining Power–On signal delay
6	VREF	Analog / Output	Bandgap Reference output voltage. Nominal voltage is 1.25V
7	AGND	Analog Ground	
8	IREF	Analog / Input	Resistor connection for defining internal current bias and PDELAY current
9	LOWBATSEN	Analog / Input	Resistive network connection for defining low battery detect threshold
10	DGND	Digital Ground	
11	PORB	CMOS / Output	Active LOW Power–On reset signal
12	LOWBATB	CMOS / Output	Active LOW low battery detect output
13	LIBATON	CMOS / Input	microprocessor control signal for Lithium battery backup switch, the switch is ON when LIBATON=HIGH and LIBATCL=HIGH
14	LIBATCL	CMOS / Input	microprocessor control signal for Lithium battery backup switch, if it is HIGH, the switch is controlled by LIBATON, otherwise, controlled by internal logic
15	VAUXADJ	CMOS / Input	microprocessor control signal for VAUX voltage control
16	VAUXCON	CMOS / Input	microprocessor control signal for VAUX voltage control
17	VAUXEN	CMOS / Input	VAUX enable, Active high
18	VAUXFBP	Analog / Input	Feedback pin for VAUX
19	VAUXREF	Analog / Output	Reference Voltage for VAUX voltage level
20	VAUXFBN	Analog / Input	Feedback pin for VAUX
21	VAUXBDV	Power	VAUX BJT base drive circuit power supply
22	VAUXCHG	Analog / Output	test pin
23	VAUXBASE	Analog / Output	test pin
24	NC		no connection
25	VAUXSW	Analog / Output	Collector output of the VAUX power BJT
26	VAUXEMR	Analog / Output	Emitter output of the VAUX power BJT
27	LIBATIN	Analog / Input	Lithium battery input for backup purposes
28	LIBATOUT	Analog / Output	Lithium battery output
29	NC		no connection
30	VMAINGND	Power Ground	Ground for VMAIN low side switch
31	VMAINSW	Analog / Input	VMAIN inductor connection
32	VMAIN	Analog / Output	VMAIN output

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage Digital Pin Voltage General Analog Pin Voltage Pin VAUXSW to Pin VAUXEMR Voltage (Continuous)	V_{BAT} $V_{digital}$ V_{analog} V_{AUXCE}	–0.3 –0.3 –0.3 –0.3	7.0 7.0 7.0 30	Vdc Vdc Vdc Vdc
Pin VMAINSW to Pin VMAIN Voltage (Continuous)	V_{syn}		0.3	Vdc
Operating Junction Temperature	$T_{j\ (max)}$		150	°C
Ambient Operating Temperature	T_a	0	70	°C
Storage Temperature	T_{stg}	–50	150	°C

STATIC ELECTRICAL CHARACTERISTICS (Circuit of Figure 1, VP = 1.8V, I_{load} = 0 mA, T_A = 0 to 70°C unless otherwise noted.)

Rating	Symbol	Min	Typ	Max	Unit
Operating Supply Voltage[1]	V_{BAT}	1.0			V
VMAIN output voltage	V_{main}	3.13	3.3	3.47	V
VMAIN output voltage range[2]	V_{main_range}	2.7		5.0	V
VMAIN output current[3]	$I_{3.3\_1.8}$			200	mA
VMAIN maximum switching frequency[4]	$Freq_{max\_VM}$			100	kHz
VMAIN peak coil static current limit	I_{LIM_VM}	0.85	1.0	1.15	A
VAUX output voltage range	VAUX_range	5.0		25	V
VAUXREF lower level voltage	$VAUX_{REF\_L}$	1.0	1.1	1.2	V
VAUXREF upper level voltage	$VAUX_{REF\_H}$	2.0	2.2	2.4	V
VAUXREF step size	$VAUX_{REF\_S}$		17		mV
VAUX maximum switching frequency	$Freq_{max\_VL}$			120	kHz
VAUX peak coil static current limit	I_{LIM_VL}		1.0		A
Quiescent Supply Current at Standby Mode[5]	$Iq_{standby}$		35	60	μA
Reference Voltage @ no load	$Vref_{no\_load}$	1.16	1.22	1.28	V
Battery Low Detect lower hysteresis threshold[6]	V_{LOBAT_L}	0.8	0.85	0.9	V
Battery Low Detect upper hysteresis threshold	V_{LOBAT_H}	1.05	1.1	1.15	V
PDELAY Pin output charging current	$Ichg_{PDELAY}$	0.8	1.0	1.2	μA
PDELAY Pin voltage threshold	Vth_{PDELAY}	1.16	1.22	1.28	V

NOTE: 1. Output current capability is reduced with supply voltage due to decreased energy transfer. The supply voltage must not be higher than VMAIN+0.6V to ensure boost operation. Max Start–up loading is typically 1V at 400 μA, 1.8V at 4.4 mA, and 2.2V at 88 mA.
NOTE: 2. Output voltage can be adjusted by external resistor to the VMAINFB pin.
NOTE: 3. At VBAT = 1.8V, output current capability increases with VBAT.
NOTE: 4. Only when current limit is not reached.
NOTE: 5. This is average current consumed by the IC from VDD, which is low–pass filtered from VMAIN, when only VMAIN is enabled and at no loading.
NOTE: 6. This is the minimum of ”LOWBATB” threshold for battery voltage, the threshold can be increased by external resistor divider from ”VBAT” to ”LOWBATSEN”.

DYNAMIC ELECTRICAL CHARACTERISTICS (Refer to TIMING DIAGRAMS, T_A = 0 to 70°C unless otherwise noted.)

Rating	Symbol	Min	Typ	Max	Unit
Minimum PORB to Control delay	t_{PORC}			500	nS
Minimum VAUXCON pulse HIGH width	t_{CW}			5.0	µS
Minimum VAUXCON pulse LOW width	t_{CC}			8.0	µS
Minimum VAUXADJ to VAUXCON delay	t_{CL}			1.0	µS
Minimum VAUXADJ pulse HIGH width	t_{JW}			1.0	µS
Minimum VAUXADJ pulse LOW width	t_{JC}			1.0	µS
Minimum VAUXCON LOW to VAUXADJ pulse delay[1]	t_{JL}			1.0	µS
Minimum hold time of VAUXADJ for Reset VAUXREF	t_{RJL}			500	nS
Minimum VAUXADJ pulse HIGH width for Reset VAUXREF	t_{RW}			1.0	µS
Minimum hold time of VAUXADJ for Decrement VAUXREF	t_{DL}			500	nS
Minimum VAUXADJ pulse HIGH width for Decrement VAUXREF	t_{DW}			1.0	µS

NOTE: 1. For not resetting VAUXREF.

TYPICAL ELECTRICAL CHARACTERISTICS

Figure 6. Efficiency of VMAIN versus Output Current (VMAIN = 3.3 V, L = 33 uH, Various V_{IN})

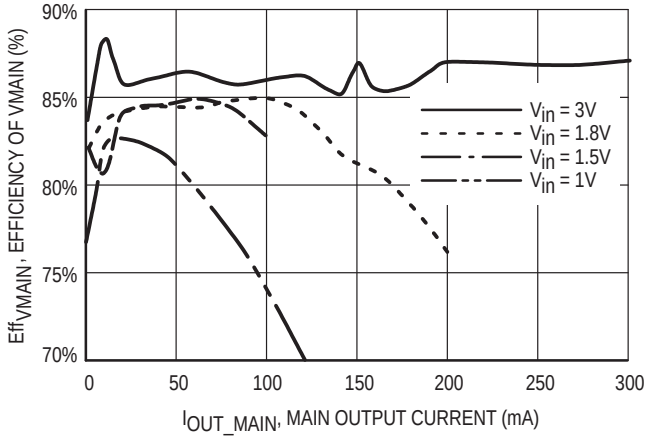


Figure 7. Efficiency of VMAIN versus Input Voltage (VMAIN = 3.3 V, L1 = 33 uH, Various I_{OUT})

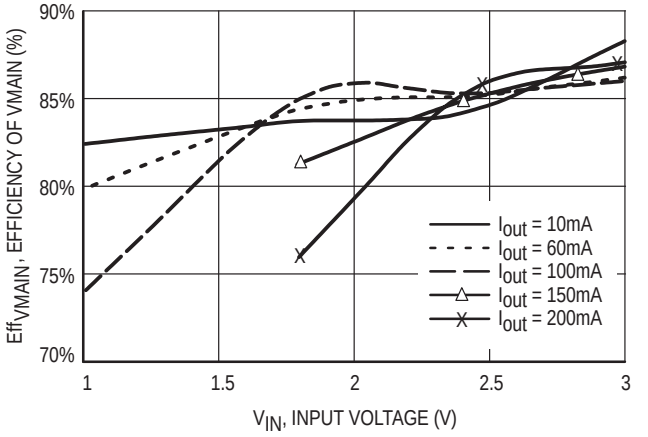


Figure 8. Efficiency of VAUX versus Output Current (VAUX = 25 V, L2 = 33 uH, Various V_{IN})

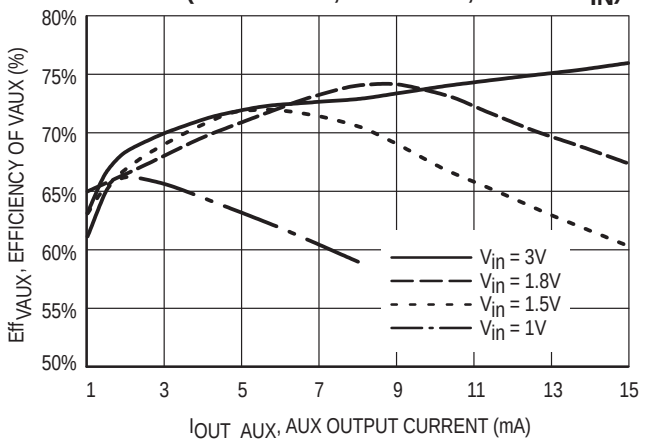
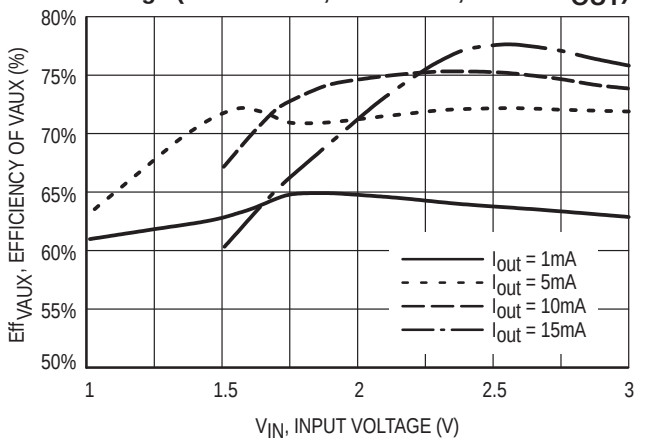


Figure 9. Efficiency of VAUX versus Input Voltage (VAUX = 25 V, L2 = 33 uH, Various I_{OUT})



TYPICAL ELECTRICAL CHARACTERISTICS (Cont'd)

Figure 10. Efficiency of VAUX versus Output Current (VAUX = 20 V, L2 = 33 uH, Various V_{IN})

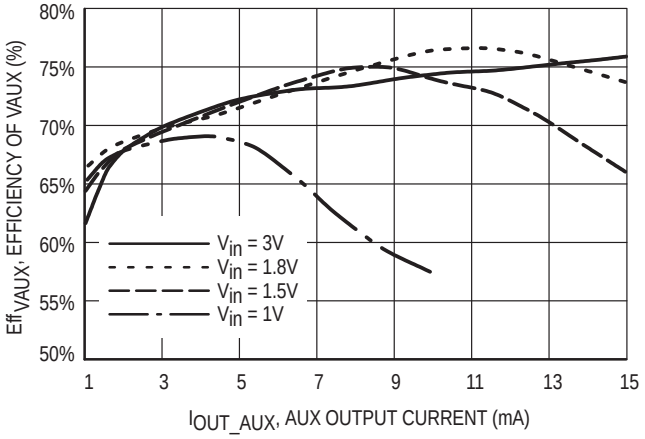


Figure 11. Efficiency of VAUX versus Input Voltage (VAUX = 20 V, L2 = 33 uH, Various I_{OUT})

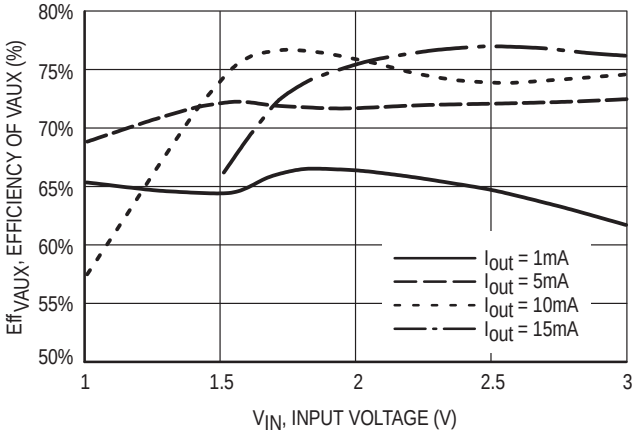


Figure 12. Efficiency of VAUX versus Output Current (VAUX = 5 V, L2 = 82 uH, Various V_{IN})

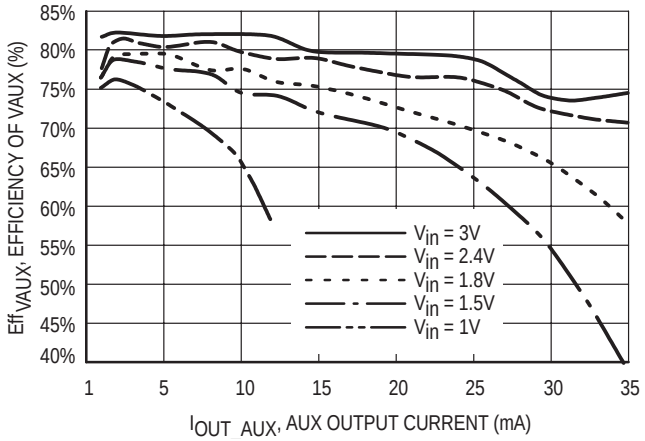


Figure 13. Efficiency of VAUX versus Input Voltage (VAUX = 5 V, L2 = 82 uH, Various I_{OUT})

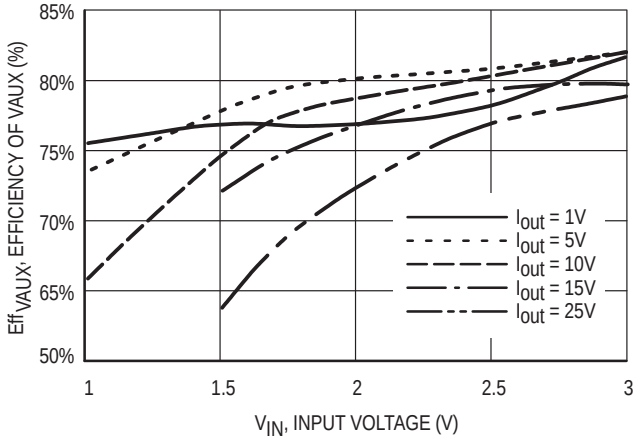
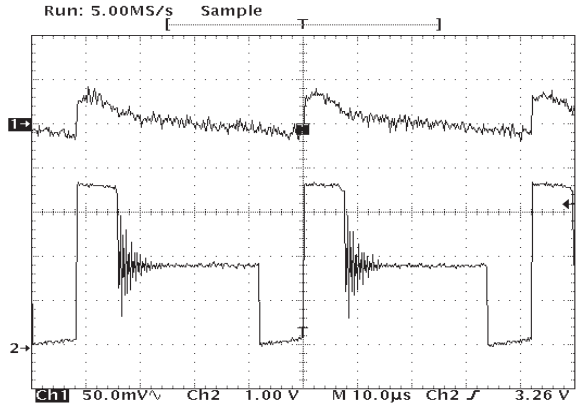


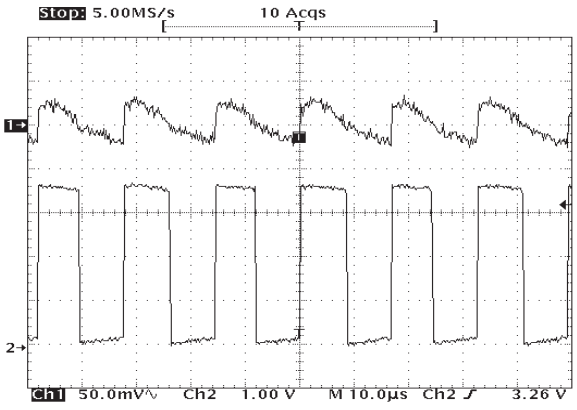
Figure 14. VMAIN Output Ripple (Medium Load)



20 uS / div

1: VMAIN = 3.3 V (50 mV/div, AC COUPLED)
2: Voltage at VMAINSW (1 V/div)

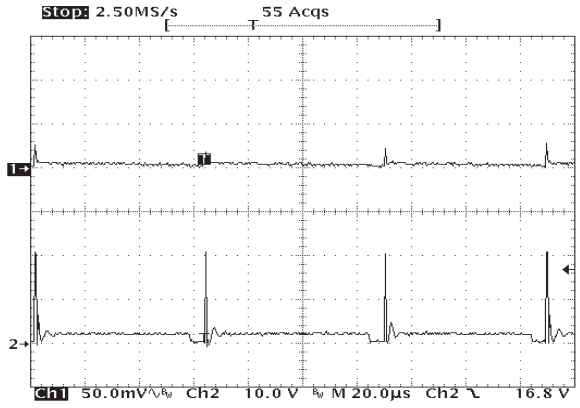
Figure 15. VMAIN Output Ripple (Heavy Load)



10 uS / div

1: VMAIN = 3.3 V (50 mV/div, AC COUPLED)
2: Voltage at VMAINSW (1 V/div)

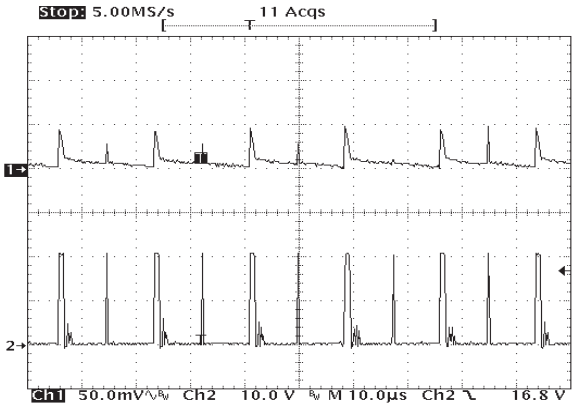
Figure 16. VAUX Output Ripple (Medium Load)



20 uS / div

1: VAUX = 20 V (50 mV/div, AC COUPLED)
2: Voltage at VAUXSW (10 V/div)

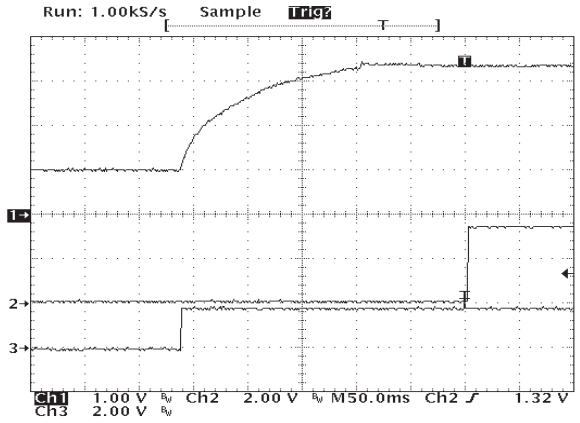
Figure 17. VAUX Output Ripple (Heavy Load)



10 uS / div

1: VAUX = 20 V (50 mV/div, AC COUPLED)
2: Voltage at VAUXSW (10 V/div)

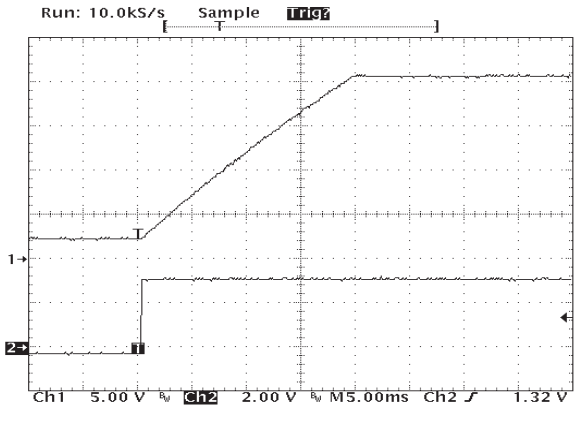
Figure 18. VMAIN Startup and Power–On Reset



50 mS / div

1: VMAIN from 1 V to 3.3 V (1 V/div)
2: Voltage of PORB (2 V/div)
3: Voltage of ENABLE (2 V/div)

Figure 19. VAUX Startup



5 mS / div

1: VAUX from 1.8 V to 20 V (5 V/div)
2: VAUXEN (2 V/div)

DETAILED OPERATING DESCRIPTION

General

The MC34280 is a power supply integrated circuit which provides two boost regulated outputs and some power management supervisory functions. Both regulators apply Pulse–Frequency–Modulation (PFM). The main boost regulator output can be externally adjusted from 2.7V to 5V. An internal synchronous rectifier is used to ensure high efficiency (achieve 87%). The auxiliary regulator with a built–in power transistor can be configured to produce a wide range of positive voltage (can be used to supply a LCD contrast voltage). This voltage can be adjusted from +5V to +25V by an external potentiometer; or by a microprocessor, digitally through a 6–bit internal DAC.

The MC34280 has been designed for battery powered hand–held products. With the low start–up voltage from 1V and the low quiescent current (typical 35 μA); the MC34280 is best suited to operate from 1 to 2 AA/ AAA cell. Moreover, supervisory functions such as low battery detection, CPU power–on reset, and back–up battery control, are also included in the chip. It makes the MC34280 the best one–chip power management solution for applications such as electronic organizers and PDAs.

Pulse Frequency Modulation (PFM)

Both regulators apply PFM. With this switching scheme, every cycle is started as the feedback voltage is lower than the internal reference. This is normally performed by internal comparator. As cycle starts, Low–Side switch (i.e. M1 in Figure 1) is turned ON for a fixed ON time duration (namely, T_{on}) unless current limit comparator senses coil current reaches its preset limit. In the latter case, M1 is OFF instantly. So T_{on} is defined as the maximum ON time of M1. When M1 is ON, coil current ramps up so energy is being stored inside the coil. At the moment just after M1 is OFF, the Synchronous Rectifier (i.e. M2 in Figure 1) or any rectification device (such as Schottky Diode of Auxiliary Regulator) is turned ON to direct coil current to charge up the output bulk capacitor. Provided that coil current is not reached, every switching cycle delivers fixed amount of energy to the bulk capacitor. So for higher loading, larger amount of energy (Charge) is withdrawn from the bulk capacitor, and as output voltage is needed to regulated, larger amount of Charge is needed to be supplied to the bulk capacitor, that means switching frequency is needed to be increased; and vice–versa.

Main Regulator

Figure 20 shows the simplified block diagram of Main Regulator. Notice that precise bias current *Iref* is generated by a VI converter and external resistor *RIref,* where

$$Iref = \frac{0.5}{RIref} \quad (A)$$

This bias current is used for all internal current bias as well as setting *VMAIN* value. For the latter application, *Iref* is doubled and fed as current sink at Pin 1. With external resistor *RMAINb* tied from Pin1 to Pin32, a constant level shift is generated in between the two pins. In close–loop operation, voltage at Pin 1 (i.e. Output feedback voltage) is needed to be regulated at the internal reference voltage level, 1.22V. Therefore, the delta voltage across Pin 1 and Pin 32 which can be adjusted by *RMAINb* determines the Main Output voltage. If the feedback voltage drops below 1.22V, internal comparator sets switching cycle to start. So, *VMAIN* can be calculated as follows.

$$VMAIN = 1.22 + \frac{RMAINb}{RIref} \quad (V)$$

From the above equation, although *VMAIN* can be adjusted by *RMAINb* and *RIref* ratio, for setting *VMAIN*, it is suggested, by changing *RMAINb* value with *RIref* kept at 480K. Since changing *RIref* will alter internal bias current which will affect timing functions of Max ON time (T_{ON1}) and Min OFF time (T_{OFF1}). Their relationships are as follows;

$$T_{ON1} = 1.7 \times 10^{-11} \times RIref \quad (S)$$

$$T_{OFF1} = 6.4 \times 10^{-12} \times RIref \quad (S)$$

Continuous Conduction Mode and Discontinuous Conduction Mode

In Figure 21, regulator is operating at Continuous Conduction Mode. A switching cycle is started as the output feedback voltage drops below internal voltage reference VREF. At that instant, the coil current does not drop to zero yet, and it starts to ramp up for the next cycle. As the coil current ramps up, loading makes the output voltage to decrease as the energy supply path to the output bulk capacitor is disconnected. And after T_{on} elapsed, M1 is OFF, M2 becomes ON, energy is dumped to the bulk capacitor. Output voltage is increased as excessive charge is pumped in, then it is decreased after the coil current drops below the loading. Notice the abrupt spike of output voltage is due to ESR of the bulk capacitor. Feedback voltage can be resistor–divided down or level–shift down from the output voltage. As this feedback voltage drops below VREF, next switching cycle starts.

DETAILED OPERATING DESCRIPTION (Cont'd)

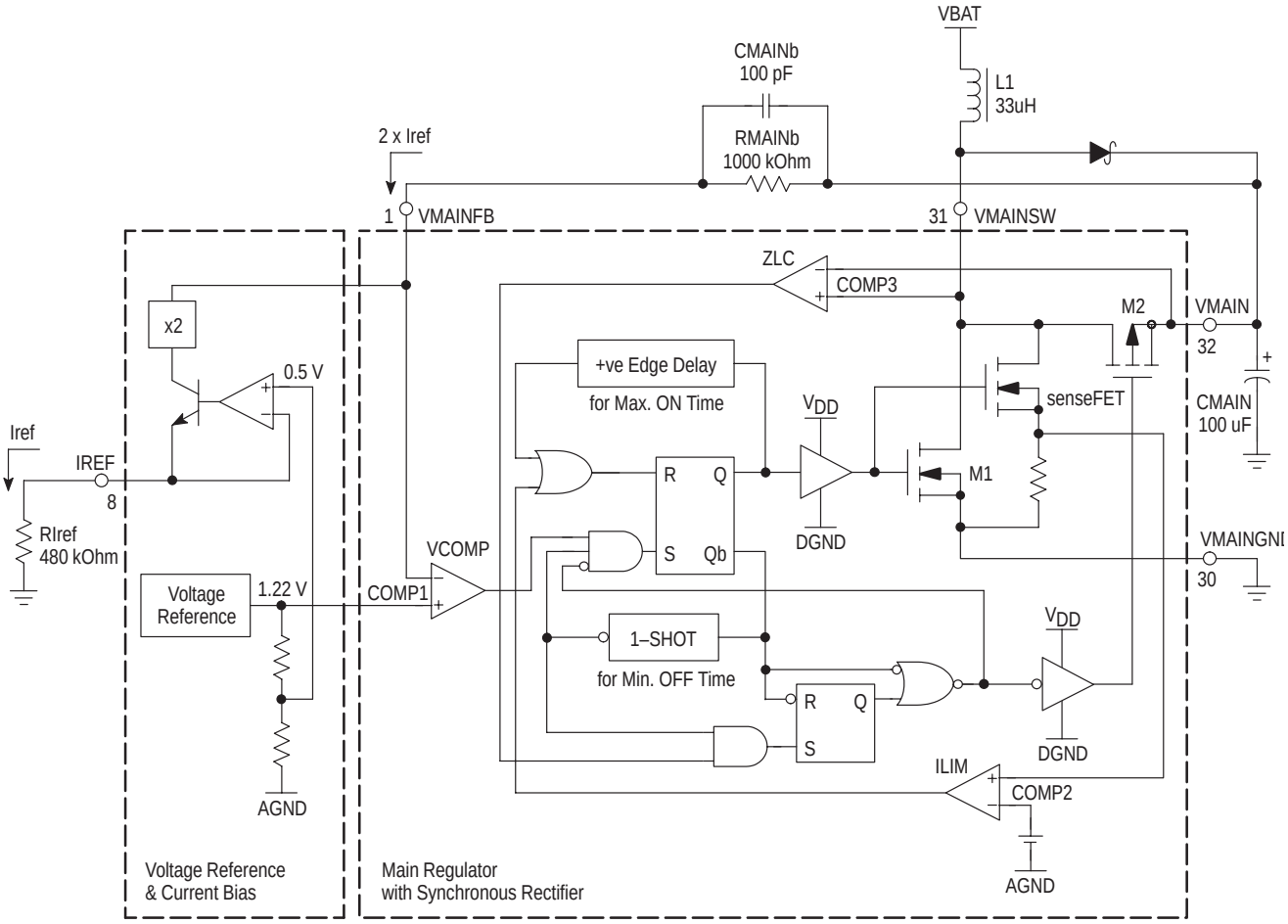


Figure 20. Simplified Block Diagram of Main Regulator

In Figure 22, regulator is operating at Discontinuous Conduction Mode, waveforms are similar to those of Figure 21. However, coil current drops to zero before next switching cycle starts.

To estimate conduction mode, below equation can be used.

$$Iroom = \frac{\eta \times T_{ON} \times Vin^2}{2 \times L \times Vout} - I_{LOAD}$$

where, η is efficiency, refer to Figure 6

if $I_{room} > 0$, the regulator is at Discontinuous Conduction mode

if $I_{room} = 0$, the regulator is at Critical Conduction mode where coil current just drops to zero and next cycle starts.

if $I_{room} < 0$, the regulator is at Continuous Conduction mode

For Continuous Conduction mode, provided that current limit is not reached,

$$T_{SW} = \frac{T_{ON}}{1 - \eta \left(\frac{Vin}{Vout}\right)} \quad (S);$$

$$I_{pk} = \frac{I_{LOAD}}{1 - \left(\frac{T_{ON}}{T_{SW}}\right)} + \frac{Vin \times T_{ON}}{2 \times L} \quad (A)$$

For Discontinuous Conduction mode, provided that current limit is not reached,

$$T_{SW} = \frac{Vin \cdot T_{ON}^2}{2 \cdot L \cdot I_{LOAD} \cdot \left(\frac{Vout}{\eta \cdot Vin} - 1\right)} \quad (S);$$

$$I_{pk} = \frac{Vin}{L} \cdot T_{ON} \quad (A)$$

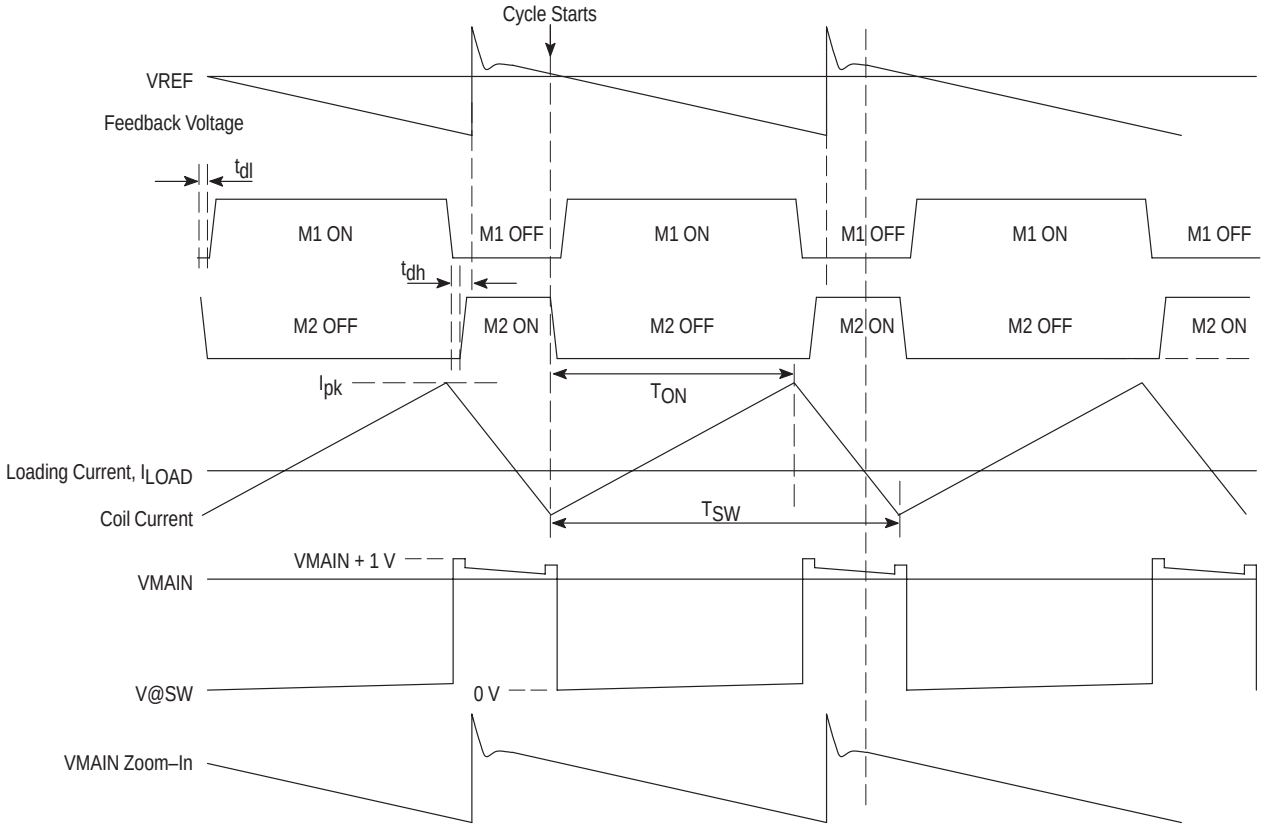


Figure 21. Waveforms of Continuous Conduction Mode

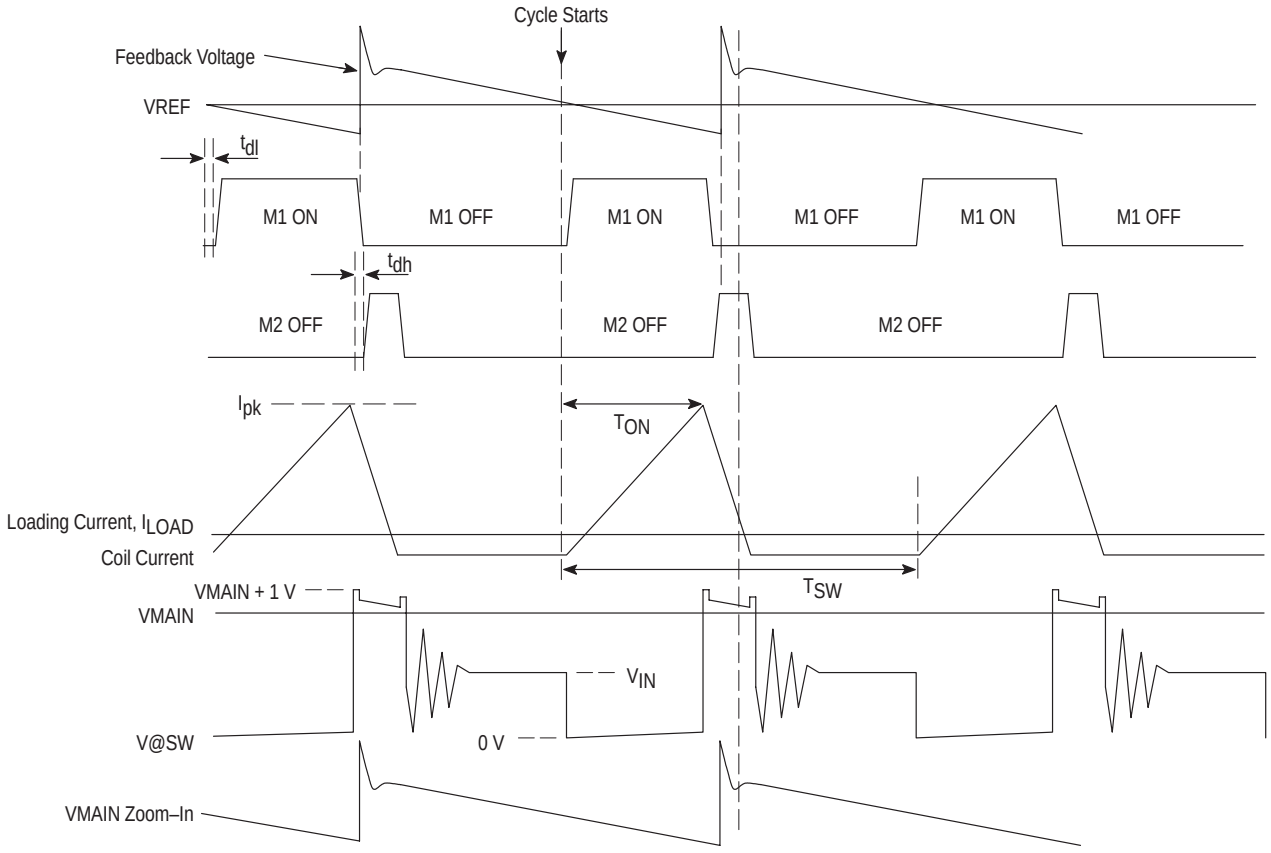


Figure 22. Waveforms of Discontinuous Conduction Mode

DETAILED OPERATING DESCRIPTION (Cont'd)

Synchronous Rectification

A Synchronous Rectifier is used in the main regulator to enhance efficiency. Synchronous rectifier is normally realized by powerFET with gate control circuitry which, however, involved relative complicated timing concerns. In Figure 20, as main switch M1 is being turned OFF, if the synchronous switch M2 is just turned ON with M1 not being completed turned OFF, current will be shunt from the output bulk capacitor through M2 and M1 to ground. This power loss lowers overall efficiency. So a certain amount of dead time is introduced to make sure M1 is completely OFF before M2 is being turned ON, this timing is indicated as t_{dh} in Figure 21.

When the main regulator is operating in continuous mode, as M2 is being turned OFF, and M1 is just turned ON with M2 not being completed OFF, the above mentioned situation will occur. So dead time is introduced to make sure M2 is completed OFF before M1 is being turned ON, this is indicated as t_{dl} in Figure 21.

When the main regulator is operating in discontinuous mode, as coil current is dropped to zero, M2 is supposed to be OFF. Fail to do so, reverse current will flow from the output bulk capacitor through M2 and then the inductor to the battery input. It causes damage to the battery. So M2–voltage–drop sensing comparator (COMP3 of Figure 20) comes with fixed offset voltage to switch M2 OFF before any reverse current builds up. However, if M2 is switch OFF too early, large residue coil current flows through the body diode of M2 and increases conduction loss. Therefore, determination on the offset voltage is essential for optimum performance.

Auxiliary Regulator

The Auxiliary Regulator is a boost regulator, applies PFM scheme to enhance high efficiency and reduce quiescent current. An internal voltage comparator (COMP1 of Figure 23) detects when the voltage of Pin VAUXFBN drops below that of Pin VAUXFBP. The internal power BJT is then switched ON for a fixed–ON–time (or until the internal current limit is reached), and coil current is allowed to build up. As the BJT is switched OFF, coil current will flow through the external Schottky diode to charge up the bulk capacitor. After a fixed–mimimum–OFF time elapses, next switching cycle will start if the output of the voltage comparator is HIGH. Refer to Figure 23, the VAUX regulation level is determined by the equation as follows,

$$V_{AUX} = VAUXFBP \cdot \left(1 + \frac{R_{AUXb}}{R_{AUXa}}\right) \quad (V)$$

Where Max ON Time, TON2, and Min OFF Time, TOFF2 can be determined by the following equations.

$$T_{ON2} = 1.7 \times 10^{-11} \times RIref \quad (S)$$

$$T_{OFF2} = 2.1 \times 10^{-12} \times RIref \quad (S)$$

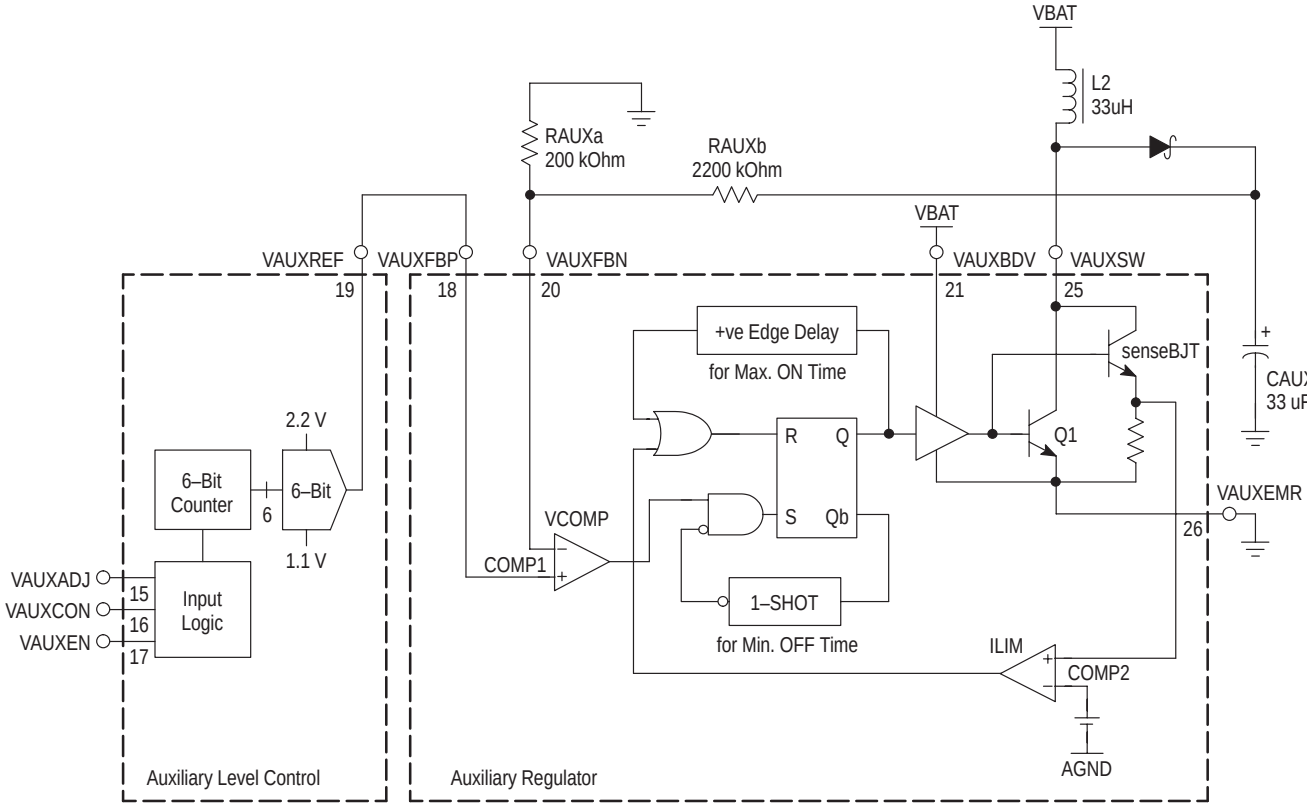


Figure 23. Simplified Block Diagram of Auxiliary Regulator

DETAILED OPERATING DESCRIPTION (Cont'd)

Auxiliary Regulator (Cont'd)

As the Auxiliary Regulator control scheme is the same as the Main Regulator, equations for conduction mode, Tsw and Ipk can also be applied, However, η to be used for caculation is refered to Figure 8, 10, or 12.

If external potentiometer is used for voltage level adjustment, internal 1.22V reference voltage can be used as shown in the application diagram of Figure 24.

Current Limit for Both regulators

From Figure 20 and Figure 23, sense devices (senseFET or senseBJT) are applied to sample coil current as the low–side switch is ON. With that sample current flowing through a sense resistor, sense–voltage is developed. Threshold detector (COMP2 in both figures) detects whether the sense–voltage is higher than preset level. If it happens, detector output reset the flip–flop to switch OFF low–side switch, and the switch can only be ON as next cycle starts.

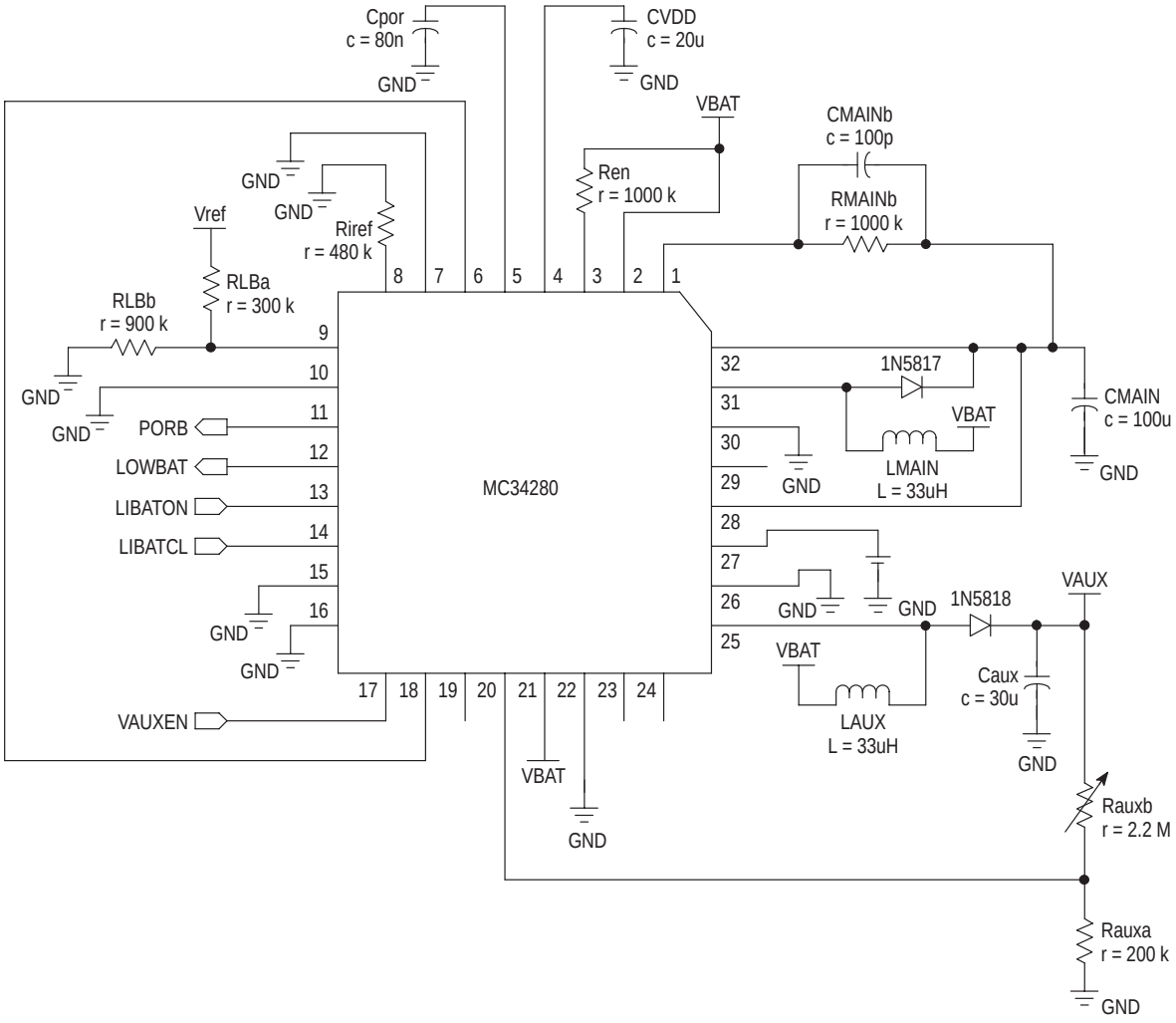


Figure 24. Application Diagram with External Potentiometer for VAUX Adjustment

DETAILED OPERATING DESCRIPTION (Cont'd)

Auxiliary voltage adjustment

The VAUX voltage can be adjusted by the microprocessor control signals, namely, VAUXCON and VAUXADJ. The control signal pattern is shown in Figure 4. The input truth table is shown in Figure 25.

When VAUXEN is LOW, the Auxiliary Regulator is shut down, only the counter content is retained. The initial counter content is mid–range of 6–bit.

At the rising edge of VAUXCON, if VAUXADJ is LOW (/ HIGH), each following VAUXADJ pulse enclosed by the VAUXCON pulse packet increments (/ decrements) the 6–bit counter. At the falling edge of VAUXCON, the counter content is then latched to a 6–bit DAC and is converted to a voltage level of VAUXREF between 1.1V and 2.2V.

At the falling edge of VAUXCON, if VAUXADJ is HIGH, the counter content will be reset to mid–range (1.65V). This is also the default setting just after power–ON reset is removed.

The 6–bit DAC converts the counter content to voltage level ranging from 1.1 to 2.2V, so there are altogether 64 levels, and each voltage step is 17mV. When the counter content reaches its maximum or minimum, further pulse of VAUXADJ will be disregarded, until counting direction is changed.

Power–ON Reset

The Power–ON Reset block accepts external active HIGH ENABLE signal to activate the IC after battery is plugged in. During the startup period (see Figure 2), the internal startup circuitry is enabled to pump up VMAIN to a certain voltage level, which is the user–defined VMAIN output level minus an offset of 0.15V. The internal power–on reset signal is then disabled to activate the main regulator and conditionally the auxiliary regulator. Meanwhile, the startup circuitry will be shut down. The Power–ON Reset block also starts to charge up the external capacitor tied from Pin PDELAY to ground with precise constant current. As the Pin PDELAY's voltage reaches an internal set threshold, Pin PORB will go HIGH to awake the microprocessor. And,

$$T_{POR} = \left(\frac{1.22}{0.5}\right) \times C_{por} \times RIref \quad (S)$$

From Figure 3, if, by any chance, VMAIN is dropped below the user–defined VMAIN output level minus 0.5V, PORB will go LOW to indicate the OUTPUT LOW situation. And, the IC will continue to function until the VMAIN is dropped below 2V.

Low–Battery–Detect

The Low–Battery–Detect block is actually a voltage comparator. Pin LOWBAT is LOW, if the voltage of external Pin LOWBATSEN is lower than 0.85V internal reference. The IC will neglect this warning signal. Pin LOWBAT will become HIGH, if the voltage of external Pin LOWBATSEN is recovered to more than 1.1V. From Figure 1, with external resistors RLBa and RLBb, thresholds of Low–Battery–Detect can be adjusted based on the equations below.

$$V_{LOBAThigh} = 1.1 \times \left(1 + \frac{R_{LBa}}{R_{LBb}}\right) \quad (V)$$

$$V_{LOBATlow} = 0.85 \times \left(1 + \frac{R_{LBa}}{R_{LBb}}\right) \quad (V)$$

VAUXEN	VAUXCON	VAUXADJ	RESULT
0	X	X	Hold the counter content
1	0	X	Hold the counter content
1		0	Set "countup" flag HIGH
1		1	Set "countup" flag LOW
1	1		Increment (/ Decrement) the counter if "countup" flag is HIGH (/ LOW)
1		0	DAC the counter content to VAUXREF voltage level (1.1 – 2.2 V)
1		1	Reset the counter to mid–range, then convert the counter content to VAUXREF voltage level (1.65V)

Figure 25. Auxiliary Voltage Control Input Truth Table

DETAILED OPERATING DESCRIPTION (Cont'd)

Lithium–Battery backup

The backup conduction path which is provided by an internal power switch (typ. 13 Ohm) can be controlled by internal logic or microprocessor.

If LIBATCL is LOW, the switch, which is then controlled by internal logic, is ON when the battery is removed and VMAIN is dropped below LIBATIN by more than 100mV, and returns OFF when the battery is plugged back in.

If LIBATCL is HIGH, the switch is controlled by microprocessor through LIBATON. The truth table is shown in Figure 26.

Efficiency and Output Ripple

For both regulators, when large values are used for feedback resistors (> 50kOhm), stray capacitance of pin 1 (VMAINFB) and pin 20 (VAUXFBN) can add "lag" to the feedback response, destabilizing the regulator and creating a larger ripple at the output. From Figure 1, ripple of Main and AUX regulator can be reduced by CMAINb, CAUXa and CAUXb ranging from 100pF to 100nF respectively. Reducing the ripple is also with improving efficiency, system designers are recommended to do experiments on capacitance values based on the PCB design.

Bypass Capacitors

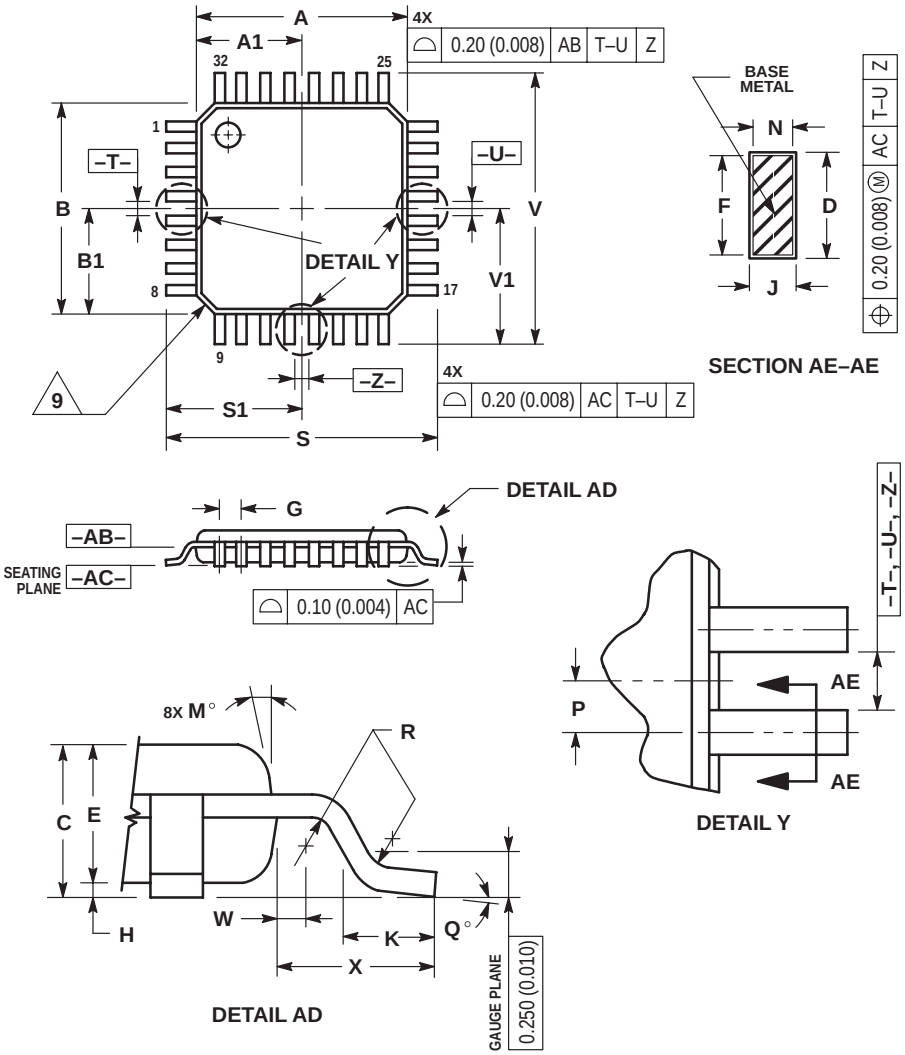
If the metal leads from battery to coils are long, its stray resistance can put additional power loss to the system as AC current is being conducted. In that case, bypass capacitors (CMAINbp and CAUXbp of Figure 1) are recommended to remove AC components of coil currents to minimize that power loss to optimize efficiency.

LIBATCL	LIBATON	Action
0	X	The switch is ON when the battery is removed and VMAIN is dropped below LIBATIN by more than 100mV; The switch is OFF when the battery is plugged in.
1	0	The switch is OFF
1	1	The switch is ON

Figure 26. Lithium Battery Backup Control Truth Table

PACKAGE DIMENSIONS

32–LEAD LQFP
FTB SUFFIX
CASE 873A–02



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

Notes

Notes

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