THOMSON COMPOSANTS MILITAIRES ET SPATIAUX

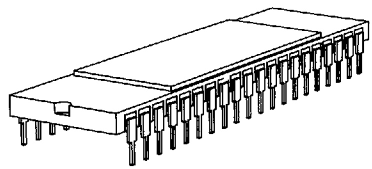
EF 6803

NMOS 8-BIT MICROPROCESSOR

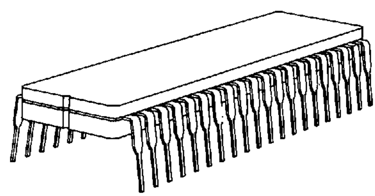
DESCRIPTION

The EF 6803 is an 8-bit single-chip microprocessor unit (MPU) which significantly enhances the capabilities of 6800 family of parts derived drom the 6801 microcomputer. It includes an upgraded 6800 microprocessor unit (MPU) which upward-source and object-code compatibility. Execution times of key instructions have been improved and several new instructions have been added including an unsigned multiply. The MPU can be expanded to a 64 K byte address space. It is TTL compatible and requires one +5 volt power supply. 128 bytes of RAM, a Serial Communications Interface (SCI), parallel I/O, and a three function programmable timer. The EF 6803 can be considered as an 6801 MCU operating in modes 2 or 3.

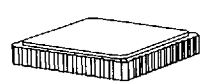
The 6801 provides eight different operating modes (0 to 7), described in this data sheet. The EF 6803 provides two operating modes (modes 2 and 3 of 6801).



C Suffix
DIL 40
Ceramic Side Brazed



J Suffix
DIL 40
Cerdip



E Suffix
LCCC 44
Leadless Ceramic Chip Carrier

PIN CONNECTIONS (see chapter 10)

See the Ordering Information at the end of the data sheet.

MAIN FEATURES

- Enhanced EF 6800 instruction set.
- 8×8 multiply instruction.
- Serial Communications Interface (SCI).
- Upward source and object code compatibility with the 6800.
- 16 bit three-function programmable timer.
- Single-chip or expanded operation to 64 K byte address space.
- Bus compatibility with the 6800 family.
- 128 bytes of RAM.
- 64 bytes of RAM retainable during powerdown.
- 29 parallel I/O and two handshake control lines.
- Internal clock generator with divide-by-four output.
- Complete development system support on DEVICE®.
- Temperature ranges :
  - 0°C to +70°C,
  - −40°C to +85°C,
  - −55°C to +125°C.

SCREENING / QUALITY

This product is manufactured in full compliance with :

- MIL-STD-883 class B.
- NFC 96883 (class G).
- TMS standard.

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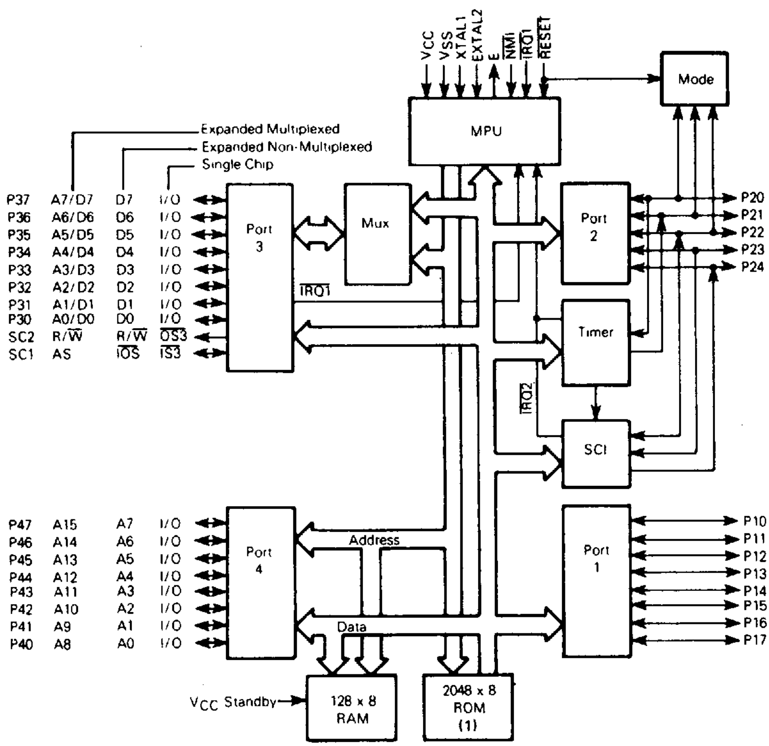
\ · GENERAL DESCRIPTION

· BLOCK DIAGRAM

he EF 6803 is a high-performance microprocessor implemented in HCMOS, low power, small geometry process. This process llows CMOS and HMOS (high density NMOS) gates to be combined on the same device. CMOS structures are used where peed and low power is required, and HMOS structures are used where minimum silicon area is desired. This technology enables the EF 6803 to be very fast while consuming less power (less than 1.5 watts) and still have a reasonably small die size. he size of the EF 6803 silicon die is 5.4 x 9.2 mm. It utilizes about 190.000 transistors, 103.000 of which are actually implemened.

igure 1 is a block diagram of the EF 6803. The processor can be divided into two main sections : the bus controller and the icromachine. This division reflects the autonomy with which the sections operate.



(1) No functioning ROM in EF6803

Figure 1 : 6801/6803 block diagram.

B · DETAILED SPECIFICATIONS

1 · SCOPE

This drawing describes the specific requirements for the microprocessor EF 6803 1 and 1.5 MHz, in compliance witl MIL-STD-883 class B or CECC 90000.

2. APPLICABLE DOCUMENTS

2.1 · MIL-STD-883

1) MIL-STD-883 : test methods and procedures for electronics.
2) MIL-M-38510 : general specifications for microcircuits.

3 · REQUIREMENTS

3.1 · General

The microcircuits are in accordance with the applicable document and as specified herein.

3.2 · Design and construction

3.2.1 · Terminal connections

Depending on the package, the terminal connections shall be is shown in § 10.1 and §10.2.

3.2.2 · Lead material and finish

Lead material and finish shall be any option of MIL-M-38510 except finish C (as described in 3.5.6.1 of 38510).

3.2.3 · Package

The macrocircuits are packaged in a hermetically sealed ceramic packages which are conform to case outlines o MIL-M-38510 appendix C (when defined) :

- 40 leads DIL Ceramic Side Brazed,
- 40 leads DIL Ceramic Cerdip,
- 44 terminals SQ LCCC.

The precise case outlines are described on Figures § 9.1, 9.2 and 9.3.

3.3 · Electrical characteristics

3.3.1 · Absolute maximum ratings (See Table 1)

Table 1

Symbol	Parameter		Test conditions	Min	Max	Unit
V_{CC}	Supply voltage			−0.3	+7.0	V
V_I	Input voltage			−0.3	+7.0	V
P_{dmax}	Max power dissipation		T_{case} = −55°C / +125°C		1.5	W
T_{case}	Operating temperature	M suffix : EF 6803/EF 68A03	f = 1 and 1.5 MHz	−55	+125	°C
		V suffix : EF 6803/EF 68A03	f = 1 and 1.5 MHz	−40	+85	°C
		No suffix : EF 6803/EF 68A03/ EF 68B03	f = 1, 1.5 and 2 MHz	0	+70	°C
T_{stg}	Storage temperature			−55	+150	°C
T_j	Junction temperature				+170	°C
T_{leads}	Lead temperature		Max 5 sec. soldering		+270	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electrical fields ; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{CC}$. Input protection is enhanced by connecting unused inputs to either V_{DD} or V_{SS}.

4 · **Thermal characteristics (at 25°C)**

ble 2

Package	Symbol	Parameter	Value	Unit
DIL 40 J and C suffix	θ JA θ JC	Thermal resistance - Ceramic junction to ambient Thermal resistance - Ceramic junction to case	45 7	°C/W °C/W
LCCC 44 E suffix	θ JA θ JC	Thermal resistance - Ceramic junction to ambient Thermal resistance - Ceramic junction to case	40 8	°C/W °C/W

ower considerations

he average chip-junction temperature, T_J, in °C can be obtained from :

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

A = Ambient Temperature, °C.
JA = Package Thermal Resistance, Junction-to-Ambient, °C/W.
D = $P_{INT} + P_{I/O}$.
INT = $I_{CC} \times V_{CC}$, Watts – Chip Internal Power.
I/O = Power Dissipation on Input and Output Pins – User Determined.

or most applications $P_{I/O} < P_{INT}$ and can be neglected.

n approximate reliationship between P_D and T_J (if $P_{I/O}$ is neglected) is :

$$P_D = K : (T_J + 273) \quad (2)$$

olving equations (1) and (2) for K gives :

$$K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D^2 \quad (3)$$

here K is a constant pertaining to the particular part K can be determined from equation (3) by measuring P_D (at equilibrium) or a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for ny value of T_A.

he total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier o heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient CA). These terms are related by the equation :

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

JC is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such hermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management n the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

.5 · Mechanical and environment

he microcircuits shall meet all mechanical environmental requirements of either MIL-STD-833 for class B devices or ECC 90000 devices.

.6 · Marking

he document where are defined the marking are identified in the related reference documents. Each microcircuit are legible nd permanently marked with the following information as minimum :

.6.1 · Thomson logo

.6.2 · Manufacturer's part number

.6.3 · Class B identification

.6.4 · Date-code of inspection lot

.6.5 · ESD identifier if available

.6.6 · Country of manufacturing

4 · QUALITY CONFORMANCE INSPECTION

4.1 · MIL-STD-883

Is in accordance with MIL-M-38510 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

5 · ELECTRICAL CHARACTERISTICS

5.1 · General requirements

All static and dynamic electrical characteristics are specified for inspection purpose, and the relevant measurements conditions are given below :

Table 3 : Static electrical characteristics for all electrical variants. See § 5.2.

Table 4 : Dynamic electrical characteristics. See § 5.3.

5.2 · Static characteristics

Table 3 · DC electrical characteristics

V_{CC} = 5.0 V_{dc} ±5 % ; V_{SS} = 0 V_{dc} ; T_C = −55°C / +125°C or −40°C / +85°C and 0°C / +70°C (unless otherwise specified)

Symbol	Characteristic		EF 6803 0°C to +70°C		EF 6803 −40°C / +85°C		EF 6803 −55°C / +125°C		Unit
			Min	Max	Min	Max	Min	Max	
V_{IH}	Input high voltage	RESET Other inputs	V_{SS} +4.0 V_{SS} +2.0	V_{CC} V_{CC}	V_{SS} +4.0 V_{SS} +2.2	V_{CC} V_{CC}	V_{SS} +4.0 V_{SS} +2.2	V_{CC} V_{CC}	V V
V_{IL}	Input low voltage	All inputs	V_{SS} −0.3	V_{SS} +0.8	V_{SS} −0.3	V_{SS} +0.8	V_{SS} −0.3	V_{SS} +0.8	V
I_{in}	Input load current (V_{in} = 0 to 2.4 V)	Port 4 SCI		0.5 0.8		0.8 1.0		0.8 1.0	mA mA
I_{in}	Input leakage current (V_{in} = 0 to 5.25 V)	NMI, IRQ1, RESET		2.5		5.0		5.0	µA
I_{TSI}	Hi-Z (off state) input current (V_{in} = 0.5 to 2.4 V)	Ports 1, 2 and 3		10		20		20	µA
V_{OH}	Output high voltage (I_{load} = −65 µA, V_{CC} = min)* (I_{load} = −100 µA, V_{CC} = min)	E, Port 4, SC1, SC2 Other outputs	V_{SS} +2.4 V_{SS} +2.4		V_{SS} +2.4 V_{SS} +2.4		V_{SS} +2.4 V_{SS} +2.4		V V
V_{OL}	Output low voltage (I_{load} = 2.0 mA, V_{CC} = min)	All outputs		V_{SS} +0.5		V_{SS} +0.6		V_{SS} +0.6	V
I_{OH}	Darlington drive current (V_O = 1.5 V)	Port 1	1.0	4.0	1.0	5.0	1.0	5.0	mA
P_{INT}	Internal power dissipation (Measured at T_A = T_L in steady-state operation)			1200		1500		1500	mW
C_{in}	Input capacitance (V_{in} = 0, T_A = 25°C, f_0 = 1.0 MHz)	Port 3, Port 4, SCI Other inputs		12.5 10		12.5 10		12.5 10	pF pF
V_{SBB} V_{SB}	V_{CC} Standby	Powerdown Powerup	4.0 4.75	5.25 5.25	4.0 4.75	5.25 5.25	4.0 4.75	5.25 5.25	V V
I_{SSB}	Standby current	Powerdown		6.0		8.0		8.0	mA

* Negociable to −100 µA (for further information contact the factory).

5.3 · Dynamic (switching) characteristics

The limits and values given in this section apply over the full case temperature range −55°C to +125°C and V_{CC} in the range 4.75 V to 5.25 V V_{IL} = 0.8 V and V_{IH} = 2.0 V.

able 4 - Control timing
V_{CC} = 5.0 V ±5 % ; V_{SS} = 0 ; f = 1 and 1.5 MHz : $-40°C \leq T_C \leq +85°C$ and $-55°C \leq T_C \leq +125°C$
f = 2 MHz : $0°C \leq T_C \leq +70°C$ only

Symbol	Characteristic	EF 6803		EF 68A03		EF 68B03		Unit
		Min	Max	Min	Max	Min	Max	
f_o	Frequency of operation	0.5	1.0	0.5	1.5	0.5	2.0	MHz
f_{XTAL}	Crystal frequency	2.0	4.0	2.0	6.0	2.0	8.0	MHz
$4f_o$	External oscillator frequency	2.0	4.0	2.0	6.0	2.0	8.0	MHz
t_{rc}	Crystal oscillator start up time	100		100		100		ms
t_{PCS}	Processor control setup time	200		140		110		ns

able 5 - Peripheral port timing (refer to Figure 2)
V_{CC} = 5.0 V ±5 % ; V_{SS} = 0 ; f = 1 and 1.5 MHz : $-40°C \leq T_C \leq +85°C$ and $-55°C \leq T_C \leq +125°C$
f = 2 MHz : $0°C \leq T_C \leq +70°C$ only

Symbol	Characteristic	EF 6803		EF 68A03		EF 68B03		Unit
		Min	Max	Min	Max	Min	Max	
t_{PDSU}	Peripheral data setup time	200		150		100		ns
t_{PDH}	Peripheral data hold time	200		150		100		ns
t_{OSD1}	Delay time, enable positive transition to OS3negative transition		350		300		250	ns
t_{OSD2}	Delay time, enable positive transition to OS3 positive transition		350		300		250	ns
t_{PWD}	Delay time, enable negative transition to peripheral data valid		350		300		250	ns
t_{CMOS}	Delay time, enable negative transition to peripheral CMOS data valid		2.0		2.0		2.0	µs
t_{PWIS}	Input strobe pulse width	200		150		100		ns
t_{IH}	Input data hold time	50		40		30		ns
t_{IS}	Input data setup time	20		20		20		ns

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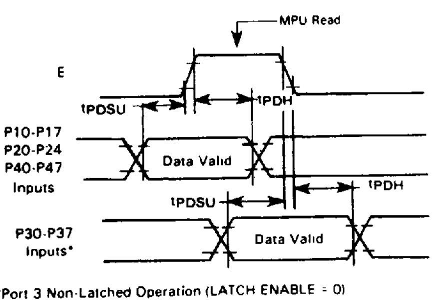
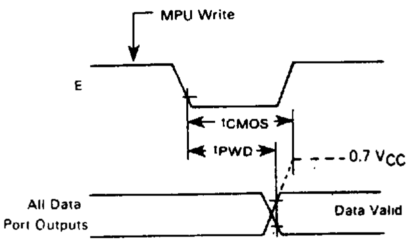


Figure 2 : Data setup and hold times (MPU read).



NOTES:
1 10 k Pullup resistor required for Port 2 to reach 0.7 V_{CC}
2 Not applicable to P21
3 Port 4 cannot be pulled above V_{CC}

Figure 3 : Data setup and hold times (MPU write).

Note : Timing measurements are referenced to and from a low voltage of 0.8 volt and a high voltage of 2.0 volts, unless otherwise specified.

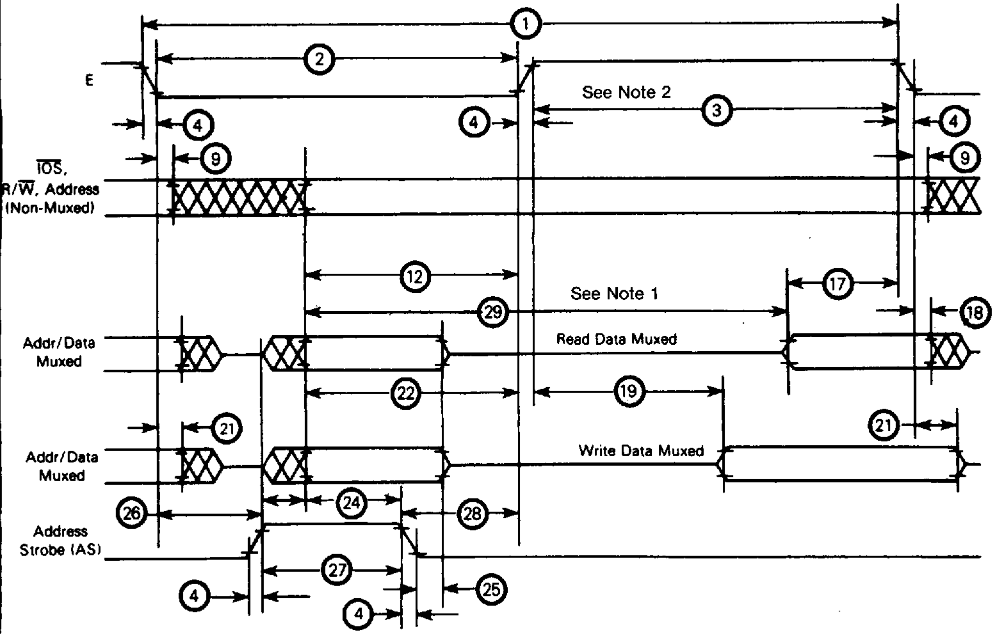
Table 6 - Bus timing (see Notes 1 and 2)

$V_{CC} = 5.0\ V \pm 5\ \%$; $V_{SS} = 0$; f = 1 and 1.5 MHz : $-40°C \leqslant T_C \leqslant +85°C$ and $-55°C \leqslant T_C \leqslant +125°C$

f = 2 MHz : $0°C \leqslant T_C \leqslant +70°C$ only

Ident. Number	Symbol	Characteristic	EF 6803		EF 68A03		EF 68B03		Unit
			Min	Max	Min	Max	Min	Max	
1	t_{cyc}	Cycle time	1.0	2.0	0.667	2.0	0.5	2.0	µs
2	PW_{EL}	Pulse width, E low	430	1000	300	1000	210	1000	ns
3	PW_{EH}	Pulse width, E high	450	1000	300	1000	220	1000	ns
4	t_r, t_f	Clock rise and fall time		25		25		20	ns
9	t_{AH}	Address hold time	20		20		10		ns
12	t_{AV}	Non-muxed address valid to E - Note 3	200		115		70		ns
17	t_{DSR}	Read data setup time	80		60		40		ns
18	t_{DHR}	Read data hold time	10		10		10		ns
19	t_{DDW}	Write data delay time		225		170		120	ns
21	t_{DHW}	Write data hold time	20		20		10		ns
22	t_{AVM}	Muxed address valid time to E rise - Note 3	200		115		80		ns
24	t_{ASL}	Muxed address valid time to AS fall - Note 3	60		40		20		ns
25	t_{AHL}	Muxed address hold time	20		20		10		ns
26	t_{ASD}	Delay time, E to AS rise Note 3	90*		60*		45*		ns
27	PW_{ASH}	Pulse width, AS high - Note 3	220		140		110		ns
28	t_{ASED}	Delay time, AS to E rise Note 3	90		60		45		ns
29	t_{ACC}	Usable access time	595		380		270		ns

Note 1 : Voltage levels shown are $V_L \leqslant 0.5\ V$, $V_H \geqslant 2.4\ V$, unless otherwise specified.
Note 2 : Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.
Note 3 : At specified cycle time.
* t_{ASD} parameters listed assume external TTL clock drive with 50 % ±5 % duty cycle. Devices driven by an external TTL clock with 50 % ±1 % duty cycle or which use a crystal have the following t_{ASD} specifications : 100 ns min (1.0 MHz devices), 65 ns min (1.5 MHz devices), 50 ns min (2 MHz devices).



Note 1 : Usable access time is computed by 12+3 - 17+4.
Note 2 : Memory devices should be enabled only during E high to avoid Port 3 bus contention.

Figure 4 : Bus timing.

Table 7 · Mode programming (refer to Figure 5)
V_{CC} = 5.0 V ±5 % ; V_{SS} = 0 ; f = 1 and 1.5 MHz : for V and M suffix
f = 2 MHz : for civil 0-70°C version

Characteristic	Symbol	Min	Max	Unit
Mode Programming Input Voltage Low*	V_{MPL}	–	1.8	V
Mode Programming Input Voltage High	V_{MPH}	4.0	–	V
Mode Programming Diode Differential (If Diodes are Used)	V_{MPDD}	0.6	–	V
$\overline{RESET}$ Low Pulse Width	PW_{RSTL}	3.0	–	E-Cycles
Mode Programming Setup Time	t_{MPS}	2.0	–	E-Cycles
Mode Programming Hold Time $\overline{RESET}$ Rise Time ≥ 1 µs $\overline{RESET}$ Rise Time < 1 µs	t_{MPH}	 0 100	 – –	ns

*For T_A = –40°C to + 105°C, V_{MPL} = 1.7 V.

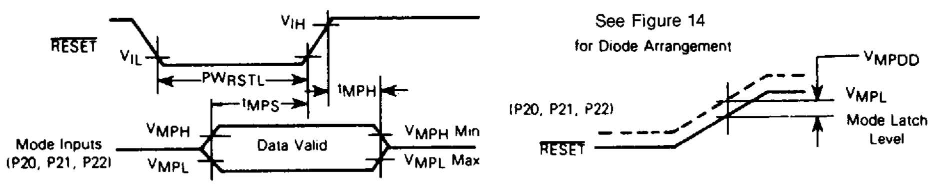


Figure 5 : Mode programming timing.

5.4 - Test conditions specific to the device

5.4.1 - Loading network

Figures 6 and 7 here below show the loading network applicable to the previous timing tables.

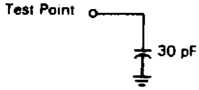
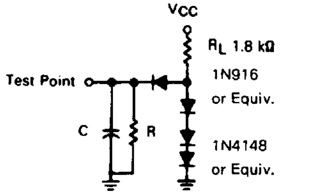


Figure 6 : CMOS load.



C = 90 pF for P30-P37, P40-P47, E, SC1, SC2
= 30 pF for P10-P17, P20-P24
R = 37 kΩ for P40-P47, E, SC1, SC2
= 24 kΩ for P10-P17, P20-P24
= 24 kΩ for P30-P37

Figure 7 : Timing test load ports 1, 2, 3, 4.

6 - FUNCTIONAL DESCRIPTION

6.1 - Introduction

The EF 6803 microprocessor unit (MPU) is an enhanced EF 6800 MPU with additional capabilities and greater throughput. It is upward source and object code compatible with the EF 6800. The programming model in depicted in Figure 8, where Accumulator D is a concatenation of Accumulators A and B. A list of new operations added to the 6800 isntruction set are shown in Table 8.

The EF 6803 can be considered 6801 that operates in Modes 2 and 3 Only.

The 6801 is an 8-bit monolithic microcomputer which can be configured to function in a wide variety of applications. The facility which provides this extraordinary flexibility is its ability to be hardware programmed into eight different operating modes. The operating mode controls the configuration of 18 of the 40 MCU pins, available on-chip resources, memory map, location (internal or external) of interrupt vectors, and type of external bus. The configuration of the remaining 22 pins is not dependent on the operating mode.

Twenty-nine pins are organized as three 8-bit ports and one 5-bit port. Each port consists of at least a Data Register and a write-only Data Direction Register. The Data Direction Register is used to define whether corresponding bits in the Data Register are configured as an input (clear) or output (set).

The term «port», by itself, refers to all of the hardware associated with the port. When the port is used as a «data port» or «I/O port», it is controlled by the port Data Direction Register and the programmer has direct access to the port pins using the port Data Register. Port pins are labled as Pij where i identifies one of four ports and j indicates the particular bit.

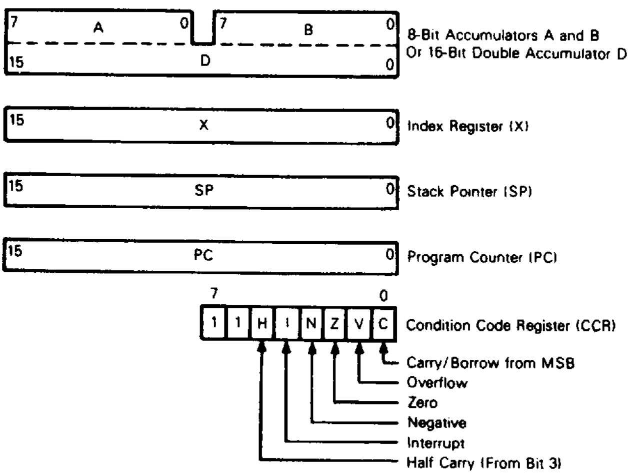


Figure 8 : Programming model.

.2 - 6801/6803 operating modes

'he 6801 provides eight different operating modes (Modes 0 through 7), the EF 6803 provides two operating modes (Modes 2 nd 3). The operating modes are hardware selectable and determine the device memory map, the configuration of Port 3, 'ort 4, SC1, SC2, and the physical location of the interrupt vectors.

.2.1 - *Fundamental modes*

'he eight operating modes can be grouped into three fundamental modes which refer to the type of bus it supports: Single hip, Expanded Non-Multiplexed, and Expanded Multiplexed. Single chip modes include 4 and 7, Expanded Non-Multiplexed 1 Mode 5 and the remaining five are Expanded Multiplexed modes. Table 9 summarizes the characteristics of the operating 1odes.

.2.1.1 - 6801 Single-Chip Modes (4,7)

1 the Single-Chip Mode, the four MCU ports are configured as parallel input/output data ports, as shown in Figure 9. The MCU unctions as a monolithic microcomputer in these two modes without external address or data buses. A maximum of 29 I/O nes and two Port 3 control lines are provided. Peripherals or another MCU can be interfaced to Port 3 in a loosely coupled ual processor configuration, as shown in Figure 10.

able 8 - New instructions

Instruction	Description
ABX	Unsigned addition of Accumulator B to Index Register
ADDD	Adds (without carry) the double accumulator to memory and leaves the sum in the double accumulator
ASLD or LSLD	Shifts the double accumulator left (towards MSB) one bit; the LSB is cleared and the MSB is shifted into the C-bit
BHS	Branch if Higher or Same; unsigned conditional branch (same as BCC)
BLO	Branch if Lower; Unsigned conditional branch (same as BCS)
BRN	Branch Never
JSR	Additional addressing mode: direct
LDD	Loads double accumulator from memory
LSL	Shifts memory or accumulator left (towards MSB) one bit; the LSB is cleared and the MSB is shifted into the C-bit (same as ASL)
LSRD	Shifts the double accumulator right (towards LSB) one bit; the MSB is cleared and the LSB is shifted into the C-bit
MUL	Unsigned multiply; multiplies the two accumulators and leaves the product in the double accumulator
PSHX	Pushes the Index Register to stack
PULX	Pulls the Index Register from stack
STD	Stores the double accumulator to memory
SUBD	Subtracts memory from the double accumulator and leaves the difference in the double accumulator
CPX	Internal processing modified to permit its use with any conditional branch instruction

1 Single-Chip Test Mode (4), the RAM responds to $XX80 through $XXFF and the ROM is removed from the internal address 1ap. A test program must first be loaded into the RAM using modes 0, 1, 2, or 6. If the MCU is Reset and then programmed 1to Mode 4, execution will begin at $XXFE:XXFF. Mode 5 can be irreversibly entered from Mode 4 without asserting RESET by etting bit 5 of the Port 2 Data Register. This mode is used primarily to test Ports 3 and 4 in the Single-Chip and Non-Multi- lexed Modes.

.2.1.2 - 6801 expanded Non-Multiplexed Mode (5)

\ modest amount of external memory space is provided in the Expanded Non-Multiplexed Mode while significant on-chip re- ources are retained. Port 3 functions as an 8-bit bidirectional data bus and Port 4 is configured initially as an input data port. \ny combination of the eight least-significant address lines may be obtained by writing to the Port 4 Data Direction Register. Stated alternatively, any combination of A0 to A7 may be provided while retaining the remainder as input data lines. Internal ullup resistors pull the Port 4 lines high until the port is configured.

'igure 11 illustrates a typical system configuration in the Expanded Non-Multiplexed Mode. The MCU interfaces directly with 800 family parts and can access 256 bytes of external address space at $100 through $1FF. IOS provides an address decode f external memory ($100-$1FF) and can be used as a memory page select or chip select line.

Table 9 - Summary of 6801/6803 operating modes

Common to all modes : Reserved register area Port 1 Port 2 Programmable timer Serial communications interface
Single chip mode 7 (6801 only) 128 bytes of RAM ; 2048 bytes of ROM Port 3 is a parallel I/O with two control lines Port 4 is a parallel I/O port SC1 is input strobe 3 (IS3) SC2 is output strobe 3 (OS3)
Expanded non-multiplexed mode 5 (6801 only) 128 bytes of RAM ; 2048 bytes of ROM 256 bytes of external memory space Port 3 is an 8-bit data bus Port 4 is an input port/address bus SC1 is input/output select (IOS) SC2 is read/write (R/W)
Expanded multiplexed modes 1,2, 3, 6 - see Note Four memory space options (64 K address space) : (1) No internal RAM or ROM (mode 3) (2) Internal RAM, no ROM (mode 2) (3) Internal RAM and ROM (mode 1) (4) Internal RAM, ROM with partial address bus (mode 6) Port 3 is a multiplexed address / data bus Port 4 is an address bus (input/address in mode 6) SC1 is address strobe (AS) SC2 is read/write (R/W)
Test modes 0 and 4 (6801 only) Expanded multiplexed test mode 0 May be used to test RAM and ROM Single chip and non-multiplexed test mode 4 (1) May be changed to mode 5 without going through reset (2) May be used to test Ports 3 and 4 as I/O ports
Note : The EF 6803 operates only in modes 2 and 3.

*6.2.1.3 - Expanded-Multiplexed Modes (0, 1, 2, 3, 6)**

A 64 K byte memory space is provided in the expanded multiplexed modes, In each of the expanded multiplexed modes Po 3 functions as a time multiplexed address/data bus with address valid on the negative edge of Address Strobe (AS), and dat valid while E is high. In Modes 0 to 3, Port 4 provides address lines A8 to A15. In Mode 6, however, Port 4 initially is configure at RESET as an input data port. The port 4 Data Direction Register can then be changed to provide any combination of addres lines, A8 to A15. Stated alternatively, any subset of A8 to A15 can be provided while retaining the remaining port 4 lines a input data lines. Internal pullup resistors pull the Port 4 lines high until software configures the port.

In Mode 0, the Reset vector is external for the first two E-cycles after the positive edge of RESET, and internal thereafter. I addition, the internal and external data buses are connected so there must be no memory map overlap in order to avoid poter tial bus conflicts. Mode 0 is used primarily to verify the ROM pattern and monitor the internal data bus witht the automate test equipment.

Only the 6801 can operate in each of the expanded multiplexed modes. The EF 6803 operates only in Modes 2 and 3.

Figure 12 depicts a typical configuration for the Expanded-Multiplexed Modes. Address Strobe can be used to control a tran parent D-type latch to capture address A0-A7, as shown in Figure 13. This allows Port 3 to function as a Data Bus when E i high.

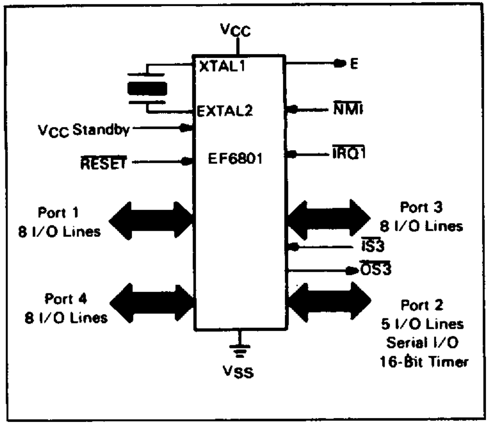


Figure 9 : Single-chip mode.

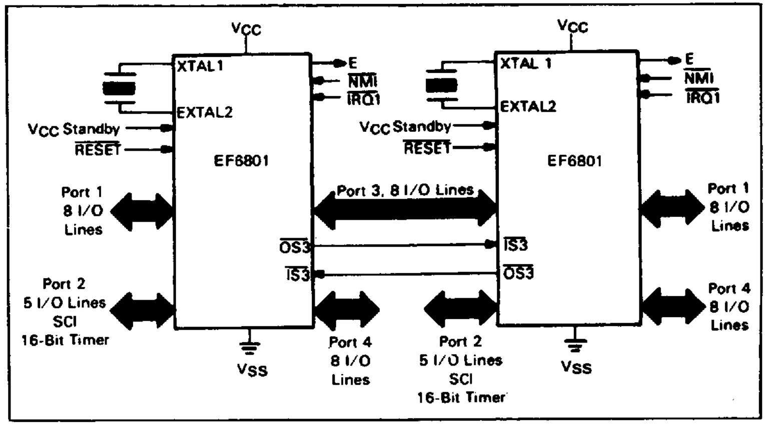


Figure 10 : Single-chip dual processor configuration.

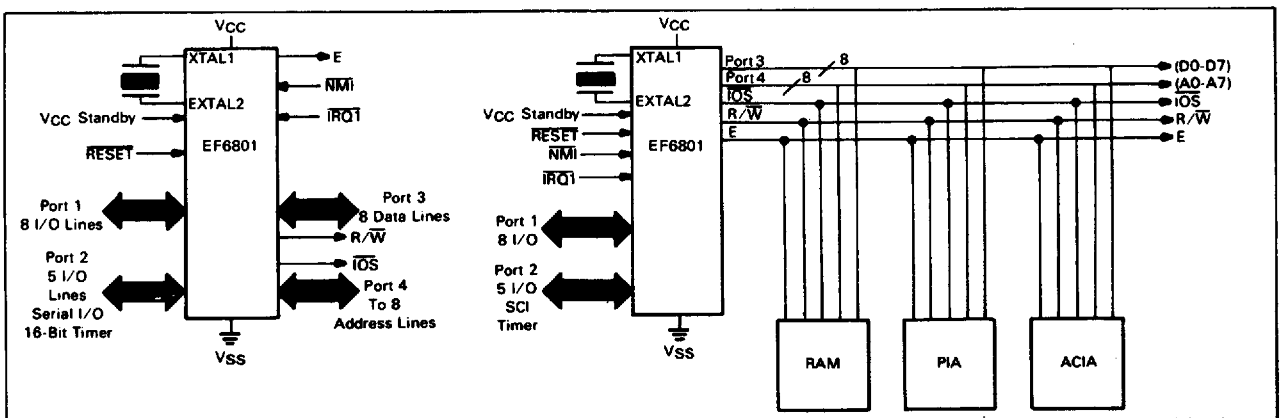


Figure 11 : Expanded non-multiplexed configuration.

5

6.2.2 · Programming the mode

The operating mode is determined at RESET by the levels asserted on P22, P21, and P20. These levels are latched into PC2, PC1, and PC0 of the program control register on the positive edge of RESET. The operating mode may be read from the Port 2 Data Register as shown below, and programming levels and timing must be met as shown in Figure 4. A brief outline of the operating mode is shown in Table 10.

PORT 2 DATA REGISTER

7	6	5	4	3	2	1	0	
PC2	PC1	PC0	P24	P23	P22	P21	P20	$0003

Circuitry to provide the programming levels is dependent primarily on the normal system usage of the three pins. If configured as output, the circuit shown in Figure 14 may be used ; otherwise, three-state buffers can be used to provide isolation while programming the mode.

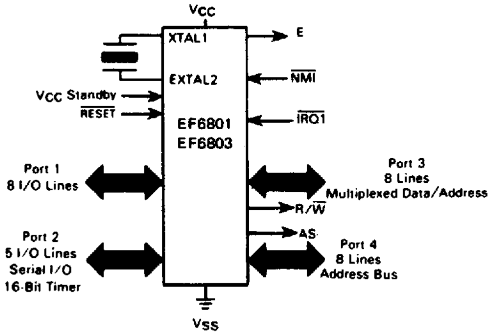
Table 10 · Mode selection summary

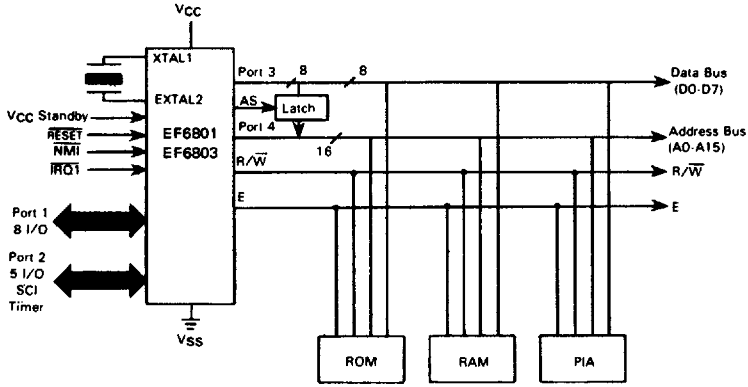
Mode*	P22 PC2	P21 PC1	P20 PC0	ROM	RAM	Interrupt Vectors	Bus Mode	Operating Mode
7	H	H	H	I	I	I	I	Single Chip
6	H	H	L	I	I	I	MUX(5, 6)	Multiplexed/Partial Decode
5	H	L	H	I	I	I	NMUX(5, 6)	Non-Multiplexed/Partial Decode
4	H	L	L	I(2)	I(1)	I	I	Single Chip Test
3	L	H	H	E	E	E	MUX(4)	Multiplexed/No RAM or ROM
2	L	H	L	E	I	E	MUX(4)	Multiplexed/RAM
1	L	L	H	I	I	E	MUX(4)	Multiplexed/RAM & ROM
0	L	L	L	I	I	I(3)	MUX(4)	Multiplexed Test

Legend:
- I — Internal
- E — External
- MUX — Multiplexed
- NMUX — Non-Multiplexed
- L — Logic "0"
- H — Logic "1"

Notes:
(1) Internal RAM is addressed at $XX80
(2) Internal ROM is disabled
(3) $\overline{RESET}$ vector is external for 2 cycles after $\overline{RESET}$ goes high
(4) Addresses associated with Ports 3 and 4 are considered external in Modes 0, 1, 2, and 3
(5) Addresses associated with Port 3 are considered external in Modes 5 and 6
(6) Port 4 default is user data input, address output is optional by writing to Port 4 Data Direction Register

*The EF6803 operates only in Modes 2 and 3





NOTE: To avoid data bus (Port 3) contention in the expanded multiplexed modes, memory devices should be enabled only during E high time.

Figure 12: Expanded multiplexed configuration.

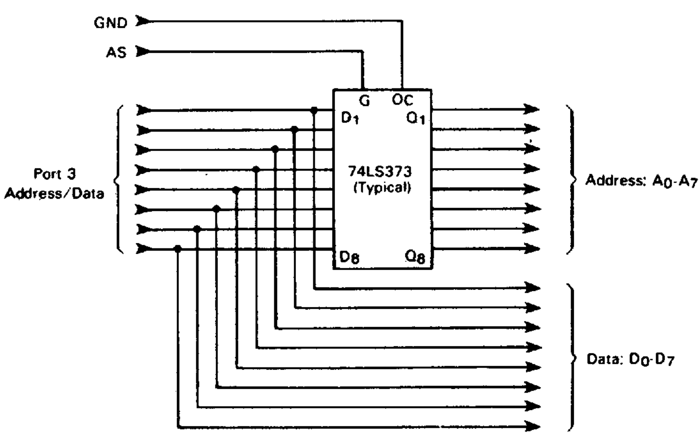
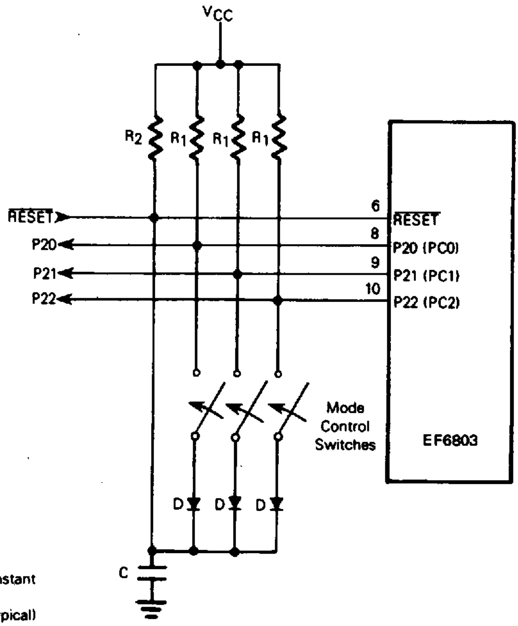


Figure 13: Typical latch arrangement.



Notes:
1. Mode 7 as shown
2. $R_2 \bullet C$ = Reset time constant
3. R_1 = 10 k (typical)
4. D = 1N914, 1N4001 (typical)
5. Diode V_f should not exceed V_{MPDD} min.

Figure 14 : Typical mode programming circuit.

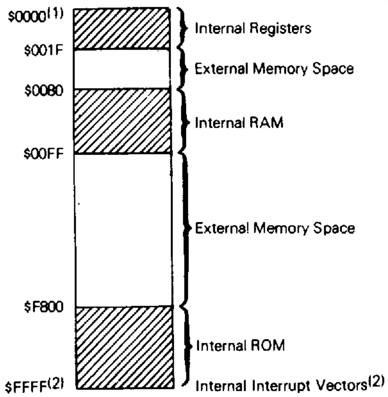
6.2.3 · Memory maps

The 6801 family can provide up to 64 K byte address space depending on the operating mode. A memory map for each operating mode is shown in Figure 15.

The first 32 locations of each map are reserved for th internal register area, as shown in Table 11, with exceptions as indicated.

Multiplexed-Test Mode

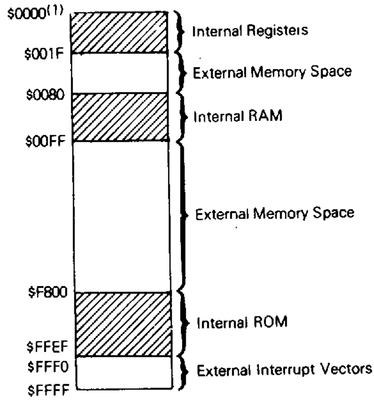
EF6801 Mode **0**



NOTES:
1) Excludes the following addresses which may be used externally: $04, $05, $06, $07, and $0F.
2) Addresses $FFFE and $FFFF are considered external if accessed within two cycles after a positive edge of $\overline{RESET}$ and internal at all other times.
3) After two MPU cycles, there must be no overlapping of internal and external memory spaces to avoid driving the data bus with more than one device.
4) This mode is the only mode which may be used to examine the interrupt vectors in internal ROM using an external $\overline{RESET}$ vector.

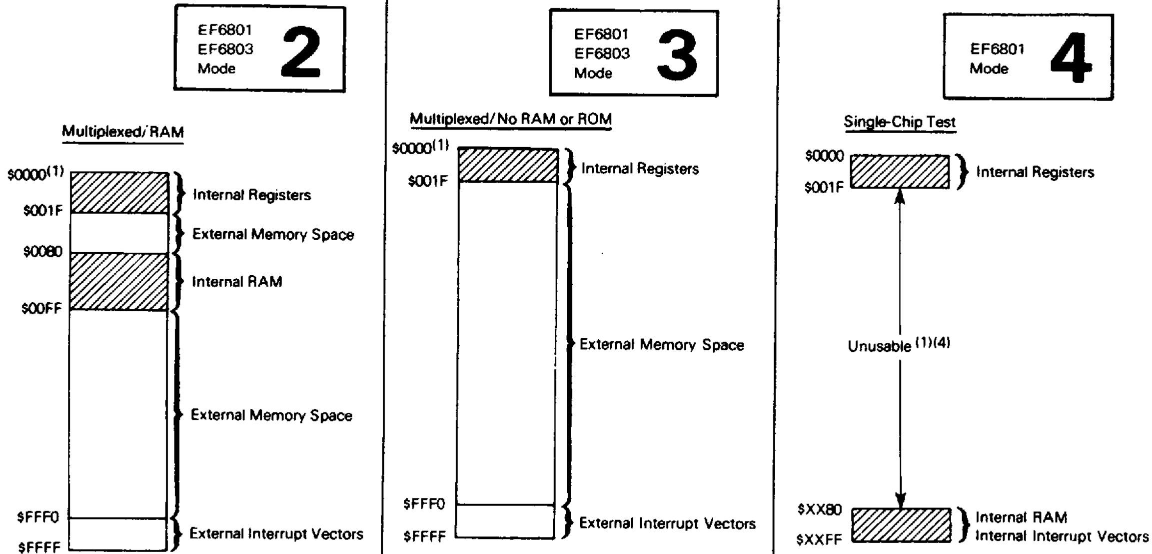
EF6801 Mode **1**

Multiplexed/RAM and ROM



NOTES:
1) Excludes the following addresses which may be used externally: $04, $05, $06, $07, and $0F.
2) Internal ROM addresses $FFF0 to $FFFF are not usable.

Figure 15 : 6801/6803 memory maps (sheet 1 of 3).

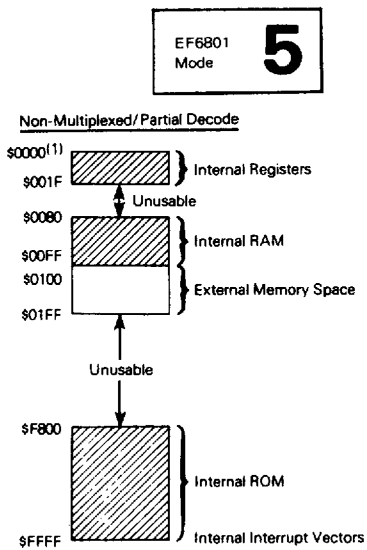


Mode 2 (Multiplexed/RAM) — NOTES:
1) Excludes the following addresses which may be used externally: $04, $05, $06, $07, and $0F.

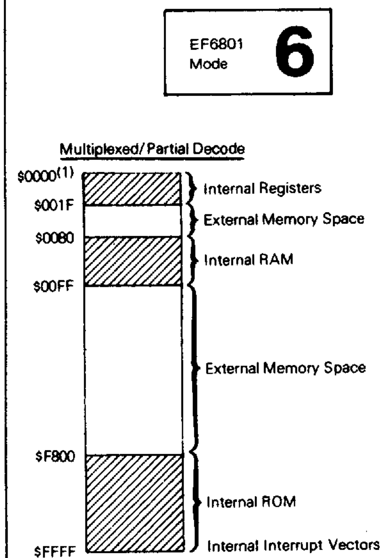
Mode 3 (Multiplexed/No RAM or ROM) — NOTES:
1) Excludes the following addresses which may be used externally: $04, $05, $06, $07, and $0F.

Mode 4 (Single-Chip Test) — NOTES:
1) The internal ROM is disabled.
2) Mode 4 may be changed to Mode 5 without having to assert $\overline{RESET}$ by writing a one into the PCO bit of the port 2 data register.
3) Addresses A8 to A15 are treated as "don't cares" to decode internal RAM.
4) Internal RAM will appear at $XX80 to $XXFF.

Figure 15 : 6801/6803 memory maps (sheet 2 of 3).



NOTES:
1) Excludes the following addresses which may not be used externally: $04, $06, and $0F (no $\overline{IOS}$).
2) This mode may be entered without going through $\overline{RESET}$ by using mode 4 and subsequently writing a one into the PCO bit of the port 2 data register.
3) Address lines A0 to A7 will not contain addresses until the data direction register for port 4 has been written with ones in the appropriate bits. These address lines will assert ones until made outputs by writing the data direction register.



NOTES:
1) Excludes the following addresses which may be used externally: $04, $06, and $0F
2) Address lines A8-A15 will not contain addresses until the data direction register for port 4 has been written with ones in the appropriate bits. These address lines will assert ones until made outputs by writing the data direction register.

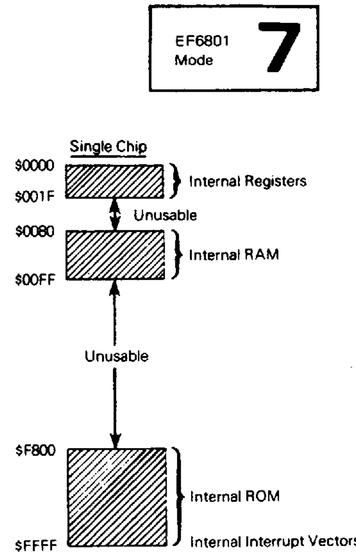


Figure 15 : 6801/6803 memory maps (sheet 3 of 3).

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6.3 - 6801/6803 interrupts

The 6801 Family supports two types of interrupt requests : maskable and non-maskable. A Non-Maskable interrupt (NMI) is always recognized and acted upon at the completion of the current instruction. Maskable interrupts are controlled by the Condition Code Register I-bit and by individual enable bits. The I-bit controls all maskable interrupts. Of the maskable interrupts, there are two types : IRQ1 and IRQ2. The Programmable Timer and Serial Communications Interface use an internal IRQ2 interrupt line, as shown in Figure 1. External devices (and IS3) use IRQ1. An IRQ1 interrupt is serviced before IRQ2 if both are pending.

All IRQ2 interrupts use hardware prioritized vectors. The single SCI interrupt and three timer interrupts are serviced in a prioritized order and each is vectored to a separate location. All interrupt vector locations are shown in Table 12.

The Interrupt flowchart is depicted in Figure 16 and is common to every interrupt excluding reset. During interrupt servicing the Program Counter, Index Register, A Accumulator, B Accumulator, and Condition Code Register are pushed to the stack. The I-bit is set to inhibit maskable interrupts and a vector is fetched corresponding to the current highest priority interrupt. The vector is transferred to the Program Counter and instruction execution is resumed. Interrupt and RESET timing are illustrated in Figures 17 and 18.

6.4 - Functional pin descriptions

V_{CC} and V_{SS}

V_{CC} and V_{SS} provide power to a large portion of the MCU. The power supply should provide +5 volts (±5 %) to V_{CC}, and V_{SS} should be tied to ground. Total power dissipation (including V_{CC} Standby), will not exceed P_D milliwatts.

V_{CC} Standby

V_{CC} Standby provides power to the standby portion ($80 through $BF) of the RAM and the STBY PWR and RAME bits of the RAM Control Register. Voltage requirements depend on whether the device is in a powerup or powerdown state. In the power-up state, the power supply should provide +5 volts (±5 %) and must reach V_{SB} volts before RESET reaches 4.0 volts. During powerdown, V_{CC} standby must remain above V_{SBB} (min) to sustain the standby RAM and STBY PWR bit. While in powerdown operation, the standby current will not exceed I_{SBB}.

It is typical to power both V_{CC} and V_{CC} Standby from the same source during normal operation. A diode must be used between them to prevent supplying power to V_{CC} during powerdown operation. V_{CC} Standby should be tied to ground in Mode 3.

Table 11 - Internal register area

Register	Address
Port 1 Data Direction Register***	00
Port 2 Data Direction Register***	01
Port 1 Data Register	02
Port 2 Data Register	03
Port 3 Data Direction Register***	04*
Port 4 Data Direction Register***	05**
Port 3 Data Register	06*
Port 4 Data Register	07**
Timer Control and Status Register	08
Counter (High Byte)	09
Counter (Low Byte)	0A
Output Compare Register (High Byte)	0B
Output Compare Register (Low Byte)	0C
Input Capture Register (High Byte)	0D
Input Capture Register (Low Byte)	0E
Port 3 Control and Status Register	0F*
Rate and Mode Control Register	10
Transmit/Receive Control and Status Register	11
Receive Data Register	12
Transmit Data Register	13
RAM Control Register	14
Reserved	15-1F

*External addresses in Modes 0, 1, 2, 3, 5, 6; cannot be accessed in Mode 5 (No IOS)
**External addresses in Modes 0, 1, 2, 3
***1 = Output, 0 = Input

Table 12 - MCU interrupt vector locations

MSB	LSB	Interrupt
FFFE	FFFF	RESET
FFFC	FFFD	NMI
FFFA	FFFB	Software Interrupt (SWI)
FFF8	FFF9	IRQ1 (or IS3)
FFF6	FFF7	ICF (Input Capture)*
FFF4	FFF5	OCF (Output Compare)*
FFF2	FFF3	TOF (Timer Overflow)*
FFF0	FFF1	SCI (RDRF + ORFE + TDRE)*

*IRQ2 Interrupt

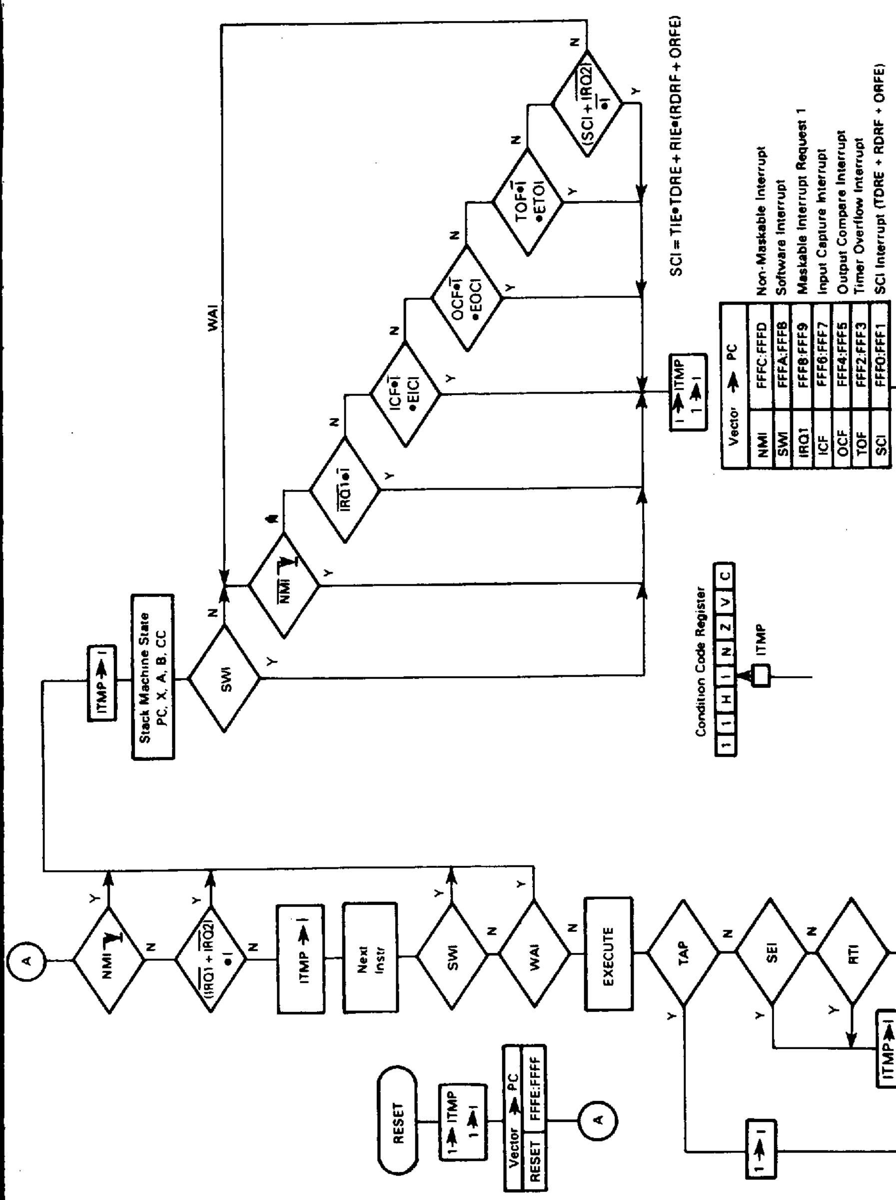

Figure 16 : Interrupt flowchart.

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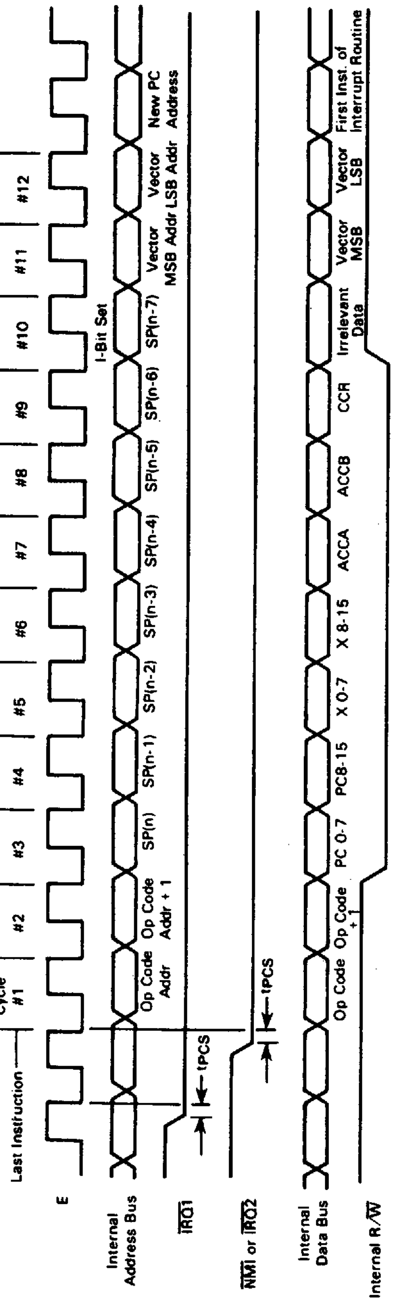


Figure 17 : Interrupt sequence.

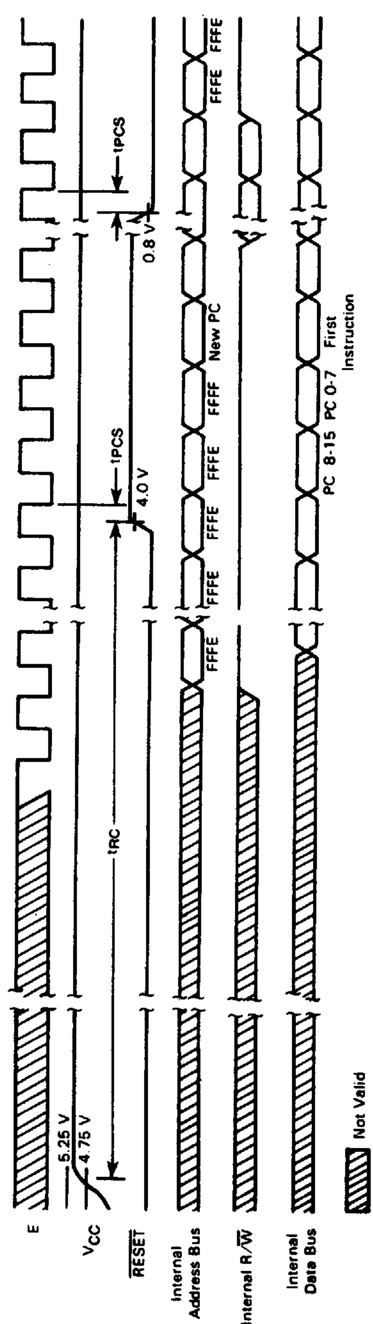


Figure 18 : Reset timing.

XTAL1 and EXTAL2

These two input pins interface either a crystal or TTL compatible clock to the MCU internal clock generator. Divide-by-four circuitry is included which allows use of the inexpensive 3.58 MHz or 4.4336 MHz Color Burst TV crystals. A 20 pF capacitor should be tied from each crystal pin to ground to ensure reliable startup and operation. Alternatively, EXTAL2 may be driven by an external TTL compatible clock at $4f_0$ with a duty cycle of 50 % (± 5 %) with XTAL1 connected to ground.

The internal oscillator is designed to interface with an AT-cut quartz crystal resonator operated in parallel resonance mode in the frequency range specified for f_{XTAL}. The cristal should be mounted as close as possible to the input pins to minimize output distortion and startup stabilization time*. The MCU is compatible with most commercially available crystals. Nominal crystal parameters are shown in Figure 19.

$\overline{RESET}$

This input is used to reset the internal state of the device and provide an orderl startup procedure. During powerup, $\overline{RESET}$ must be held below 0.8 volts : (1) at least t_{RC} after V_{CC} reaches 4.75 volts in order to provide sufficient time for the clock generator to stabilize, and (2) until V_{CC} Standby reaches 4.75 volts. $\overline{RESET}$ must be held low at least three E-cycles if asserted during powerup operation.

E (Enable)

This is an output clock used primarily for bus synchronization. It is TTL compatible and is the slightly skewed divide-by-four result of the device input clock frequency. It will drive one Schottky TTL load and 90 pF, and all data given in cycles is referenced to this clock unless otherwise noted.

$\overline{NMI}$ (Non-Maskable-Interrupt)

An $\overline{NMI}$ negative edge requests an MCU interrupt sequence, but the current instruction will be completed before it responds to the request. The MCU will then begin an interrupt sequence. Finally, a vector is fetched from $FFFC and $FFFD, transferred to the Program Counter and instruction execution is resumed. $\overline{NMI}$ typically requires a 3.3 kΩ (nominal) resistor to V_{CC}. There is no internal $\overline{NMI}$ pullup resistor. $\overline{NMI}$ must be held low for at least one E-cycle to be recognized under all conditions.

$\overline{IRQ1}$ (Maskable interrupt request 1)

$\overline{IRQ1}$ is a level-sensitive input which can be used to request an interrupt sequence. The MPU will complete the current instruction before it responds to the request. If the interrupt mask bit (I-bit) in the Condition Code Register is clear, the MCU will begin an interrupt sequence. A vector is fetched from $FFF8 and $FFF9, transferred to the Program Counter, and instruction execution is resumed.

$\overline{IRQ1}$ typically requires an external 3.3 KΩ (nominal) resistor to V_{CC} for wire-OR applications. $\overline{IRQ1}$ has no internal pullup resistor.

SC1 and SC2 (strobe control 1 and 2)

The function of SC1 and SC2 depends on the operating mode. SC1 is configured as an output in all modes except single chip mode, whereas SC2 is always an output. SC1 and SC2 can drive one Schottky load and 90 pF.

SC1 and SC2 in Single-Chip Mode

In Single-Chip Mode, SC1 and SC2 are configured as an input and output, respectively, and both function as Port 3 control lines. SC1 functions as $\overline{IS3}$ and can be used to indicate that Port 3 input data is ready or output data has been accepted. Three options associated with $\overline{IS3}$ are controlled by Port 3 Control and Status Register and are discussed in the Port 3 description. If unused, $\overline{IS3}$ can remain unconnected.

SC2 is configured as $\overline{OS3}$ and can be used to strobe output data or acknowledge input data or acknowledge input data. It is controlled by Output Strobe Select (OSS) in the Port 3 Control and Status Register. The strobe is generated by a read (OSS = 0) or write (OSS = 1) to the Port 3 Data Register.

SC1 and SC2 in Expanded Non-Multiplexed Mode

In the Expanded Non-Multiplexed Mode, both SC1 and SC2 are configured as outputs. SC1 functions as Input/Output Select ($\overline{IOS}$) and is asserted only when $0100 throuGh $01FF is sensed on the internal address bus.

SC2 is configured as Read/Write and is used to control the direction of data bus transfers. An MPU read is enabled when Read/Write and E are high.

SC1 and SC2 in Expanded Multiplexed Mode

In the Expanded Multiplexed Modes, both SC1 and SC2 are configured as outputs. SC1 functions as Address Strobe and can be used to demultiplex the eight least significant addresses and the data bus. A latch controlled by Address Strobe captures address on the negative edge, as shown in Figure 13.

SC2 is configured as Read/Write and is used to control the direction of data bus transfers. An MPU read is enabled when Read/Write and E are high.

P10-P17 (Port 1)

Port 1 is a mode independent 8-bit I/O port with each line an input or output as defined by the Port 1 Data Direction Register. The TTL compatible three-state output buffers can drive on Schottky TTL load and 30 pF, Darlington transistors, or CMOS devices using external pullup resistors. It is configured as a data input port by $\overline{RESET}$. Unused lines can remain unconnected.

P20-P24 (Port 2)

Port 2 is a mode-independent, 5-bit, multipurpose I/O port. The voltage levels present on P20, P21, and P22 on the rising edge of $\overline{RESET}$ determine the operating mode of the MCU. The entire port is then configured as a data input port. The Port 2 lines can be selectively configured as a data output lines by setting the appropriate bits in the Port 2 Data Direction Register. The Port 2 Data Register is used to move data through the port. However, if P21 is configured as an output, it will be tied to the Timer Output Compare function and cannot be used to provide output from the Port 2 Data Register.

Port 2 can also be used to provide an interface for the Serial Communications Interface and the timer Input Edge function. These configurations are described in the Programmable Timer and Serial Communications Interface (SCI) section.

The Port 2 three-state, TTL-compatible output buffers are capable of driving one Schottky TTL load and 30 pF, or CMOS devices using external pullup resistors.

PORT 2 DATA REGISTER

7	6	5	4	3	2	1	0	
PC2	PC1	PC0	P24	P23	P22	P21	P20	$0003

(a) Nominal Recommended Crystal Parameters

Nominal Crystal Parameters*

	3.58 MHz	4.00 MHz	5.0 MHz	6.0 MHz	8.0 MHz
RS	60 Ω	50 Ω	30-50 Ω	30-50 Ω	20-40 Ω
C_0	3.5 pF	6.5 pF	4-6 pF	4-6 pF	4-6 pF
C_1	0.015 pF	0.025 pF	0.01-0.02 pF	0.01-0.02 pF	0.01-0.02 pF
Q	>40 K	>30 K	>20 K	>20 K	>20 K

*NOTE: These are representative AT-cut crystal parameters only. Crystals of other types of cut may also be used.

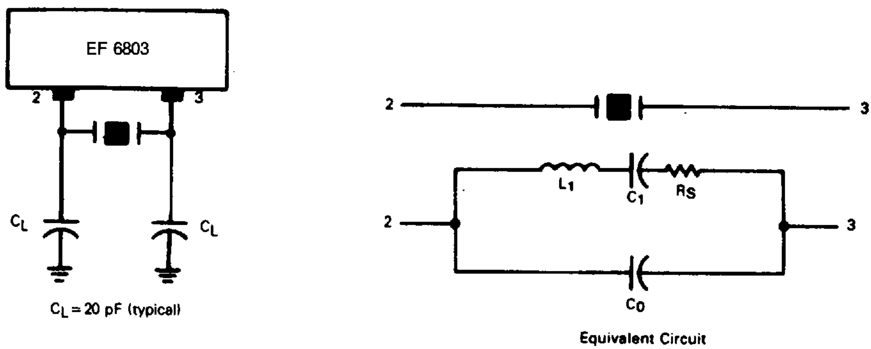


Figure 19 : 6801/6803 oscillator characteristics
a) Nominal recommanded crystal parameters.

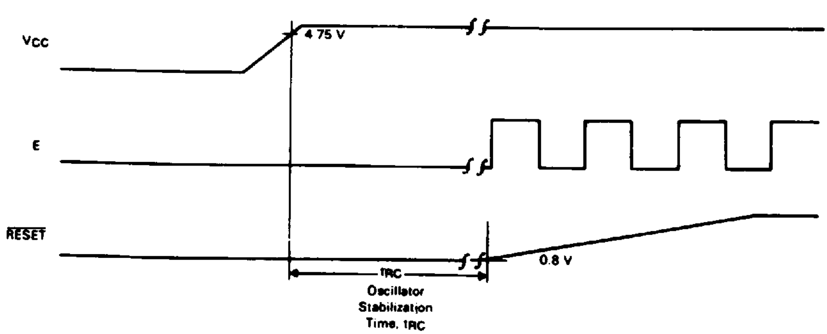


Figure 19 : 6801/6803 oscillator characteristics
b) Oscillator stabilization time (t_{RC}).

P30-P37 (Port 3)
Port 3 can be configured as an I/O port, a bidirectional 8-bit data bus, or a multiplexed address/data bus depending on the operating mode. The TTL compatible three-state output buffers can drive on Schottky TTL load and 90 pF. Unused lines can remain unconnected.

Port 3 In Single-Chip Mode
Port 3 is an 8-bit I/O port in the Single-Chip Mode, with each line configured by the Port 3 Data Direction Register. There are also two lines, $\overline{IS3}$ and $\overline{OS3}$, which can be used to control Port 3 data transfers.

Three Port 3 options are controlled by the Port 3 Control and Status Register and are available only in Single-Chip Mode : (1) Port 3 input data can be latched using IS3 as a control signal, (2) $\overline{OS3}$ can be generated by either an MPU read or write to the Port 3 Data Register, and (3) an $\overline{IRQ1}$ interrupt can be enabled by an $\overline{IS3}$ negative edge.

Port 3 control and status register

7	6	5	4	3	2	1	0	
IS3 Flag	IS3 IRQ1 Enable	X	OSS	Latch Enable	X	X	X	$000F

Bit 0-2 not used.

Bit 3 LATCH ENABLE. This bit controls hte input latch for Port 3. If set, input data is latched by an $\overline{IS3}$ negative edge. The latch is transparent after a read of the Port 3 Data Register. LATCH ENABLE is cleared during reset.

Bit 4 OSS (Output Strobe Select). This bit determines whether $\overline{OS3}$ will be generated by a read or write of the Port 3 Data Register. When clear, the strobe is generated by a read ; when set, it is generated by a write. OSS is cleared during reset.

Bit 5 Not used.

Bit 6 IS3 IRQ1 ENABLE. When set, an $\overline{IRQ1}$ interrupt will be enabled whenever IS3 FLAG is set ; when clear, the interrupt is inhibited. This is cleared during reset.

Bit 7 IS3 FLAG. This read-only status bit is set by an $\overline{IS3}$ negative edge. It is cleared by a read of the Port 3 Control and Status Register (with IS3 FLAG set) followed by a read or write to the Port 3 Data Register or during reset.

Port 3 In Expanded Non-Multiplexed Mode
Port 3 is configured as a bidirection data bus (D7-D0) in the Expanded Non-Multiplexed Mode. The direction of data transfers is controlled by Read/Write (SC2). Data is clocked by E (Enable).

Port 3 In Expanded Multiplexed Mode
Port 3 is configured as a time multiplexed address (A0-A7) and data bus (D7-D0) in the Expanded Multiplexed Modes, where Address Strobe (AS) can be used to demultiplex the two buses. Port 3 is held in a high impedance state between valid address and data to prevent bus conflicts.

P40-P47 (Port 4)
Port 4 is configured as an 8-bit I/O port, as address outputs, or as data inputs depending on the operating mode. Port 4 can drive on Schottky TTL load and 90 pF and is the only port with internal pullup resistors. Unused lines can remain unconnected.

Port 4 In Single-Chip Mode
In Single-Chip Mode, Port 4 functions as an 8-bit I/O port with each line configured by the Port 4 Data Direction Resgister. Internal pullup resistors allow the port to directly interface with CMOS at 5 volt levels. External pullup resistors to more than 5 volts, however, cannot be used.

Port 4 In Expanded Non-Multiplexed Mode
Port 4 is configured from reset as an 8-bit input port, where the Port 4 Data Direction Register can be written to provide any or all of eight address lines, A0 to A7. Internal pullup resistors pull the lines high until the Port 4 Data Direction Register is configured.

Port 4 In Expanded Multiplexed Mode
In all Expanded Multiplexed modes except Mode 6, Port 4 functions as half of the address bus and provides A8 to A15. In Mode 6, the port is configured from reset as an 8-bit parallel input port, where the Port 4 Data Direction Register can be written to provide any or all of upper address lines A8 to A15. Internal pullup resistors pull the lines high until the Port 4 Data Direction Register is configured, where bit 0 controls A8.

RAM control register ($14)
The RAM Control Register includes two bits which can be used to control RAM accesses and determine the adequacy of the standby power source during powerdown operation. It is intended that RAME be cleared and STBY PWR be set as part of a powerdown procedure.

6.5 - RAM control register

7	6	5	4	3	2	1	0
STBY PWR	RAME	X	X	X	X	X	X

Bit 0-5 Not used.

Bit 6 RAME RAM Enable. This read/write bit can be used to remove the entire RAM from the internal memory map. RAME is set (enabled) during reset provided standby power is available on the positive edge of $\overline{RESET}$. If RAME is set and not in mode 3, the RAM is clear, any access to a RAM address is external. If RAM is included in the internal map.

Bit 7 STBY PWR Standby Power. This bit is a read/write status bit which, when once set, remains set as long as V_{CC} standby remains above V_{SBB} (minimum). As long as this bit is set following a period of standby operation, the standby power supply has adequately preserved the data in the standby RAM. If this bit is cleared during a period of standby operation, it indicates that V_{CC} standby had fallen to a level sufficiently below V_{SBB} (minimum) to suspect that data in the standby RAM is not valid. This bit can be set only by software and is not affected during reset.

6.6 · Programmable timer

The programmable timer can be used to perform input waveform measurements while independently generating an output waveform. Pulse widths can vary from several microseconds to many seconds. A block diagram of the timer is shown in Figure 20.

Counter ($09:0A)

The key timer element is a 16-bit free-running counter which is incremented by E (enable). It is cleared during reset and is read-only with one exception : a write to the counter ($09) will preset it to $FFF8. This feature, intended for testing, can disturb serial operations because the counter provides the SCI internal bit rate clock. TOF is set whenever the counter contains all ones.

Output compare register ($0B:0C)

The output compare register is a 16-bit read/write register used to control an output waveform or provide ar arbitrary timeout flag. It is compared with the free-running counter on each E cycle. When a match occurs, OCF is set and OLVL is clocked to an output level register. If port 2, bit 1, is configured as an output, OLVL will appear at P21 and the output compare register and OLVL can then be changed for the next and OLVL is clocked to an output level register. If Port 2, bit 1, is configured as an output, OLVL will appear at P21 and the Output Compare Register and OLVL can then be changed for the next compare. The function is inhibited for one cycle after a write to its high byte ($0B) to ensure a valid compare. The Output Compare Register is set to $FFF at $\overline{RESET}$.

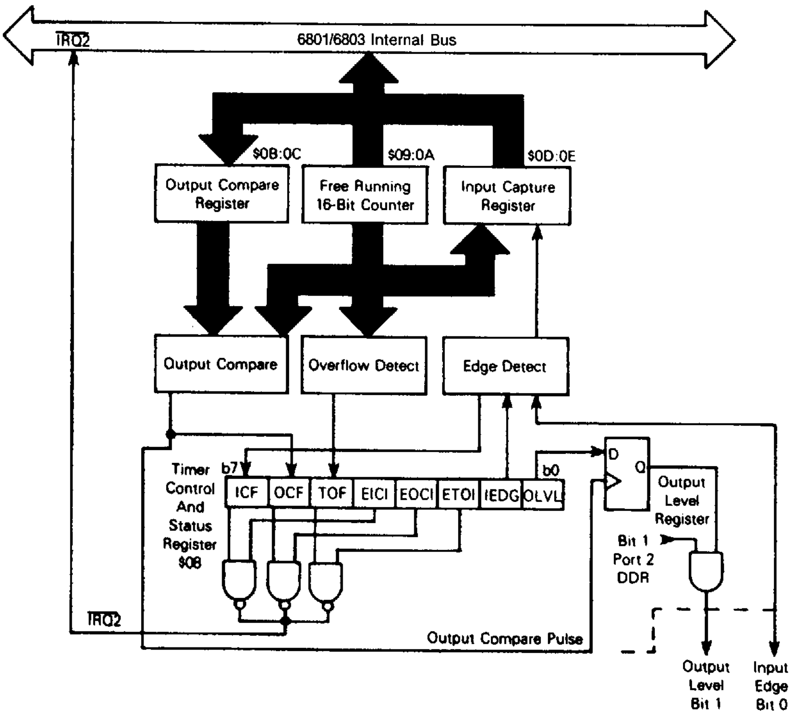


Figure 20 : Block diagram of programmable timer.

nput capture register ($0D:0E)
he Input Capture Register is a 16-bit read-only register used to store the free-running counter when a «proper» input transition ccurs as defined by IEDG. Port 2, bit 0 should be configured as an input, but the edge detect circuit always senses P20 even hen configured as an output. An input capture can occur independently of ICF : the register always contains the most current alue. Counter transfer is inhibited, however, between accesses of a double byte MPU read. The input pulse width must be at east two E-cycles to ensure an input capture under all conditions.

imer control and status register ($08)
he Timer Control and Status Register (TCSR) is an 8-bit register of which all bits readable, while only bits 0-4 can be written. he three most significant bits provide the timer status and indicate if :
- a proper level transition has been detected,
- a match has occured between the free-running counter and the output compare register,
- the free-running counter has overflowed.

ach of the three events can generate an $\overline{IRQ2}$ interrupt and is controlled by an individual enable bit in the TCSR.

imer Control and Status Register (TCSR)

7	6	5	4	3	2	1	0	
ICF	OCF	TOF	EICI	EOCI	ETOI	IEDG	OLVL	$0008

3it 0 OLVL Output level, OLVL is clocked to the output level register by a successful output compare and will appear at P21 if Bit 1 of the Port 2 Data Direction Register is set. It is cleared during reset.

3it 1 EIDG Input Edge, IEDG is cleared during reset and controls which level transition will trigger a counter transfer to the Input Capture Register.
IEDG = 0 Transfer on a negative-edge
IEDG = 1 Transfer on a positive-edge.

3it 2 ETOI Enable Timer Overflow Interrupt. When set, an $\overline{IRQ2}$ interrupt is enabled for a timer overflow ; when clear, the interrupt is inhibited. It is cleared during reset.

3it 3 EOCI Enable Output Compare Interrupt. When set, an $\overline{IRQ2}$ interrupt is enabled for an output compare ; when clear, the interrupt is inhibited. It is cleared during reset.

3it 4 EICI Enable Input Capture Interrupt. When set, an $\overline{IRQ2}$ interrupt is enabled for an input capture ; when clear, the interrupt is inhibited. It is cleared during reset.

3it 5 TOF Timer Overflow Flag. TOF is set when the counter contains all 1's. It is cleared by reading the TCSR (with TOF set) then reading the counter high byte ($09), or during reset.

3it 6 OCF Output Compare Flag. OCF is set when the Output Compare Register matches the free-running counter. It is cleared by reading the TCSR (with OCF set) and then writing to the Output Compare Register ($0B or $0C), or during reset.

3it 7 ICF Input Capture Flag. ICF is set to indicate a proper level transition ; it is cleared by reading the TCSR (with ICF set) and then the input Capture Register High Byte ($0D), or during reset.

.7 - Serial Communications Interface (SCI)
 full-duplex asynchronous Serial Communications Interface (SCI) is provided with two data formats and a variety of rates. The CI transmitter and receiver are functionally independent, but use the same data format and bit rate. Serial data formats inlude standard mark/space (NRZ) and Bi-phase and both provide one start bit, eight data bits, and one stop bit. «Baud» and «bit ate» are used synonymously in the following description.

Vake-up feature
n a typical serial loop multi-processor configuration, the software protocol will usually identify the addressee(s) at the beginning of the message. In order to permit uninterested MPU's to ignore the remainder of the message, a wake-up feature is included whereby all further SCI receiver flag (and interrupt) processing can be inhibited until its data line goes idle. An SCI receiver s re-enabled by an idle string of ten consecutive 1's or during reset. Software must provide for the required idle string between onsecutive messages and prevent it within messages.

rogrammable options
he following features of the SCI are programmable :
- format : standard mark/space (NRZ) or Bi-phase,
- clock : external or internal bit rate clock,
- baud : one of 4 per E-clock frequency, or external clock (×8 desired baud),
- wake-up feature : enabled or disabled,
- interrupt requests : enabled individually for transmitter and receiver,
- clock output : internal bit rate clock enabled or disabled to P22.

erial communications registers
he Serial Communications Interface includes four addressable registers as depicted in Figure 21. It is controlled by the Rate nd Mode Control Register and the Transmit/Receive Control and Status Register. Data is transmitted and received utilizing write-only Transmit Register and a read-only Receive Register. The shift registers are not accessible to software.

ate and Mode Control Register (RMCR) ($10)
he Rate and Mode Control Register controls the SCI bit rate, format, clock source, and under certain conditions, the configuation of P22. The register consists of four write-only bits which are cleared during reset. The two least significant bits control he bit rate of the internal clock and the remaining two bits control the format and clock source.

6.8 · Rate and Mode Control Register (RMCR)

7	6	5	4	3	2	1	0	
X	X	X	X	CC1	CC0	SS1	SS0	$0010

Bit 1:Bit 0 SS1:SS0 Speed Select. These two bits select the Baud rate when using, the internal clock. Four rates may be se lected which are a function of the MCU input frequency. Table 13 lists bit time and rates for three selected MC frequencies.

Bit 3:Bit 2 CC1:CC0 Clock Control and Format Select. These two bits control the format and select the serial clock source If CC1 is set, the DDR value for P22 is forced to the complement of CC0 and cannot be altered until CC1 is clea red. If CC1 is cleared after having been set, its DDR value is unchanged. Table 14 defines the formats, clock sou ce, and use of P22.

If both CC1 and CC0 are set, an external TTL compatible clock must be connected to P22 at eight times (8X) the desired bi rate, but not greater than E, with a duty cycle of 50 % (± 10 %). If CC1:CC0 = 10, the internal bit rate clock is provided at P2 regardless of the values for TE or RE.

Note : The source of SCI internal bit rate clock is the timer free running counter. An MPU write to the counter can disturb serial opera tions.

Transmit / Receive Control and Status Register (TRCSR) ($11)

The Transmit / Receive Control and Status Register controls the transmitter, receiver, wake-up feature, and two individual inte rupts and monitors the status of serial operations. All eight bits are readable while bits 0 to 4 are also writable. The registe is initialized to $20 by RESET.

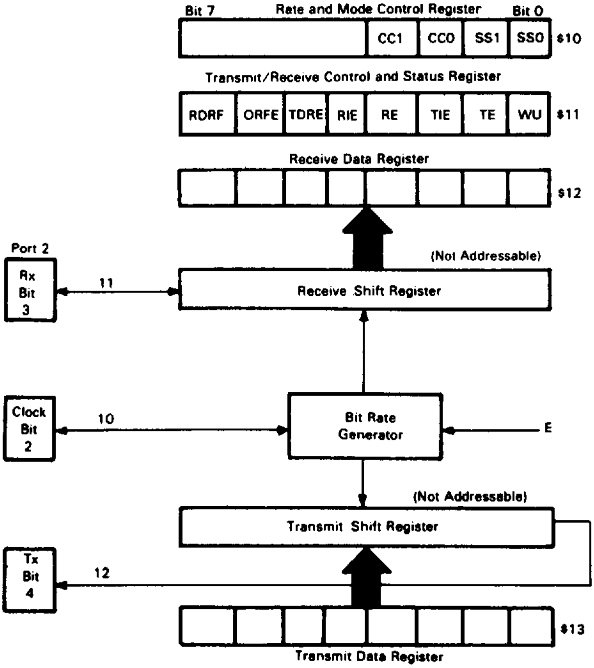


Figure 21 : SCI registers.

.9 - Transmit/Receive Control and Status Register (TRCSR)

7	6	5	4	3	2	1	0	
RDRF	ORFE	TDRE	RIE	RE	TIE	TE	WU	$0011

Bit 0 WU «Wake-up» on Idle Line. When set, WU enables the wake-up function ; it is cleared by ten consecutive 1's or during reset. WU will not set if the line is idle.

Bit 1 TE Transmit Enable. When set, P24 DDR bit is set, cannot be changed, and will remain set if TE is subsequently cleared. When TE is changed from clear to set, the transmitter is connected to P24 and a preamble of nine consecutive 1's is transmitted. TE is cleared during reset.

Bit 2 TIE Transmit Interrupt Enable. When set, an $\overline{IRQ2}$ interrupt is enabled when TDRE is set ; when clear, the interrupt in inhibited. TE is cleared during reset.

Bit 3 RE Receive Enable. When set, the P23 DDR bit is cleared, cannot be changed, and will remain clear if RE is subsequently cleared. While RE is set, the SCI receiver is enabled. RE is cleared during reset.

BIT 4 RIE Receiver Interrupt Enable. When set, an $\overline{IRQ2}$ interrupt is enabled when RDRF and/or ORFE is set ; when clear, the interrupt is inhibited, RIE is cleared during reset.

Bit 5 TDRE Transmit Data Register Empty. TDRE is set when the Transmit Data Register is transferred to the output serial shift register or during reset. It is cleared by reading the TRCSR (with TDRE set) and then writing to the Transmit Data Register. Additional data will be transmitted only if TDRE has been cleared.

Bit 6 ORFE Overrun Framing Error. If set, ORFE indicates either an overrun or framing error. An overrun is a new byte ready to transfer to the Receiver Data Register with RDRF still set. A receiver framing error has occured when the byte boundaries of the bit stream are not synchronized to the bit counter. An overrun can be distinguished from a framing error by the state of RDRF : if RDRF is set, then an overrun has occurred ; otherwise a framing error is transferred to the Receive Data Register in an overrun condition. Unframed data causing a framing error has been detected. Data is not transferred to the Receive Data Register. However, subsequent data transfer is blocked until the framing error flag is cleared*. ORFE is cleared by reading the TRCSR (with ORFE set) then the Receive Data Register, or during reset.

Bit 7 RDRF Receive Data Register Full. RDRF is set when the input serial shift register is transferred to the Receive Data Register. It is cleared by reading the TRCSR (with RDRF set), and then the Receive Data Register, or during reset.

5

Table 13 - SCI bit times and rates

SS1:SS0		4f₀→ / E	2.4576 MHz / 614.4 kHz	4.0 Mhz / 1.0 MHz	4.9152 MHz / 1.2288 MHz
0	0	÷ 16	26 μs/38,400 Baud	16 μs/62,500 Baud	13.0 μs/76,800 Baud
0	1	÷ 128	208 μs/4,800 baud	128 μs/7812.5 Baud	104.2 μs/9,600 Baud
1	0	÷ 1024	1.67 ms/600 Baud$	1.024 ms/976.6 Baud	833.3 μs/1,200 Baud
1	1	÷ 4096	6.67 ms/150 Baud	4.096 ms/244.1 Baud	3.33 ms/300 Baud
*External (P22)			13.0 μs/76,800 Baud	8.0 μs/125,000 Baud	6.5 μs/153,600 Baud

*Using maximum clock rate

Table 14 - SCI format and clock source control

CC1:CC0	Format	Clock Source	Port 2 Bit 2
00	Bi-Phase	Internal	Not Used
01	NRZ	Internal	Not Used
10	NRZ	Internal	Output
11	NRZ	External	Input

Serial operations
The SCI is initialized by writing control bytes first to the Rate and Mode Control Register and then to the Transmit/Receive Co trol and Status Register. When TE is set, the output of the transmit serial shift register is connected to P24 and serial outp is initiated by transmitting a 9-bit preamble of 1's.

At this point one of two situations exist :
– if the Transmit Data Register is empty (TDRE = 1), a continuous string of 1's will be sent indicating an idle line, or
– if a byte has been written to the Transmit-Data Register (TDRE = 0), it will be transferred to the output serial shift regist (synchronized with the bit rate clock), TDRE will be set, and transmission will begin.

The start bit (0), eight data bits (beginning with bit 0) and a stop bit (1), will be transmitted. If TDRE is still set when the ne byte transfer should occur, 1's will be sent until more data is provided. In Bi-phase format, the output toggles at the start each bit and at half-bit time when a «1» is sent. Receive operation is controlled by RE which configures P23 as an input a enables the receiver. SCI data formats are illustrated in Figure 22.

6.10 · Instruction set

The EF 6803 is upward source and object code compatible with the EF 6800. Execution times of key instructions have been r duced and several new instructions have been added, including a hardware multiply. A list of new operations added to th EF 6800 instruction set is shown in Table 8.

In addition, two new special opcodes, 4E and 5E, are provided for test purposes. These opcodes force the Program Count to increment like a 16-bit counter, causing address lines used in the expanded modes to increment until the device is res These opcodes have no mnemonics.

The coding of the first (or only) byte corresponding to an executable is sufficient to identify the instruction and the addressin mode. The hexadecimal equivalents of the binary codes, which result from the translation of the 82 instructions in all vali modes of addressing, are shown in Table 15. There are 220 valid machine codes, 34 unassigned codes, and 2 codes reserve for test purposes.

6.10.1 · Programming model

A programming model for the EF 6803 is shown in Figure 9. Accumulator A can be concatenated with accumulator B and joi tly referred ti as accumulator D where A is the most significant byte. Any operation which modifies the double accumulat will also modify accumulator A and/or B. Other registers are defined as follows :

Program counter : The program counter is a 16-bit register which always points to the next instruction.

Stack pointer : The stack pointer is a 16-bit register which contains the address of the next available location in a pushdow pullup (LIFO) queue. The stack resides in random access memory at a location defined by the programmer.

Index register : Th Index Register is a 16-bit register which can be used to store data or provide an address for the indexe mode of addressing.

Accumulators : The MPU contains two 8-bit accumulators, A and B, which are used to store operands and results from th arithmetic logic unit (ALU). They can also be concatenated and referred to as the D (double) accumulator.

Condition Code Registers : The condition code register indicates the results of an instruction and includes the following fiv condition bits : Negative (N), Zero (Z), Overflow (V), Carry/Borrow from MSB (C), and Half Carry from bit 3 (H). These bits are te table by the conditional branch instructions. Bit 4 is the interrupt mask (I-bit) and inhibits all maskable interrupts when set. Th two unused bits B6 and B7, are read as ones.

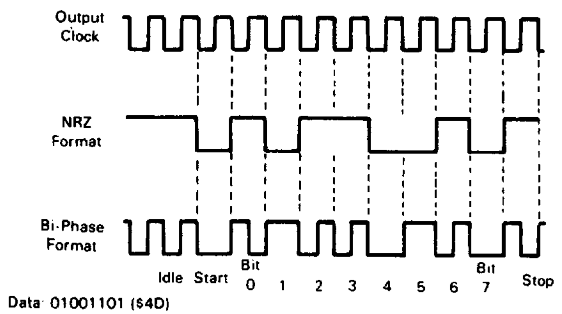


Figure 22 : SCI data formats.

6.10.2 - Addressing modes

Six addressing modes can be used to reference memory. A summary of addressing modes for all instructions is presented in Tables 16, 17, 18 and 19, where execution times are provided in E-cycles. Instructions execution times are summarized in Table 20. With an input frequency of 4 MHz, E-cycles are equivalent to microseconds. A cycle-by-cycle description of bus activity for each instruction is provided in Table 21 and a description of selected instructions is shown in Figure 23.

Immediate Addressing : The operand or «immediate byte(s)» is contained in the following byte(s) of the instruction where the number of bytes matches the size of the register. These are two or three byte instructions.

Direct Addressing : The least significant byte of the operand address is contained in the second byte of the instruction and the most significant byte is assumed to be $00. Direct addressing allows the user to access $00 through $FF using two byte instructions and execution time is reduced by eliminating the additional memory access. In most applications, the 256-byte area is reserved for frequently referenced data.

Extended Addressing : The second and third bytes of the instruction contain the absolute address of the operand. These are three byte instructions.

Indexed Addressing : The unsigned offset contained in the second byte of the instruction is added with carry to the Index Register and used to reference memory without changing the Index Register. These are two byte instructions.

Inherent Addressing : The operand(s) are registers and no memory reference is required. These are single byte instructions.

Relative Addressing : Relative addressing is used only for branch instructions. If the branch condition is true, the Program Counter is overwritten with the sum of a signed single byte displacement in the second byte of the instruction and the current Program Counter. This provides a branch range of −126 to 129 bytes from the first byte of the instruction. These are two byte instructions.

Table 15 - CPU instruction map

OP	MNEM	MODE	~	#
00	*			
01	NOP	INHER	2	1
02	*			
03	*			
04	LSRD		3	1
05	ASLD		3	1
06	TAP		2	1
07	TPA		2	1
08	INX		3	1
09	DEX		3	1
0A	CLV		2	1
0B	SEV		2	1
0C	CLC		2	1
0D	SEC		2	1
0E	CLI		2	1
0F	SEI		2	1
10	SBA		2	1
11	CBA		2	1
12	*			
13	*			
14	*			
15	*			
16	TAB		2	1
17	TBA		2	1
18	*			
19	DAA	INHER	2	1
1A	*			
1B	ABA	INHER	2	1
1C	*			
1D	*			
1E	*			
1F	*			
20	BRA	REL	3	2
21	BRN		3	2
22	BHI		3	2
23	BLS		3	2
24	BCC		3	2
25	BCS		3	2
26	BNE		3	2
27	BEQ		3	2
28	BVC		3	2
29	BVS		3	2
2A	BPL		3	2
2B	BMI		3	2
2C	BGE		3	2
2D	BLT		3	2
2E	BGT		3	2
2F	BLE	REL	3	2
30	TSX	INHER	3	1
31	INS		3	1
32	PULA		4	1
33	PULB		4	1

OP	MNEM	MODE	~	#
34	DES	INHER	3	1
35	TXS		3	1
36	PSHA		3	1
37	PSHB		3	1
38	PULX		5	1
39	RTS		5	1
3A	ABX		3	1
3B	RTI		10	1
3C	PSHX		4	1
3D	MUL		10	1
3E	WAI		9	1
3F	SWI		12	1
40	NEGA		2	1
41	*			
42	*			
43	COMA		2	1
44	LSRA		2	1
45	*			
46	RORA		2	1
47	ASRA		2	1
48	ASLA		2	1
49	ROLA		2	1
4A	DECA		2	1
4B	*			
4C	INCA		2	1
4D	TSTA		2	1
4E	T			
4F	CLRA		2	1
50	NEGB		2	1
51	*			
52	*			
53	COMB		2	1
54	LSRB		2	1
55	*			
56	RORB		2	1
57	ASRB		2	1
58	ASLB		2	1
59	ROLB		2	1
5A	DECB		2	1
5B	*			
5C	INCB		2	1
5D	TSTB		2	1
5E	T			
5F	CLRB	INHER	2	1
60	NEG	INDXD	6	2
61	*			
62	*			
63	COM		6	2
64	LSR		6	2
65	*			
66	ROR		6	2
67	ASR	INDXD	6	2

OP	MNEM	MODE	~	#
68	ASL	INDXD	6	2
69	ROL		6	2
6A	DEC		6	2
6B	*			
6C	INC		6	2
6D	TST		6	2
6E	JMP		3	2
6F	CLR	INDXD	6	2
70	NEG	EXTND	6	3
71	*			
72	*			
73	COM		6	3
74	LSR		6	3
75	*			
76	ROR		6	3
77	ASR		6	3
78	ASL		6	3
79	ROL		6	3
7A	DEC		6	3
7B	*			
7C	INC		6	3
7D	TST		6	3
7E	JMP		3	3
7F	CLR	EXTND	6	3
80	SUBA	IMMED	2	2
81	CMPA		2	2
82	SBCA		2	2
83	SUBD		4	3
84	ANDA		2	2
85	BITA		2	2
86	LDAA		2	2
87	*			
88	EORA		2	2
89	ADCA		2	2
8A	ORAA		2	2
8B	ADDA		2	2
8C	CPX	IMMED	4	3
8D	BSR	REL	6	2
8E	LDS	IMMED	3	3
8F	*			
90	SUBA	DIR	3	2
91	CMPA		3	2
92	SBCA		3	2
93	SUBD		5	2
94	ANDA		3	2
95	BITA		3	2
96	LDAA		3	2
97	STAA		3	2
98	EORA		3	2
99	ADCA		3	2
9A	ORAA		3	2
9B	ADDA		3	2

OP	MNEM	MODE	~	#
9C	CPX	DIR	5	2
9D	JSR		5	2
9E	LDS		4	2
9F	STS	DIR	4	2
40	SUBA	INDXD	4	2
A1	CMPA		4	2
A2	SBCA		4	2
A3	SUBD		6	2
A4	ANDA		4	2
A5	BITA		4	2
A6	LDAA		4	2
A7	STAA		4	2
A8	EORA		4	2
A9	ADCA		4	2
AA	ORAA		4	2
AB	ADDA		4	2
AC	CPX		6	2
AD	JSR		6	2
AE	LDS		5	2
AF	STS	INDXD	5	2
B0	SUBA	EXTND	4	3
B1	CMPA		4	3
B2	SBCA		4	3
B3	SUBD		6	3
B4	ANDA		4	3
B5	BITA		4	3
B6	LDAA		4	3
B7	STAA		4	3
B8	EORA		4	3
B9	ADCA		4	3
BA	ORAA		4	3
BB	ADDA		4	3
BC	CPX		6	3
BD	JSR		6	3
BE	LDS		5	3
BF	STS	EXTND	5	3
C0	SUBB	IMMED	2	2
C1	CMPB		2	2
C2	SBCB		2	2
C3	ADDD		4	3
C4	ANDB		2	2
C5	BITB		2	2
C6	LDAB		2	2
C7	*			
C8	EORB		2	2
C9	ADCB		2	2
CA	ORAB		2	2
CB	ADDB		2	2
CC	LDD		3	3
CD	*			
CD	LDX	IMMED	3	3
CF	*			

OP	MNEM	MODE	~	#
D0	SUBB	DIR	3	2
D1	CMPB		3	2
D2	SBCB		3	2
D3	ADDD		5	2
D4	ANDB		3	2
D5	BITB		3	2
D6	LDAB		3	2
D7	STAB		3	2
D8	EORB		3	2
D9	ADCB		3	2
DA	ORAB		3	2
DB	ADDB		3	2
DC	LDD		4	2
DD	STD		4	2
DE	LDX		4	2
DF	STX	DIR	4	2
E0	SUBB	INDXD	4	2
E1	CMPB		4	2
E2	SBCB		4	2
E3	ADDD		6	2
E4	ANDB		4	2
E5	BITB		4	2
E6	LDAB		4	2
E7	STAB		4	2
E8	EORB		4	2
E9	ADCB		4	2
EA	ORAB		4	2
EB	ADDB		4	2
EC	LDD		5	2
ED	STD		5	2
EE	LDX		5	2
EF	STX	INDXD	5	2
F0	SUBB	EXTND	4	3
F1	CMPB		4	3
F2	SBCB		4	3
F3	ADDD		6	3
F4	ANDB		4	3
F5	BITB		4	3
F6	LDAB		4	3
F7	STAB		4	3
F8	EORB		4	3
F9	ADCB		4	3
FA	ORAB		4	3
FB	ADDB		4	3
FC	LDD		5	3
FD	STD		5	3
FE	LDX		5	3
FF	STX	EXTND	5	3

*UNDEFINED OP CODE

NOTES:

1. Addressing Modes
   INHER = Inherent INDXD = Indexed IMMED = Immediate
   REL = Relative EXTND = Extended DIR = Direct
2. Unassigned opcodes are indicated by "*" and should not be executed.
3. Codes marked by "T" force the PC to function as a 16-bit counter.

Table 16 - Index register and stack manipulation instructions

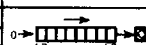
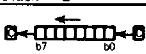
Pointer Operations	Mnemonic	Immed			Direct			Index			Extnd			Inherent			Boolean/ Arithmetic Operation	Condition Codes					
																		5	4	3	2	1	0
		OP	~	#	OP	~	#	OP	~	#	OP	~	#	OP	~	#		H	I	N	Z	V	C
Compare Index Reg	CPX	8C	4	3	9C	5	2	AC	6	2	BC	6	3				X - M : M + 1	●	●	↕	↕	↕	↕
Decrement Index Reg	DEX													09	3	1	X - 1 → X	●	●	●	↕	●	●
Decrement Stack Pntr	DES													34	3	1	SP - 1 → SP	●	●	●	●	●	●
Increment Index Reg	INX													08	3	1	X + 1 → X	●	●	●	↕	●	●
Increment Stack Pntr	INS													31	3	1	1 SP + 1 → SP	●	●	●	●	●	●
Load Index Reg	LDX	CE	3	3	DE	4	2	EE	5	2	FE	5	3				M → X_H, (M + 1) → X_L	●	●	↕	↕	R	●
Load Stack Pntr	LDS	8E	3	3	9E	4	2	AE	5	2	BE	5	3				M → SP_H, (M + 1) → SP_L	●	●	↕	↕	R	●
Store Index Reg	STX				DF	4	2	EF	5	2	FF	5	3				X_H → M, X_L → (M + 1)	●	●	↕	↕	R	●
Store Stack Pntr	STS				9F	4	2	AF	5	2	BF	5	3				SP_H → M, SP_L → (M + 1)	●	●	↕	↕	R	●
Index Reg → Stack Pntr	TXS													35	3	1	X - 1 → SP	●	●	●	●	●	●
Stack Pntr → Index Reg	TSX													30	3	1	SP + 1 → X	●	●	●	●	●	●
Add	ABX													3A	3	1	B + X → X	●	●	●	●	●	●
Push Data	PSHX													3C	4	1	X_L → M_{SP}, SP - 1 → SP X_H → M_{SP}, SP - 1 → SP	●	●	●	●	●	●
Pull Data	PULX													38	5	1	SP + 1 → SP, M_{SP} → X_H SP + 1 → SP, M_{SP} → X_L	●	●	●	●	●	●

Table 17 - Accumulator and memory instructions

Accumulator and Memory Operations	MNE	Immed			Direct			Index			Extend			Inher			Boolean Expression	Condition Codes					
		Op	~	#	Op	~	#	Op	~	#	Op	~	#	Op	~	#		H	I	N	Z	V	C
Add Acmltrs	ABA													1B	2	1	A + B → A	↕	●	↕	↕	↕	↕
Add B to X	ABX													3A	3	1	00:B + X → X	●	●	●	●	●	●
Add with Carry	ADCA	89	2	2	99	3	2	A9	4	2	B9	4	3				A + M + C → A	↕	●	↕	↕	↕	↕
	ADCB	C9	2	2	D9	3	2	E9	4	2	F9	4	3				B + M + C → B	↕	●	↕	↕	↕	↕
Add	ADDA	8B	2	2	9B	3	2	AB	4	2	BB	4	3				A + M → A	↕	●	↕	↕	↕	↕
	ADDB	CB	2	2	DB	3	2	EB	4	2	FB	4	3				B + M → A	↕	●	↕	↕	↕	↕
Add Double	ADDD	C3	4	3	D3	5	2	E3	6	2	F3	6	3				D + M:M + 1 → D	●	●	↕	↕	↕	↕
And	ANDA	84	2	2	94	3	2	A4	4	2	B4	4	3				A · M → A	●	●	↕	↕	R	●
	ANDB	C4	2	2	D4	3	2	E4	4	2	F4	4	3				B · M → B	●	●	↕	↕	R	●
Shift Left, Arithmetic	ASL							68	6	2	78	6	3				C ← [b7 … b0] ← 0	●	●	↕	↕	↕	↕
	ASLA													48	2	1		●	●	↕	↕	↕	↕
	ASLB													58	2	1		●	●	↕	↕	↕	↕

— Continued —

Table 17 - Accumulator and memory instructions (Continued)

Accumulator and Memory Operations	MNE	Immed			Direct			Index			Extend			Inher			Boolean Expression	Condition Codes					
		Op	~	#	Op	~	#	Op	~	#	Op	~	#	Op	~	#		H	I	N	Z	V	C
Shift Left Dbl	ASLD													05	3	1		●	●	↕	↕	↕	↕
Shift Right, Arithmetic	ASR							67	6	2	77	6	3					●	●	↕	↕	↕	↕
	ASRA													47	2	1		●	●	↕	↕	↕	↕
	ASRB													57	2	1		●	●	↕	↕	↕	↕
Bit Test	BITA	85	2	2	95	3	2	A5	4	2	B5	4	3				A · M	●	●	↕	↕	R	●
	BITB	C5	2	2	D5	3	2	E5	4	2	F5	4	3				B · M	●	●	↕	↕	R	●
Compare Acmltrs	CBA													11	2	1	A - B	●	●	↕	↕	↕	↕
Clear	CLR							6F	6	2	7F	6	3				00 → M	●	●	R	S	R	R
	CLRA													4F	2	1	00 → A	●	●	R	S	R	R
	CLRB													5F	2	1	00 → B	●	●	R	S	R	R
Compare	CMPA	81	2	2	91	3	2	A1	4	2	B1	4	3				A - M	●	●	↕	↕	↕	↕
	CMPB	C1	2	2	D1	3	2	E1	4	2	F1	4	3				B - M	●	●	↕	↕	↕	↕
1's Complement	COM							63	6	2	73	6	3				$\overline{M}$ → M	●	●	↕	↕	R	S
	COMA													43	2	1	$\overline{A}$ → A	●	●	↕	↕	R	S
	COMB													53	2	1	$\overline{B}$ → B	●	●	↕	↕	R	S
Decimal Adj, A	DAA													19	2	1	Adj binary sum to BCD	●	●	↕	↕	↕	↕
Decrement	DEC							6A	6	2	7A	6	3				M - 1 → M	●	●	↕	↕	↕	●
	DECA													4A	2	1	A - 1 → A	●	●	↕	↕	↕	●
	DECB													5A	2	1	B - 1 → B	●	●	↕	↕	↕	●
Exclusive OR	EORA	88	2	2	98	3	2	A8	4	2	B8	4	3				A ⊕ M → A	●	●	↕	↕	R	●
	EORB	C8	2	2	D8	3	2	E8	4	2	F8	4	3				B ⊕ M → B	●	●	↕	↕	R	●
Increment	INC							6C	6	2	7C	6	3				M + 1 → M	●	●	↕	↕	↕	●
	INCA													4C	2	1	A + 1 → A	●	●	↕	↕	↕	●
	INCB													5C	2	1	B + 1 → B	●	●	↕	↕	↕	●
Load Acmltrs	LDAA	86	2	2	96	3	2	A6	4	2	B6	4	3				M → A	●	●	↕	↕	R	●
	LDAB	C6	2	2	D6	3	2	E6	4	2	F6	4	3				M → B	●	●	↕	↕	R	●
Load Double	LDD	CC	3	3	DC	4	2	EC	5	2	FC	5	3				M:M + 1 → D	●	●	↕	↕	R	●
Logical Shift, Left	LSL							68	6	2	78	6	3					●	●	↕	↕	↕	↕
	LSLA													48	2	1		●	●	↕	↕	↕	↕
	LSLB													58	2	1		●	●	↕	↕	↕	↕
	LSLD													05	3	1		●	●	↕	↕	↕	↕
Shift Right, Logical	LSR							64	6	2	74	6	3					●	●	R	↕	↕	↕
	LSRA													44	2	1		●	●	R	↕	↕	↕
	LSRB													54	2	1		●	●	R	↕	↕	↕
	LSRD													04	3	1		●	●	R	↕	↕	↕
Multiply	MUL													3D	10	1	A X B → D	●	●	●	●	●	↕
2's Complement (Negate)	NEG							60	6	2	70	6	3				00 - M → M	●	●	↕	↕	↕	↕
	NEGA													40	2	1	00 - A → A	●	●	↕	↕	↕	↕
	NEGB													50	2	1	00 - B → B	●	●	↕	↕	↕	↕
No Operation	NOP													01	2	1	PC + 1 → PC	●	●	●	●	●	●
Inclusive OR	ORAA	8A	2	2	9A	3	2	AA	4	2	BA	4	3				A + M → A	●	●	↕	↕	R	●
	ORAB	CA	2	2	DA	3	2	EA	4	2	FA	4	3				B + M → B	●	●	↕	↕	R	●
Push Data	PSHA													36	3	1	A → Stack	●	●	●	●	●	●
	PSHB													37	3	1	B → Stack	●	●	●	●	●	●
Pull Data	PULA													32	4	1	Stack → A	●	●	●	●	●	●
	PULB													33	4	1	Stack → B	●	●	●	●	●	●
Rotate Left	ROL							69	6	2	79	6	3					●	●	↕	↕	↕	↕
	ROLA													49	2	1		●	●	↕	↕	↕	↕
	ROLB													59	2	1		●	●	↕	↕	↕	↕
Rotate Right	ROR							66	6	2	76	6	3					●	●	↕	↕	↕	↕
	RORA													46	2	1		●	●	↕	↕	↕	↕
	RORB													56	2	1		●	●	↕	↕	↕	↕
Subtract Acmltr	SBA													10	2	1	A - B → A	●	●	↕	↕	↕	↕
Subtract with Carry	SBCA	B2	2	2	92	3	2	A2	4	2	B2	4	3				A - M - C → A	●	●	↕	↕	↕	↕
	SBCB	C2	2	2	D2	3	2	E2	4	2	F2	4	3				B - M - C → B	●	●	↕	↕	↕	↕
Store Acmltrs	STAA				97	3	2	A7	4	2	B7	4	3				A → M	●	●	↕	↕	R	●
	STAB				D7	3	2	E7	4	2	F7	4	3				B → M	●	●	↕	↕	R	●
	STD				DD	4	2	ED	5	2	FD	5	3				D → M:M + 1	●	●	↕	↕	R	●
Subtract	SUBA	80	2	2	90	3	2	A0	4	2	B0	4	3				A - M → A	●	●	↕	↕	↕	↕
	SUBB	C0	2	2	D0	3	2	E0	4	2	F0	4	3				B - M → B	●	●	↕	↕	↕	↕
Subtract Double	SUBD	83	4	3	93	5	2	A3	6	2	B3	6	3				D - M:M + 1 → D	●	●	↕	↕	↕	↕
Transfer Acmltr	TAB													16	2	1	A → B	●	●	↕	↕	R	●
	TBA													17	2	1	B → A	●	●	↕	↕	R	●
Test, Zero or Minus	TST							6D	6	2	7D	6	3				M - 00	●	●	↕	↕	R	R
	TSTA													4D	2	1	A - 00	●	●	↕	↕	R	R
	TSTB													5D	2	1	B - 00	●	●	↕	↕	R	R

The condition code register notes are listed after Table 19.

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Table 18 - Jump and branch instructions

		Direct			Relative			Index			Extnd			Inherent				Cond. Code Reg.					
																		5	4	3	2	1	0
Operations	Mnemonic	OP	~	#	OP	~	#	OP	~	#	OP	~	#	OP	~	#	Branch Test	H	I	N	Z	V	C
Branch Always	BRA				20	3	2										None	●	●	●	●	●	●
Branch Never	BRN				21	3	2										None	●	●	●	●	●	●
Branch If Carry Clear	BCC				24	3	2										C = 0	●	●	●	●	●	●
Branch If Carry Set	BCS				25	3	2										C = 1	●	●	●	●	●	●
Branch If = Zero	BEQ				27	3	2										Z = 1	●	●	●	●	●	●
Branch If ≥ Zero	BGE				2C	3	2										N ⊕ V = 0	●	●	●	●	●	●
Branch If > Zero	BGT				2E	3	2										Z + (N ⊕ V) = 0	●	●	●	●	●	●
Branch If Higher	BHI				22	3	2										C + Z = 0	●	●	●	●	●	●
Branch If Higher or Same	BHS				24	3	2										C = 0	●	●	●	●	●	●
Branch If ≤ Zero	BLE				2F	3	2										Z + (N ⊕ V) = 1	●	●	●	●	●	●
Branch If Carry Set	BLO				25	3	2										C = 1	●	●	●	●	●	●
Branch If Lower Or Same	BLS				23	3	2										C + Z = 1	●	●	●	●	●	●
Branch If < Zero	BLT				2D	3	2										N ⊕ V = 1	●	●	●	●	●	●
Branch If Minus	BMI				2B	3	2										N = 1	●	●	●	●	●	●
Branch If Not Equal Zero	BNE				26	3	2										Z = 0	●	●	●	●	●	●
Branch If Overflow Clear	BVC				28	3	2										V = 0	●	●	●	●	●	●
Branch If Overflow Set	BVS				29	3	2										V = 1	●	●	●	●	●	●
Branch If Plus	BPL				2A	3	2										N = 0	●	●	●	●	●	●
Branch To Subroutine	BSR				8D	6	2										See Special Operations - Figure 26	●	●	●	●	●	●
Jump	JMP							6E	3	2	7E	3	3					●	●	●	●	●	●
Jump To Subroutine	JSR	9D	5	2				AD	6	2	BD	6	3					●	●	●	●	●	●
No Operation	NOP													01	2	1		●	●	●	●	●	●
Return From Interrupt	RTI													3B	10	1	See Special Operations - Figure 26	↕	↕	↕	↕	↕	↕
Return From Subroutine	RTS													39	5	1		●	●	●	●	●	●
Software Interrupt	SWI													3F	12	1		●	S	●	●	●	●
Wait For Interrupt	WAI													3E	9	1		●	●	●	●	●	●

Table 19 - Condition code register manipulation instructions

	Inherent					Cond. Code Reg.					
						5	4	3	2	1	0
Operations	Mnemonic	OP	~	#	Boolean Operation	H	I	N	Z	V	C
Clear Carry	CLC	0C	2	1	0 → C	●	●	●	●	●	R
Clear Interrupt Mask	CLI	0E	2	1	0 → I	●	R	●	●	●	●
Clear Overflow	CLV	0A	2	1	0 → V	●	●	●	●	R	●
Set Carry	SEC	0D	2	1	1 → C	●	●	●	●	●	S
Set Interrupt Mask	SEI	0F	2	1	1 → I	●	S	●	●	●	●
Set Overflow	SEV	0B	2	1	1 → V	●	●	●	●	S	●
Accumulator A → CCR	TAP	06	2	1	A → CCR	↕	↕	↕	↕	↕	↕
CCR → Accumulator A	TPA	07	2	1	CCR → A	●	●	●	●	●	●

LEGEND

- OP Operation Code (Hexadecimal)
- ~ Number of MPU Cycles
- M_{SP} Contents of memory location pointed to by Stack Pointer
- \# Number of Program Bytes
- \+ Arithmetic Plus
- \- Arithmetic Minus
- ● Boolean AND
- X Arithmetic Multiply
- \+ Boolean Inclusive OR
- ⊕ Boolean Exclusive OR
- $\overline{M}$ Complement of M
- → Transfer Into
- 0 Bit = Zero
- 00 Byte = Zero

CONDITION CODE SYMBOLS

- H Half-carry from bit 3
- I Interrupt mask
- N Negative (sign bit)
- Z Zero (byte)
- V Overflow, 2's complement
- C Carry/Borrow from MSB
- R Reset Always
- S Set Always
- ↕ Affected
- ● Not Affected

Table 20 - Instruction execution times in E-cycles

	ADDRESSING MODE					
	Immediate	Direct	Extended	Indexed	Inherent	Relative
ABA	●	●	●	●	2	●
ABX	●	●	●	●	3	●
ADC	2	3	4	4	●	●
ADD	2	3	4	4	●	●
ADDD	4	5	6	6	●	●
AND	2	3	4	4	●	●
ASL	●	●	6	6	2	●
ASLD	●	●	●	●	3	●
ASR	●	●	6	6	2	●
BCC	●	●	●	●	●	3
BCS	●	●	●	●	●	3
BEQ	●	●	●	●	●	3
BGE	●	●	●	●	●	3
BGT	●	●	●	●	●	3
BHI	●	●	●	●	●	3
BHS	●	●	●	●	●	3
BIT	2	3	4	4	●	●
BLE	●	●	●	●	●	3
BLO	●	●	●	●	●	3
BLS	●	●	●	●	●	3
BLT	●	●	●	●	●	3
BMI	●	●	●	●	●	3
BNE	●	●	●	●	●	3
BPL	●	●	●	●	●	3
BRA	●	●	●	●	●	3
BRN	●	●	●	●	●	3
BSR	●	●	●	●	●	6
BVC	●	●	●	●	●	3
BVS	●	●	●	●	●	3
CBA	●	●	●	●	2	●
CLC	●	●	●	●	2	●
CLI	●	●	●	●	2	●
CLR	●	●	6	6	2	●
CLV	●	●	●	●	2	●
CMP	2	3	4	4	●	●
COM	●	●	6	6	2	●
CPX	4	5	6	6	●	●
DAA	●	●	●	●	2	●
DEC	●	●	6	6	2	●
DES	●	●	●	●	3	●
DEX	●	●	●	●	3	●
EOR	2	3	4	4	●	●
INC	●	●	6	6	●	●
INS	●	●	●	●	3	●

	ADDRESSING MODE					
	Immediate	Direct	Extended	Indexed	Inherent	Relative
INX	●	●	●	●	3	●
JMP	●	●	3	3	●	●
JSR	●	5	6	6	●	●
LDA	2	3	4	4	●	●
LDD	3	4	5	5	●	●
LDS	3	4	5	5	●	●
LDX	3	4	5	5	●	●
LSL	●	●	6	6	2	●
LSLD	●	●	●	●	3	●
LSR	●	●	6	6	2	●
LSRD	●	●	●	●	3	●
MUL	●	●	●	●	10	●
NEG	●	●	6	6	2	●
NOP	●	●	●	●	2	●
ORA	2	3	4	4	●	●
PSH	●	●	●	●	3	●
PSHX	●	●	●	●	4	●
PUL	●	●	●	●	4	●
PULX	●	●	●	●	5	●
ROL	●	●	6	6	2	●
ROR	●	●	6	6	2	●
RTI	●	●	●	●	10	●
RTS	●	●	●	●	5	●
SBA	●	●	●	●	2	●
SBC	2	3	4	4	●	●
SEC	●	●	●	●	2	●
SEI	●	●	●	●	2	●
SEV	●	●	●	●	2	●
STA	●	3	4	4	●	●
STD	●	4	5	5	●	●
STS	●	4	5	5	●	●
STX	●	4	5	5	●	●
SUB	2	3	4	4	●	●
SUBD	4	5	6	6	●	●
SWI	●	●	●	●	12	●
TAB	●	●	●	●	2	●
TAP	●	●	●	●	2	●
TBA	●	●	●	●	2	●
TPA	●	●	●	●	2	●
TST	●	●	6	6	2	●
TSX	●	●	●	●	3	●
TXS	●	●	●	●	3	●
WAI	●	●	●	●	9	●

6.11 - Summary of cycle-by-cycle operation

Table 21 provides a detailed description of the information present on the address bus, data bus, and the read/write (R/W) line during each cycle of each instruction.

The information is useful in comparing actual with expected results during debug of both software and hardware as the program is executed. The information is categorized in groups according to addressing mode and number of cycles per instruction. In general, instructions with the same addressing mode and number of cycles execute in the same manner. Exceptions are indicated in the table.

Note that during MPU reads of internal locations, the resultant value will not appear on the external data bus except in mode 0. «High order» byte refers to the most-significant byte of a 16-bit value.

Table 21 - Cycle-by-cycle operation (sheet 1 of 5)

Address Mode and Instructions		Cycles	Cycle #	Address Bus	R/$\overline{W}$ Line	Data Bus
IMMEDIATE						
ADC	EOR	2	1	Opcode Address	1	Opcode
ADD	LDA		2	Opcode Address + 1	1	Operand Data
AND	ORA					
BIT	SBC					
CMP	SUB					
LDS		3	1	Opcode Address	1	Opcode
LDX			2	Opcode Address + 1	1	Operand Data (High Order Byte)
LDD			3	Opcode Address + 2	1	Operand Data (Low Order Byte)
CPX		4	1	Opcode Address	1	Opcode
SUBD			2	Opcode Address + 1	1	Operand Data (High Order Byte)
ADDD			3	Opcode Address + 2	1	Operand Data (Low Order Byte)
			4	Address Bus FFFF	1	Low Byte of Restart Vector
DIRECT						
ADC	EOR	3	1	Opcode Address	1	Opcode
ADD	LDA		2	Opcode Address + 1	1	Address of Operand
AND	ORA		3	Address of Operand	1	Operand Data
BIT	SBC					
CMP	SUB					
STA		3	1	Opcode Address	1	Opcode
			2	Opcode Address + 1	1	Destination Address
			3	Destination Address	0	Data from Accumulator
LDS		4	1	Opcode Address	1	Opcode
LDX			2	Opcode Address + 1	1	Address of Operand
LDD			3	Address of Operand	1	Operand Data (High Order Byte)
			4	Operand Address + 1	1	Operand Data (Low Order Byte)
STS		4	1	Opcode Address	1	Opcode
STX			2	Opcode Address + 1	1	Address of Operand
STD			3	Address of Operand	0	Register Data (High Order Byte)
			4	Address of Operand + 1	0	Register Data (Low Order Byte)
CPX		5	1	Opcode Address	1	Opcode
SUBD			2	Opcode Address + 1	1	Address of Operand
ADDD			3	Operand Address	1	Operand Data (High Order Byte)
			4	Operand Address + 1	1	Operand Data (Low Order Byte)
			5	Address Bus FFFF	1	Low Byte of Restart Vector
JSR		5	1	Opcode Address	1	Opcode
			2	Opcode Address + 1	1	Irrelevant Data
			3	Subroutine Address	1	First Subroutine Opcode
			4	Stack Pointer	0	Return Address (Low Order Byte)
			5	Stack Pointer − 1	0	Return Address (High Order Byte)

Table 21 - Cycle-by-cycle operation (sheet 2 of 5)

Address Mode and Instructions		Cycles	Cycle #	Address Bus	R/$\overline{W}$ Line	Data Bus
EXTENDED						
JMP		3	1	Opcode Address	1	Opcode
			2	Opcode Address + 1	1	Jump Address (High Order Byte)
			3	Opcode Address + 2	1	Jump Address (Low Order Byte)
ADC	EOR	4	1	Opcode Address	1	Opcode
ADD	LDA		2	Opcode Address + 1	1	Address of Operand
AND	ORA		3	Opcode Address + 2	1	Address of Operand (Low Order Byte)
BIT	SBC		4	Address of Operand	1	Operand Data
CMP	SUB					
STA		4	1	Opcode Address	1	Opcode
			2	Opcode Address + 1	1	Destination Address (High Order Byte)
			3	Opcode Address + 2	1	Destination Address (Low Order Byte)
			4	Operand Destination Address	0	Data from Accumulator
LDS		5	1	Opcode Address	1	Opcode
LDX			2	Opcode Address + 1	1	Address of Operand (High Order Byte)
LDD			3	Opcode Address + 2	1	Address of Operand (Low Order Byte)
			4	Address of Operand	1	Operand Data (High Order Byte)
			5	Address of Operand + 1	1	Operand Data (Low Order Byte)
STS		5	1	Opcode Address	1	Opcode
STX			2	Opcode Address + 1	1	Address of Operand (High Order Byte)
STD			3	Opcode Address + 2	1	Address of Operand (Low Order Byte)
			4	Address of Operand	0	Operand Data (High Order Byte)
			5	Address of Operand + 1	0	Operand Data (Low Order Byte)
ASL	LSR	6	1	Opcode Address	1	Opcode
ASR	NEG		2	Opcode Address + 1	1	Address of Operand (High Order Byte)
CLR	ROL		3	Opcode Address + 2	1	Address of Operand (Low Order Byte)
COM	ROR		4	Address of Operand	1	Current Operand Data
DEC	TST*		5	Address Bus FFFF	1	Low Byte of Restart Vector
INC			6	Address of Operand	0	New Operand Data
CPX		6	1	Opcode Address	1	Opcode
SUBD			2	Opcode Address + 1	1	Operand Address (High Order Byte)
ADDD			3	Opcode Address + 2	1	Operand Address (Low Order Byte)
			4	Operand Address	1	Operand Data (High Order Byte)
			5	Operand Address + 1	1	Operand Data (Low Order Byte)
			6	Address Bus FFFF	1	Low Byte of Restart Vector
JSR		6	1	Opcode Address	1	Opcode
			2	Opcode Address + 1	1	Address of Subroutine (High Order Byte)
			3	Opcode Address + 2	1	Address of Subroutine (Low Order Byte)
			4	Subroutine Starting Address	1	Opcode of Next Instruction
			5	Stack Pointer	0	Return Address (Low Order Byte)
			6	Stack Pointer − 1	0	Return Address (High Order Byte)

* TST does not perform the write cycle during the sixth cycle. The sixth cycle is another address bus = $FFFF.

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Table 21 - Cycle-by-cycle operation (sheet 3 of 5)

Address Mode and Instructions	Cycles	Cycle #	Address Bus	R/$\overline{W}$ Line	Data Bus
INDEXED					
JMP	3	1	Opcode Address	1	Opcode
		2	Opcode Address + 1	1	Offset
		3	Address Bus FFFF	1	Low Byte of Restart Vector
ADC EOR	4	1	Opcode Address	1	Opcode
ADD LDA		2	Opcode Address + 1	1	Offset
AND ORA		3	Address Bus FFFF	1	Low Byte of Restart Vector
BIT SBC		4	Index Register Plus Offset	1	Operand Data
CMP SUB					
STA	4	1	Opcode Address	1	Opcode
		2	Opcode Address + 1	1	Offset
		3	Address Bus FFFF	1	Low Byte of Restart Vector
		4	Index Register Plus Offset	0	Operand Data
LDS	5	1	Opcode Address	1	Opcode
LDX		2	Opcode Address + 1	1	Offset
LDD		3	Address Bus FFFF	1	Low Byte of Restart Vector
		4	Index Register Plus Offset	1	Operand Data (High Order Byte)
		5	Index Register Plus Offset + 1	1	Operand Data (Low Order Byte)
STS	5	1	Opcode Address	1	Opcode
STX		2	Opcode Address + 1	1	Offset
STD		3	Address Bus FFFF	1	Low Byte of Restart Vector
		4	Index Register Plus Offset	0	Operand Data (High Order Byte)
		5	Index Register Plus Offset + 1	0	Operand Data (Low Order Byte)
ASL LSR	6	1	Opcode Address	1	Opcode
ASR NEG		2	Opcode Address + 1	1	Offset
CLR ROL		3	Address Bus FFFF	1	Low Byte of Restart Vector
COM ROR		4	Index Register Plus Offset	1	Current Operand Data
DEC TST*		5	Address Bus FFFF	1	Low Byte of Restart Vector
INC		6	Index Register Plus Offset	0	New Operand Data
CPX	6	1	Opcode Address	1	Opcode
SUBD		2	Opcode Address + 1	1	Offset
ADDD		3	Address Bus FFFF	1	Low Byte of Restart Vector
		4	Index Register + Offset	1	Operand Data (High Order Byte)
		5	Index Register + Offset + 1	1	Operand Data (Low Order Byte)
		6	Address Bus FFFF		Low Byte of Restart Vector
JSR	6	1	Opcode Address	1	Opcode
		2	Opcode Address + 1	1	Offset
		3	Address Bus FFFF	1	Low Byte of Restart Vector
		4	Index Register + Offset	1	First Subroutine Opcode
		5	Stack Pointer	0	Return Address (Low Order Byte)
		6	Stack Pointer − 1	0	Return Address (High Order Byte)

*TST does not perform the write cycle during the sixth cycle. The sixth cycle is another address bus = $FFFF.

Table 21 - Cycle-by-cycle operation (sheet 4 of 5)

Address Mode and Instructions	Cycles	Cycle #	Address Bus	R/$\overline{W}$ Line	Data Bus
INHERENT					
ABA DAA SEC ASL DEC SEI ASR INC SEV CBA LSR TAB CLC NEG TAP CLI NOP TBA CLR ROL TPA CLV ROR TST COM SBA	2	1 2	Opcode Address Opcode Address + 1	1 1	Opcode Opcode of Next Instruction
ABX	3	1 2 3	Opcode Address Opcode Address + 1 Address Bus FFFF	1 1 1	Opcode Irrelevant Data Low Byte of Restart Vector
ASLD LSRD	3	1 2 3	Opcode Address Opcode Address + 1 Address Bus FFFF	1 1 1	Opcode Irrelevant Data Low Byte of Restart Vector
DES INS	3	1 2 3	Opcode Address Opcode Address + 1 Previous Stack Pointer Contents	1 1 1	Opcode Opcode of Next Instruction Irrelevant Data
INX DEX	3	1 2 3	Opcode Address Opcode Address + 1 Address Bus FFFF	1 1 1	Opcode Opcode of Next Instruction Low Byte of Restart Vector
PSHA PSHB	3	1 2 3	Opcode Address Opcode Address + 1 Stack Pointer	1 1 0	Opcode Opcode of Next Instruction Accumulator Data
TSX	3	1 2 3	Opcode Address Opcode Address + 1 Stack Pointer	1 1 1	Opcode Opcode of Next Instruction Irrelevant Data
TXS	3	1 2 3	Opcode Address Opcode Address + 1 Address Bus FFFF	1 1 1	Opcode Opcode of Next Instruction Low Byte of Restart Vector
PULA PULB	4	1 2 3 4	Opcode Address Opcode Address + 1 Stack Pointer Stack Pointer + 1	1 1 1 1	Opcode Opcode of Next Instruction Irrelevant Data Operand Data from Stack
PSHX	4	1 2 3 4	Opcode Address Opcode Address + 1 Stack Pointer Stack Pointer − 1	1 1 0 0	Opcode Irrelevant Data Index Register (Low Order Byte) Index Register (High Order Byte)
PULX	5	1 2 3 4 5	Opcode Address Opcode Address + 1 Stack Pointer Stack Pointer + 1 Stack Pointer + 2	1 1 1 1 1	Opcode Irrelevant Data Irrelevant Data Index Register (High Order Byte) Index Register (Low Order Byte)
RTS	5	1 2 3 4 5	Opcode Address Opcode Address + 1 Stack Pointer Stack Pointer + 1 Stack Pointer + 2	1 1 1 1 1	Opcode Irrelevant Data Irrelevant Data Address of Next Instruction (High Order Byte) Address of Next Instruction (Low Order Byte)
WAI	9	1 2 3 4 5 6 7 8 9	Opcode Address Opcode Address + 1 Stack Pointer Stack Pointer − 1 Stack Pointer − 2 Stack Pointer − 3 Stack Pointer − 4 Stack Pointer − 5 Stack Pointer − 6	1 1 0 0 0 0 0 0 0	Opcode Opcode of Next Instruction Return Address (Low Order Byte) Return Address (High Order Byte) Index Register (Low Order Byte) Index Register (High Order Byte) Contents of Accumulator A Contents of Accumulator B Contents of Condition Code Register

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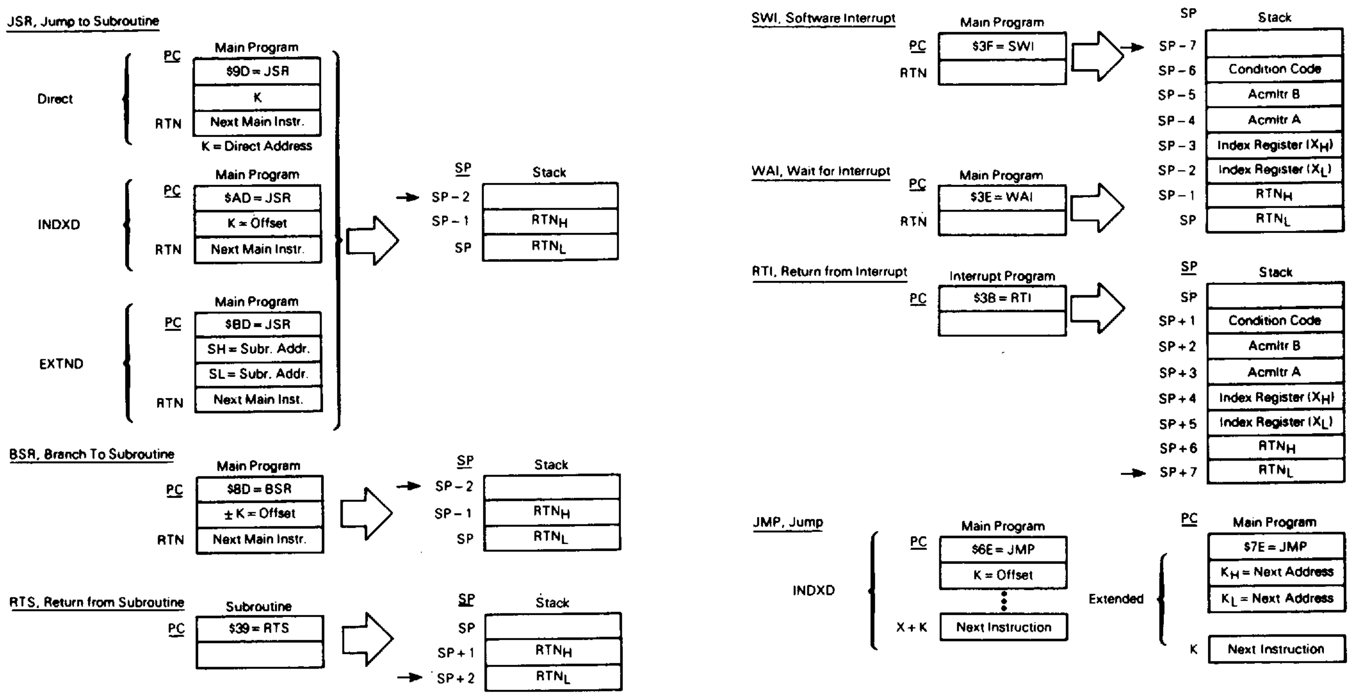
Table 21 · Cycle-by-cycle operation (sheet 5 of 5)

Address Mode and Instructions	Cycles	Cycle #	Address Bus	R/$\overline{W}$ Line	Data Bus
INHERENT					
MUL	10	1	Opcode Address	1	Opcode
		2	Opcode Address + 1	1	Irrelevant Data
		3	Address Bus FFFF	1	Low Byte of Restart Vector
		4	Address Bus FFFF	1	Low Byte of Restart Vector
		5	Address Bus FFFF	1	Low Byte of Restart Vector
		6	Address Bus FFFF	1	Low Byte of Restart Vector
		7	Address Bus FFFF	1	Low Byte of Restart Vector
		8	Address Bus FFFF	1	Low Byte of Restart Vector
		9	Address Bus FFFF	1	Low Byte of Restart Vector
		10	Address Bus FFFF	1	Low Byte of Restart Vector
RTI	10	1	Opcode Address	1	Opcode
		2	Opcode Address + 1	1	Irrelevant Data
		3	Stack Pointer	1	Irrelevant Data
		4	Stack Pointer + 1	1	Contents of Condition Code Register from Stack
		5	Stack Pointer + 2	1	Contents of Accumulator B from Stack
		6	Stack Pointer + 3	1	Contents of Accumulator A from Stack
		7	Stack Pointer + 4	1	Index Register from Stack (High Order Byte)
		8	Stack Pointer + 5	1	Index Register from Stack (Low Order Byte)
		9	Stack Pointer + 6	1	Next Instruction Address from Stack (High Order Byte)
		10	Stack Pointer + 7	1	Next Instruction Address from Stack (Low Order Byte)
SWI	12	1	Opcode Address	1	Opcode
		2	Opcode Address + 1	1	Irrelevant Data
		3	Stack Pointer	0	Return Address (Low Order Byte)
		4	Stack Pointer − 1	0	Return Address (High Order Byte)
		5	Stack Pointer − 2	0	Index Register (Low Order Byte)
		6	Stack Pointer − 3	0	Index Register (High Order Byte)
		7	Stack Pointer − 4	0	Contents of Accumulator A
		8	Stack Pointer − 5	0	Contents of Accumulator B
		9	Stack Pointer − 6	0	Contents of Condition Code Register
		10	Stack Pointer − 7	1	Irrelevant Data
		11	Vector Address FFFA (Hex)	1	Address of Subroutine (High Order Byte)
		12	Vector Address FFFB (Hex)	1	Address of Subroutine (Low Order Byte)
RELATIVE					
BCC BHT BNE BLO BCS BLE BPL BHS BEQ BLS BRA BRN BGE BLT BVC BGT BMI BVS	3	1	Opcode Address	1	Opcode
		2	Opcode Address + 1	1	Branch Offset
		3	Address Buss FFFF	1	Low Byte of Restart Vector
BSR	6	1	Opcode Address	1	Opcode
		2	Opcode Address + 1	1	Branch Offset
		3	Address Bus FFFF	1	Low Byte of Restart Vector
		4	Subroutine Starting Address	1	Opcode of Next Instruction
		5	Stack Pointer	0	Return Address (Low Order Byte)
		6	Stack Pointer − 1	0	Return Address (High Order Byte)



Legend:
RTN = Address of next instruction in Main Program to be executed upon return from subroutine
RTN_H = Most significant byte of Return Address
RTN_L = Least significant byte of Return Address
→ = Stack Pointer After Execution
K = 8-bit Unsigned Value

Figure 23 : Special operations.

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7 · PREPARATION FOR DELIVERY

7.1 · Packaging

Microcircuit are prepared for delivery in accordance with MIL-M-38510 or CECC 90000.

7.2 · Certificate of compliance

TMS offers a certificate of compliance with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or CECC 90000 and guarantying the parameters are tested at extreme temperatures for the entire temperature range.

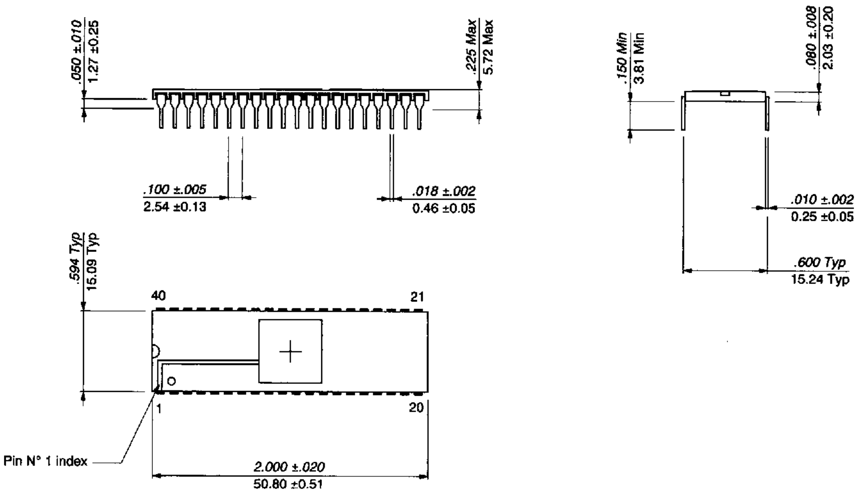
8 · HANDLING

MOS device must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

a) Device should be handled on benches with conductive and grounded surface.
b) Ground-test equipment, tools and operator.
c) Do not handle devices by the leads.
d) Store devices in conductive foam or carriers.
e) Avoid use of plastic, rubber, or silk in MOS areas.
f) Maintain relative humidity above 50 %, if pratical.

9 - PACKAGE MECHANICAL DATA

9.1 - 40 pins - DIL Ceramic Side Brazed



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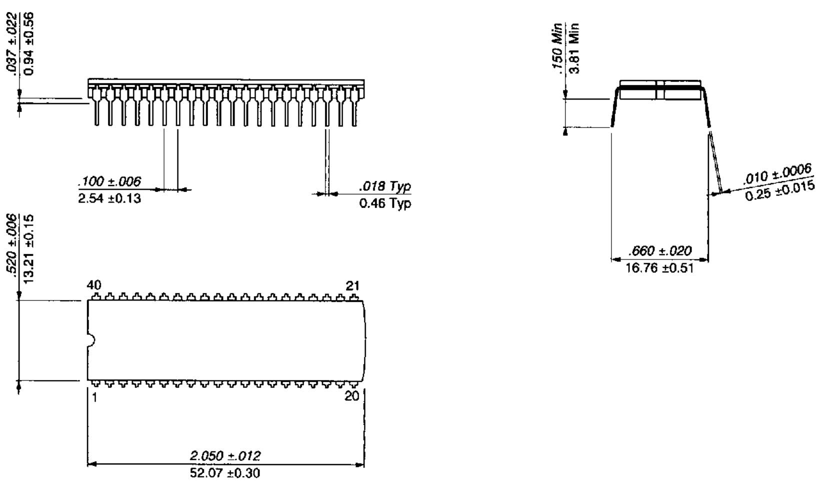
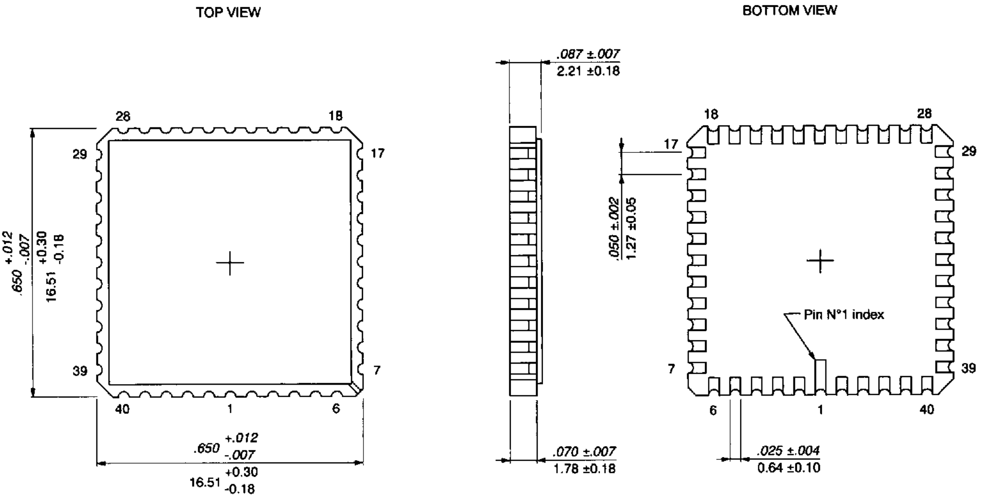
9.2 - 40 pins - DIL Cerdip

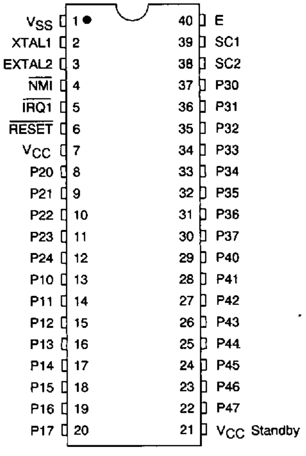


9.3 - 44 pins - Leadless Ceramic Chip Carrier

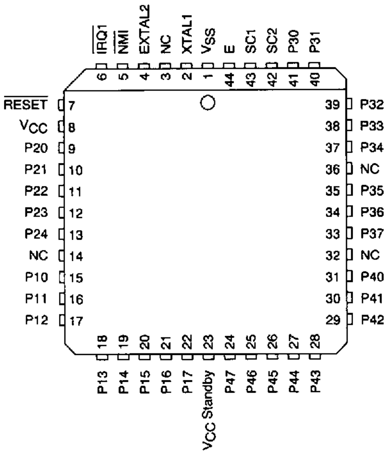


10 - TERMINAL CONNECTIONS

10.1 - DIL 40 - Pin assignment



10.2 - LCCC 44 - Pin assignment



11 · ORDERING INFORMATION

11.1 · Hi-REL product

Commercial TMS Part-Number (see Note)	Norms	Package	Temperature range T_C (°C)	Frequency (MHz)	Drawing number
EF6803JMG/B	NFC 96883 - Class G	DIL Cerdip	– 55 / + 125	1	Data-sheet
EF6803CMG/B	NFC 96883 - Class G	DIL Side Brazed	– 55 / + 125	1	Data-sheet
EF6803EMG/B	NFC 96883 - Class G	LCCC	– 55 / + 125	1	Data-sheet
EF68A03JMG/B	NFC 96883 - Class G	DIL Cerdip	– 55 / + 125	1.5	Data-sheet
EF68A03CMG/B	NFC 96883 - Class G	DIL Side Brazed	– 55 / + 125	1.5	Data-sheet
EF68A03EMG/B	NFC 96883 - Class G	LCCC	– 55 / + 125	1.5	Data-sheet
EF6803JMB/C	MIL STD 883 - Class B	DIL Cerdip	– 55 / + 125	1	Data-sheet
EF6803CMB/C	MIL STD 883 - Class B	DIL Side Brazed	– 55 / + 125	1	Data-sheet
EF68A03JMB/C	MIL STD 883 - Class B	DIL Cerdip	– 55 / + 125	1.5	Data-sheet
EF68A03CMB/C	MIL STD 883 - Class B	DIL Side Brazed	– 55 / + 125	1.5	Data-sheet
Note : THOMSON COMPOSANTS MILITAIRES ET SPATIAUX.					

11.2 · Standard product

Commercial TMS Part-Number (see Note)	Norms	Package	Temperature range T_C (°C)	Frequency (MHz)	Drawing number
EF6803CV	TMS standard	DIL Side Brazed	– 40 / + 85	1	Data sheet
EF6803JV	TMS standard	Cerdip DIL	– 40 / + 85	1	Data sheet
EF68A03CV	TMS standard	DIL Side Brazed	– 40 / + 85	1.5	Data sheet
EF68A03JV	TMS standard	Cerdip DIL	– 40 / + 85	1.5	Data sheet
EF6803JM	TMS standard	Cerdip DIL	– 55 / + 125	1	Data sheet
EF6803CM	TMS standard	DIL Side Brazed	– 55 / + 125	1	Data sheet
EF6803EM	TMS standard	LCCC	– 55 / + 125	1	Data sheet
EF68A03JM	TMS standard	Cerdip DIL	– 55 / + 125	1.5	Data sheet
EF68A03CM	TMS standard	DIL Side Brazed	– 55 / + 125	1.5	Data sheet
EF68A03EM	TMS standard	LCCC	– 55 / + 125	1.5	Data sheet
EF6803C	TMS standard	DIL Side Brazed	0 / + 70	1	Data sheet
EF6803J	TMS standard	Cerdip DIL	0 / + 70	1	Data sheet
EF68A03C	TMS standard	DIL Side Brazed	0 / + 70	1.5	Data sheet
EF68A03J	TMS standard	Cerdip DIL	0 / + 70	1.5	Data sheet
EF68B03J	TMS standard	Cerdip DIL	0 / + 70	2	Data sheet
Note : THOMSON COMPOSANTS MILITAIRES ET SPATIAUX.					

EF6803 C M B/C

Type — EF6803

Packages:
C = Ceramic DIL (side brased)
E = Ceramic LCCC
E1 = LCC+HOT Solder DIL
J = Tin dipped Cerdip DIL

Temperature /Tcase:
M = -55°C/ +125°C
V = -40°C/ +85°C
_ = 0/ +70°C

Screening:
___ = Standard
G/B = NFC 96883 Cl.G
B/B = MIL STD 883 Cl.B Rev B
B/C = MIL STD 883 Cl.B