Am27S27/27S27A
4,096-Bit (512x8) Bipolar Registered PROM

DISTINCTIVE CHARACTERISTICS

- On-chip, edge-triggered registers — ideal for pipelined microprogrammed systems
- Versatile synchronous and asynchronous enables for simplified word expansion
- Predetermined OFF outputs on power-up

- Fast 30 ns address setup and 17 ns clock to output times
- Excellent performance over the military range
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)

GENERAL DESCRIPTION

The Am27S27 (512 words by 8 bits) is a fully decoded, Schottky array, TTL-Programmable Read-Only Memory (PROM), incorporating D-type master-slave data registers on chip. This device has three-state outputs compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls and state machines.

This device contains an 8-bit parallel data register in the array-to-output path which allows PROM data to be stored while other data is being addressed. This meets the requirements for pipelined microprogrammable control stores where instruction execute and instruction fetch are performed in parallel.

To offer the system designer maximum flexibility, this device contains both asynchronous and synchronous output enables.

Upon power-up the outputs ($Q_0 - Q_7$) will be in a floating or high-impedance state.
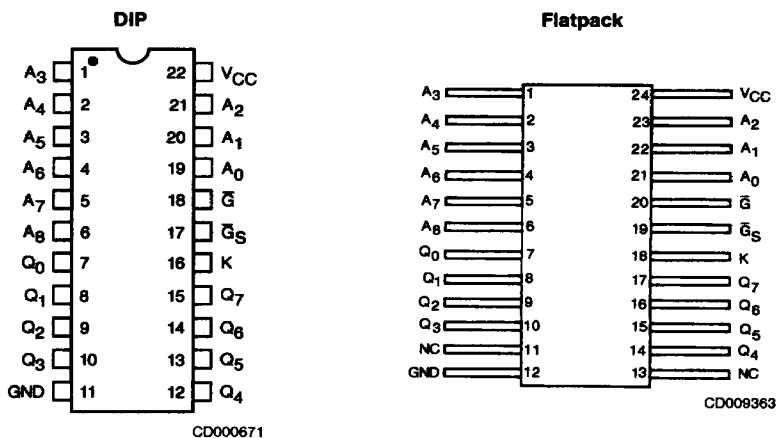
BLOCK DIAGRAM

BD006183
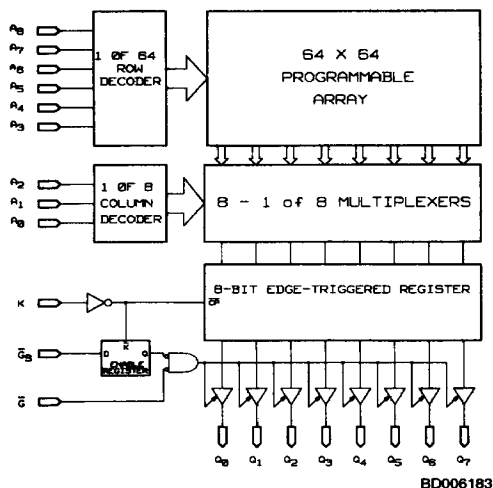
PRODUCT SELECTOR GUIDE

Part Number	Am27S27A		Am27S27	
Address Setup Time	30 ns	35 ns	50 ns	55 ns
Clock-to-Output Delay	17 ns	20 ns	27 ns	30 ns
Operating Range	C	M	C	M

CONNECTION DIAGRAMS
Top View

DIP

```
A3  ┌1      22┐ VCC
A4  ┌2      21┐ A2
A5  ┌3      20┐ A1
A6  ┌4      19┐ A0
A7  ┌5      18┐ Ḡ
A8  ┌6      17┐ ḠS
Q0  ┌7      16┐ K
Q1  ┌8      15┐ Q7
Q2  ┌9      14┐ Q6
Q3  ┌10     13┐ Q5
GND ┌11     12┐ Q4
```

CD000671

Flatpack

```
A3  ═1      24═ VCC
A4  ═2      23═ A2
A5  ═3      22═ A1
A6  ═4      21═ A0
A7  ═5      20═ Ḡ
A8  ═6      19═ ḠS
Q0  ═7      18═ K
Q1  ═8      17═ Q7
Q2  ═9      16═ Q6
Q3  ═10     15═ Q5
NC  ═11     14═ Q4
GND ═12     13═ NC
```

CD009363

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL

LS000131

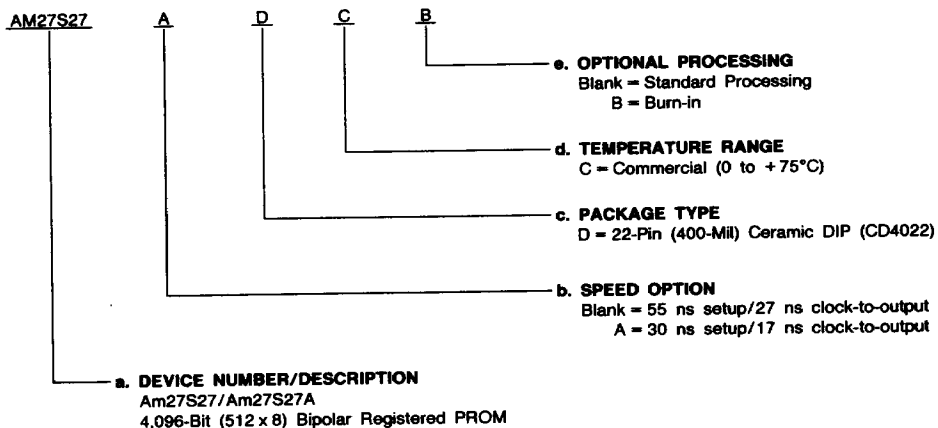Powered by ICminer.com Electronic-Library Service CopyRight 2003
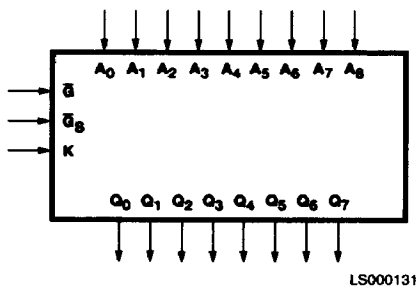
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:
- **a. Device Number**
- **b. Speed Option** (if applicable)
- **c. Package Type**
- **d. Temperature Range**
- **e. Optional Processing**

AM27S27   A   D   C   B

e. OPTIONAL PROCESSING
Blank = Standard Processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +75°C)

c. PACKAGE TYPE
D = 22-Pin (400-Mil) Ceramic DIP (CD4022)

b. SPEED OPTION
Blank = 55 ns setup/27 ns clock-to-output
A = 30 ns setup/17 ns clock-to-output

a. DEVICE NUMBER/DESCRIPTION
Am27S27/Am27S27A
4,096-Bit (512 x 8) Bipolar Registered PROM

Valid Combinations	
AM27S27	DC, DCB
AM27S27A	

Valid Combinations

Valid Combinations list configurations planned to supported in volume for this device. Consult the local AMD sales office to confirm availability of specific combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.
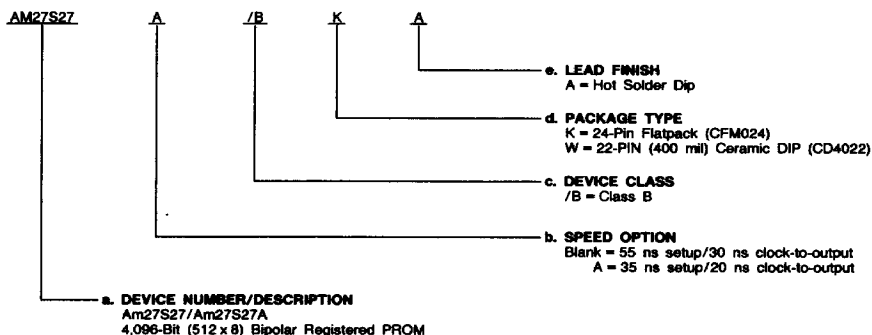
MILITARY ORDERING INFORMATION

APL and CPL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) is formed by a combination of:
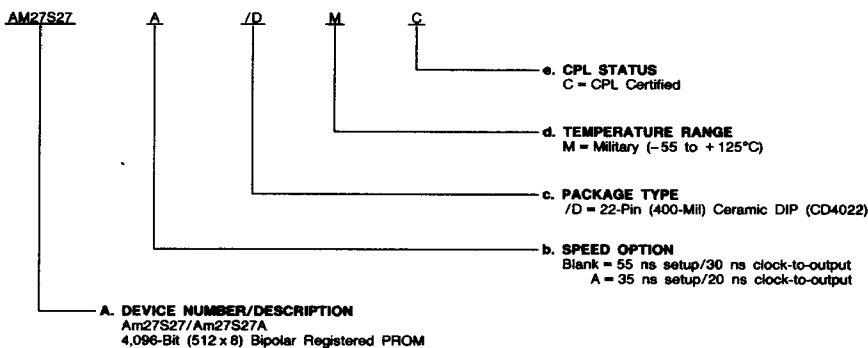
APL Products: a. Device Number
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish

CPL Products: a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. CPL Status

APL Products

AM27S27   A   /B   K   A

e. LEAD FINISH
A = Hot Solder Dip

d. PACKAGE TYPE
K = 24-Pin Flatpack (CFM024)
W = 22-PIN (400 mil) Ceramic DIP (CD4022)

c. DEVICE CLASS
/B = Class B

b. SPEED OPTION
Blank = 55 ns setup/30 ns clock-to-output
A = 35 ns setup/20 ns clock-to-output

a. DEVICE NUMBER/DESCRIPTION
Am27S27/Am27S27A
4,096-Bit (512 x 8) Bipolar Registered PROM

CPL Products

AM27S27   A   /D   M   C

e. CPL STATUS
C = CPL Certified

d. TEMPERATURE RANGE
M = Military (−55 to +125°C)

c. PACKAGE TYPE
/D = 22-Pin (400-Mil) Ceramic DIP (CD4022)

b. SPEED OPTION
Blank = 55 ns setup/30 ns clock-to-output
A = 35 ns setup/20 ns clock-to-output

A. DEVICE NUMBER/DESCRIPTION
Am27S27/Am27S27A
4,096-Bit (512 x 8) Bipolar Registered PROM

	Valid Combinations	
A P L	AM27S27	/BKA, /BWA
	AM27S27A	
C P L	AM27S27	/DMC
	AM27S27A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

PIN DESCRIPTION

$A_0 - A_8$ **Address Inputs (Input)**

The 9-bit field presented at the address inputs selects one of the 512 memory locations to be read from.

K   Clock (Input)

The clock is used to load data into the parallel registers from the memory array. Data transfer occurs on the LOW-to-HIGH transition of K.

$Q_0 - Q_7$ **Data Output Port (Output)**

Parallel data output from the pipeline register. The disabled state of these outputs is floating or high impedance.

$\overline{G}$ **Asynchronous Output Enable (Input)**

Provides direct control of the Q_n output three-state drivers independent of K.

$\overline{G}_S$ **Synchronous Output Enable (Input)**

Controls the state of the Q_n output three-state drivers in conjunction with K. This is useful where more than one registered PROM is bussed together for word depth expansion. In this case, the enable becomes the most significant address bit and, as such, must be synchronized with the data.

V_{CC} **Device Power Supply Pin**

The most positive of the logic power supply pins.

GND   Device Power Supply Pin

The most negative of the logic power supply pins.

FUNCTIONAL DESCRIPTION

When V_{CC} power is first applied, the synchronous enable ($\overline{G}_S$) flip-flop will be in the set condition causing the outputs, $Q_0 - Q_7$, to be in the OFF or high-impedance state, eliminating the need for a register clear input. This occurs regardless of the state of the asynchronous enable input. A LOW-to-HIGH transition of the clock input (K) while $\overline{G}_S$ input is LOW is required after power-up in order to enable the outputs to an active state. Reading data is accomplished by first applying the binary word address to the address inputs, $A_0 - A_8$, and a logic LOW to the synchronous output enable, $\overline{G}_S$. During the address setup time, stored data is accessed and loaded into the master flip-flops of the data register. Since the synchronous enable setup time is less than the address setup requirement, additional decoding delays may occur in the enable path without reducing memory performance. Upon the next LOW-to-HIGH transition of the clock, K, data is trans-ferred to the slave flip-flops which drive the output buffers. Provided that the asynchronous enable, $\overline{G}$, is also LOW, stored data will appear on the outputs, $Q_0 - Q_7$. If $\overline{G}_S$ is HIGH when the positive clock edge occurs, outputs go to the OFF or high-impedance state. The outputs may be disabled at any time by switching $\overline{G}$ to a HIGH level. Following the positive clock edge, the address and synchronous enable inputs are free to change; changes will not affect the outputs until another positive clock edge occurs. This unique feature allows the PROM decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs. For less complex applications either enable may be effectively eliminated by tying it to ground.

The on-chip edge-triggered register simplifies system timing since the PROM clock may be derived directly from system clock without introducing dangerous race conditions. Other register timing requirements are similar to those of standard Schottky registers and are easily implemented.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65 to +150°C
Ambient Temperature with
   Power Applied .... −55 to +125°C
Supply Voltage .... −0.5 V to +7.0 V
DC Voltage Applied to Outputs
   (Except During Programming) .... −0.5 to +V_{CC} Max.
DC Voltage Applied to Outputs
   During Programming .... 21 V
Output Current into Outputs During
   Programming (Max Duration of 1 sec) .... 250 mA
DC Input Voltage .... −0.5 V to +5.5 V
DC Input Current .... −30 mA to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
   Ambient Temperature (T_A) .... 0 to +75°C
   Supply Voltage (V_{CC}) .... +4.75 V to +5.25 V

Military (M) Devices*
   Case Temperature (T_C) .... −55 to +125°C
   Supply Voltage (V_{CC}) .... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at T_C = +25°C, +125°C, and −55°C.

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA V_{IN} = V_{IH} or V_{IL}		2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}				0.50	V
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 4)		2.0			V
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 4)				.8	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.45 V				−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V				25	µA
I_I	Input HIGH Current	V_{CC} = Max., V_{IN} = 5.5 V				40	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = Max., V_{OUT} = 0.0 V (Note 2)		−20		−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = Max.				185	mA
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18 mA				−1.2	V
I_{CEX}	Output Leakage Current	V_{CC} = Max. $V\overline{E}$ = 2.4 V	V_O = 4.5 V			40	µA
			V_O = 0.4 V			−40	
C_{IN}	Input Capacitance	V_{CC} = 5.00 V., T_A = 25°C (Note 3)			5		pF
C_{OUT}	Output Capacitance	V_{IN}/V_{OUT} = 2.0 V. @ f = 1 MHz (Note 3)			12		

Notes:
1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.
4. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

5

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted*) (see Note 1)

| No.	Parameter Symbol	Parameter Description		Am27S27A Min.	Am27S27A Max.	Am27S27 Min.	Am27S27 Max.	Unit
1	TAVKH	Address to K HIGH Setup Time	COM'L	30		50		ns
			MIL	35		55		ns
2	TKHAX	Address to K HIGH Hold Time	COM'L	0		0		ns
			MIL	0		0		ns
3	TKHQV1	Delay from K HIGH to Output Valid, for initially active outputs (HIGH or LOW)	COM'L		17		27	ns
			MIL		20		30	ns
4	TKHKL TKLKH	K Pulse Width (HIGH or LOW)	COM'L	20		20		ns
			MIL	20		20		ns
5	TGLQV	Asynchronous Output Enable LOW to Output Valid (HIGH or LOW)	COM'L		25		35	ns
			MIL		30		45	ns
6	TGHQZ	Asynchronous Output Enable HIGH to Output High Z (see Note 2)	COM'L		25		30	ns
			MIL		30		40	ns
7	TGSVKH	$\overline{GS}$ to K HIGH Setup Time	COM'L	10		12		ns
			MIL	10		15		ns
8	TKHGSX	$\overline{GS}$ to K HIGH Hold Time	COM'L	0		0		ns
			MIL	0		0		ns
9	TKHQV2	Delay from K HIGH to Output Valid, for initially Hi-Z outputs	COM'L		25		35	ns
			MIL		30		45	ns
10	TKHQZ	Delay from K HIGH to Output Hi-Z (see Note 2)	COM'L		25		35	ns
			MIL		30		45	ns

See also Switching Test Circuit Diagrams.
Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in A.
2. TGHQZ and TKHQZ are measured at steady state HIGH output voltage −0.5 V and steady state LOW output voltage + 0.5 V output levels using the test load in B.

*Subgroups 7 and 8 apply to functional tests.

SWITCHING TEST CIRCUITS
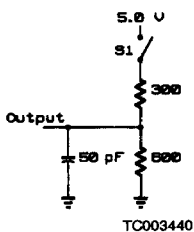
A. Output Load for all tests except TGVQZand TKHQZ
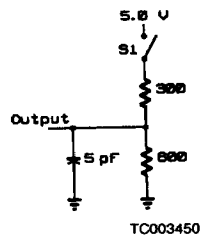

B. Output Load for TGVQZ and TKHQZ

Notes: 1. All device test loads should be located within 2″ of device output pin.
2. S₁ is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests.
S₁ is closed for all other AC tests.
3. Load capacitance includes all stray and fixture capacitance.

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
///////	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
///////	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
XXXXX	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
))))—(((	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010
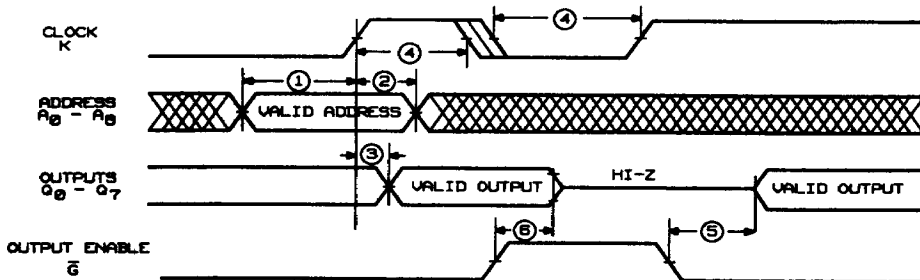
WF021110

Diagram A. Using Asynchronous Enable
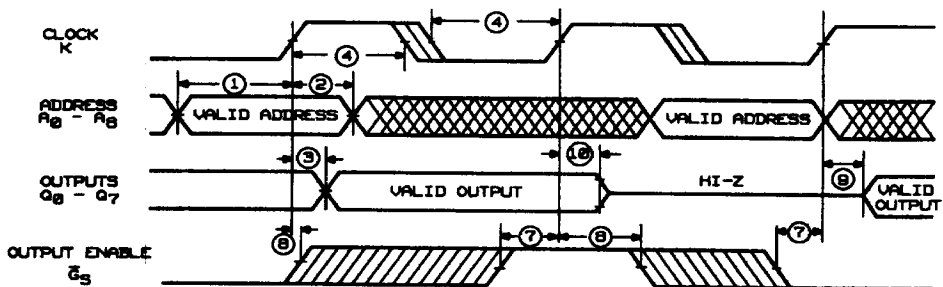
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Diagram B. Using Synchronous Enable