MINGSTAR ELECTRONIC CORPORATION

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TFT-LCD DIGITAL CONTROLLER LSI (UPS051)

PRELIMINARY SPECIFICATION

MODEL NAME: UPS051

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Appendix

A. General description:

This timing controller is a synchronizing signal controlling CMOS LSI for Unipac COG type LCD module. It accepts the digital signal and provides all the necessary control timing signals to the LCD source and gate drivers. This controller converts the digital input data to the analog alternated and amplified signals for the driving of the TFT-LCD panel. This controller also supports different resolution modes.

B. Feature:

* Single power supply : +5.0 Volts.
* Low power consumption.
* 64 pins LQFP.
* Built-In PWM circuit.
* Built-In polarity inverted circuit.
* Provides timing scan signals for Left / Right and Up / Down shift control.
* Built-In GAMMA correction function.
* Multi-resolution modes.
* Optional 3.3V input level.
* NTSC/PAL system timing

C. Pin description:

Pin-no	Symbol	I/O	Description	Remark
1	DCLK	I	Data clock input.	
2	STHR	O	Source driver start pulse. When (1).H_DIR=L, STHR is output pin of start pulse. (2).H_DIR=H, STHR is high impedance state.	
3	STHL	O	Source driver start pulse. When (1).H_DIR=L, STHL is high impedance state. (2).H_DIR=H, STHL is output pin of start pulse.	
4	STVR	O	Gate driver start pulse. When (1).V_DIR=L, STVR is output pin of start pulse. (2).V_DIR=H, STVR is high impedance state.	
5	STVL	O	Gate driver start pulse. When (1).V_DIR=L, STVL is high impedance state. (2).V_DIR=H, STVL is output pin of start pulse.	
6	VOE_OUT	O	Gate driver output enable control signal.	
7	V_CK	O	Gate driver shift clock.	
8	HOE_OUT	O	Source driver output enable control signal.	
9	VCC1	-	Power pin for digital circuits.	
10	VCI	I	Test pin, pull to ground.	
11	GND1	-	Ground pin for digital circuit.	
12	GME	I	Gamma correction enable control signal. (Normally pulled-up)	Note 1
13	HSD	I	Horizontal synchronization signal, negative polarity.	
14	VSD	I	Vertical synchronization signal, negative polarity.	
15	Q1H_OUT	O	Source driver sample & hold sequence control signal.	
16	PFRP_OUT	O	Polarity alternating signal for Vcom.	
17	GND2	-	Ground pin for PWM circuits.	
18	VCC2	-	Power pin for PWM circuits.	
19	PWM_OUT3	O	PWM output.	
20	FBK3	I	Reference voltage feedback.	
21	GND3	-	Ground pin for PWM circuits.	
22	VCC3	-	Power pin for PWM circuits.	
23	PWM_OUT2	O	PWM output.	
24	PWM_OUT1	O	PWM output.	
25	FBK1	I	Reference voltage feedback.	
26	FBK2	I	Reference voltage feedback.	
27	RSC	I	Resolution mode selection pin. (Normally pulled-up)	Note 2
28	UD_OUT	O	Inverted V_DIR signal output.	
29	LR_OUT	O	Inverted H_DIR signal output.	
30	V_DIR	I	Up/Down scan control pin. (Normally pulled-up)	
31	H_DIR	I	Left/Right scan control pin. (Normally pulled-up)	

Pin-no	Symbol	I/IO	Description	Remark
32	IN1	I	Test pin, pull to ground.	
33	VCC4	-	Power pin for digital circuits of DAC.	
34	VIN	I	Test pin, pull to ground.	
35	NPC	I	NTSC/PAL system setting pin (Normally pulled-up , NTSC)	Note 3
36	GND4	-	Ground pin for digital circuit of ADC and DAC.	
37	IOUT	O	DAC setting pin.	
38	VTEST	I	Vertical timing test mode selection. (Normally pulled-up)	
39	GR_IN	I	Global reset. It should be connected to Vcc in normal operation. If connected to GND, the controller is in reset state. (Normally pulled-up)	
40	VOUT3	O	Alternated, amplified video output.	
41	RSB	I	Resolution mode selection pin. (Normally pulled-up)	Note 2
42	VOUT2	O	Alternated, amplified video output.	
43	RSA	I	Resolution mode selection pin. (Normally pulled-up)	Note 2
44	VOUT1	O	Alternated, amplified video output.	
45	VCC5	-	Power pin for analog circuits of DAC.	
46	GND5	-	Ground pin for analog circuits of DAC.	
47	VG	I	Setting pin of DAC.	
48	VREF	I	Reference voltage setting pin of DAC.	
49	IREF	I	Reference current setting pin of DAC.	
50	DDX0	I	Digital data input, LSB.	
51	DDX1	I	Digital data input.	
52	DDX2	I	Digital data input.	
53	DDX3	I	Digital data input.	
54	GND1	-	Ground pin for digital circuits.	
55	VCC3IO	-	Power pin for 3.3V input optional.	Note 4
56	VCC1	-	Power pin for digital circuits.	
57	DDX4	I	Digital data input	
58	DDX5	I	Digital data input	
59	DDX6	I	Digital data input	
60	DDX7	I	Digital data input, MSB.	
61	CPH3_OUT	O	Source driver shift clock .	
62	CPH2_OUT	O	Source driver shift clock .	
63	CPH1_OUT	O	Source driver shift clock .	
64	DEM	I	Data enable control signal. (Normally pulled-up)	

Note 1: GME=H , Gamma correction (Normally pulled-up)
GME=L , No gamma correction
Note 2: Use RSA , RSB and RSC to select different resolution modes :

Resolution mode	RSA	RSB	RSC
220× 280	L	L	L
220 × 528	H	H	L
234× 480 (2.5")	H	H	H
234× 480 (4.0")	L	L	H
234× 960	H	L	H
234× 1152	L	H	L
234× 1440	L	H	H

Note 3: NPC=H , NTSC System (Normally pulled-up)
NPC=L , PAL System

Note 4: When connected to 3.3V , the input level of I/Ps (DEM , DCLK , HSD , VSD , V_DIR , H_DIR , DDX0 ~ DDX7) is 3.3V , and when connected to 5.0V , the input level of I/Ps are 5.0V .

D. DC characteristics

a. Absolute maximum ratings:

Symbol	Parameter	Rating	Units	Remark
V_{CC}	Power supply	-0.3 to 6.0	V	Note 1
V_{IN}	Input voltage	-0.3 to VCC + 0.3	V	
V_{OUT}	Output voltage	-0.3 to VCC + 0.3	V	
T_{STG}	Storage temperature	-40 to 95	℃	

Note 1: For all V_{CC} inputs, including V_{CC1}, V_{CC2}, V_{CC3}, V_{CC4}, V_{CC5} and V_{CC3IO} .

b. Recommended operating conditions:

Symbol	Parameter	Min	Typ	Max	Units	Remark
V_{CC}	Power supply	4.75	5.0	5.25	V	Note 1
V_{IN}	Input voltage	0	-	V_{CC}	V	
T_{OPR}	Operating temperature	0	25	85	℃	

Note 1: For all V_{CC} inputs, including V_{CC1}, V_{CC2}, V_{CC3}, V_{CC4} , V_{CC5} and V_{CC3IO} .

c. General DC characteristics:

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IL}	Input leakage current	no pull-up or pull-down	-1	-	1	μA
I_{OZ}	Tri-state leakage current		-10	-	10	μA
C_{IN}	Input capacitance		-	3	-	pF
C_{OUT}	Output capacitance		3	-	6	pF
C_{BID}	Bi-directional buffer capacitance		3	-	6	pF

d. DC electrical characteristics for 3.3V operation:
(Under recommended operating conditions and V_{CC}=3.0V～3.6V, Tj= 0℃ to +115℃)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Remark
V_{IL}	Input Low voltage	CMOS	-	-	0.3× V_{CC}	V	Note 1
V_{IH}	Input High voltage	CMOS	0.7× V_{CC}	-	-	V	Note 1
V_{t-}	Schmitt trigger negative going threshold voltage	CMOS	-	1.22	-	V	
V_{t+}	Schmitt trigger positive going threshold voltage	CMOS	-	2.08	-	V	
V_{OL}	Output low voltage	I_{OL}=2,4,8,12, 16,24mA	-	-	0.4	V	
V_{OH}	Output high voltage	I_{OH}=2,4,8,12, 16,24mA	2.4	-	-	V	
R_I	Input pull up/down resistance	Vil=0V or Vih=V_{CC}	-	75	-	KΩ	

Note 1: The applicable pins are DEM, DCLK, HSD, VSD, V_DIR, H_DIR DDX0 ～ DDX7.

e. DC electrical characteristics for 5V operation:

(Under recommended operating conditions and V_{CC}=4.75V～5.25V, Tj= 0℃ to +115℃)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low voltage	CMOS	-	-	0.3× V_{CC}	V
V_{IH}	Input High voltage	CMOS	0.7× V_{CC}	-	-	V
V_{t-}	Schmitt trigger negative going threshold voltage	CMOS	-	1.84	-	V
V_{t+}	Schmitt trigger positive going threshold voltage	CMOS	-	3.22	-	V
V_{OL}	Output low voltage	I_{OL}=2,4,8,12,16,24mA	-	-	0.4	V
V_{OH}	Output high voltage	I_{OH}=2,4,8,12,16,24mA	3.5	-	-	V
R_I	Input pull up/down resistance	Vil=0V or Vih=V_{CC}	-	50	-	KΩ

f. Current consumption for different resolution modes:

1. 280 mode:

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Remark
Current for V_{CC1}	I_{CC1}	V_{CC1}=+5V	-	5.5	-	mA	Pin 9 + Pin 56
Current for V_{CC2} + V_{CC3}	I_{CC2} +I_{CC3}	V_{CC2} , V_{CC3} =+5V	-	2.5	-	mA	Pin 18+Pin 22
Current for V_{CC4}	I_{CC4}	V_{CC4}=+5V	-	1	-	mA	
Current for V_{CC5}	I_{CC5}	V_{CC5}=+5V	-	39	-	mA	
Current for V_{CC3IO}	I_{CC3IO}	V_{CC3IO}=+5V	-	0.2	-	mA	
		V_{CC3IO}=+3.3V	-	0.2	-	mA	

2. 480 mode:

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Remark
Current for V_{CC1}	I_{CC1}	V_{CC1}=+5V	-	8.5	-	mA	Pin 9 + Pin 56
Current for V_{CC2} + V_{CC3}	I_{CC2} +I_{CC3}	V_{CC2} , V_{CC3} =+5V	-	2.6	-	mA	Pin 18+Pin 22
Current for V_{CC4}	I_{CC4}	V_{CC4}=+5V	-	1.5	-	mA	
Current for V_{CC5}	I_{CC5}	V_{CC5}=+5V	-	40	-	mA	
Current for V_{CC3IO}	I_{CC3IO}	V_{CC3IO}=+5V	-	0.2	-	mA	
		V_{CC3IO}=+3.3V	-	0.2	-	mA	

3. 528 mode:

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Remark
Current for V_{CC1}	I_{CC1}	V_{CC1}=+5V	-	9	-	mA	Pin 9 + Pin 56
Current for V_{CC2} + V_{CC3}	I_{CC2} +I_{CC3}	V_{CC2} , V_{CC3} =+5V	-	2.7	-	mA	Pin 18+Pin 22
Current for V_{CC4}	I_{CC4}	V_{CC4}=+5V	-	1.3	-	mA	
Current for V_{CC5}	I_{CC5}	V_{CC5}=+5V	-	41	-	mA	
Current for V_{CC3IO}	I_{CC3IO}	V_{CC3IO}=+5V	-	0.2	-	mA	
		V_{CC3IO}=+3.3V	-	0.2	-	mA	

4. 1152 mode:

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Remark
Current for V_{CC1}	I_{CC1}	V_{CC1}=+5V	-	19.6	-	mA	Pin 9 + Pin 56
Current for V_{CC2} + V_{CC3}	I_{CC2} +I_{CC3}	V_{CC2} , V_{CC3} =+5V	-	3.6	-	mA	Pin 18+Pin 22
Current for V_{CC4}	I_{CC4}	V_{CC4}=+5V	-	3.6	-	mA	
Current for V_{CC5}	I_{CC5}	V_{CC5}=+5V	-	41	-	mA	
Current for V_{CC3IO}	I_{CC3IO}	V_{CC3IO}=+5V	-	0.2	-	mA	
		V_{CC3IO}=+3.3V	-	0.2	-	mA	

5. 960 mode:

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Remark
Current for V_{CC1}	I_{CC1}	V_{CC1}=+5V	-	17.0	-	mA	Pin 9 + Pin 56
Current for V_{CC2} + V_{CC3}	I_{CC2} +I_{CC3}	V_{CC2} , V_{CC3} =+5V	-	3.2	-	mA	Pin 18+Pin 22
Current for V_{CC4}	I_{CC4}	V_{CC4}=+5V	-	3.2	-	mA	
Current for V_{CC5}	I_{CC5}	V_{CC5}=+5V	-	41	-	mA	
Current for V_{CC3IO}	I_{CC3IO}	V_{CC3IO}=+5V	-	0.2	-	mA	
		V_{CC3IO}=+3.3V	-	0.2	-	mA	

6. 1440 mode:

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Remark
Current for V_{CC1}	I_{CC1}	V_{CC1}=+5V	-	24	-	mA	Pin 9 + Pin 56
Current for V_{CC2} + V_{CC3}	I_{CC2} +I_{CC3}	V_{CC2} , V_{CC3} =+5V	-	4.0	-	mA	Pin 18+Pin 22
Current for V_{CC4}	I_{CC4}	V_{CC4}=+5V	-	4.0	-	mA	
Current for V_{CC5}	I_{CC5}	V_{CC5}=+5V	-	41	-	mA	
Current for V_{CC3IO}	I_{CC3IO}	V_{CC3IO}=+5V	-	0.2	-	mA	
		V_{CC3IO}=+3.3V	-	0.2	-	mA	

E. AC characteristics

a. Input signal characteristics

Timing diagrams of input signal are shown in Fig 1 and Fig 2.

1. 280 mode

1-1. Input timing chart

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK	Frequency	1/Tc	-	5.67	-	MHz	
	High time	Tch	-	-	-	ns	
	Low time	Tcl	-	-	-	ns	
HSD	Period	TH	60	63.56	67	μs	
			-	360	-	CLK	
	Display period	THd	-	49.4	-	μs	
			280			CLK	
	Pulse width	THp	5	25	-	CLK	
	Hsync-CLK timing	THc	20	-	Tc-20	ns	
VSD	Period	TV	-	16.6	-	ms	
			-	262	-	TH	
	Display period	TVd	-	13.97	-	ms	
			220			TH	
	Pulse width	TVp	3	-	-	TH	
DATA R0~R7 G0~G7 B0~B7	CLK-DATA timing	Tds	10	-	-	ns	
	DATA-CLK timing	Tdh	10	-	-	ns	
	Rising time Falling time	Tdrf	-	-	10	ns	

1-2. Horizontal display position

1-2-1. ENAB mode:

The horizontal display position is determined by DEM signal and the input data corresponding to the rising edge of DEM.

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
Enable signal	Setup time	Tes	-	TBD	-	ns	
	Pulse width	Tep	-	288	-	CLK	
Hsync-Enable signal timing		THe	33	-	57	CLK	

1-2-2. Fix mode:

When DEM is fixed "Low", the display starts from the data of C62(clock) as shown in Fig 2. Be careful that the module does not work when DEM is fixed "High".

1-3. Vertical display position

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Vertical display position	TVS		25		H	NTSC
			34		H	PAL

2. 480 mode

2-1. Input timing chart

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK	Frequency	1/Tc	-	9.70	-	MHz	
	High time	Tch	-	-	-	ns	
	Low time	Tcl	-	-	-	ns	
HSD	Period	TH	60	63.56	67	μs	
			-	617	-	CLK	
	Display period	THd	-	49.4	-	μs	
			480			CLK	
	Pulse width	THp	5	44	-	CLK	
	Hsync-CLK timing	THc	20	-	Tc-20	ns	
VSD	Period	TV	-	16.6	-	ms	
			-	262	-	TH	
	Display period	TVd	-	14.83	-	ms	
			234			TH	
	Pulse width	TVp	3	-	-	TH	
DATA R0~R7 G0~G7 B0~B7	CLK-DATA timing	Tds	10	-	-	ns	
	DATA-CLK timing	Tdh	10	-	-	ns	
	Rising time Falling time	Tdrf	-	-	10	ns	

2-2. Horizontal display position

2-2-1. ENAB mode:

The horizontal display position is determined by DEM signal and the input data corresponding to the rising edge of DEM.

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
Enable signal	Setup time	Tes	-	TBD	-	ns	
	Pulse width	Tep	-	480	-	CLK	
Hsync-Enable signal timing		THe	60	-	105	CLK	

2-2-2. Fix mode:

When DEM is fixed "Low", the display starts from the data of C106(clock) as shown in Fig 2. Be careful that the module does not work when DEM is fixed "High".

2-3. Vertical display position

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Vertical display position	TVS		18		H	NTSC
			27		H	PAL

3. 528 mode

3-1. Input timing chart

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK	Frequency	1/Tc	-	10.7	-	MHz	
	High time	Tch	-	-	-	ns	
	Low time	Tcl	-	-	-	ns	
HSD	Period	TH	60	63.56	67	μs	
			-	679	-	CLK	
	Display period	THd	-	49.4	-	μs	
			528			CLK	
	Pulse width	THp	5	48	-	CLK	
	Hsync-CLK timing	THc	20	-	Tc-20	ns	

VSD	Period	TV	-	16.6	-	ms	
			-	262	-	TH	
	Display period	TVd	-	13.97	-	ms	
			220			TH	
	Pulse width	TVp	3	-	-	TH	
DATA R0~R7 G0~G7 B0~B7	CLK-DATA timing	Tds	10	-	-	ns	
	DATA-CLK timing	Tdh	10	-	-	ns	
	Rising time Falling time	Tdrf	-	-	10	ns	

3-2. Horizontal display position

3-2-1. ENAB mode:

The horizontal display position is determined by DEM signal and the input data corresponding to the rising edge of DEM.

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
Enable signal	Setup time	Tes	-	TBD	-	ns	
	Pulse width	Tep	-	576	-	CLK	
Hsync-Enable signal timing		THe	57	-	90	CLK	

3-2-2. Fix mode:

When DEM is fixed "Low", the display starts from the data of C118(clock) as shown in Fig 2. Be careful that the module does not work when DEM is fixed "High".

3-3. Vertical display position

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Vertical display position	TVS		25		H	NTSC
			34		H	PAL

4. 1152 mode

4-1. Input timing chart

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK	Frequency	1/Tc	-	23.3	-	MHz	
	High time	Tch	-	-	-	ns	
	Low time	Tcl	-	-	-	ns	
HSD	Period	TH	60	63.56	67	μs	
			-	1482	-	CLK	
	Display period	THd	-	49.4	-	μs	
			1152			CLK	
	Pulse width	THp	5	109	-	CLK	
	Hsync-CLK timing	THc	20	-	Tc-20	ns	
VSD	Period	TV	-	16.6	-	ms	
			-	262	-	TH	
	Display period	TVd	-	14.83	-	ms	
			234			TH	
	Pulse width	TVp	3	-	-	TH	
DATA R0~R7 G0~G7 B0~B7	CLK-DATA timing	Tds	10	-	-	ns	
	DATA-CLK timing	Tdh	10	-	-	ns	
	Rising time Falling time	Tdrf	-	-	10	ns	

4-2. Horizontal display position

4-2-1. ENAB mode:

The horizontal display position is determined by DEM signal and the input data corresponding to the rising edge of DEM.

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
Enable signal	Setup time	Tes	-	TBD	-	ns	
	Pulse width	Tep	-	1152	-	CLK	
Hsync-Enable signal timing		THe	108	-	243	CLK	

4-2-2. Fix mode:

When DEM is fixed "Low", the display starts from the data of C247(clock) as shown in Fig 2. Be careful that the module does not work when DEM is fixed "High".

4-3. Vertical display position

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Vertical display position	TVS		18		H	NTSC
			27		H	PAL

5. 960 mode

5-1. Input timing chart

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK	Frequency	1/Tc	-	19.4	-	MHz	
	High time	Tch	-	-	-	ns	
	Low time	Tcl	-	-	-	ns	
HSD	Period	TH	60	63.56	67	μs	
			-	1235	-	CLK	
	Display period	THd	-	49.4	-	μs	
			960			CLK	
	Pulse width	THp	5	91	-	CLK	
	Hsync-CLK timing	THc	20	-	Tc-20	ns	
VSD	Period	TV	-	16.6	-	ms	
			-	262	-	TH	
	Display period	TVd	-	14.83	-	ms	
			234			TH	
	Pulse width	TVp	3	-	-	TH	
DATA R0~R7 G0~G7 B0~B7	CLK-DATA timing	Tds	10	-	-	ns	
	DATA-CLK timing	Tdh	10	-	-	ns	
	Rising time Falling time	Tdrf	-	-	10	ns	

5-2. Horizontal display position

5-2-1. ENAB mode:

The horizontal display position is determined by DEM signal and the input data corresponding to the rising edge of DEM.

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
Enable signal	Setup time	Tes	-	TBD	-	ns	
	Pulse width	Tep	-	960	-	CLK	
Hsync-Enable signal timing		THe	97	-	204	CLK	

5-2-2. Fix mode:

When DEM is fixed "Low", the display starts from the data of C207(clock) as shown in Fig 2. Be careful that the module does not work when DEM is fixed "High".

5-3. Vertical display position

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Vertical display position	TVS		18		H	NTSC
			27		H	PAL

6. 1440 mode

6-1. Input timing chart

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK	Frequency	1/Tc	-	29.1	-	MHz	
	High time	Tch	-	-	-	ns	
	Low time	Tcl	-	-	-	ns	
HSD	Period	TH	60	63.56	67	μs	
			-	1853	-	CLK	
	Display period	THd	-	49.4	-	μs	
			1440			CLK	
	Pulse width	THp	5	137	-	CLK	
	Hsync-CLK timing	THc	20	-	Tc-20	ns	
VSD	Period	TV	-	16.6	-	ms	
			-	262	-	TH	
	Display period	TVd	-	14.83	-	ms	
			234			TH	
	Pulse width	TVp	3	-	-	TH	
DATA R0~R7 G0~G7 B0~B7	CLK-DATA timing	Tds	10	-	-	ns	
	DATA-CLK timing	Tdh	10	-	-	ns	
	Rising time Falling time	Tdrf	-	-	10	ns	

6-2. Horizontal display position

6-2-1. ENAB mode:

The horizontal display position is determined by DEM signal and the input data corresponding to the rising edge of DEM.

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
Enable signal	Setup time	Tes	-	TBD	-	ns	
	Pulse width	Tep	-	1440	-	CLK	
Hsync-Enable signal timing		THe	145	-	305	CLK	

6-2-2. Fix mode:

When DEM is fixed "Low", the display starts from the data of C309(clock) as shown in Fig 2. Be careful that the module does not work when DEM is fixed "High".

6-3. Vertical display position

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Vertical display position	TVS		18		H	NTSC
			27		H	PAL

b. Output signal characteristics

1. 280 mode

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Rising time	t_r	-	-	10	ns	Note 1
Falling time	t_f	-	-	10	ns	Note 1
Clock high and low level pulse width	t_{CPH}	-	3	-	t_{DCLK}	CPH1~CPH3_OUT
Clock pulse duty	t_{CWH}	40	50	60	%	CPH1~CPH3_OUT
3 φ clock phase difference	t_{C12} t_{C23} t_{C31}	-	t_{CPH} /3	-	ns	
STH setup time	t_{SUH}	-	t_{CPH} /6	-	ns	
STH pulse width	t_{STH}	-	1	-	t_{CPH}	
HOE_OUT pulse width	t_{OEH}	-	3	-	t_{CPH}	
Sample & hold disable time	t_{DIS1}	-	11	-	t_{CPH}	
VOE_OUT pulse width	t_{OEV}	-	5	-	t_{CPH}	
V_CK pulse width	t_{CKV}	-	5	-	t_{CPH}	
HSD/I-HOE_OUT timing difference	t_1	-	8	-	t_{CPH}	
HSD/I-V_CK timing difference	t_2	-	6	-	t_{CPH}	
HSD/I-VOE_OUT timing difference	t_3	-	2	-	t_{CPH}	
STV setup time	t_{SUV}	-	3	-	t_{CPH}	
STV pulse width	t_{STV}	-	1	-	t_H	
VSD/I-STVR timing difference(V_DIR="L")	t_{VS1}	-	16	-	t_H	
VSD/I-STVL timing difference(V_DIR="H")	t_{VS2}	-	20	-	t_H	
HOE-STV timing difference	t_{OES}	-	2	-	t_H	

Note 1: For all of the logic signals.

2. 480 mode (2.5")

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Rising time	t_r	-	-	10	ns	Note 1
Falling time	t_f	-	-	10	ns	Note 1
Clock high and low level pulse width	t_{CPH}	-	3	-	t_{DCLK}	CPH1~CPH3_OUT
Clock pulse duty	t_{CWH}	40	50	60	%	CPH1~CPH3_OUT
3 φ clock phase difference	t_{C12} t_{C23} t_{C31}	-	t_{CPH} /3	-	ns	
STH setup time	t_{SUH}	-	t_{CPH} /6	-	ns	
STH pulse width	t_{STH}	-	1	-	t_{CPH}	
HOE_OUT pulse width	t_{OEH}	-	6	-	t_{CPH}	
Sample & hold disable time	t_{DIS1}	-	17	-	t_{CPH}	
VOE_OUT pulse width	t_{OEV}	-	10	-	t_{CPH}	
V_CK pulse width	t_{CKV}	-	7	-	t_{CPH}	
HSD/I-HOE_OUT timing difference	t_1	-	12	-	t_{CPH}	
HSD/I-V_CK timing difference	t_2	-	11	-	t_{CPH}	
HSD/I-VOE_OUT timing difference	t_3	-	2	-	t_{CPH}	
STV setup time	t_{SUV}	-	8	-	t_{CPH}	
STV pulse width	t_{STV}	-	1	-	t_H	
VSD/I-STVR timing difference(V_DIR="L")	t_{VS1}	-	16	-	t_H	
VSD/I-STVL timing difference(V_DIR="H")	t_{VS2}	-	20	-	t_H	
HOE-STV timing difference	t_{OES}	-	2	-	t_H	

Note 1: For all of the logic signals.

3. 480 mode (4.0")

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Rising time	t_r	-	-	10	ns	Note 1
Falling time	t_f	-	-	10	ns	Note 1
Clock high and low level pulse width	t_{CPH}	-	3	-	t_{DCLK}	CPH1~CPH3_OUT
Clock pulse duty	t_{CWH}	40	50	60	%	CPH1~CPH3_OUT
3 φ clock phase difference	t_{C12} t_{C23} t_{C31}	-	t_{CPH} /3	-	ns	
STH setup time	t_{SUH}	-	t_{CPH} /6	-	ns	
STH pulse width	t_{STH}	-	1	-	t_{CPH}	
HOE_OUT pulse width	t_{OEH}	-	4	-	t_{CPH}	
Sample & hold disable time	t_{DIS1}	-	14	-	t_{CPH}	
VOE_OUT pulse width	t_{OEV}	-	14	-	t_{CPH}	
V_CK pulse width	t_{CKV}	-	25	-	t_{CPH}	
HSD/I-HOE_OUT timing difference	t_1	-	17	-	t_{CPH}	
HSD/I-V_CK timing difference	t_2	-	10	-	t_{CPH}	
HSD/I-VOE_OUT timing difference	t_3	-	2	-	t_{CPH}	
STV setup time	t_{SUV}	-	7	-	t_{CPH}	
STV pulse width	t_{STV}	-	1	-	t_H	
VSD/I-STVR timing difference(V_DIR="L")	t_{VS1}	-	16	-	t_H	
VSD/I-STVL timing difference(V_DIR="H")	t_{VS2}	-	20	-	t_H	
HOE-STV timing difference	t_{OES}	-	2	-	t_H	

Note 1: For all of the logic signals.

4. 528 mode

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Rising time	t_r	-	-	10	ns	Note 1
Falling time	t_f	-	-	10	ns	Note 1
Clock high and low level pulse width	t_{CPH}	-	3	-	t_{DCLK}	CPH1~CPH3_OUT
Clock pulse duty	t_{CWH}	40	50	60	%	CPH1~CPH3_OUT
3 φ clock phase difference	t_{C12} t_{C23} t_{C31}	-	t_{CPH} /3	-	ns	
STH setup time	t_{SUH}	-	t_{CPH} /6	-	ns	
STH pulse width	t_{STH}	-	1	-	t_{CPH}	
HOE_OUT pulse width	t_{OEH}	-	6	-	t_{CPH}	
Sample & hold disable time	t_{DIS1}	-	11	-	t_{CPH}	
VOE_OUT pulse width	t_{OEV}	-	11	-	t_{CPH}	
V_CK pulse width	t_{CKV}	-	13	-	t_{CPH}	
HSD/I-HOE_OUT timing difference	t_1	-	14	-	t_{CPH}	
HSD/I-V_CK timing difference	t_2	-	9	-	t_{CPH}	
HSD/I-VOE_OUT timing difference	t_3	-	2	-	t_{CPH}	
STV setup time	t_{SUV}	-	6	-	t_{CPH}	
STV pulse width	t_{STV}	-	1	-	t_H	
VSD/I-STVR timing difference(V_DIR="L")	t_{VS1}	-	16	-	t_H	
VSD/I-STVL timing difference(V_DIR="H")	t_{VS2}	-	20	-	t_H	
HOE-STV timing difference	t_{OES}	-	2	-	t_H	

Note 1: For all of the logic signals.

5. 1152 mode

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Rising time	t_r	-	-	10	ns	Note 1
Falling time	t_f	-	-	10	ns	Note 1
Clock high and low level pulse width	t_{CPH}	-	3	-	t_{DCLK}	CPH1~CPH3_OUT
Clock pulse duty	t_{CWH}	40	50	60	%	CPH1~CPH3_OUT
3 φ clock phase difference	t_{C12} t_{C23} t_{C31}	-	t_{CPH} /3	-	ns	
STH setup time	t_{SUH}	-	t_{CPH} /6	-	ns	
STH pulse width	t_{STH}	-	1	-	t_{CPH}	
HOE_OUT pulse width	t_{OEH}	-	12	-	t_{CPH}	
Sample & hold disable time	t_{DIS1}	-	24	-	t_{CPH}	
VOE_OUT pulse width	t_{OEV}	-	39	-	t_{CPH}	
V_CK pulse width	t_{CKV}	-	60	-	t_{CPH}	
HSD/I-HOE_OUT timing difference	t_1	-	46	-	t_{CPH}	
HSD/I-V_CK timing difference	t_2	-	22	-	t_{CPH}	
HSD/I-VOE_OUT timing difference	t_3	-	4	-	t_{CPH}	
STV setup time	t_{SUV}	-	15	-	t_{CPH}	
STV pulse width	t_{STV}	-	1	-	t_H	
VSD/I-STVR timing difference(V_DIR="L")	t_{VS1}	-	16	-	t_H	
VSD/I-STVL timing difference(V_DIR="H")	t_{VS2}	-	20	-	t_H	
HOE-STV timing difference	t_{OES}	-	2	-	t_H	

Note 1: For all of the logic signals.

6. 960 mode

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Rising time	t_r	-	-	10	ns	Note 1
Falling time	t_f	-	-	10	ns	Note 1
Clock high and low level pulse width	t_{CPH}	-	3	-	t_{DCLK}	CPH1~CPH3_OUT
Clock pulse duty	t_{CWH}	40	50	60	%	CPH1~CPH3_OUT
3 φ clock phase difference	t_{C12} t_{C23} t_{C31}	-	t_{CPH} /3	-	ns	
STH setup time	t_{SUH}	-	t_{CPH} /6	-	ns	
STH pulse width	t_{STH}	-	1	-	t_{CPH}	
HOE_OUT pulse width	t_{OEH}	-	8	-	t_{CPH}	
Sample & hold disable time	t_{DIS1}	-	29	-	t_{CPH}	
VOE_OUT pulse width	t_{OEV}	-	28	-	t_{CPH}	
V_CK pulse width	t_{CKV}	-	50	-	t_{CPH}	
HSD/I-HOE_OUT timing difference	t_1	-	33	-	t_{CPH}	
HSD/I-V_CK timing difference	t_2	-	19	-	t_{CPH}	
HSD/I-VOE_OUT timing difference	t_3	-	3	-	t_{CPH}	
STV setup time	t_{SUV}	-	15	-	t_{CPH}	
STV pulse width	t_{STV}	-	1	-	t_H	
VSD/I-STVR timing difference(V_DIR="L")	t_{VS1}	-	16	-	t_H	
VSD/I-STVL timing difference(V_DIR="H")	t_{VS2}	-	20	-	t_H	
HOE-STV timing difference	t_{OES}	-	2	-	t_H	

Note 1: For all of the logic signals.

7. 1440 mode

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Rising time	t_r	-	-	10	ns	Note 1
Falling time	t_f	-	-	10	ns	Note 1
Clock high and low level pulse width	t_{CPH}	-	3	-	t_{DCLK}	CPH1~CPH3_OUT
Clock pulse duty	t_{CWH}	40	50	60	%	CPH1~CPH3_OUT
3 φ clock phase difference	t_{C12} t_{C23} t_{C31}	-	t_{CPH} /3	-	ns	
STH setup time	t_{SUH}	-	t_{CPH} /6	-	ns	
STH pulse width	t_{STH}	-	1	-	t_{CPH}	
HOE_OUT pulse width	t_{OEH}	-	12	-	t_{CPH}	
Sample & hold disable time	t_{DIS1}	-	42	-	t_{CPH}	
VOE_OUT pulse width	t_{OEV}	-	42	-	t_{CPH}	
V_CK pulse width	t_{CKV}	-	75	-	t_{CPH}	
HSD/I-HOE_OUT timing difference	t_1	-	49	-	t_{CPH}	
HSD/I-V_CK timing difference	t_2	-	28	-	t_{CPH}	
HSD/I-VOE_OUT timing difference	t_3	-	4	-	t_{CPH}	
STV setup time	t_{SUV}	-	15	-	t_{CPH}	
STV pulse width	t_{STV}	-	1	-	t_H	
VSD/I-STVR timing difference(V_DIR="L")	t_{VS1}	-	16	-	t_H	
VSD/I-STVL timing difference(V_DIR="H")	t_{VS2}	-	20	-	t_H	
HOE-STV timing difference	t_{OES}	-	2	-	t_H	

Note 1: For all of the logic signals.

c. Video signal output characteristics(refer to the attached drawing Fig.7)

Item	Symbol	Min.	Typ.	Max.	Unit.	Remark
Video signal amplitude (Vout1, Vout2, Vout3)	V_{IAC}	-	3.5	-	V	AC Component
	V_{IDC}	-	3.15	-	V	DC Component

F. Color sequence for different resolution modes:

a. Delta type arrangement color filter :

Due to the “Delta” type arrangement of LCD’s color filter, the R.G.B data are different in odd lines and even lines. Please follow the corresponding sequence under different conditions which are shown in Tab.1

Tab.1 Color sequence for different resolution modes. (Delta type)

Scanning direction control setting	V_DIR (Note 1)	Low	Low	High	High
Display modules	H_DIR (Note 2)	High	Low	High	Low
4”: 480X 234 (MTL040DXX)	Odd Line	B R G	G R B	G B R	R B G
	Even Line	G B R	R B G	B R G	G R B
1.8”: 280X 220 (SM26X Series) 2.0”: 528X 220 (MTL020DXX) 2.5”: 480X 234 (MTL025DXX)	Odd Line	R G B	B G R	G B R	R B G
	Even Line	G B R	R B G	R G B	B G R

Note 1: V_DIR is an Up/Down scanning direction control pin of UPS051.
When V_DIR is high , the scanning direction control is from “ Down to Up “.
When V_DIR is low , the scanning direction control is from “ Up to Down “.

Note 2: H_DIR is a Left/Right scanning direction control pin of UPS051.
When LR is high, the scanning direction is from “left to Right”.
When LR is low, the scanning direction is from “right to Left”.

Note 3: The sequence specified in each column represents the order of data which should be sent to UPS051 for cycle #1, 2, 3, 4, 5, · · · ·

Note 4: The Q1H_OUT (Pin 15) signal can be used as the index to specify odd line or even line for users.

b. Stripe type arrangement color filter

The R.G.B sequences are same in odd line and even line in stripe type arrangement color filter.

Tab.2 Color sequence for different resolution modes. (Stripe type)

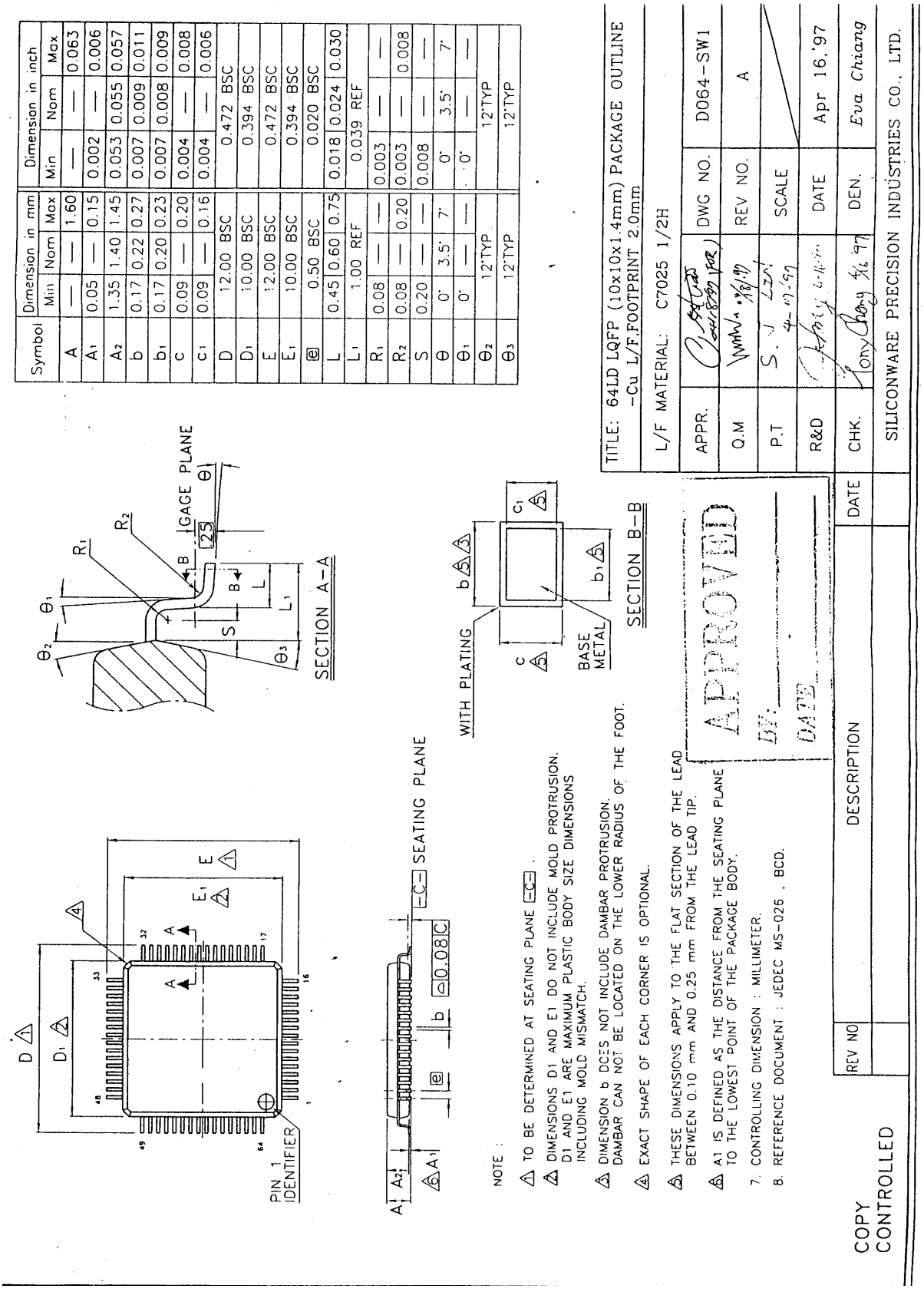
Display module	H_DIR	High	Low
6.8" : 1152× 234 (MTL068DXX) 5.6" : 960× 234 (MTL056DXX) 7.0" : 1440× 234 (MTL070DXX)	Odd line Even line	R G B	B G R

G. Reliability test item:

No.	Test items	Conditions	Remark
1	High temperature storage	Ta = 80℃ 240H	
2	Low temperature storage	Ta = -25℃ 240H	
3	High temperature operation	Ta = 60℃ 240H	
4	Low temperature operation	Ta = 0℃ 240H	
5	High temperature and high humidity	Ta = 60℃・95%RH 240H	Operation
6	Heat shock	-25℃～+80℃/50 cycles 2H/cycle	Non-operation
7	Electrostatic discharge	± 200V,200pF(0Ω),once for each terminal	Non-operation

Note : Ta is the Ambient temperature.

H. Package information



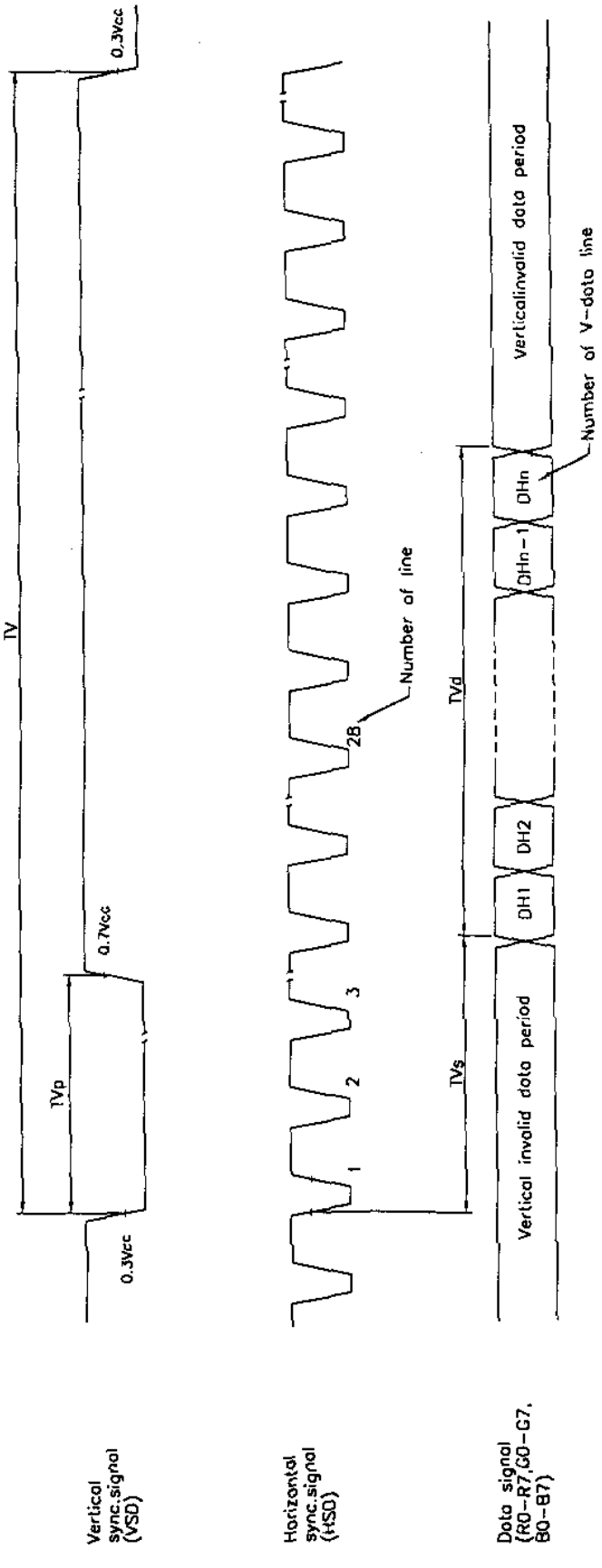


Fig.1 Input Vertical timing

File:f:\PDMEM0606\UP20DTC.dwg

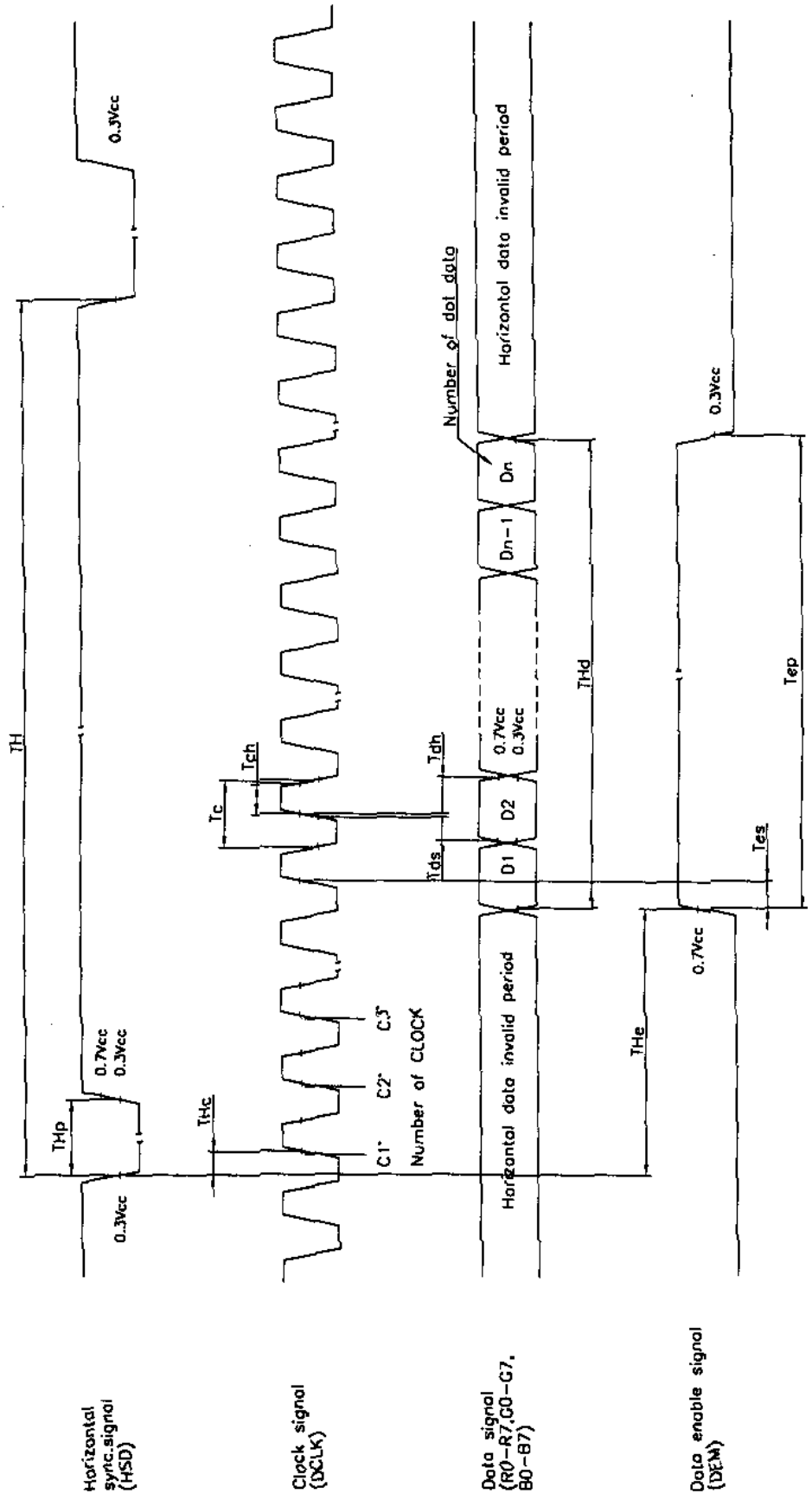


Fig.2 Input horizontal timing

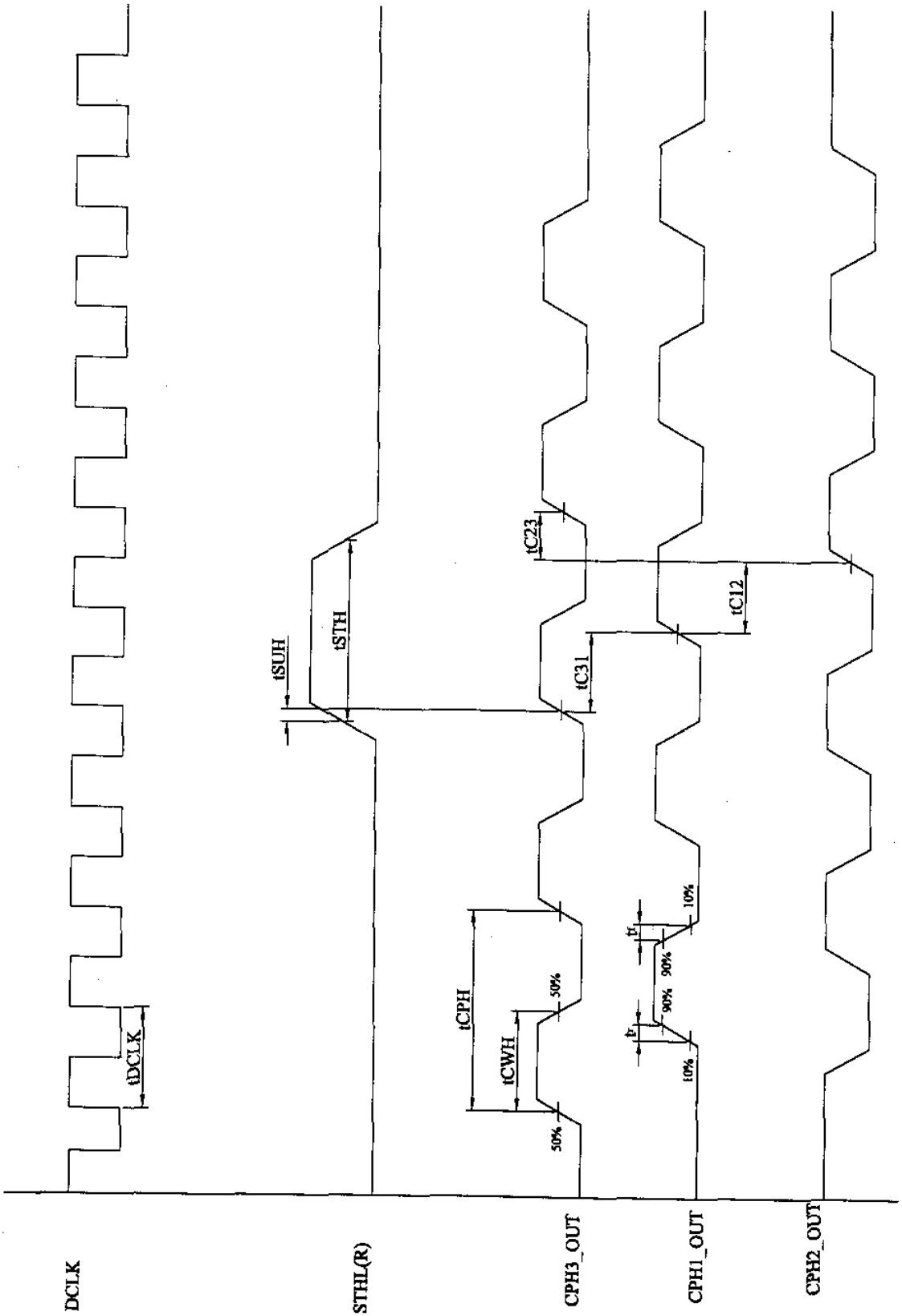


Fig.3 Sampling clock timing

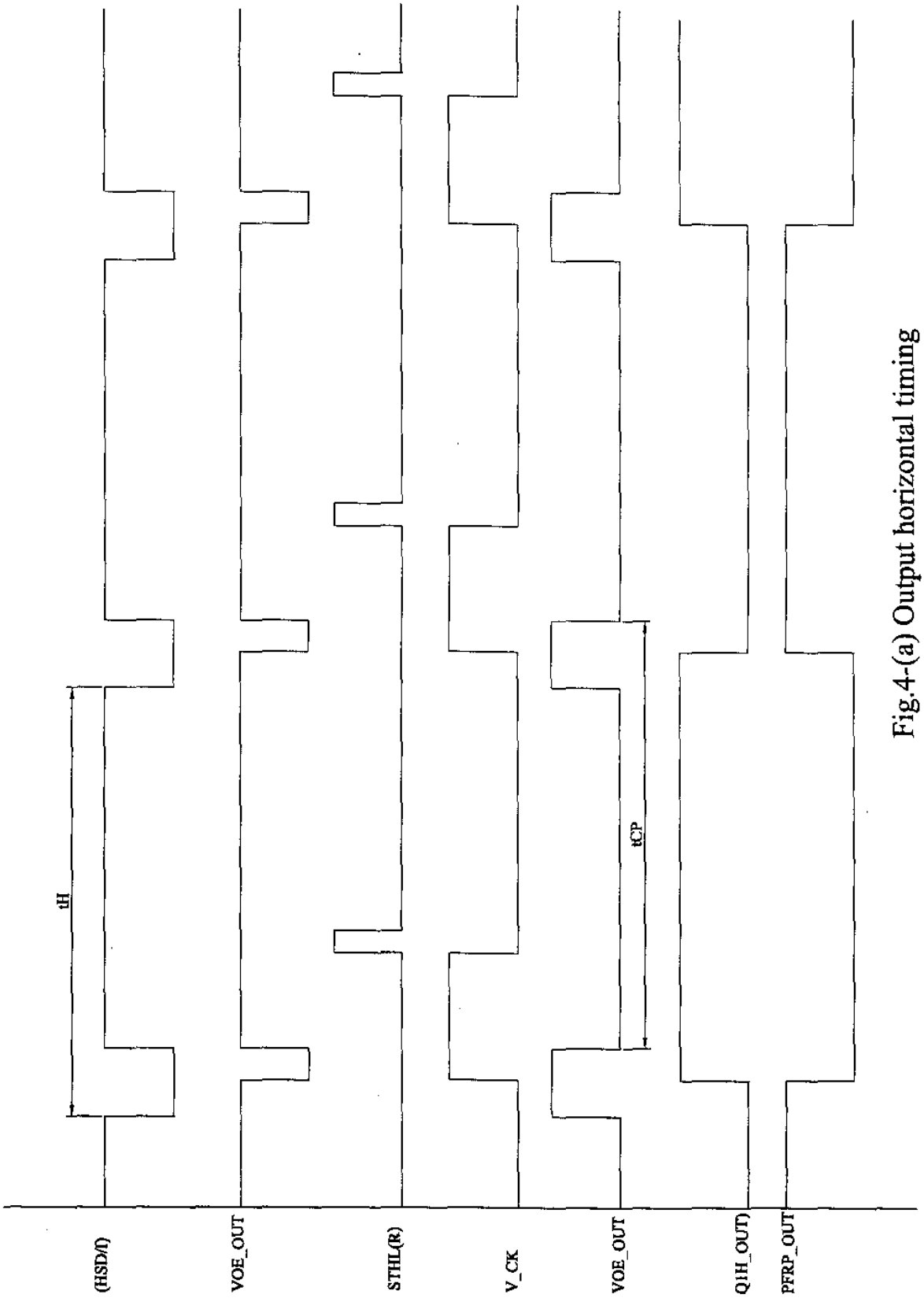


Fig.4-(a) Output horizontal timing

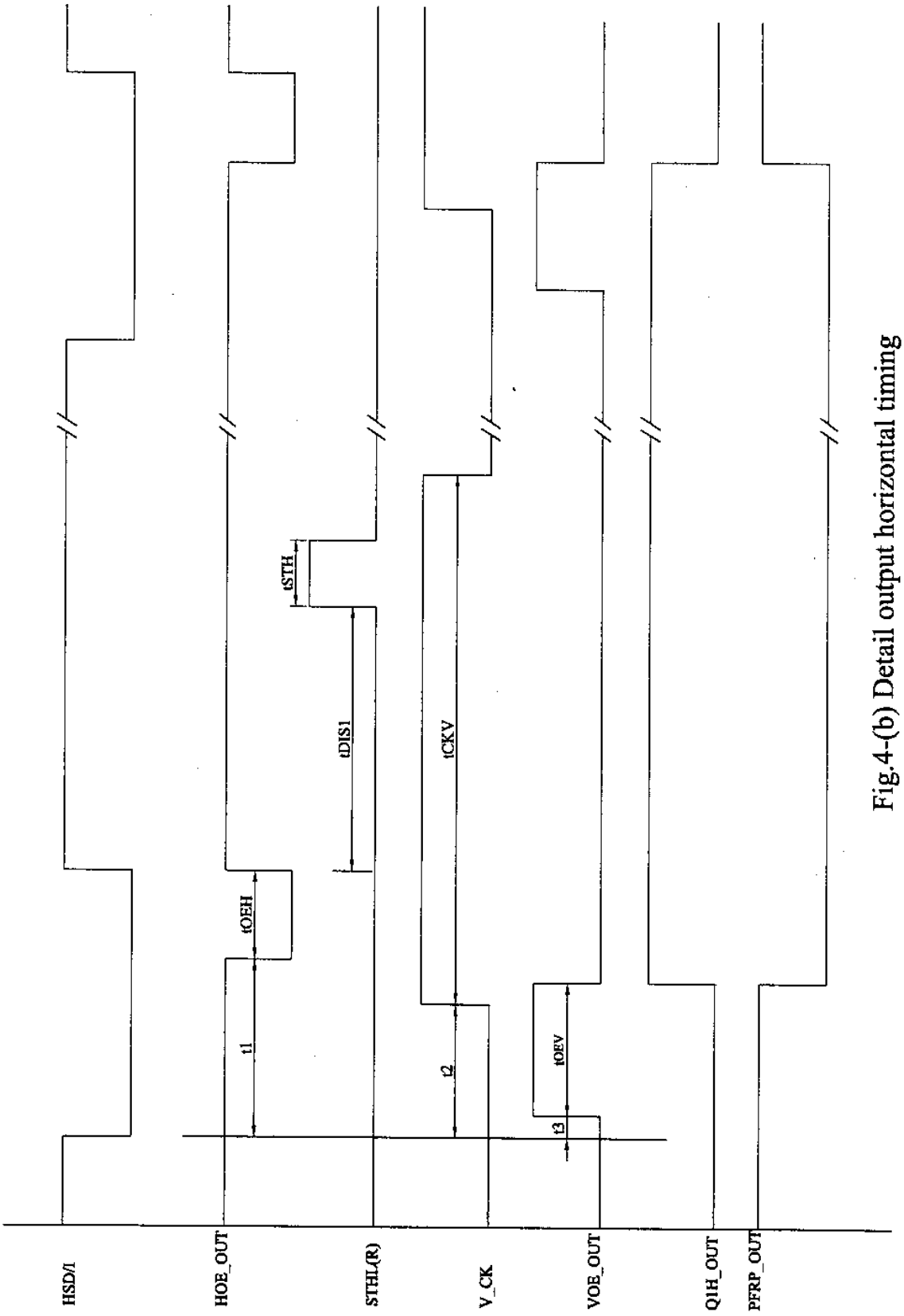


Fig.4-(b) Detail output horizontal timing

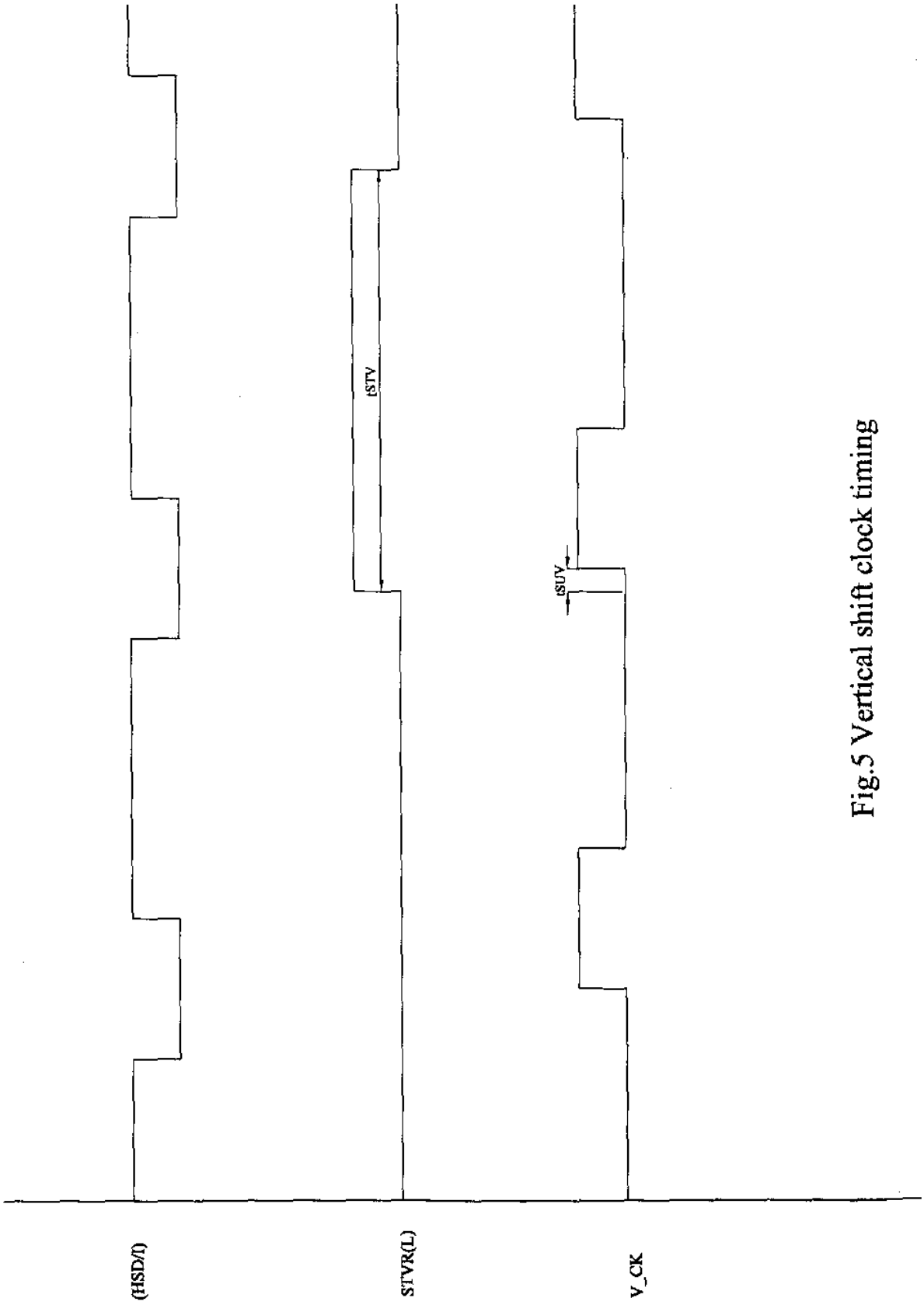


Fig.5 Vertical shift clock timing

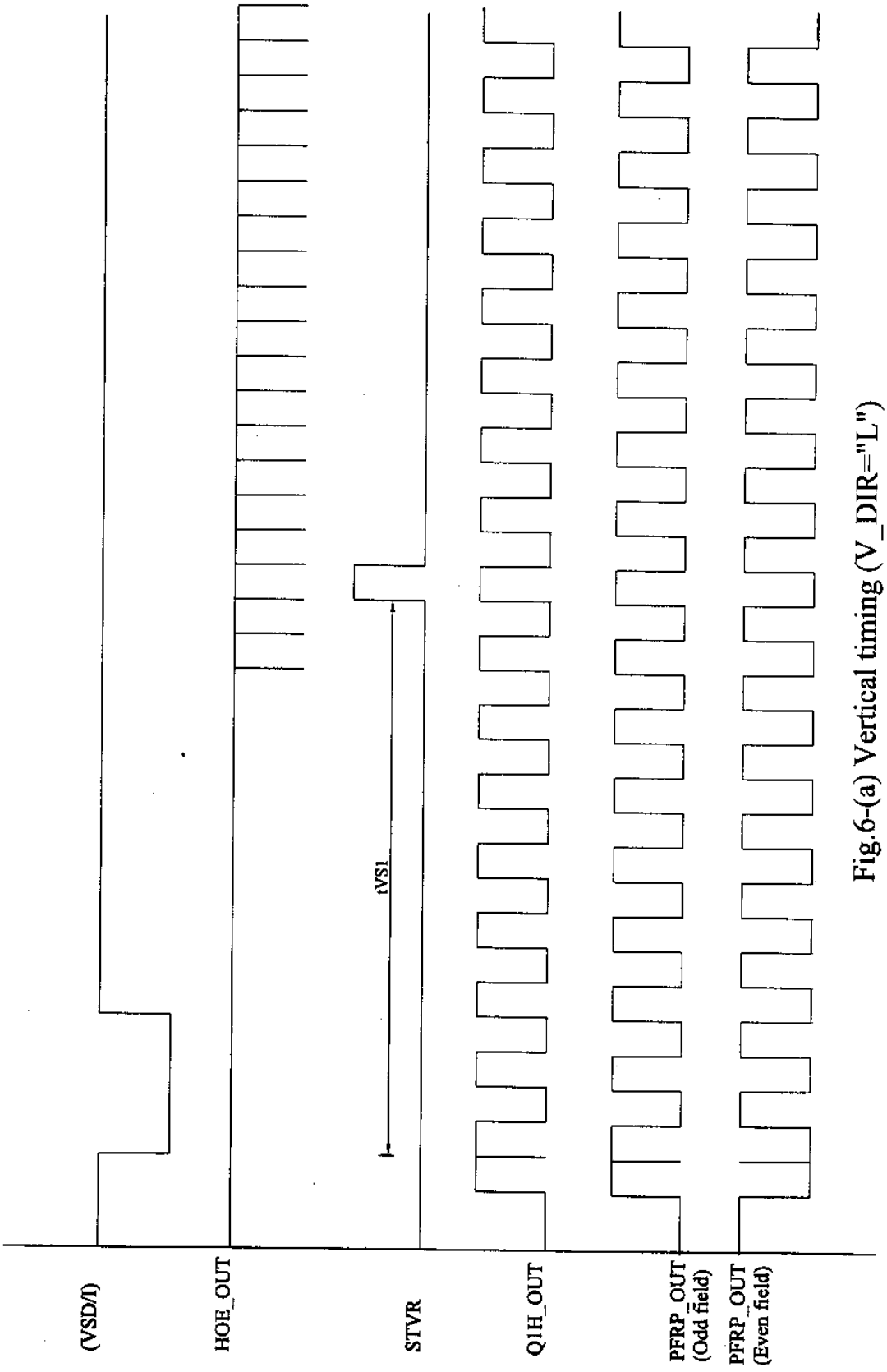


Fig.6-(a) Vertical timing (V_DIR="L")

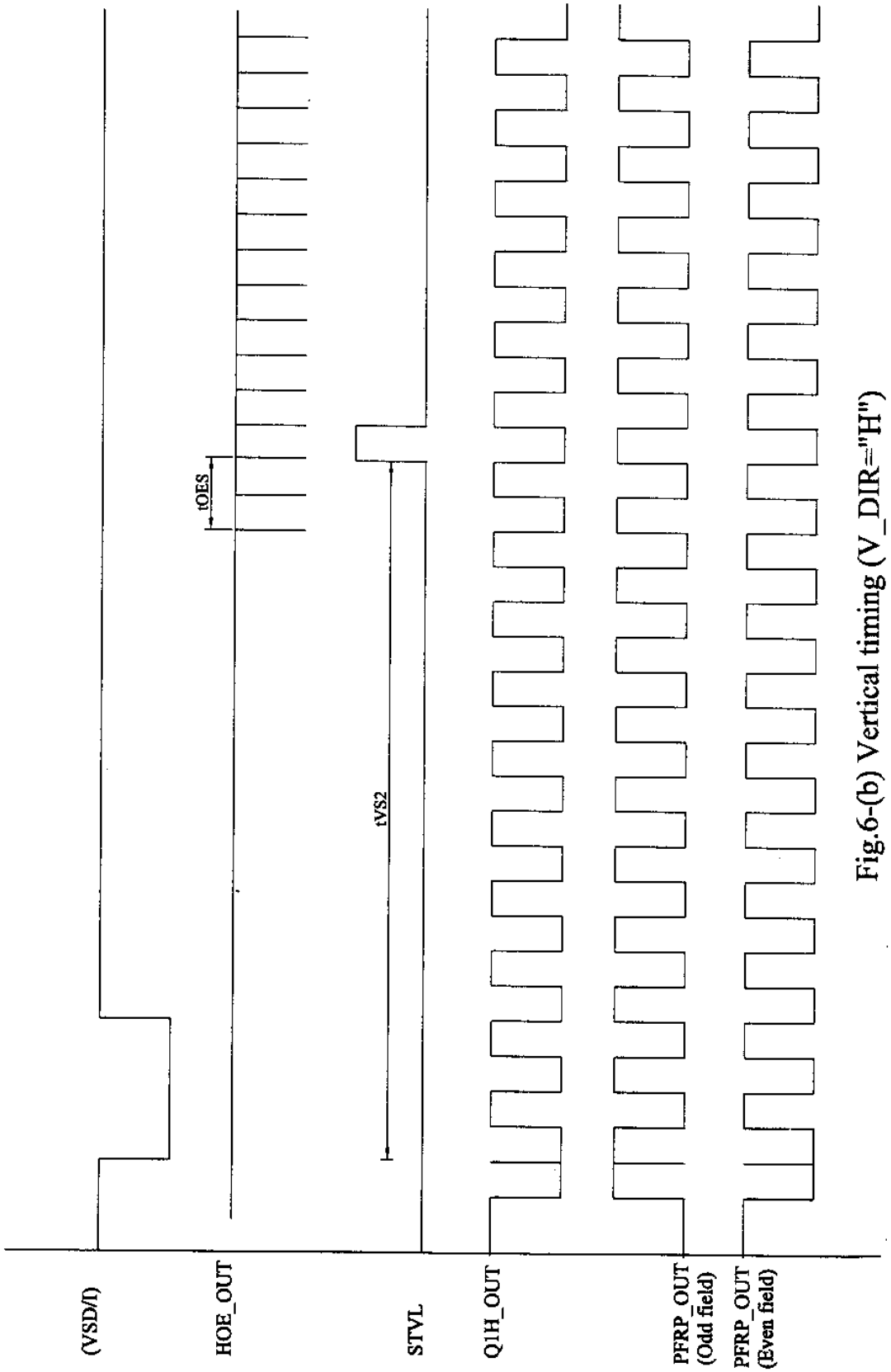


Fig.6-(b) Vertical timing (V_DIR="H")

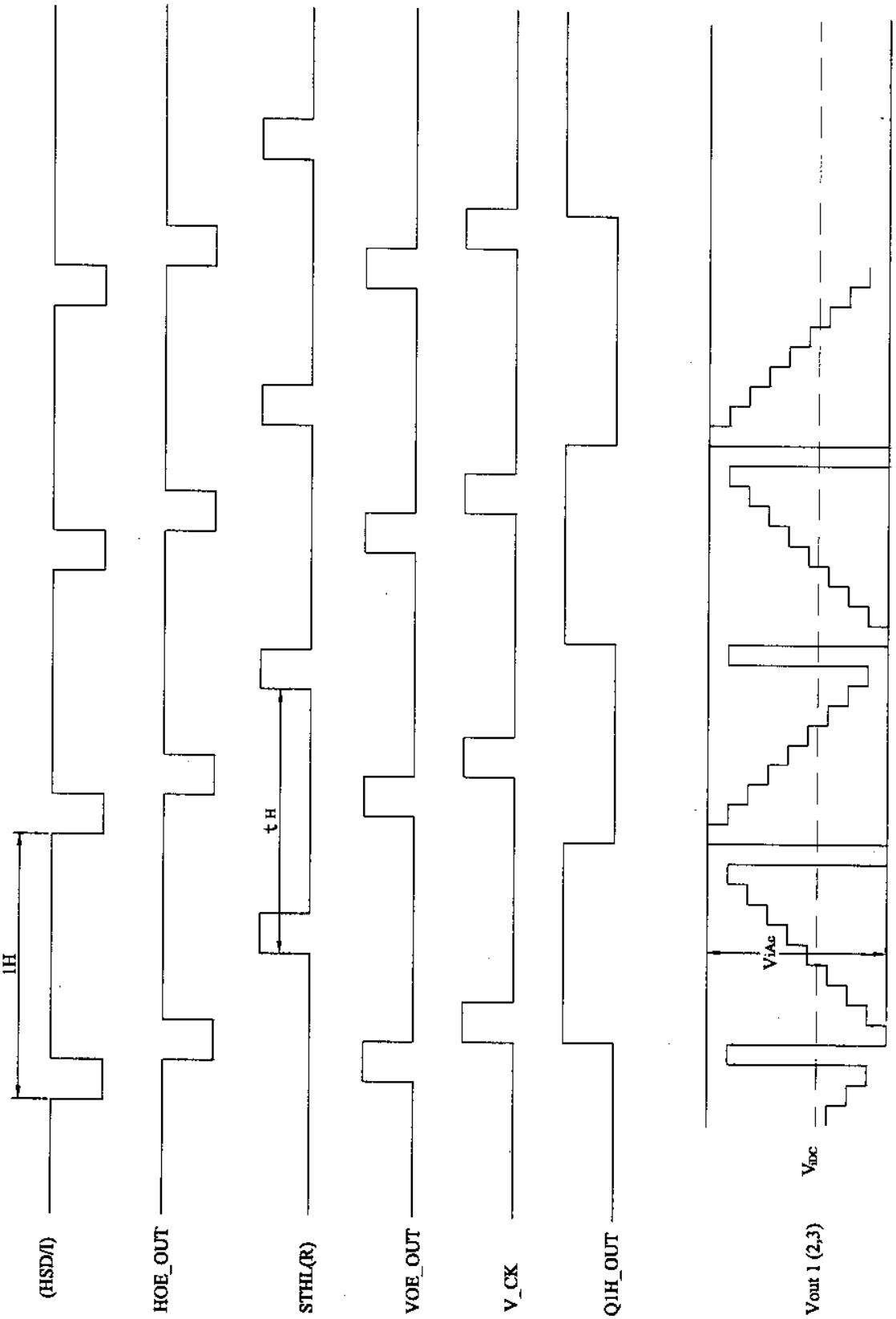


Fig.7 Vout 1(2,3) amplitude

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