Integrated Device Technology, Inc.

# 256KB AND 512KB SECONDARY CACHE MODULES FOR THE INTEL® PENTIUM™ PROCESSOR

**PRELIMINARY**
**IDT7MPV6179**
**IDT7MPV6189**
**IDT7MP6181**
**IDT7MP6182**

## FEATURES

- 256KB, 512KB 3.3V I/O compatible secondary cache module family
- Ideal for use with many Intel Pentium CPU-based systems, especially those using the Intel 82430NX (Neptune) PCIset
- Separate 3.3V and 5V power supplies
- Operates with Pentium processor external bus speeds of 66MHz
- Low-cost, low-profile cardedge module with 160 leads
- Uses Burndy Computerbus™ connector, part number CELP2X80SC3Z48
- Multiple GND pins and decoupling capacitors for maximum noise immunity

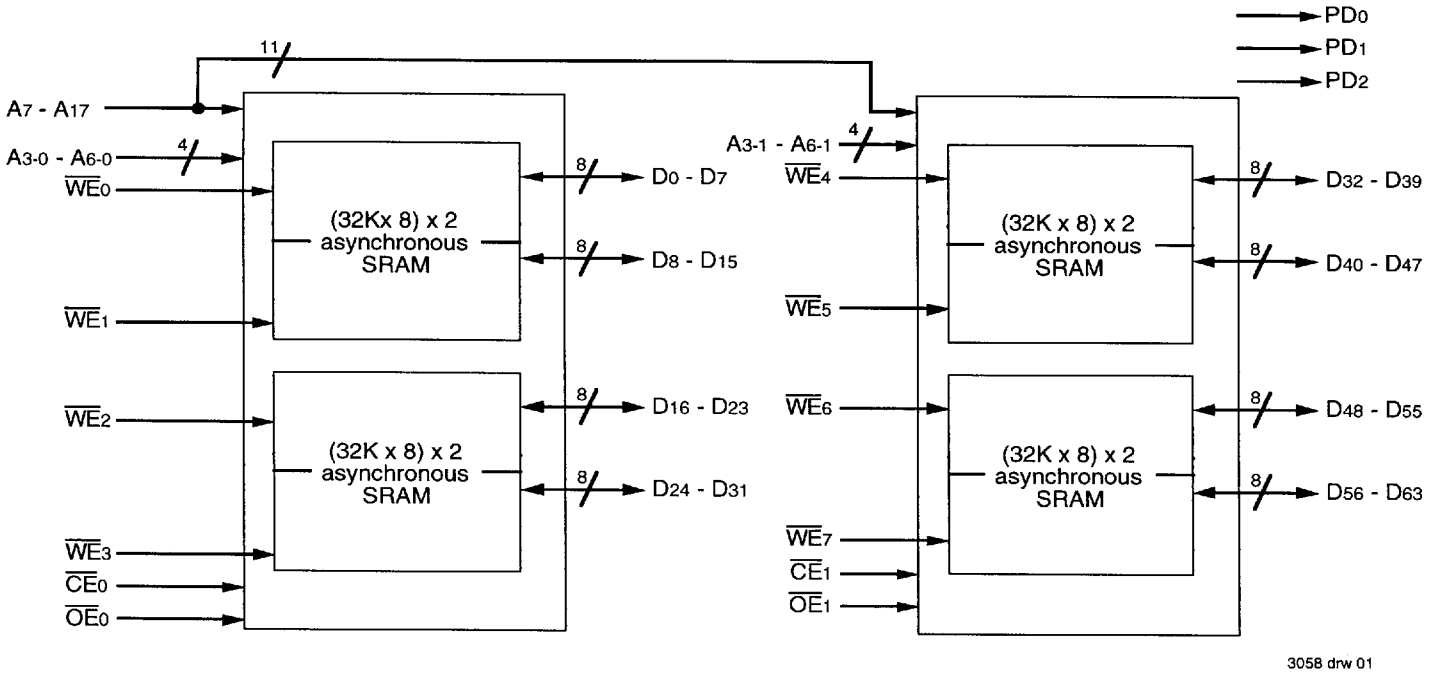
## DESCRIPTION

The IDT7MPV6179/89 and IDT7MP6181/82 are a family of 256KB and 512KB secondary caches that are ideal for use with many Intel Pentium CPU-based systems, especially those using the Intel 82430NX (Neptune) PCIset. The IDT7MPV6179/89 and IDT7MP6181/82 use asynchronous and burst CacheRAMs™ respectively in plastic surface mount packages mounted on a multilayer epoxy laminate (FR-4) board. Extremely high speeds are achieved using IDT's high-performance, high-reliability BiCMOS and CMOS technologies. The IDT7MPV6189 is a latched address asynchronous SRAM version of the IDT7MP6179 which saves the designer a latch on the motherboard as well as giving the opportunity to further improve performance with the use of the IDT7MP6181/82 burst SRAMs module versions.

The low-profile cardedge package configuration allows 160 signal leads to be placed on a package 4.35" long. Depending on which cache configuration is used, the module is a maximum of 0.445" thick and a maximum of 1.15" tall.

All inputs and outputs of the IDT7MPV6179/89 and IDT7MP6181/82 are TTL-compatible, and operate from separate 3.3V power supplies for the asynchronous SRAM versions and 5.0V for the burst cache SRAM versions. Burst SRAM versions are 3.3V I/O compatible. Equal clock line trace lengths ensure minimum clock skew. Multiple GND pins and on-board decoupling capacitors ensure maximum protection from noise.

## FUNCTIONAL BLOCK DIAGRAM
## IDT7MPV6179

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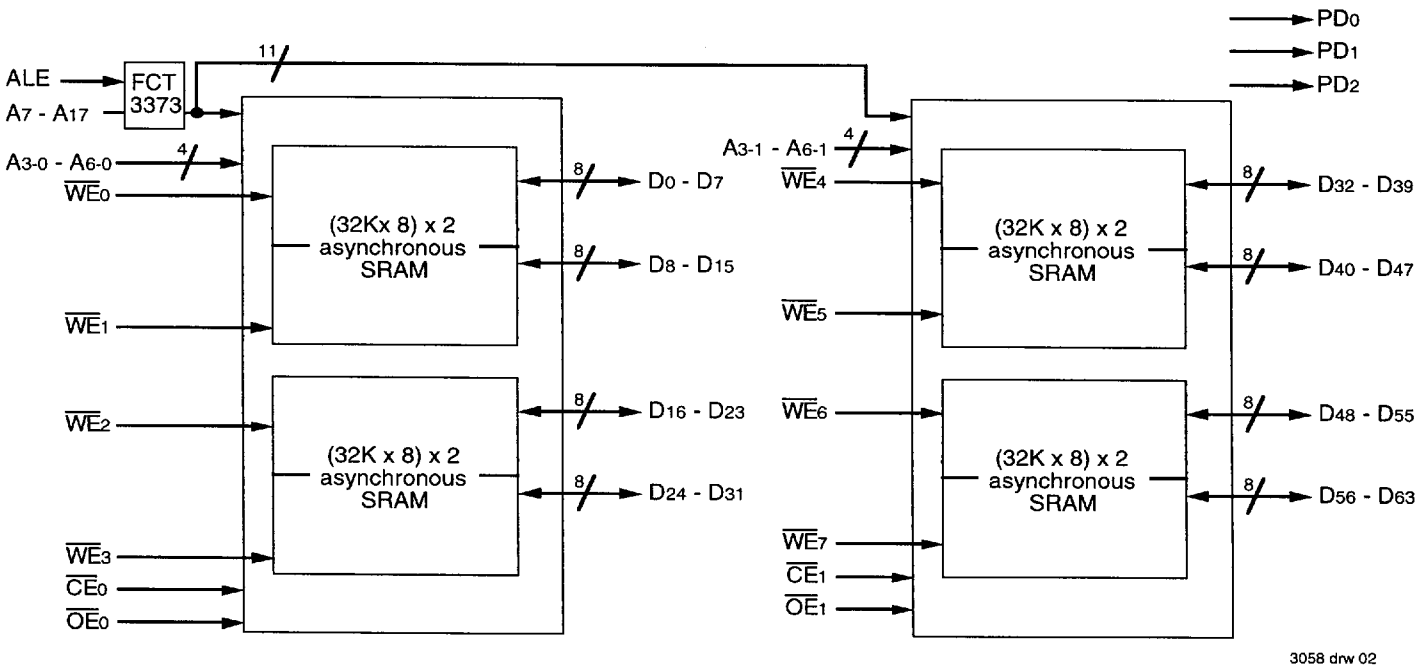
## FUNCTIONAL BLOCK DIAGRAM
## IDT7MPV6189

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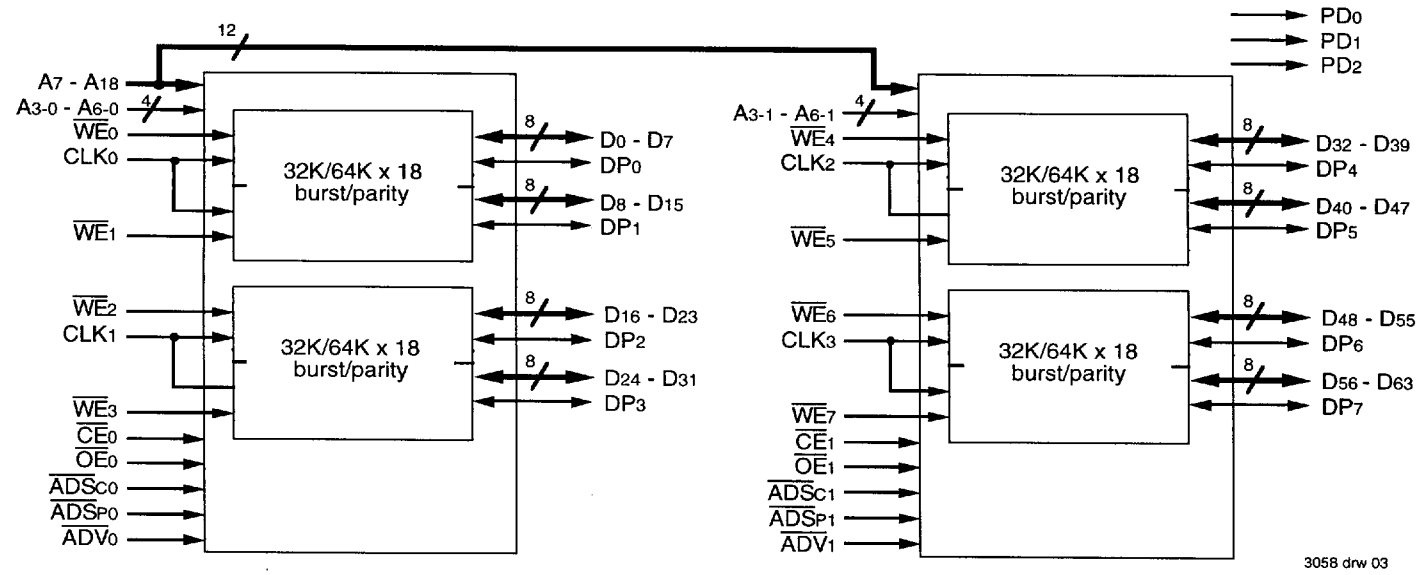
## IDT7MP6181/82

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## PIN CONFIGURATION[3]

| | | | |
|---|---|---|---|
| GND | 81 | 1 | GND |
| D63 | 82 | 2 | D62 |
| VCC5 | 83 | 3 | VCC3 |
| D61 | 84 | 4 | D60 |
| VCC5 | 85 | 5 | VCC3 |
| D59 | 86 | 6 | D58 |
| D57 | 87 | 7 | D56 |
| GND | 88 | 8 | GND |
| (1) DP7 | 89 | 9 | DP6 (1) |
| D55 | 90 | 10 | D54 |
| D53 | 91 | 11 | D52 |
| D51 | 92 | 12 | D50 |
| GND | 93 | 13 | GND |
| D49 | 94 | 14 | D48 |
| D47 | 95 | 15 | D46 |
| D45 | 96 | 16 | D44 |
| D43 | 97 | 17 | D42 |
| GND | 98 | 18 | GND |
| D41 | 99 | 19 | D40 |
| (1) DP5 | 100 | 20 | DP4 (1) |
| D39 | 101 | 21 | D38 |
| D37 | 102 | 22 | D36 |
| D35 | 103 | 23 | D34 |
| GND | 104 | 24 | GND |
| D33 | 105 | 25 | D32 |
| D31 | 106 | 26 | D30 |
| D29 | 107 | 27 | D28 |
| D27 | 108 | 28 | D26 |
| D25 | 109 | 29 | D24 |
| GND | 110 | 30 | GND |
| (1) DP3 | 111 | 31 | DP2 (1) |
| D23 | 112 | 32 | D22 |
| D21 | 113 | 33 | D20 |
| VCC5 | 114 | 34 | VCC3 |
| D19 | 115 | 35 | D18 |
| GND | 116 | 36 | GND |
| D17 | 117 | 37 | D16 |
| VCC5 | 118 | 38 | VCC3 |
| D15 | 119 | 39 | D14 |
| D13 | 120 | 40 | D12 |
| GND | 121 | 41 | GND |
| D11 | 122 | 42 | D10 |
| VCC5 | 123 | 43 | VCC3 |
| D9 | 124 | 44 | D8 |
| (1) DP1 | 125 | 45 | DP0 (1) |
| VCC5 | 126 | 46 | VCC3 |
| D7 | 127 | 47 | D6 |
| D5 | 128 | 48 | D4 |
| D3 | 129 | 49 | D2 |
| D1 | 130 | 50 | D0 |
| GND | 131 | 51 | GND |
| A3-1 | 132 | 52 | A3-0 |
| A4-1 | 133 | 53 | A4-0 |
| A5-1 | 134 | 54 | A5-0 |
| A6-1 | 135 | 55 | A6-0 |
| A7 | 136 | 56 | A8 |
| GND | 137 | 57 | GND |
| A9 | 138 | 58 | A10 |
| A11 | 139 | 59 | A12 |
| A13 | 140 | 60 | A14 |
| A15 | 141 | 61 | A16 |
| A17 | 142 | 62 | A18 |
| GND | 143 | 63 | GND |
| (2)ALE | 144 | 64 | PD0 |
| PD1 | 145 | 65 | PD2 |
| (1) CLK0 | 146 | 66 | CLK1 (1) |
| (1) CLK2 | 147 | 67 | CLK3 (1) |
| GND | 148 | 68 | GND |
| $\overline{WE7}$ | 149 | 69 | $\overline{WE6}$ |
| $\overline{WE5}$ | 150 | 70 | $\overline{WE4}$ |
| $\overline{WE3}$ | 151 | 71 | $\overline{WE2}$ |
| $\overline{WE1}$ | 152 | 72 | $\overline{WE0}$ |
| GND | 153 | 73 | GND |
| (1) $\overline{ADSC1}$ | 154 | 74 | $\overline{ADSC0}$ (1) |
| $\overline{CE1}$ | 155 | 75 | $\overline{CE0}$ |
| (1) $\overline{ADV1}$ | 156 | 76 | $\overline{ADV0}$ (1) |
| $\overline{OE1}$ | 167 | 77 | $\overline{OE0}$ |
| VCC5 | 158 | 78 | VCC3 |
| (1) $\overline{ADSP1}$ | 159 | 79 | $\overline{ADSP0}$ (1) |
| GND | 160 | 80 | GND |

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**LOW PROFILE CARDEDGE MODULE**
**TOP VIEW**

**NOTES:**
1. These pins are no connects for the asynchronous module versions.
2. This pin is a no connect for all modules but the IDT7MPV6189.
3. VCC3 is connected only to the asynchronous SRAMs for the IDT7MP6179/89 and VCC5 is connected to only the burst cache SRAMs for the IDT7MP6181/82.

## PIN NAMES

| | |
|---|---|
| A3 – A18 | Address Inputs |
| ALE | Address Latch Enable Input |
| D0 – D63 | Inputs/Outputs |
| DP0 – DP7 | Parity Inputs/Outputs |
| $\overline{CE0}$ – $\overline{CE1}$ | Chip Enable Inputs |
| $\overline{WE0}$ – $\overline{WE7}$ | Byte Write Enable Inputs |
| $\overline{OE0}$ – $\overline{OE1}$ | Output Enable Inputs |
| $\overline{ADSP0}$ – $\overline{ADSP1}$ | Address Status Processor Inputs |
| $\overline{ADSC0}$ – $\overline{ADSC1}$ | Address Status Cache Controller Inputs |
| $\overline{ADV0}$ – $\overline{ADV1}$ | Burst Address Advance Inputs |
| CLK0 – CLK3 | Clock Inputs |
| PD0 – PD2 | Presence Detect Pins |
| N.C. | No Connect |
| GND | Ground |
| VCC3 | Power Supply for Asynchronous SRAMs only |
| VCC5 | Power Supply for Burst Cache SRAMs only |

3058 tbl 01

## PRESENCE DETECT TABLE[1]

| PD2 | PD1 | PD0 | SRAM | Type | Size | Module |
|---|---|---|---|---|---|---|
| N.C. | N.C. | N.C. | — | — | — | No cache present |
| N.C. | N.C. | GND | — | — | — | Reserved |
| N.C. | GND | N.C. | 71V256 | Asynch | 256KB | IDT7MPV6179/89 |
| N.C. | GND | GND | — | — | — | Reserved |
| GND | N.C. | N.C. | — | — | — | Reserved |
| GND | N.C. | GND | — | — | — | Reserved |
| GND | GND | N.C. | 71420 | Burst | 256KB | IDT7MP6181 |
| GND | GND | GND | 64K x 18 | Burst | 512KB | IDT7MP6182 |

**NOTE:** 3058 tbl 02
1. The IDT71V256 is the 3.3V 32K x 8 SRAM. The IDT71420 and IDT71620 are respectively 32K x 18 and 64K x 18 burst cache SRAMs which operate from a 5V supply, but are compatible in a 3.3V environment.

## CAPACITANCE[1, 2]

(TA = +25°C, f = 1.0 MHz)

| Symbol | Parameter[1] | Condition | '6179/89 | '6181/2 | Unit |
|---|---|---|---|---|---|
| CIN1 | Input Capacitance (Address) | VIN = 0V | 45/10 | 25 | pF |
| CIN2 | Input Capacitance ($\overline{CE}$, $\overline{OE}$, Control) | VIN = 0V | 25 | 15 | pF |
| CIN3 | Input Capacitance ($\overline{WE}$, CLK) | VIN = 0V | 8 | 8 | pF |
| CI/O | I/O Capacitance | VOUT = 0V | 10 | 10 | pF |

**NOTES:** 3058 tbl 03
1. These parameters are guaranteed by design but not tested.
2. These parameters are maximum values.

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Rating | Value | Unit |
|---|---|---|---|
| $V_{TERM}$ | Terminal Voltage with Respect to GND | –0.5 to +7.0 | V |
| $T_A$ | Operating Temperature | 0 to +70 | °C |
| $T_{BIAS}$ | Temperature Under Bias | –10 to +85 | °C |
| $T_{STG}$ | Storage Temperature | –55 to +125 | °C |
| $I_{OUT}$ | DC Output Current | 50 | mA |

3058 tbl 04

**NOTE:**
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC5}$ | Supply Voltage | 4.75 | 5.0 | 5.25 | V |
| $V_{CC3}$ | Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| GND | Supply Voltage | 0 | 0 | 0.0 | V |
| $V_{IH}$ | Input High Voltage | 2.2 | — | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | –0.5[1] | — | 0.8 | V |

3058 tbl 05

**NOTE:**
1. $V_{IL}$ = –1.0V for pulse width less than 5ns, once per cycle.

## RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

| Module | Ambient Temperature | GND | Vcc |
|---|---|---|---|
| 7MP6179/89 | 0°C to +70°C | 0V | 3.3V ± 10% |
| 7MP6181/82 | 0°C to +70°C | 0V | 5.0V ± 5% |

3058 tbl 06

## DC ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 3.3V ± 10% for the 7MPV6179/89, $V_{CC}$ = 5.0V ± 5% for the 7MP6181/82 $T_A$ = 0°C to 70°C)

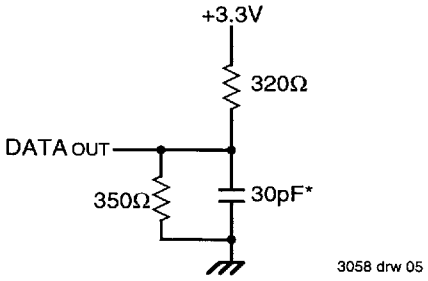
| Symbol | Parameter | Test Condition | 7MPV6179/89 | | 7MP6181/82 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| $I_{LI}$ | Input Leakage Current (Address) | $V_{CC}$ = Max, $V_{IN}$ = GND to $V_{CC}$ | — | 20/5 | — | 40 | µA |
| $I_{LI}$ | Input Leakage Current ($\overline{CE}$, $\overline{OE}$, Control) | $V_{CC}$ = Max, $V_{IN}$ = GND to $V_{CC}$ | — | 10 | — | 20 | µA |
| $I_{LI}$ | Input Leakage Current ($\overline{WE}$, CLK) | $V_{CC}$ = Max, $V_{IN}$ = GND to $V_{CC}$ | — | 5 | | 5 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$ = 0V to $V_{CC}$, $V_{CC}$ = Max. | — | 5 | — | 5 | µA |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 8mA, $V_{CC}$ = Min. | — | 0.4 | — | 0.4 | V |
| $V_{OH}$ | Output HighVoltage | $I_{OH}$= –4mA, $V_{CC}$ = Min. | 2.4 | — | 2.4 | — | V |
| $I_{CC}$ | Operating Power Supply Current | $V_{CC}$ = Max., $\overline{CE} \le V_{IL}$, f = $f_{MAX}$, Outputs Open | — | 850 | — | 1000 | mA |
| $I_{SB}$ | Standby Power Supply Current | $V_{CC}$ = Max., $\overline{CE} \ge V_{IH}$, f = $f_{MAX}$, Outputs Open | — | 120 | — | 400 | mA |
| $I_{SB1}$ | Full Standby Power Supply Current | $V_{CC}$ = Max., $\overline{CE} \ge V_{CC}$ - 0.2V, f = 0, $V_{IN} \le$ 0.2V or $V_{IN} \ge V_{CC}$ - 0.2V, Outputs Open | — | 10 | — | 180 | mA |

3058 tbl 07

## AC TEST CONDITIONS – IDT7MPV6179/89

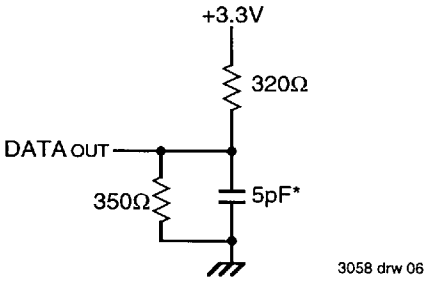
| | |
|---|---|
| Input Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 3ns |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| Output Load | See Figures 1 and 2 |

3058 tbl 08




*including scope and jig capacitances

**Figure 1. Output Load**



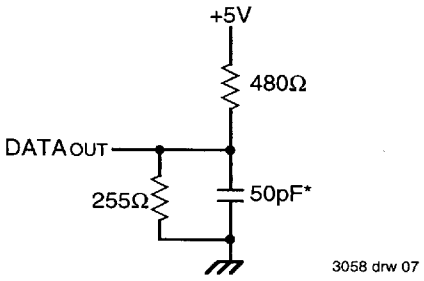

*including scope and jig capacitances

**Figure 2. Output Load (for $t_{OHZ}$, $t_{CHZ}$, $t_{OLZ}$ and $t_{CLZ}$)**

## AC TEST CONDITIONS – IDT7MP6181/82

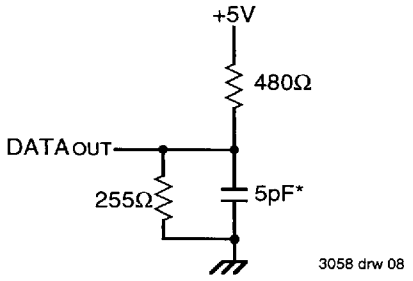
| | |
|---|---|
| Input Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 5ns |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| Output Load | See Figures 3 and 4 |

3058 tbl 09




*including scope and jig capacitances

**Figure 3. Output Load**

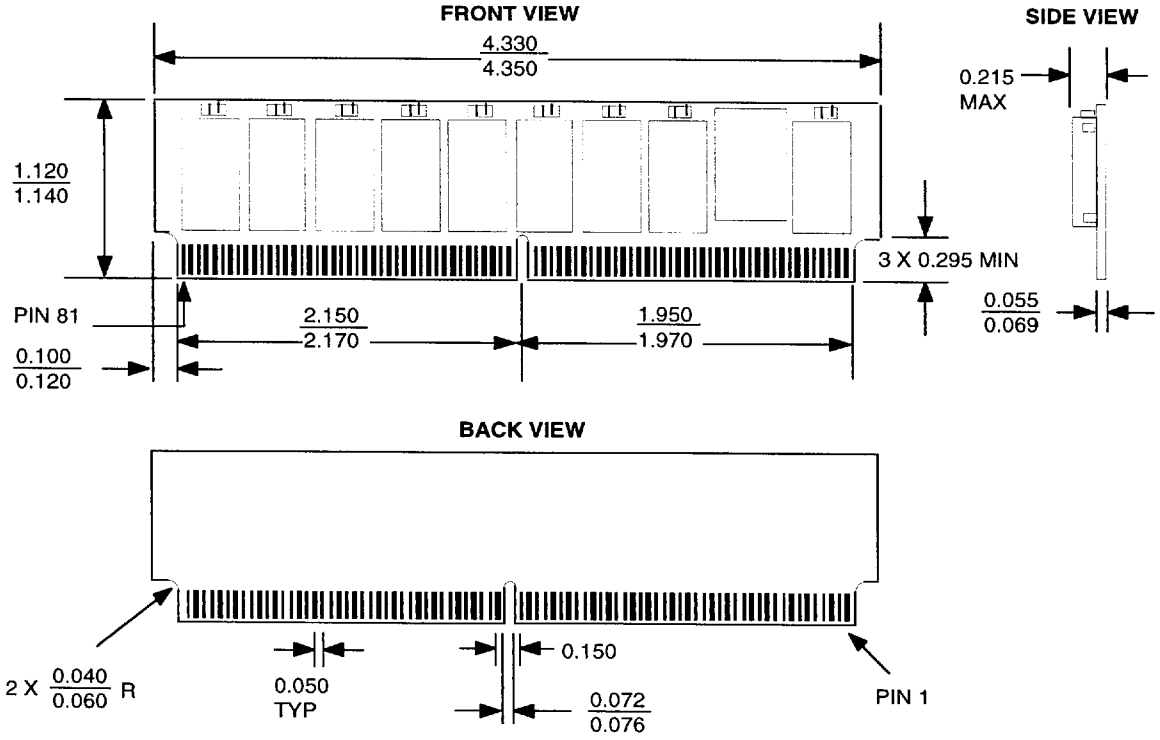



*including scope and jig capacitances

**Figure 4. Output Load (for $t_{OHZ}$, $t_{CHZ}$, $t_{OLZ}$ and $t_{CLZ}$)**

## PACKAGE DIMENSIONS

### IDT7MPV6179

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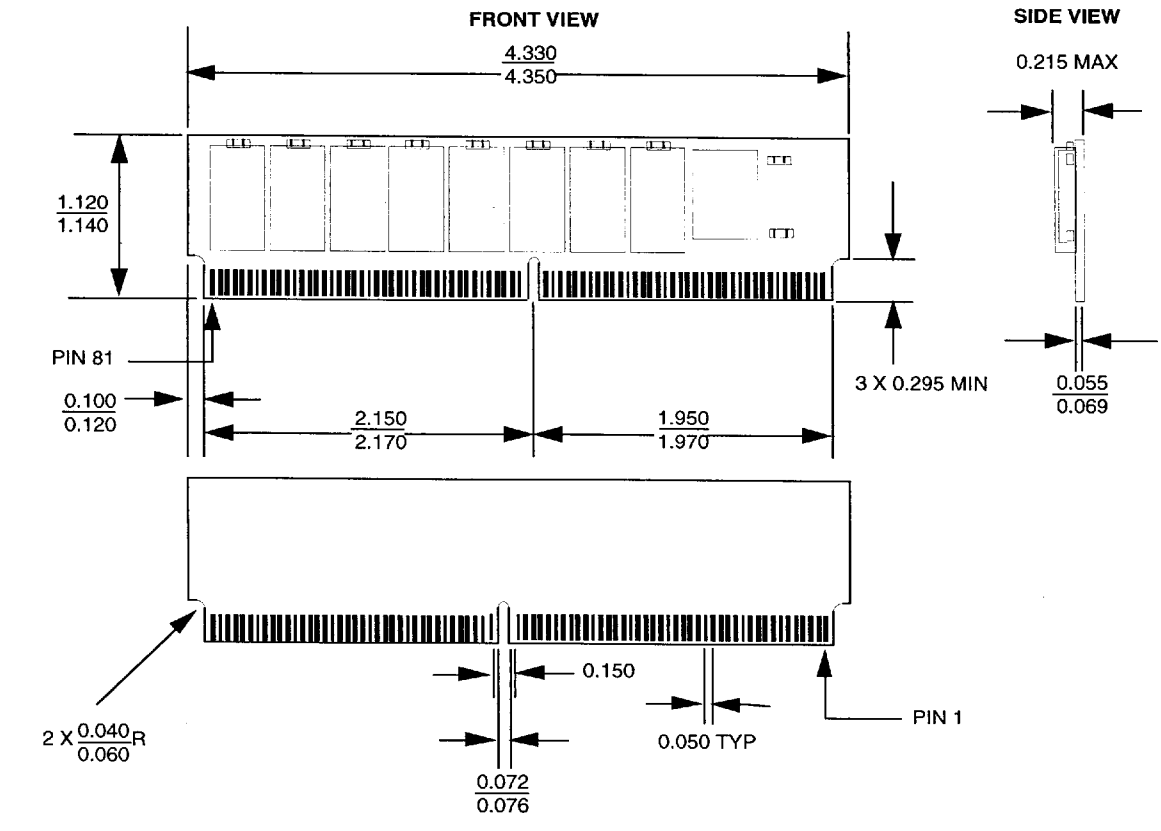
### IDT7MPV6189

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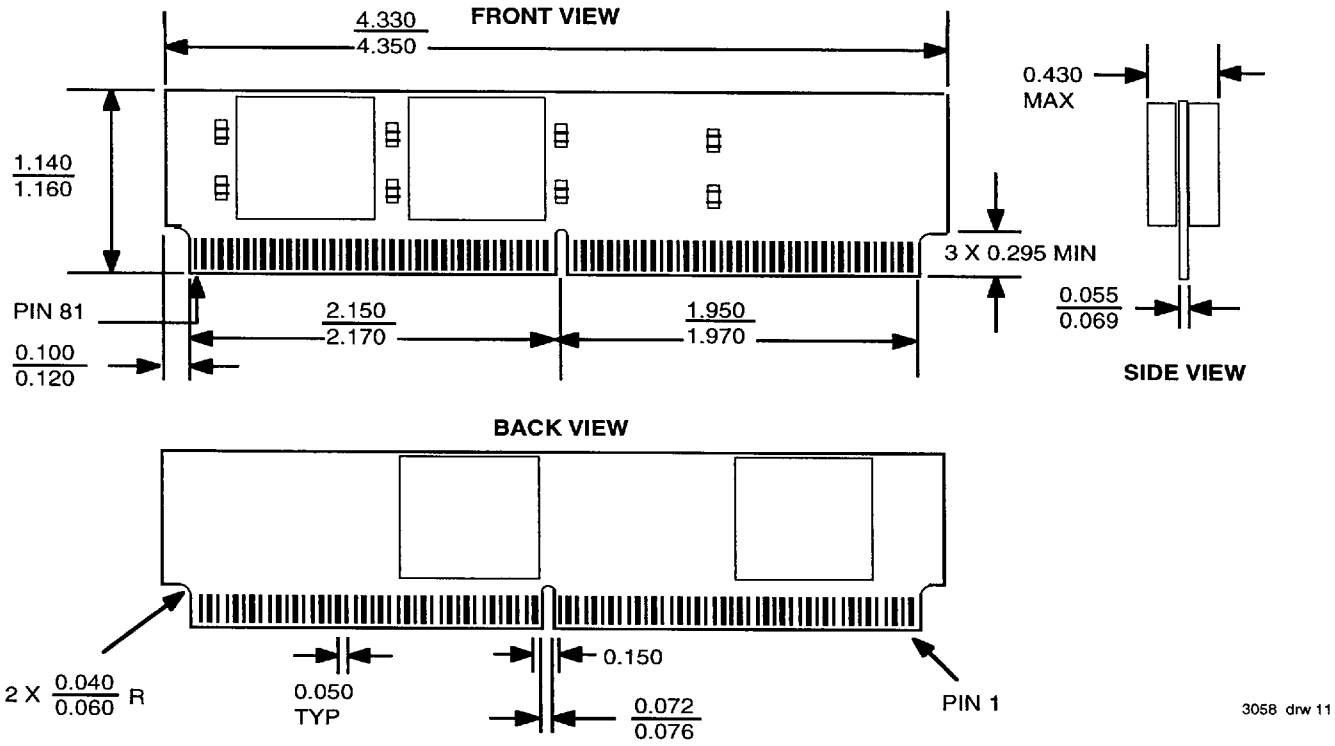
## IDT7MP6181/82

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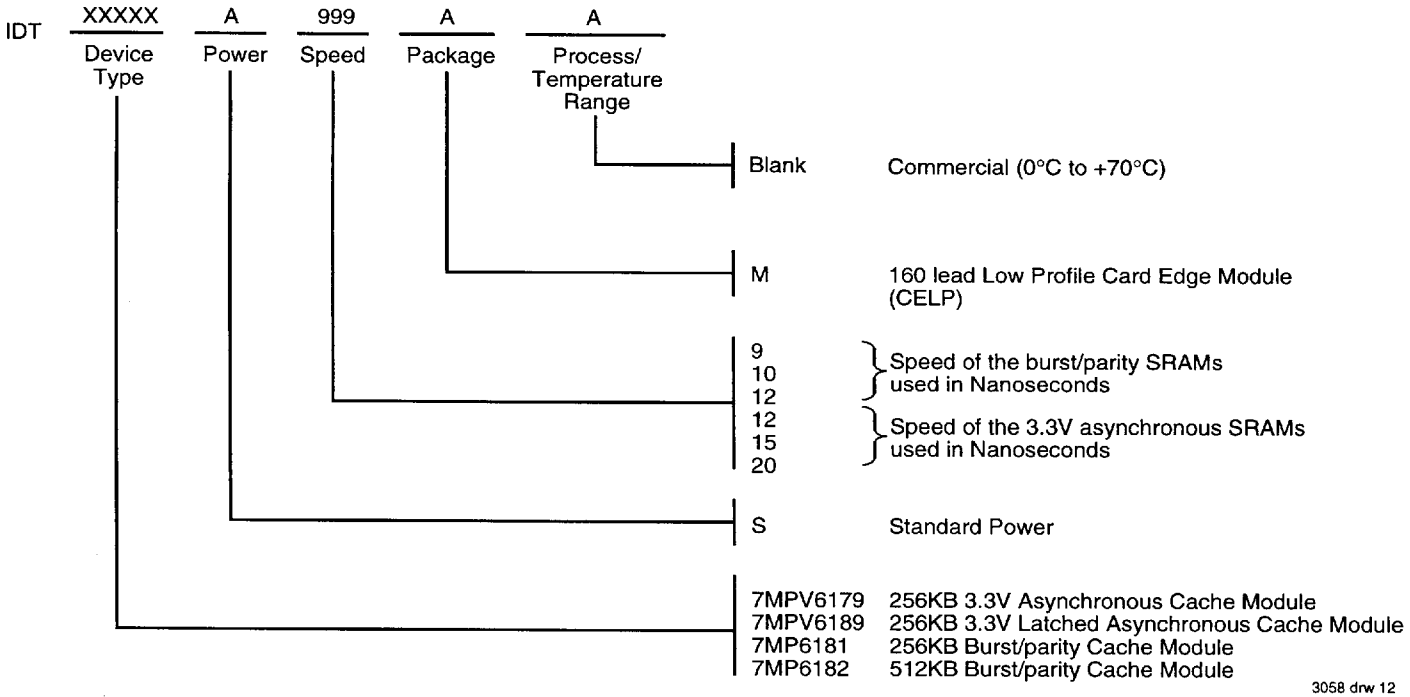
## ORDERING INFORMATION

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**Integrated Device Technology, Inc.**

2975 Stender Way, Santa Clara, CA 95052-8015 Telephone: (408) 727-6116 FAX 408-492-8674