Integrated Device Technology, Inc.

HIGH-SPEED 2K x 9 DUAL-PORT STATIC RAM WITH BUSY & INTERRUPT

PRELIMINARY
IDT70121S/L
IDT70125S/L

T-46-23-12

FEATURES:

- High-speed access
  - Military: 35/45/55/70ns (max.)
  - Commercial: 25/35/45/55ns (max.)
- Low-power operation
  - IDT70121/70125S
    Active: 400mW (typ.)
    Standby: 7mW (typ.)
  - IDT70121/70125L
    Active: 400mW (typ.)
    Standby: 2mW (typ.)
- Fully asychronous operation from either port
- MASTER IDT70121 easily expands data bus width to 18 bits or more using SLAVE IDT70125 chip
- On-chip port arbitration logic (IDT70121 only)
- $\overline{BUSY}$ output flag on Master; $\overline{BUSY}$ input on Slave
- $\overline{INT}$ flag for port-to-port communication
- Battery backup operation—2V data retention
- TTL compatible, signal 5V (±10%) power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature range (-40°C to +85°C) is available, tested to military electrical specifications

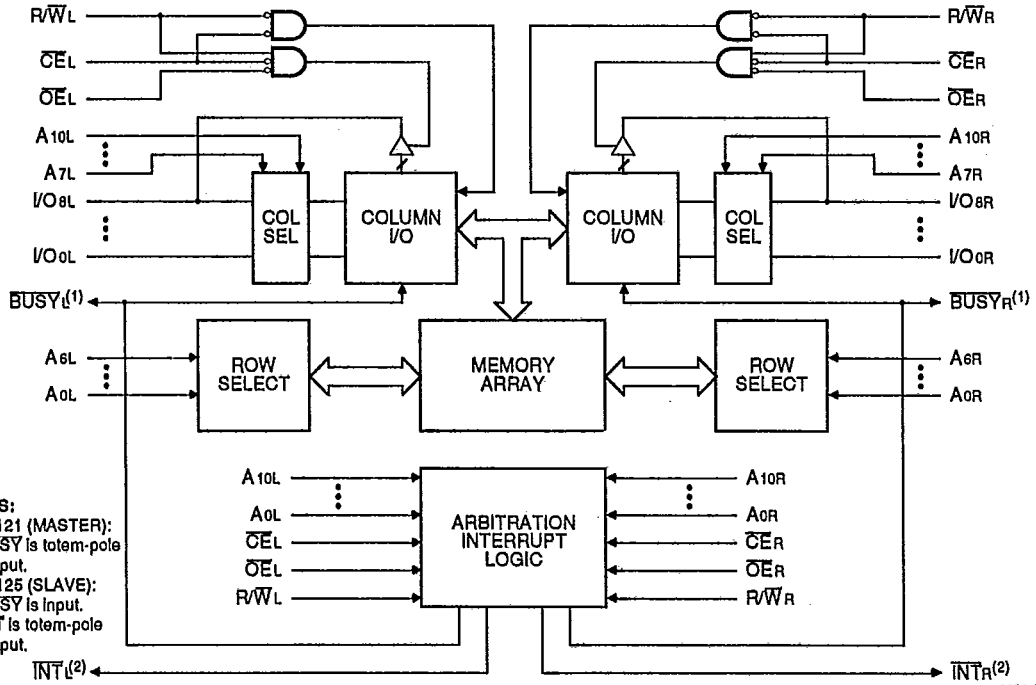
DESCRIPTION:

The IDT70121/IDT70125 are high-speed 2K x 9 dual-port static RAMs. The IDT70121 is designed to be used as a stand-alone 9-bit dual-port RAM or as a "MASTER" dual-port RAM together with the IDT70125 "SLAVE" dual-port in 18-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 18-bit-or-wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power-down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

The IDT70121/IDT70125 utilizes a 9-bit wide data path to allow for Data/Control and parity bits at the user's option. This feature is especially useful in data communications

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. 70121 (MASTER): $\overline{BUSY}$ is totem-pole output. 70125 (SLAVE): $\overline{BUSY}$ is input.
2. $\overline{INT}$ is totem-pole output.

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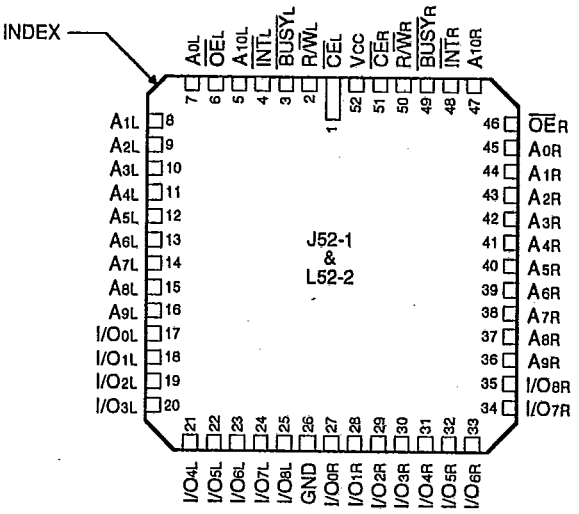
DESCRIPTION (Continued):

applications where it is necessary to use a parity bit for transmission/reception error checking.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 400mW of power at maximum access times as fast as 25ns. Low-power (L) versions offer battery backup data retention capability with each port typically consuming 200µW from a 2V battery.

The IDT70121/IDT70125 devices are packaged in 52-pin LCCs and 52-pin PLCCs. The military devices are processed 100% in compliance to the test methods of MIL-STD-883, Method 5004.

PIN CONFIGURATIONS



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LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	50	50	mA

2654 tbl 01

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed Vcc + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2654 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0.0	V
VIH	Input High Votage	2.2	–	6.0(2)	V
VIL	Input Low Voltage	–0.5(1)	–	0.8	V

2654 tbl 03

NOTE:
1. VIL = –3.0V for pulse width less than 20ns.
2. VTERM must not exceed Vcc + 0.5V.

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DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	70121S 70125S		70121L 70125L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[7]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4mA	2.4	—	2.4	—	V

2654 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1,6] (V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Version		70121 x 25[2] 70125 x 25[2]		70121 x 35 70125 x 35		70121 x 45 70125 x 45		70121 x 55 70125 x 55		70121 x 70[3] 70125 x 70[3]		Unit
					Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ ≤ V_{IL} Outputs Open f = f_{MAX}[4]	Mil.	S	—	—	125	290	125	285	125	280	125	275	mA
				L	—	—	125	230	125	225	125	220	125	215	
			Com'l.	S	125	260	125	250	125	245	125	240	—	—	
				L	125	220	125	210	125	205	125	200	—	—	
I_{SB1}	Standby Current (Both Ports—TTL Level Inputs)	$\overline{CE_L}$ and $\overline{CE_R}$ ≥ V_{IH} f = f_{MAX}[4]	Mil.	S	—	—	30	80	30	80	30	80	30	80	mA
				L	—	—	30	60	30	60	30	60	30	60	
			Com'l.	S	30	65	30	65	30	65	30	65	—	—	
				L	30	45	30	45	30	45	30	45	—	—	
I_{SB2}	Standby Current (One Port—TTL Level Inputs)	$\overline{CE_L}$ or $\overline{CE_R}$ ≥ V_{IH} Active Port Outputs Open, f = f_{MAX}[4]	Mil.	S	—	—	80	185	80	180	80	175	80	170	mA
				L	—	—	80	150	80	145	80	140	80	135	
			Com'l.	S	80	175	80	165	80	160	40	155	—	—	
				L	80	145	80	135	80	130	40	125	—	—	
I_{SB3}	Full Standby Current (Both Ports—CMOS Level Inputs)	Both Ports $\overline{CE_R}$ and $\overline{CE_L}$ ≥ V_{CC} − 0.2V V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0[5]	Mil.	S	—	—	1.0	30	1.0	30	1.0	30	1.0	30	mA
				L	—	—	0.2	10	0.2	10	0.2	10	0.2	10	
			Com'l.	S	1.0	15	1.0	15	1.0	15	1.0	15	—	—	
				L	0.2	5	0.2	5	0.2	5	0.2	5	—	—	
I_{SB4}	Full Standby Current (One Port—CMOS Level Inputs)	One Port $\overline{CE_L}$ or $\overline{CE_R}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}[4]	Mil.	S	—	—	70	175	70	170	70	165	70	160	mA
				L	—	—	70	140	70	135	70	130	70	125	
			Com'l.	S	70	170	70	160	70	155	70	150	—	—	
				L	70	140	70	130	70	125	70	120	—	—	

2654 tbl 05

NOTES:
1. "x" in part numbers indicates power rating (S or L).
2. 0°C to +70°C temperature range only.
3. −55°C to +125°C temperature range only.
4. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of Input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
6. V_{CC}=5V, T_A=+25°C for Typ.
7. At V_{CC}≤2.0V input leakages are undefined.

6

DATA RETENTION CHARACTERISTICS (L Version Only)

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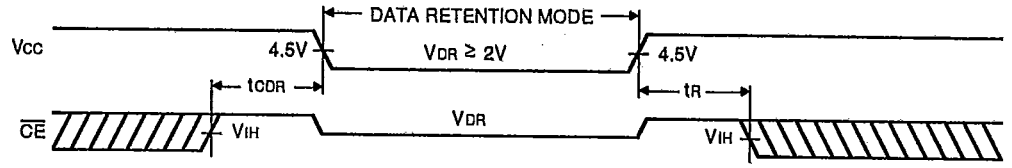
Symbol	Parameter	Test Condition		70121L/70125L Min.	Typ.(1)	Max.	Unit
V_{DR}	Vcc for Data Retention	V_{CC} = 2.0V, $\overline{CE} \geq V_{CC} - 0.2V$		2	—	—	V
I_{CCDR}	Data Retention Current		Mil.	—	100	4000	µA
			Com'l.	—	100	1500	µA
t_{CDR}(3)	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		0	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	ns

2654 tbl 06

NOTES:
1. Vcc = 2V, TA = +25°C.
2. tRC = Read Cycle Time.
3. This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM

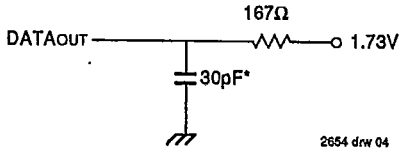


2654 drw 03

AC TEST CONDITIONS

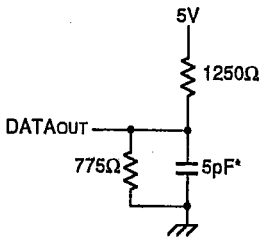
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 & 3

2654 tbl 07



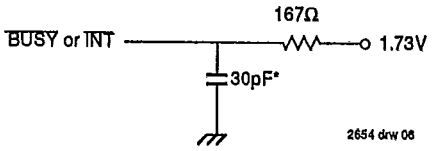
2654 drw 04

Figure 1. Equivalent Output Load



2654 drw 05

Figure 2. Output Load
(for tHZ, tLZ, tWZ, and tOW)



2654 drw 06

Figure 3. Equivalent $\overline{BUSY}$ and $\overline{INT}$ Output Load

* Including scope and jig.

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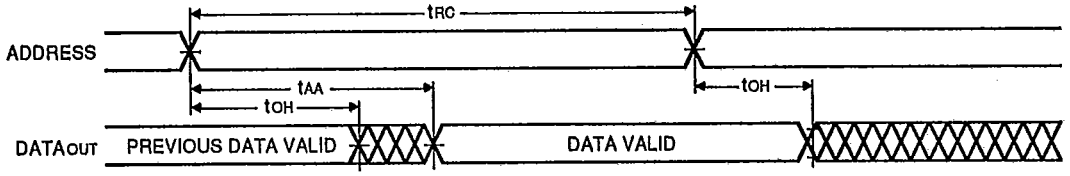
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[5]

Symbol	Parameter	70121 x 25[2] 70125 x 25[2] Min.	Max.	70121 x 35 70125 x 35 Min.	Max.	70121 x 45 70125 x 45 Min.	Max.	70121 x 55 70125 x 55 Min.	Max.	70121 x 70[3] 70125 x 70[3] Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	25	—	35	—	45	—	55	—	70	—	ns
tAA	Address Access Time	—	25	—	35	—	45	—	55	—	70	ns
tACE	Chip Enable Access Time	—	25	—	35	—	45	—	55	—	70	ns
tAOE	Output Enable Access Time	—	12	—	25	—	30	—	35	—	40	ns
tOH	Output Hold from Address Change	0	—	0	—	0	—	0	—	0	—	ns
tLZ	Output Low Z Time[1,4]	0	—	0	—	0	—	0	—	0	—	ns
tHZ	Output High Z Time[1,4]	—	10	—	15	—	20	—	30	—	35	ns
tPU	Chip Enable to Power-Up Time[4]	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power-Down Time[4]	—	50	—	50	—	50	—	50	—	50	ns

2654 tbl 08

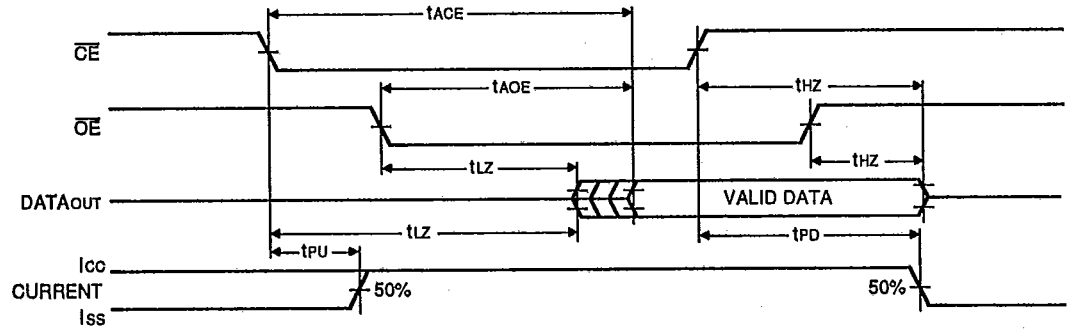
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C range only.
4. This parameter guaranteed but not tested.
5. "x" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1,2,4]



2654 drw 08

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE[1,3]



2654 drw 09

NOTES:
1. R/W is high for Read Cycles.
2. Device is continuously enabled, CE = VIL.
3. Addresses valid prior to, or coincident with, CE transition low.
4. OE = VIL.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[6]

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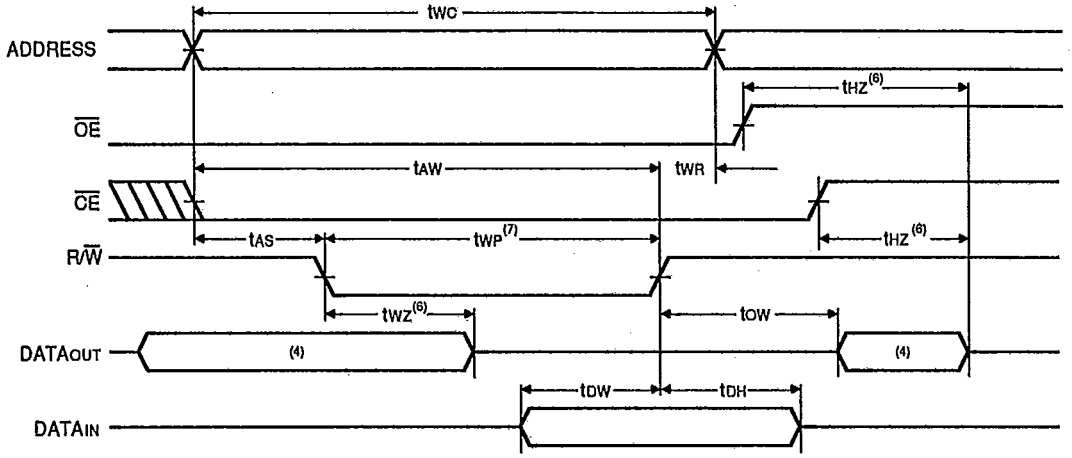
Symbol	Parameter	70121 x 25[2] 70125 x 25[2]		70121 x 35 70125 x 35		70121 x 45 70125 x 45		70121 x 55 70125 x 55		70121 x 70[3] 70125 x 70[3]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle												
tWC	Write Cycle Time[5]	25	—	35	—	45	—	55	—	70	—	ns
tEW	Chip Enable to End of Write	20	—	30	—	35	—	40	—	50	—	ns
tAW	Address Valid to End of Write	20	—	30	—	35	—	40	—	50	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width[7]	20	—	30	—	35	—	40	—	50	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	12	—	20	—	20	—	20	—	..30	—	ns
tHZ	Output High Z Time[1,4]	—	10	—	15	—	20	—	30	—	35	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z[1,4]	—	10	—	15	—	20	—	30	—	35	ns
tOW	Output Active from End of Write[1,4]	0	—	0	—	0	—	0	—	0	—	ns

2654 tbl 09

NOTES:
1. Transition is measured ±500mV from low or high voltage with load (Figures 1, 2 and 3).
2. 0°C to +70°C temperature range only.
3. –55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. For MASTER/SLAVE combination, tWC = tBAA + tWP.
6. "x" in part numbers indicates power rating (S or L).
7. Specified for $\overline{OE}$ at high (Refer to "Timing Waveform of Write Cycle", Note 7).

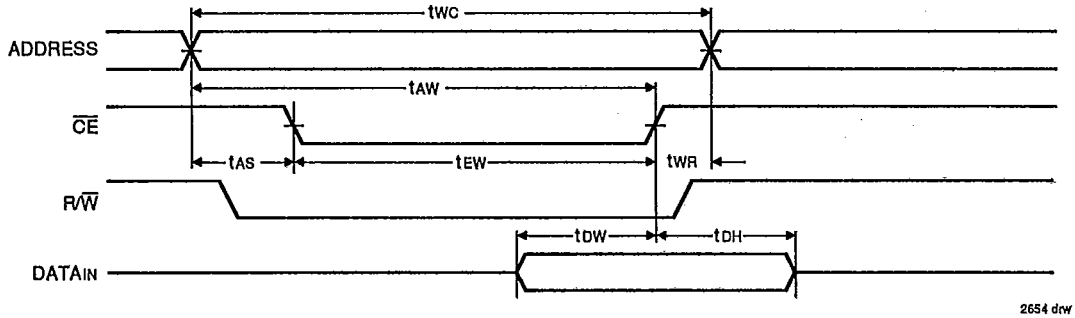
TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1,2,3,7)

T-46-23-12



2654 drw 10

TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1,2,3,5)



2654 drw 11

NOTES:
1. R/$\overline{W}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ± 500mV from steady state with a 5pF load (including scope and jig). This parameter is sampled and not 100% tested.
7. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[8]

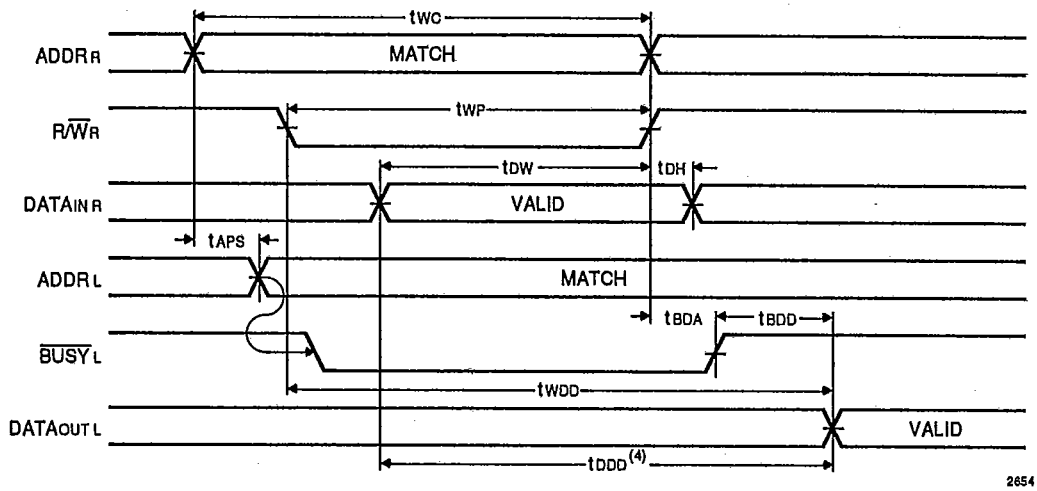
T-46-23-12

Symbol	Parameter	70121 x 25[1] 70125 x 25[1] Min.	Max.	70121 x 35 70125 x 35 Min.	Max.	70121 x 45 70125 x 45 Min.	Max.	70121 x 55 70125 x 55 Min.	Max.	70121 x 70[2] 70125 x 70[2] Min.	Max.	Unit
Busy Timing (For Master IDT70121 Only)												
tBAA	$\overline{BUSY}$ Access Time to Address	—	25	—	35	—	35	—	45	—	45	ns
tBDA	$\overline{BUSY}$ Disable Time to Address	—	20	—	30	—	35	—	40	—	40	ns
tBAC	$\overline{BUSY}$ Access Time to Chip Enable	—	20	—	30	—	30	—	35	—	35	ns
tBDC	$\overline{BUSY}$ Disable Time to Chip Enable	—	20	—	25	—	25	—	30	—	30	ns
tWDD	Write Pulse to Data Delay[3]	—	50	—	60	—	70	—	80	—	95	ns
tDDD	Write Data Valid to Read Data Delay[3]	—	35	—	45	—	55	—	65	—	80	ns
tAPS	Arbitration Priority Set-up Time[4]	5	—	5	—	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[5]	—	Note 5	—	Note 5	—	Note 5	—	Note 5	—	Note 5	ns
Busy Timing (For Slave IDT70125 Only)												
tWB	Write to $\overline{BUSY}$ Input[6]	0	—	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[7]	15	—	20	—	20	—	20	—	20	—	ns
tWDD	Write Pulse to Data Delay[9]	—	50	—	60	—	70	—	80	—	95	ns
tDDD	Write Data Valid to Read Data Delay[9]	—	35	—	45	—	55	—	65	—	80	ns

2654 tbl 10

NOTES:
1. 0°C to +70°C temperature range only.
2. –55°C to +125°C temperature range only.
3. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (For Master IDT70121 Only)."
4. To ensure that the earlier of the two ports wins.
5. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
6. To ensure that a write cycle is inhibited during contention.
7. To ensure that a write cycle is completed after contention.
8. "x" in part numbers indicates power rating (S or L).
9. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ Port-to-Port Delay (For SLAVE IDT70125 Only)."

TIMING WAVEFORM OF READ WITH $\overline{BUSY}$[1,2,3] (FOR MASTER IDT70121) T-46-23-12



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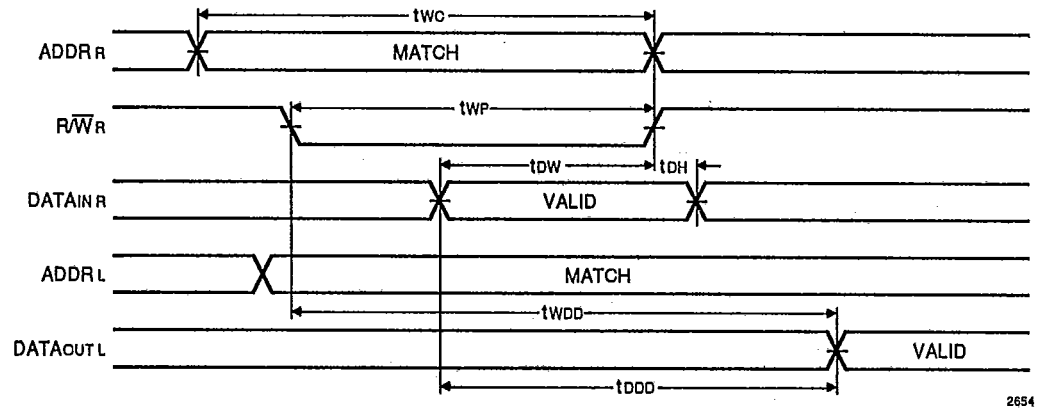
NOTES:
1. To ensure that the earlier of the two ports wins.
2. Write Cycle parameters should be adhered to, to ensure proper writing.
3. Device is continuously enabled for both ports.
4. $\overline{OE}$ at LOW for the reading port.

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY[1,2,3] (FOR SLAVE IDT70125 ONLY)

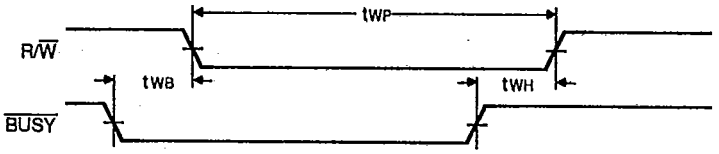


2654 drw 13

NOTES:
1. Assume $\overline{BUSY}$ input at HIGH for the writing port, and $\overline{OE}$ at LOW for the reading port.
2. Write Cycle parameters should be adhered to, to ensure proper writing.
3. Device is continuously enabled for both ports.

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ (FOR SLAVE IDT70125 ONLY)

T-46-23-12



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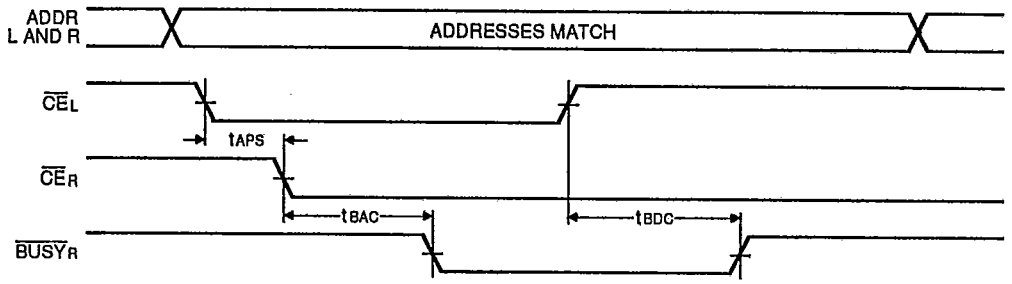
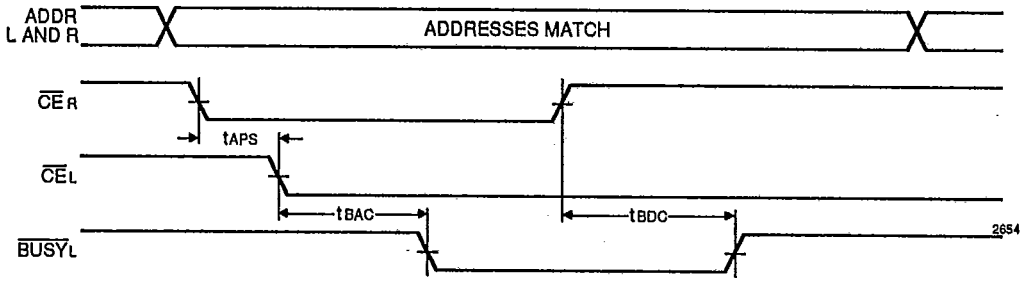
TIMING WAVEFORM OF CONTENTION CYCLE NO. 1, $\overline{CE}$ ARBITRATION (FOR MASTER IDT70121 ONLY)

$\overline{CE}_L$ VALID FIRST:



$\overline{CE}_R$ VALID FIRST:

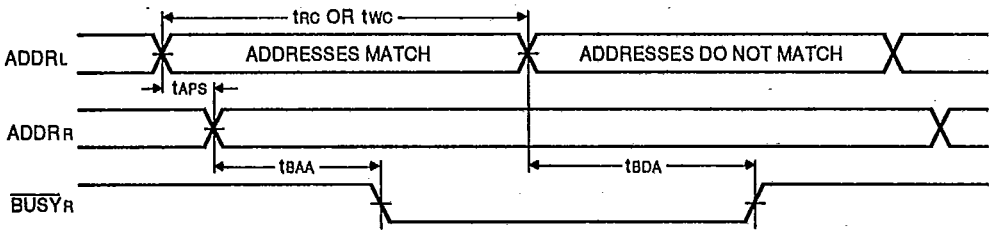


2654 drw 15

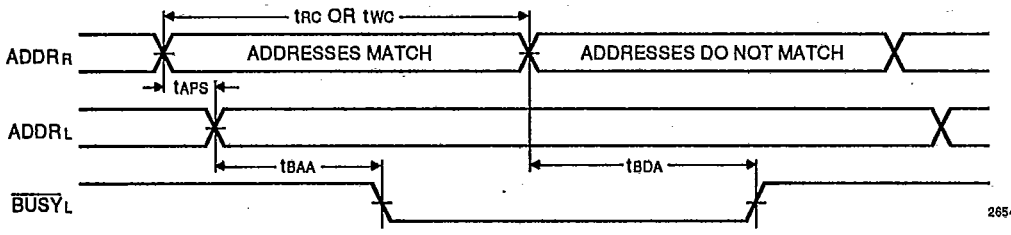
T-46-23-12

TIMING WAVEFORM OF CONTENTION CYCLE NO. 2, ADDRESS VALID ARBITRATION (FOR MASTER IDT70121 ONLY)[1]

LEFT ADDRESS VALID FIRST:



RIGHT ADDRESS VALID FIRST:



2654 drw 16

NOTE:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[3]

Symbol	Parameter	70121 x 25[1] 70125 x 25[1] Min.	Max.	70121 x 35 70125 x 35 Min.	Max.	70121 x 45 70125 x 45 Min.	Max.	70121 x 55 70125 x 55 Min.	Max.	70121 x 70[2] 70125 x 70[2] Min.	Max.	Unit
Interrupt Timing												
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	25	—	35	—	40	—	45	—	50	ns
tINR	Interrupt Reset Time	—	25	—	35	—	40	—	45	—	50	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. −55°C to +125°C temperature range only.
3. "X" in part numbers indicates power rating (S or L).

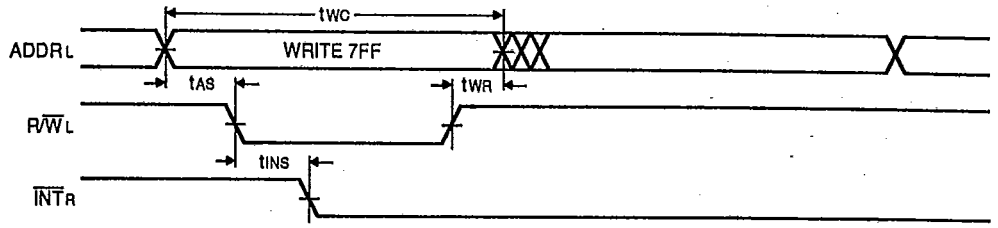
2654 tbl 11

6

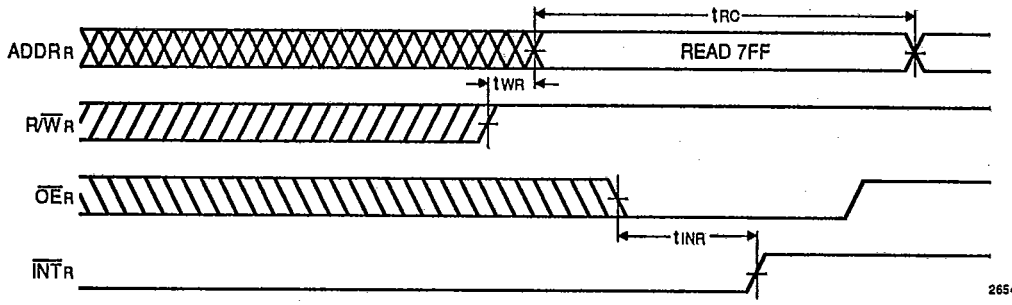
TIMING WAVEFORM OF INTERRUPT MODE(1,2)

T-46-23-12

LEFT SIDE SETS $\overline{INT}_R$:



RIGHT SIDE CLEARS $\overline{INT}_R$:



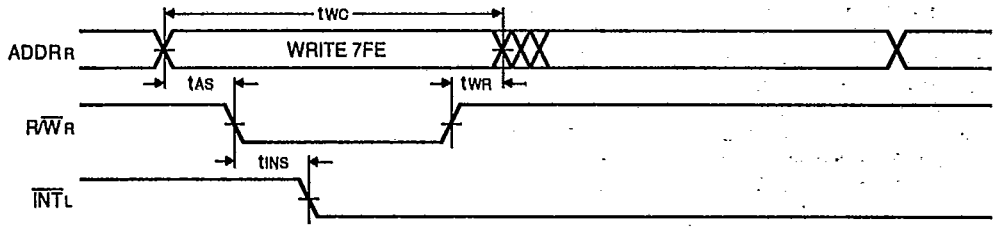
2654 drw 17

NOTES:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$.
2. $\overline{INT}_L$ and $\overline{INT}_R$ are reset (high) during power-up.

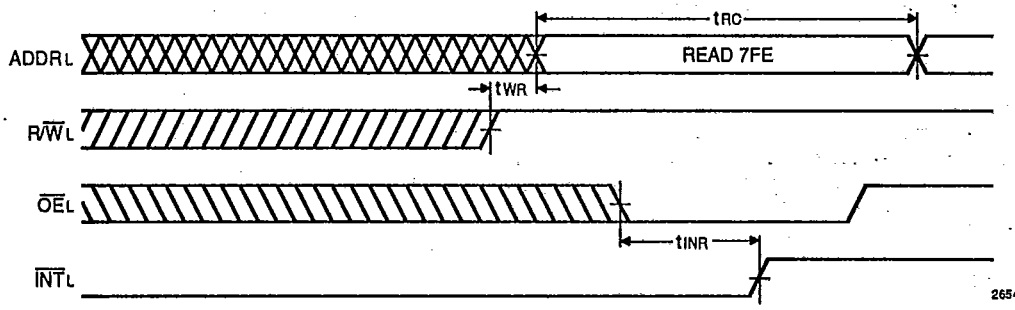
T-46-23-12

TIMING WAVEFORM OF INTERRUPT MODE(1,2)

RIGHT SIDE SETS $\overline{INT}_L$:



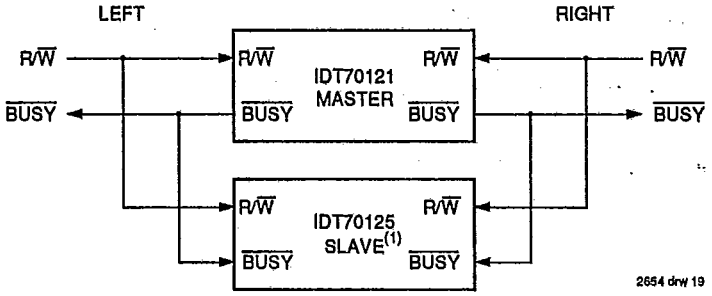
LEFT SIDE CLEARS $\overline{INT}_L$:



2654 drw 18

NOTES:
1. $\overline{CE}_L = \overline{CE}_R = V_{IL}$.
2. $\overline{INT}_L$ and $\overline{INT}_R$ are reset to V_{OH} during power-up.

18-BIT MASTER/SLAVE DUAL-PORT MEMORY SYSTEMS



2654 drw 19

NOTE:
1. No arbitration in IDT70125 (SLAVE). $\overline{BUSY}_{IN}$ inhibits write in IDT70125 (SLAVE).

FUNCTIONAL DESCRIPTION

The IDT70121/IDT70125 provide two ports with separate control, address, and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power-down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power-down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in Table I.

The interrupt flag ($\overline{INT}$) permits communication between ports or systems. If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is set when the right port writes to memory location 7FE (HEX). The left port clears the interrupt by reading address location 7FE. Likewise, the right port interrupt flag ($\overline{INT}_R$) is set when the left port writes to memory location 7FF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 7FF. The message (9 bits) at 7FE or 7FF is user-defined. If the interrupt function is not used, address locations 7FE and 7FF are not used as mail boxes but as part of the random access memory. Refer to Table II for the interrupt operation.

ARBITRATION LOGIC, FUNCTIONAL DESCRIPTION

The arbitration logic will resolve an address match or a chip enable match down to 5ns minimum and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the delayed port.

The $\overline{BUSY}$ flags are provided for the situation when both ports simultaneously access the same memory location. When this situation occurs, on-chip arbitration logic will determine which port has access and sets the delayed port's $\overline{BUSY}$ flag. $\overline{BUSY}$ is set at speeds that permit the processor to hold the operation and its respective address and data. It is important to note that the write operation is invalid for the port that has $\overline{BUSY}$ set LOW. The delayed port will have access when $\overline{BUSY}$ goes inactive.

Contention occurs when both left and right ports are active and both addresses match. When this situation occurs, the on-chip arbitration logic determines access. Two modes of arbitration are provided: (1) if the addresses match and are valid before $\overline{CE}$, on-chip logic arbitrates between $\overline{CE}_L$ and $\overline{CE}_R$ for access; or (2) if the $\overline{CE}$s are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to Table III). In either mode of arbitration, the delayed port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation.

DATA BUS WIDTH EXPANSION, MASTER/SLAVE DESCRIPTION

Expanding the data bus width to eighteen-or-more-bits in a dual-port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another activates its $\overline{BUSY}_R$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To avoid this "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding dual-port RAMs in width, the writing of the SLAVE RAMs must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all dual-port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

TRUTH TABLES

TABLE I. NON-CONTENTION READ/WRITE CONTROL[4]

Left or Right Port[1]				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-8}	Function
X	H	X	Z	Port Disabled and in Power-Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L$ = H, Power-Down Mode, I_{SB1} or I_{SB3}
L	L	X	DATAIN	Data on Port Written Into Memory[2]
H	L	L	DATAOUT	Data in Memory Output on Port[3]
H	L	H	Z	High Impedance Outputs

2654 tbl 12

NOTES:
1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$.
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

2654 tbl 13

NOTE:
1. This parameter is determined by device characterization but is not production tested.

TABLE II. INTERRUPT FLAG[1,4]

Left Port					Right Port					
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{0L} - A_{10L}$	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{0L} - A_{10R}$	$\overline{INT}_R$	Function
L	L	X	7FF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	7FF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	7FE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	7FE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

2654 tbl 14

NOTES:
1. Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = H.
2. If $\overline{BUSY}_L$ = L, then NC.
3. If $\overline{BUSY}_R$ = L, then NC.
4. H = HIGH, L = LOW, X = DON'T CARE, NC = NO CHANGE

TABLE III. ARBITRATION[2]

Left Port		Right Port		Flags[1]		
$\overline{CE}_L$	$A_{0L} - A_{10L}$	$\overline{CE}_R$	$A_{0R} - A_{10R}$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	Function
H	X	H	X	H	H	No Contention
L	Any	H	X	H	H	No Contention
H	X	L	Any	H	H	No Contention
L	$\neq A_{0R} - A_{10R}$	L	$\neq A_{0L} - A_{10L}$	H	H	No Contention
Address Arbitration With $\overline{CE}$ Low Before Address Match						
L	LV5R	L	LV5R	H	L	L-Port Wins
L	RV5L	L	RV5L	L	H	R-Port Wins
L	Same	L	Same	H	L	Arbitration Resolved
L	Same	L	Same	L	H	Arbitration Resolved
$\overline{CE}$ Arbitration With Address Match Before $\overline{CE}$						
LL5R	= $A_{0R} - A_{10R}$	LL5R	= $A_{0L} - A_{10L}$	H	L	L-Port Wins
RL5L	= $A_{0R} - A_{10R}$	RL5L	= $A_{0L} - A_{10L}$	L	H	R-Port Wins
LW5R	= $A_{0R} - A_{10R}$	LW5R	= $A_{0L} - A_{10L}$	H	L	Arbitration Resolved
LW5R	= $A_{0R} - A_{10R}$	LW5R	= $A_{0L} - A_{10L}$	L	H	Arbitration Resolved

2654 tbl 15

NOTES:
1. $\overline{INT}$ Flags Don't Care.
2. X = DON'T CARE, L = LOW, H = HIGH
   LV5R = Left Address Valid ≥ 5ns before right address.
   RV5L = Right Address Valid ≥ 5ns before left address.
   Same = Left and Right Addresses match within 5ns of each other.
   LL5R = Left $\overline{CE}$ = LOW ≥ 5ns before Right $\overline{CE}$.
   RL5L = Right $\overline{CE}$ = LOW ≥ 5ns before Left $\overline{CE}$.
   LW5R = Left and right $\overline{CE}$ = LOW within 5ns of each other.