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1. GENERAL DESCRIPTION

The W19B160B is a 16Mbit, 2.7~3.6 volt CMOS flash memory organized as 2M × 8 or 1M × 16 bits. For flexible erase capability, the 16Mbits of data are divided into one 16Kbyte, two 8Kbyte, one 32Kbyte, and thirty-one 64Kbyte sectors. The word-wide (× 16) data appears on DQ15-DQ0, and byte-wide (× 8) data appears on DQ7–DQ0. The device can be programmed and erased in-system with a standard 2.7~3.6V power supply. A 12-volt V_{PP} is not required. The unique cell architecture of the W19B160B results in fast program/erase operations with extremely low current consumption. The device can also be programmed and erased by using standard EPROM programmers.

2. FEATURES

Performance

- 2.7~3.6-volt write (program and erase) operations
- Fast write operation
  - Sector erase time: 0.7s (Typical)
  - Chip erases time: 25 s (Typical)
  - Byte/Word programming time: 5/7 μs (Typical)
- Read access time: 70 ns
- Typical program/erase cycles:
  - 100K
- Twenty-year data retention
- Ultra low power consumption
  - Active current (Read): 9mA (Typical)
  - Active current (Program/erase): 20mA (Typical)
  - Standby current: 0.2 μA (Typical)

Architecture

- Sector erases architecture
  - One 16Kbyte, two 8Kbyte, one 32Kbyte, and thirty-one 64Kbyte sectors
  - Top or bottom boot block configurations available
  - Supports full chip erase
- JEDEC standard byte-wide and word-wide pin-outs TTL compatible I/O
- Manufactured on WinStack-S 0.13μm process technology
- Available packages: 48-pin TSOP and 48-ball TFBGA (6x8mm)

Software Features

- Compatible with common Flash Memory Interface (CFI) specification
  - Flash device parameters stored directly on the device
  - Allows software driver to identify and use a variety of different current and future Flash products
- End of program detection

- Software method: Toggle bit/Data polling

- Erase Suspend /Erase Resume
  - Suspend an erase operation to read data or program data.
  - Resume erase suspend operation.
- Unlock bypass program command
  - Allows the system to program bytes or words to device faster than standard program command.

Hardware Features

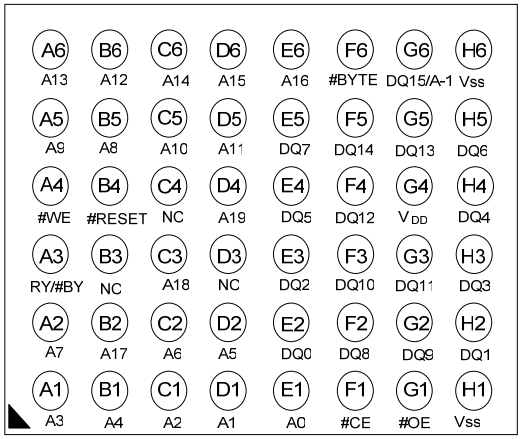
- Ready/#Busy output (RY/#BY)
  - Detect program or erase cycle completion
- Hardware reset pin (#RESET)
  - Reset the internal state machine to the read mode
- Sector Protection
  - Sectors can be locked in-system or via programmer
  - Temporary Sector Unprotect allows changing data in protected sectors in-system

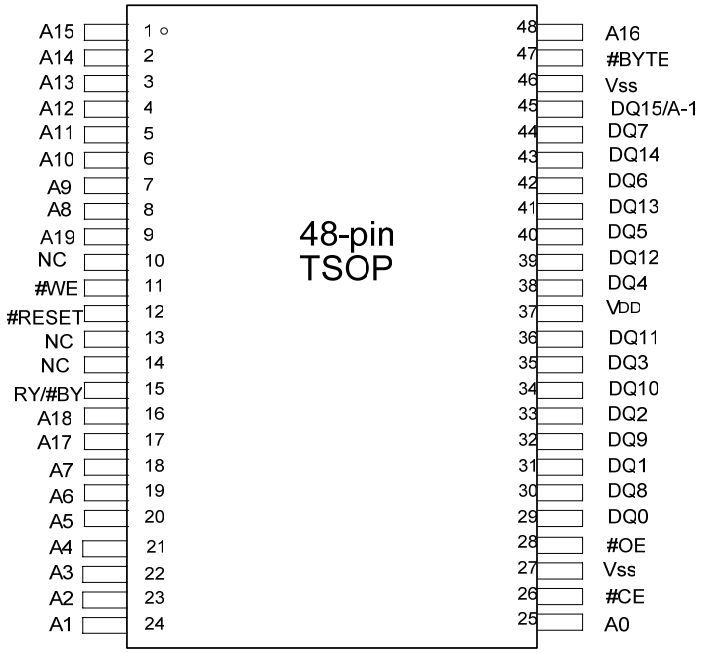
Temperature range

- Extended temperature range (-20℃ to 85 ℃)
- Industrial devices ambient temperature(-40℃ to +85℃)

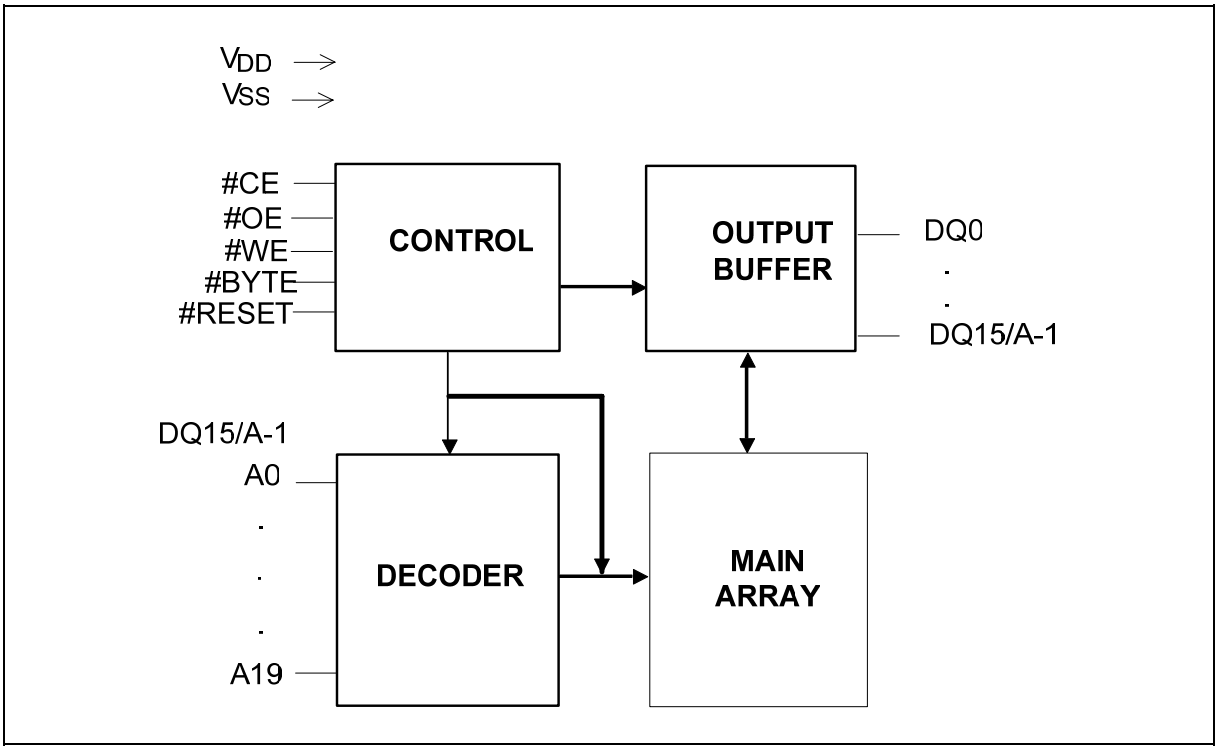
3. PIN CONFIGURATIONS

48-Ball TFBGA
(Top View, Balls Face Down)





4. BLOCK DIAGRAM



5. PIN DESCRIPTION

SYMBOL	PIN NAME	
A0–A19	Address Inputs	
DQ0–DQ14	Data Inputs/Outputs	
DQ15/A-1	Word mode	DQ15 is Data Inputs/Outputs
	Byte mode	A-1 is Address input
#CE	Chip Enable	
#OE	Output Enable	
#WE	Write Enable	
#BYTE	Byte Enable Input	
#RESET	Hardware Reset	
RY/#BY	Ready/Busy Status	
V_{DD}	Power Supply	
V_{SS}	Ground	
NC	No Connection	

6. FUNCTIONAL DESCRIPTION

6.1 DEVICE BUS OPERATION

6.1.1 Word/Byte Configuration

The #BYTE pin controls the device data I/O pins operate whether in the byte or word configuration. When the #BYTE pin is '1', the device is in word configuration; DQ15-DQ0 are active and controlled by #CE and #OE.

When the #BYTE pin is '0', the device is in byte configuration, and only data I/O pins DQ7-DQ0 are active and controlled by #CE and #OE. The data I/O pins DQ8-DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

6.1.2 Reading Array Data

To read array data from the outputs, the #CE and #OE pins must be set to V_{IL}. #CE is the power control and used to select the device. #OE is the output control gates array data to the output pins. #WE should stay at V_{IH}. The #BYTE pin determines the device outputs array data whether in words or bytes.

The internal state machine is set for reading array data when device power-up, or after hardware reset. This ensures that no excess modification of the memory content occurs during the power transition. In this mode there is no command necessary to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are changed.

6.1.3 Writing Commands/Command Sequences

In writhing a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive #WE and #CE to V_{IL}, and #OE to V_{IH}.

For program operations, the #BYTE pin determines the device accepts program data whether in bytes or in words. Refer to "Word/Byte Configuration" for more information.

The erase operation can erase a sector, multiple sectors, even the entire device. The "sector address" is the address bits required to solely select a sector.

6.1.4 Program and Erase Operation Status

During an erase or program operation, the system may check the status of the operation by reading the status bits on DQ7 – DQ0. Refer to "Write Operation Status" and "AC Characteristics" for more information.

6.1.5 Standby Mode

When the system is not reading or writing to the device, the device will be in a standby mode. In this mode, current consumption is greatly reduced, and the outputs are in the high impedance state, independent from the #OE input.

When the #CE and #RESET pins are both held at $V_{DD} \pm 0.3V$, the device enters into the CMOS standby mode (note that this is a more restricted voltage range than V_{IH}.) When #CE and #RESET are

held at V_{IH}, but not within V_{DD} ±0.3V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

When the device is deselected during erasing or programming, the device initiates active current until the operation is completed.

6.1.6 Automatic Sleep Mode

The automatic sleep mode minimizes device's energy consumption. When addresses remain stable for t_{ACC} +30 nS, the device will enable this mode automatically. The automatic sleep mode is independent from the #CE, #WE, and #OE control signals. Standard address access timings provide new data when addresses are changed. In sleep mode, output data is latched and always available to the system.

6.1.7 #RESET: Hardware Reset Pin

The #RESET pin provides a hardware method to reset the device to reading array data. When the #RESET pin is set to low for at least a period of t_{RP}, the device will immediately terminate every operations in progress, tri-states all output pins, and ignores all read/write commands for the duration of the #RESET pulse. The device also resets the internal state machine to reading array data mode. To ensure data integrity, the interrupted operation needs to be reinitiated when the device is ready to accept another command sequence.

Current is reduced for the duration of the #RESET pulse. When #RESET is held at Vss ±0.3V, the device initiates the CMOS standby current (I_{CC4}). If #RESET is held at V_{IL} but not within Vss ±0.3V, the standby current will be greater.

The #RESET pin may be tied to the system-reset circuitry. Thus the system reset would also reset the device, enabling the system to read the boot-up firmware from the device.

If #RESET is asserted during the program or erase operation, the RY/#BY pin will be at “0” (busy) until the internal reset operation is complete. If #RESET is asserted when a program or erase operation is not processing (RY/#BY pin is “1”), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). After the #RESET pin returns to V_{IH}, the system can read data t_{RH}.

6.1.8 Output Disable Mode

When the #OE input is at V_{IH}, output from the device is disabled. The output pins are set in the high impedance state.

6.1.9 Auto-select Mode

The auto select mode offers manufacturer and device identification, as well as sector protection verification, through identifier codes output on DQ7-DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the auto select codes can also be accessed in-system through the command register.

When using programming equipment , the auto select mode requires V_{ID} (8.5 V to 11.5 V) on address pins A9. Address pins A6, A1, and A0 must be as shown in auto select table. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7-DQ0.

To access the auto select codes in-system, the host system can issue the auto select command through the command register. This method does not require V_{ID}. Also refer to the auto select Command Sequence section for more information.

6.1.10 Sector Protection and Un-protection

The sector protection feature will disable both program and erase operations in any sectors. The sector un-protection feature will re-enables both program and erase operations in previously protected sectors. Sector protection / un-protection can be implemented through two methods.

The primary method requires V_{ID} on the #RESET pin, and can be implemented either in-system or through programming equipment. This method uses standard microprocessor bus cycle timing.

The alternate method intended only for programming equipment requires V_{ID} on address pin A9 and #OE It is possible to determine whether a sector is protected or unprotected. See the auto select Mode section for details.

6.1.11 Temporary Sector Unprotect

This feature allows temporary un-protection of previously protected sectors to change data in-system. When the #RESET pin is set to V_{ID}, the Sector Unprotect mode is activated. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. What if V_{ID} is removed from the #RESET pin, all the previously protected sectors are protected again.

6.1.12 Hardware Data Protection

The command sequence requirements of unlock cycles for programming or erasing provides data protection against negligent writes. In addition, the following hardware data protection measures prevent inadvertent erasure or programming, which might be caused by spurious system level signals during V_{DD} power-up and power-down transitions, or from system noise.

6.1.13 Write Pulse “Glitch” Protection

Noise pulses, which is less than 5nS (typical) on #OE, #CE or #WE, do not initiate a write cycle.

6.1.14 Logical Inhibit

Write cycles are inhibited by holding any one of #OE = V_{IL}, #CE = V_{IH} or #WE = V_{IH}. #CE and #WE must be a logical zero while #OE is a logical one to initiate a write cycle.

6.1.15 Power-Up Write Inhibit

During power up, if #WE = #CE = V_{IL} and #OE = V_{IH}, the device does not accept commands on the rising edge of #WE. The internal state machine is automatically reset to the read mode on power-up.

6.2 COMMAND DEFINITIONS

The device operation can be initiated by writing specific address and data commands or sequences into the command register. The device will be reset to reading array data when writing incorrect address and data values or writing them in the improper sequence.

The addresses will be latched on the falling edge of #WE or #CE, whichever happens later; while the data will be latched on the rising edge of #WE or #CE, whichever happens first. Please refer to timing waveforms.

6.2.1 Reading Array Data

After device power-up, it is automatically set to reading array data. There is no commands are required to retrieve data. After completing an Embedded Program or Embedded Erase algorithm, the device is ready to read array data.

The system must initiate the reset command to return the device to read mode if DQ5 goes high during an active program or erase operation; otherwise, the device is in the auto select mode. See Reset Command section and Requirements for Reading Array Data in the Device Bus Operations section for more information.

6.2.2 Reset Command

The device will be to the read when writing the reset command. For this command, the address bits are Don't Care.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to which the system was writing to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device, to which the system was writing to the read mode. The reset command may be written between the sequence cycles in an auto select command sequence. When in the auto select mode, the reset command must be written to return to the read mode. If DQ5 goes high during a program or erase operation, writing the reset command returns the device to the read mode.

6.2.3 Auto-select Command Sequence

The auto select command sequence provides the host system to access the manufacturer and device codes, and determine whether a sector is protected or not. This is an alternative method, which is intended for PROM programmers and requires V_{ID} on address pin A9. The auto select command sequence may be written to an address within the device that is in the read mode. When the device is actively programming or erasing, the auto select command may not be written.

The first writing two unlock cycles initiate the auto select command sequence. This is followed by a third write cycle that contains the auto select command. The device then enters into the auto select mode. The system may read at any address without initiating another auto select command sequence:

- A read cycle at address XX00h returns the manufacturer code.
- A read cycle at address XX01h in word mode (or XX02h in byte mode) returns the device code.
- A read cycle to an address containing a sector address (SA), and the address 02h on A7-A0 in word mode (or the address 04h in byte mode) returns 01h if the sector is protected, or 00h if it is unprotected.

To return to read mode and exit the auto select mode, the system must write the reset command.

6.2.4 Byte/Word Program Command Sequence

The device can be programmed either by word or byte, which depending on the state of the #BYTE pin. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program setup command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The device automatically provides internally generated program pulses and verifies the programmed cell margin.

Once the Embedded Program algorithm is complete, the device then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/#BY. Please refer to the Write Operation Status section for bits' information.

Any commands written to the device during the Embedded Program Algorithm are ignored. Please note that a hardware reset will immediately stop the program operation. The program command sequence should be reinitiated when the device has returned to the read mode, in order to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. A bit cannot be programmed from “0” back to “1.” If trying to do so may cause that device to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate that the operation is successful. However, a succeeding read will show that the data is still “0.” Only erase operations can change “0” to “1.”

6.2.5 Chip Erase Command Sequence

Chip erase is a six-bus cycle operation. Writing two unlock cycles initiates the chip erase command sequence, which is followed by a set-up command. After chip erase command, two additional unlock write cycles are then followed, which in turn invokes the Embedded Erase algorithm. The system preprogram is not required prior to erase. Before electrical erase, the Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern. Any controls or timings during these operations is not required in system.

As the Embedded Erase algorithm is complete, the device returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, or RY/#BY. Please refer to the Write Operation Status section for information on these status bits.

Any commands written during the chip erase operation will be ignored. However, a hardware reset shall terminate the erase operation immediately. If this happens, to ensure data integrity, the chip erase command sequence should be reinitiated when the device has returned to reading array data.

6.2.6 Sector Erase Command Sequence

Sector erase is a six-bus cycle operation. Writing two unlock cycles initiates the sector erase command sequence, which is followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command.

The device does not require the system to preprogram before erase. Before electrical erase, the Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern. Any controls or timings during these operations is not required in system.

As the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. Please refer to the Write Operation Status section for information on these status bits.

However, a hardware reset shall terminate the erase operation immediately. If this occurs, to ensure data integrity, the sector erase command sequence should be reinitiated once the device has returned to reading array data.

6.2.7 Erase Suspend /Erase Resume Commands

The Erase Suspend Command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50us time out period during the sector erase command sequence. The Erase Suspend Command is ignored if written during the chip erase operation or embedded program algorithm. Writing the Erase Suspend Command during the Sector Erase time-out immediately terminals the time-out period and suspends the erase operation. Addresses are as don't cares when writer the Erase Suspend Command.

When the Erase Suspend Command is written during a sector erase operation, the device requires a maximum of 20us to suspend the erase operation. However, when the Erase Suspend Command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the system can read array data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Normal read and writes timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on DQ7-DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See Write Operation Status for information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See Write Operation Status for more information.

The system may also write the auto-select command sequence when the device is in the erase suspend mode. The device allows reading auto-select codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the auto-select mode, the device reverts to the erase suspend mode, and is ready for another valid operation. See Auto-select Command Sequence for more information.

The system must write the erase resume command (address bits are don't care) to exit the erase suspend mode and continue the sector erase operation. Further writes of the resume command are ignored. Another Erase Suspend Command can be written after the device has resumed erasing.

6.2.8 Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program bytes or words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device enters the unlock bypass command mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses

with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Command Definitions shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock By-pass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h; the second cycle the data 00h. Addresses are don't care for both cycles. The device then returns to reading array data.

Program/Erase operation refer Program Algorithm and Erase Algorithm illustration.

6.3 WRITE OPERATION STATUS

The device provides several bits to determine the status of a program or erase operation: DQ5, DQ6, and DQ7. Each of DQ7 and DQ6 provides a method for determining whether a program or erase operation is complete or in progress. The device also offers a hardware-based output signal, RY/#BY, to determine whether an Embedded Program or Erase operation is in progress or has been completed.

6.3.1 DQ7: #Data Polling

The #Data Polling bit, DQ7, indicates whether an Embedded Program or Erase algorithm is in progress or completed. Data Polling is valid after the rising edge of the final #WE pulse in the command sequence.

During the Embedded Program algorithm, the device outputs on DQ7 and the complement of the data programmed to DQ7. When the Embedded Program algorithm is complete, the device outputs the data programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, #Data Polling on DQ7 is active for about 1μS, and then the device returns to the read mode.

During the Embedded Erase algorithm, #Data Polling produces "0" on DQ7.Once the Embedded Erase algorithm has completed, #Data Polling produces "1" on DQ7. An address within any of the sectors selected for erasure must be provided to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, #Data Polling on DQ7 is active for about 100μS, and then the device returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just before the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ0-DQ6 while Output Enable (#OE) is set to low. That is, the device may change from providing status information to valid data on DQ7. Depending on when it samples the DQ7 output, the system may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ0-DQ6 may be still invalid. Valid data on DQ7-DQ0 will appear on successive read cycles.

6.3.2 RY/#BY: Ready/#Busy

The RY/#BY is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/#BY status is valid after the rising edge of the final #WE pulse in the

command sequence. Since RY/#BY is an open-drain output, several RY/#BY pins can be tied together in parallel with a pull-up resistor to V_{DD}.

When the output is low (Busy), the device is actively erasing or programming. When the output is high (Ready), the device is in the read mode.

6.3.3 DQ6: Toggle Bit

Toggle Bit on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete. Toggle Bit may be read at any address, and is valid after the rising edge of the final #WE pulse in the command sequence (before the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either #OE or #CE to control the read cycles. Once the operation has completed, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for about 100μS, and then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors which are protected.

If a program address falls within a protected sector, DQ6 toggles for about 1 μs after the program command sequence is written, and then returns to reading array data.

6.3.4 DQ2: Toggle Bit II

When used with DQ6, the “Toggle Bit II” on DQ2 indicates whether a particular sector is actively erasing (i.e., the Embedded Erase algorithm is in progress), or the sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final #WE pulse in the command sequence.

DQ2 toggles as the system reads at addresses within those sectors that have been selected for erasure. (The system may use either #OE or #CE to control the read cycles.) But DQ2 cannot distinguish that whether the sector is actively erasing or is erase-suspended. By comparison, DQ6 indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Therefore, both status bits are required for sector and mode information.

6.3.5 Reading Toggle Bits DQ6/DQ2

Whenever the system initially starts to read toggle bit status, it must read DQ0–DQ7 at least twice in a row to determine whether a toggle bit is toggling or not. Typically, the system would note and store the value of the toggle bit after the first read. While after the second read, the system would compare the new value of the toggle bit with the first one. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ0–DQ7 on the following read cycle.

However, if after the initial two read cycles, the system finds that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high or not(see the section on DQ5). If DQ5 is high, the system should then determine again whether the toggle bit is toggling or not, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation, and the system must write the reset command to return to reading array data.

Then the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, and determines the status as described in the previous paragraph. Alternatively, the system may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm while it returns to determine the status of the operation.

6.3.6 DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether erasure has begun or not. (The sector erase timer does not apply to the chip erase command.) The entire time-out applies after each additional sector erase command if additional sectors are selected for erasure. Once the timeout period has completed, DQ3 switches from “0” to “1.” If the time between additional sector erase commands from the system can be assumed to be less than 50 μS, the system need not monitor, DQ3 does not need to be monitored. Please also refer to Sector Erase Command Sequence section.

After the sector erase command is written, the system should read the status of DQ7 (#Data Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is“1,” the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is “0,” the device will accept additional sector erase commands.

The system software should check the status of DQ3 before and following each subsequent sector erase command to ensure the command has been accepted. If DQ3 is high on the second status check, the last command might not have been accepted.

6.3.7 DQ5 : Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. DQ5 produces “1” under these conditions which indicates that the program or erase cycle was not successfully completed.

The device may output “1” on DQ5 if the system tries to program “1” to a location that was previously programmed to “0.” Only the erase operation can change “0” back to “1.” Under this condition, the device stops the operation, and while the timing limit has been exceeded, DQ5 produces “1.”

7. SPECIAL CHARACTERISTIC

The W19B160B provides a good performance in the wireless products. It is concerned with access speed. If the access speed is quick to meet the demand of specification (70nS), the system’s application is widely and performance is better than other low speed products.

8. TABLE OF OPERATION MODES

8.1 Device Bus Operations

MODE	#CE	#OE	#WE	#RESET	ADDRESS (1)	DQ0-DQ7	DQ8-DQ15	
							BYTE =VIH	BYTE =VIL
Read	L	L	H	H	AIN	DOUT	DOUT	DQ8-DQ14=High-Z DQ15=A-1
Write	L	H	L	H	AIN	DIN	DIN	
Standby	VDD ± 0.3V	X	X	VDD ± 0.3V	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	X	High-Z	High-Z	High-Z
Sector Protect (2)	L	H	L	VID	SA, A6=L, A1=H, A0=L	DIN	X	X
Sector Unprotect (2)	L	H	L	VID	SA, A6=H, A1=H, A0=L	DIN	X	X
Temporary Sector Unprotect	X	X	X	VID	AIN	DIN	DIN	High-Z

Legend : L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 8.5-11.5V, X = Don't Care, SA = Sector Address, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out

Notes :

1. Addresses are A19:A0 in word mode (#BYTE = V_{IH}), A19:A-1 in byte mode (#BYTE = V_{IL}).
2. The sector protect and sector unprotect functions may also be implemented via programming equipment. See the" Sector Protection and Unprotect ion" section.Auto-select Codes (High Voltage Method)

DESCRIPTION	#CE	#OE	#WE	A19 TO A12	A11 TO A10	A9	A8 TO A7	A6	A5 TO A2	A1	A0	DQ8 TO DQ15	DQ7 TO DQ0
Manufacturer ID: Winbond	0	0	1	X	X	V_{ID}	X	0	X	0	0	X	DAh
Device ID: W19B160BT (Top Boot Block)	0	0	1	X	X	V_{ID}	X	0	X	0	1	22h (Word)	C4h
Device ID: W19B160BB (Bottom Boot Block)	0	0	1	X	X	V_{ID}	X	0	X	0	1	22h (Word)	49h
Sector Protection Verification	0	0	1	SA	X	V_{ID}	X	0	X	1	0	X	01h (protected) 00h (unprotected)

Legend : SA= Sector Address, X= Don't Care , V_{ID} = 8.5-11.5V , L = Logic 0 = V_{IL} , H = Logic 1 = V_{IH}.

8.2 Sector Address Table (Top Boot Block)

SECTOR	SECTOR ADDRESS A19-A12	SECTOR SIZE (KBYTES/KWORDS)	(X8) ADDRESS RANGE	(X16) ADDRESS RANGE
SA0	00000XXX	64/32	000000h-00FFFFh	00000h-07FFFh
SA1	00001XXX	64/32	010000h-01FFFFh	08000h-0FFFFh
SA2	00010XXX	64/32	020000h-02FFFFh	10000h-17FFFh
SA3	00011XXX	64/32	030000h-03FFFFh	18000h-1FFFFh
SA4	00100XXX	64/32	040000h-04FFFFh	20000h-27FFFh
SA5	00101XXX	64/32	050000h-05FFFFh	28000h-2FFFFh
SA6	00110XXX	64/32	060000h-06FFFFh	30000h-37FFFh
SA7	00111XXX	64/32	070000h-07FFFFh	38000h-3FFFFh
SA8	01000XXX	64/32	080000h-08FFFFh	40000h-47FFFh
SA9	01001XXX	64/32	090000h-09FFFFh	48000h-4FFFFh
SA10	01010XXX	64/32	0A0000h-0AFFFFh	50000h-57FFFh
SA11	01011XXX	64/32	0B0000h-0BFFFFh	58000h-5FFFFh
SA12	01100XXX	64/32	0C0000h-0CFFFFh	60000h-67FFFh
SA13	01101XXX	64/32	0D0000h-0DFFFFh	68000h-6FFFFh
SA14	01110XXX	64/32	0E0000h-0EFFFFh	70000h-77FFFh
SA15	01111XXX	64/32	0F0000h-0FFFFFh	78000h-7FFFFh
SA16	10000XXX	64/32	100000h-10FFFFh	80000h-87FFFh
SA17	10001XXX	64/32	110000h-11FFFFh	88000h-8FFFFh
SA18	10010XXX	64/32	120000h-12FFFFh	90000h-97FFFh
SA19	10011XXX	64/32	130000h-13FFFFh	98000h-9FFFFh
SA20	10100XXX	64/32	140000h-14FFFFh	A0000h-A7FFFh
SA21	10101XXX	64/32	150000h-15FFFFh	A8000h-AFFFFh
SA22	10110XXX	64/32	160000h-16FFFFh	B0000h-B7FFFh
SA23	10111XXX	64/32	170000h-17FFFFh	B8000h-BFFFFh
SA24	11000XXX	64/32	180000h-18FFFFh	C0000h-C7FFFh
SA25	11001XXX	64/32	190000h-19FFFFh	C8000h-CFFFFh
SA26	11010XXX	64/32	1A0000h-1AFFFFh	D0000h-D7FFFh
SA27	11011XXX	64/32	1B0000h-1BFFFFh	D8000h-DFFFFh
SA28	11100XXX	64/32	1C0000h-1CFFFFh	E0000h-E7FFFh
SA29	11101XXX	64/32	1D0000h-1DFFFFh	E8000h-EFFFFh
SA30	11110XXX	64/32	1E0000h-1EFFFFh	F0000h-F7FFFh
SA31	111110XX	32/16	1F0000h-1F7FFFh	F8000h-FBFFFh
SA32	11111100	8/4	1F8000h-1F9FFFh	FC000h-FCFFFh
SA33	11111101	8/4	1FA000h-1FBFFFh	FD000h-FDFFFh
SA34	1111111X	16/8	1FC000h-1FFFFFh	FE000h-FFFFFh

Note : The address range is [A19: A-1] in byte mode (#BYTE =VIL) or [A19:A0] in word mode (#BYTE =VIH).

8.3 Sector Address Table (Bottom Boot Block)

SECTOR	SECTOR ADDRESS A19-A12	SECTOR SIZE (KBYTES/KWORDS)	(X8) ADDRESS RANGE	(X16) ADDRESS RANGE
SA0	0000000X	16/8	000000h-003FFFh	00000h-01FFFh
SA1	00000010	8/4	004000h-005FFFh	02000h-02FFFh
SA2	00000011	8/4	006000h-007FFFh	03000h-03FFFh
SA3	000001XX	32/16	008000h-00FFFFh	04000h-07FFFh
SA4	00001XXX	64/32	010000h-01FFFFh	08000h-0FFFFh
SA5	00010XXX	64/32	020000h-02FFFFh	10000h-17FFFh
SA6	00011XXX	64/32	030000h-03FFFFh	18000h-1FFFFh
SA7	00100XXX	64/32	040000h-04FFFFh	20000h-27FFFh
SA8	00101XXX	64/32	050000h-05FFFFh	28000h-2FFFFh
SA9	00110XXX	64/32	060000h-06FFFFh	30000h-37FFFh
SA10	00111XXX	64/32	070000h-07FFFFh	38000h-3FFFFh
SA11	01000XXX	64/32	080000h-08FFFFh	40000h-47FFFh
SA12	01001XXX	64/32	090000h-09FFFFh	48000h-4FFFFh
SA13	01010XXX	64/32	0A0000h-0AFFFFh	50000h-57FFFh
SA14	01011XXX	64/32	0B0000h-0BFFFFh	58000h-5FFFFh
SA15	01100XXX	64/32	0C0000h-0CFFFFh	60000h-67FFFh
SA16	01101XXX	64/32	0D0000h-0DFFFFh	68000h-6FFFFh
SA17	01110XXX	64/32	0E0000h-0EFFFFh	70000h-77FFFh
SA18	01111XXX	64/32	0F0000h-0FFFFFh	78000h-7FFFFh
SA19	10000XXX	64/32	100000h-10FFFFh	80000h-87FFFh
SA20	10001XXX	64/32	110000h-11FFFFh	88000h-8FFFFh
SA21	10010XXX	64/32	120000h-12FFFFh	90000h-97FFFh
SA22	10011XXX	64/32	130000h-13FFFFh	98000h-9FFFFh
SA23	10100XXX	64/32	140000h-14FFFFh	A0000h-A7FFFh
SA24	10101XXX	64/32	150000h-15FFFFh	A8000h-AFFFFh
SA25	10110XXX	64/32	160000h-16FFFFh	B0000h-B7FFFh
SA26	10111XXX	64/32	170000h-17FFFFh	B8000h-BFFFFh
SA27	11000XXX	64/32	180000h-18FFFFh	C0000h-C7FFFh
SA28	11001XXX	64/32	190000h-19FFFFh	C8000h-CFFFFh
SA29	11010XXX	64/32	1A0000h-1AFFFFh	D0000h-D7FFFh
SA30	11011XXX	64/32	1B0000h-1BFFFFh	D8000h-DFFFFh
SA31	11100XXX	64/32	1C0000h-1CFFFFh	E0000h-E7FFFh
SA32	11101XXX	64/32	1D0000h-1DFFFFh	E8000h-EFFFFh
SA33	11110XXX	64/32	1E0000h-1EFFFFh	F0000h-F7FFFh
SA34	11111XXX	64/32	1F0000h-1FFFFFh	F8000h-FFFFFh

Note: The address range is [A19:A-1] in byte mode (#BYTE =VIL) or [A19:A0] in word mode (#BYTE =VIH).

8.4 CFI Query Identification String

DESCRIPTION	ADDRESS (WORD MODE)	DATA	ADDRESS (BYTE MODE)
Query-unique ASCII string "QRY"	10h 11h 12h	0051h 0052h 0059h	20h 22h 24h
Primary OEM Command Set	13h 14h	0002h 0000h	26h 28h
Address for Primary Extended Table	15h 16h	0040h 0000h	2Ah 2Ch
Alternate OEM Command Set (00h=none exists)	17h 18h	0000h 0000h	2Eh 30h
Address for Alternate OEM Extended Table (00h=none exists)	19h 1Ah	0000h 0000h	32h 34h

8.5 System Interface String

DESCRIPTION	ADDRESS (WORD MODE)	DATA	ADDRESS (BYTE MODE)
V_{DD} Min. (write/erase) D7-D4: volt , D3-D0: 100 mV	1Bh	0027h	36h
V_{DD} Max. (write/erase) D7-D4: volt , D3-D0: 100 mV	1Ch	0036h	38h
V_{PP} Min. voltage (00h=no Vpp pin present)	1Dh	0000h	3Ah
V_{PP} Max. voltage (00h=no Vpp pin present)	1Eh	0000h	3Ch
Typical timeout per single byte/word write 2^N S	1Fh	0004h	3Eh
Typical timeout for Min. size buffer write 2^N S (00h=not supported)	20h	0000h	40h
Typical timeout per individual block erase 2^N mS	21h	000Ah	42h
Typical timeout for full chip erase 2^N mS (00h=not supported)	22h	0000h	44h
Max. timeout for byte/word write 2^N times typical	23h	0005h	46h
Max. timeout for buffer write 2^N times typical	24h	0000h	48h
Max. timeout per individual block erase 2^N times typical	25h	0004h	4Ah
Max. timeout full chip erase 2^N times typical (00h = not supported)	26h	0000h	4Ch

8.6 Device Geometry Definition

DESCRIPTION	ADDRESS (WORD MODE)	DATA	ADDRESS (BYTE MODE)
Device size =2^N bytes	27h	0015h	4Eh
Flash device interface description (refer to CFI publication 100)	28h	0002h	50h
	29h	0000h	52h
Max. number of bytes in multi-byte write=2^N (00h=not supported)	2Ah	0000h	54h
	2Bh	0000h	56h
Number Of Erase Block Regions Within Devices	2Ch	0004h	58h
Erase block region 1 information (refer to the CFI specification or CFI publication 100)	2Dh	0000h	5Ah
	2Eh	0000h	5Ch
	2Fh	0040h	5Eh
	30h	0000h	60h
Erase Block Region 2 Information	31h	0001h	62h
	32h	0000h	64h
	33h	0020h	66h
	34h	0000h	68h
Erase Block Region 3 Information	35h	0000h	6Ah
	36h	0000h	6Ch
	37h	0080h	6Eh
	38h	0000h	70h
Erase Block Region 4 Information	39h	001Eh	72h
	3Ah	0000h	74h
	3Bh	0000h	76h
	3Ch	0001h	78h

8.7 Primary Vendor-Specific Extended Query

DESCRIPTION	ADDRESS (WORD MODE)	DATA	ADDRESS (BYTE MODE)
Query-unique ASCII string "PRI"	40h 41h 42h	0050h 0052h 0049h	80h 82h 84h
Major version number, ASCII	43h	0031h	86h
Minor version number, ASCII	44h	0030h	88h
Address sensitive unlock 0 = Required, 1 = Not required	45h	0000h	8Ah
Erase Suspend 00 = Not supported, 01=Supported	46h	0000h	8Ch
Sector protect 0 = Not supported, X=number of sectors in per group	47h	0001h	8Eh
Sector Temporary Unprotect 00 = Not supported, 01=Supported	48h	0001h	90h
Sector protect/unprotect scheme 00 = Not supported, 01=Supported	49h	0001h	92h
Simultaneous operation 00 = Not supported, 01=Supported	4Ah	0000h	94h
Burst mode type 00 = Not supported, 01=Supported	4Bh	0000h	96h
Page mode type 00 = Not Supported, 01=4 Word Page, 02=8 Word Page	4Ch	0000h	98h

8.8 Command Definitions

COMMAND SEQUENCE (1)		CYCLE	BUS CYCLES (2-5)											
			FIRST		SECOND		THIRD		FOURTH		FIFTH		SIXTH	
			ADDR	DATA	ADDR	DATA	ADDR	DATA	ADDR	DATA	ADDR	DATA	ADDR	DATA
Read (note 6)		1	RA	RD										
Reset (note 7)		1	XXX	F0										
Normal Program	Word	4	555	AA	2AA	55	555	A0	PA	PD				
	Byte		AAA		555		AAA							
Chip Erase	Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
	Byte		AAA		555		AAA		AAA		555		AAA	
Sector Erase	Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
	Byte		AAA		555		AAA		AAA		555			
Unlock pass	Word	3	555	AA	2AA	55	555	20						
	Byte		AAA		555		AAA							
Unlock bypass program		2	XXX	A0	PA	PD								
Unlock bypass reset		2	XXX	90	XXX	F0								
Erase suspend		1	XXX	B0										
Erase resume		1	XXX	30										
AUTOSELECT(note8) Manufacturer Code	Word	4	555	AA	2AA	55	555	90	X00	DA				
	Byte		AAA		555		AAA							
AUTOSELECT(note8) Device Code	Word	4	555	AA	2AA	55	555	90	X01	(note11)				
	Byte		AAA		555		AAA		x02					
AUTOSELECT(note8) Sector Protect Verify (note 9)	Word	4	555	AA	2AA	55	555	90	(SA) X02	XX00 XX01				
	Byte		AAA		555		AAA		(SA) X04	00 01				
Common Flash Interface (CFI) Query (note 10)	Word	1	55	98										
	Byte		AA											

Legend:

X = Don't Care

RA = Address of the memory location to be read.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the #WE or #CE pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of #WE or #CE pulse, whichever happens first.

RD = Data read from location RA during read operation.

SA = Address of the sector to be verified (in auto select mode) or erased. Address bits A19-A12 uniquely select any sector.

Notes:

1. See Bus Operations Table for details.
2. All values are in hexadecimal.
3. Except for the read cycle and the fourth cycle of the auto select command sequence, all bus cycles are write cycles.
4. Data bits DQ15-DQ8 are don't care for unlock and command cycle.
5. Unless otherwise noted, address bits A19-A11 are don't cares for unlock and command cycles.
6. No unlock or command cycles required when reading array data.
7. When device is in the auto select mode, the reset command is required to return to reading array data, or if DQ5 goes high (while the device is providing status data).

8. The fourth cycle of the auto select command sequence is a read cycle.
9. The data is 00h for an unprotected sector and 01h for a protected sector.
10. Command is valid when device is ready to read array data or when device is in auto select mode.
11. See Auto-select Codes table for device ID information.

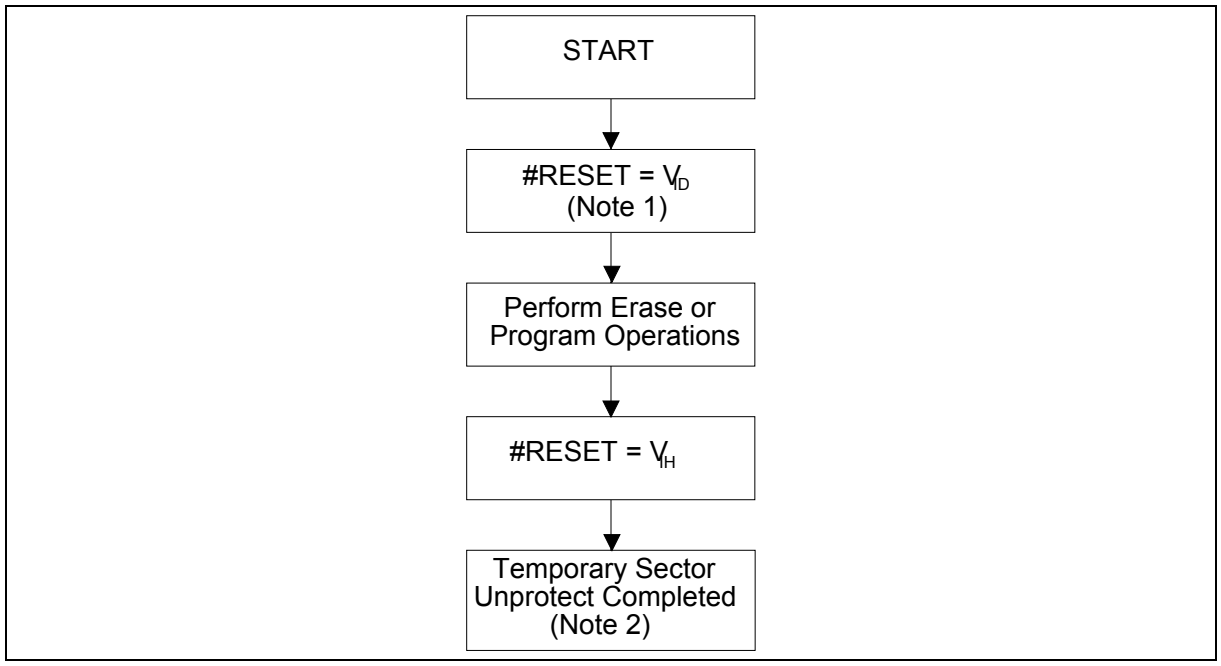
8.9 Write Operation Status

STATUS			DQ7 (NOTE 2)	DQ6	DQ5 (NOTE1)	DQ3	DQ2 (NOTE 2)	RY/#BY
Standard Mode	Embedded Program Algorithm		#DQ7	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Erase-Suspend-Read	Erase Suspended Sector	1	No toggle	0	N/A	Toggle	1
		Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend-Program		#DQ7	Toggle	0	N/A	N/A	0

Notes:

1. DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.
2. DQ7 and DQ2 requires a valid address when reading status information. Please refer to related sections for details.

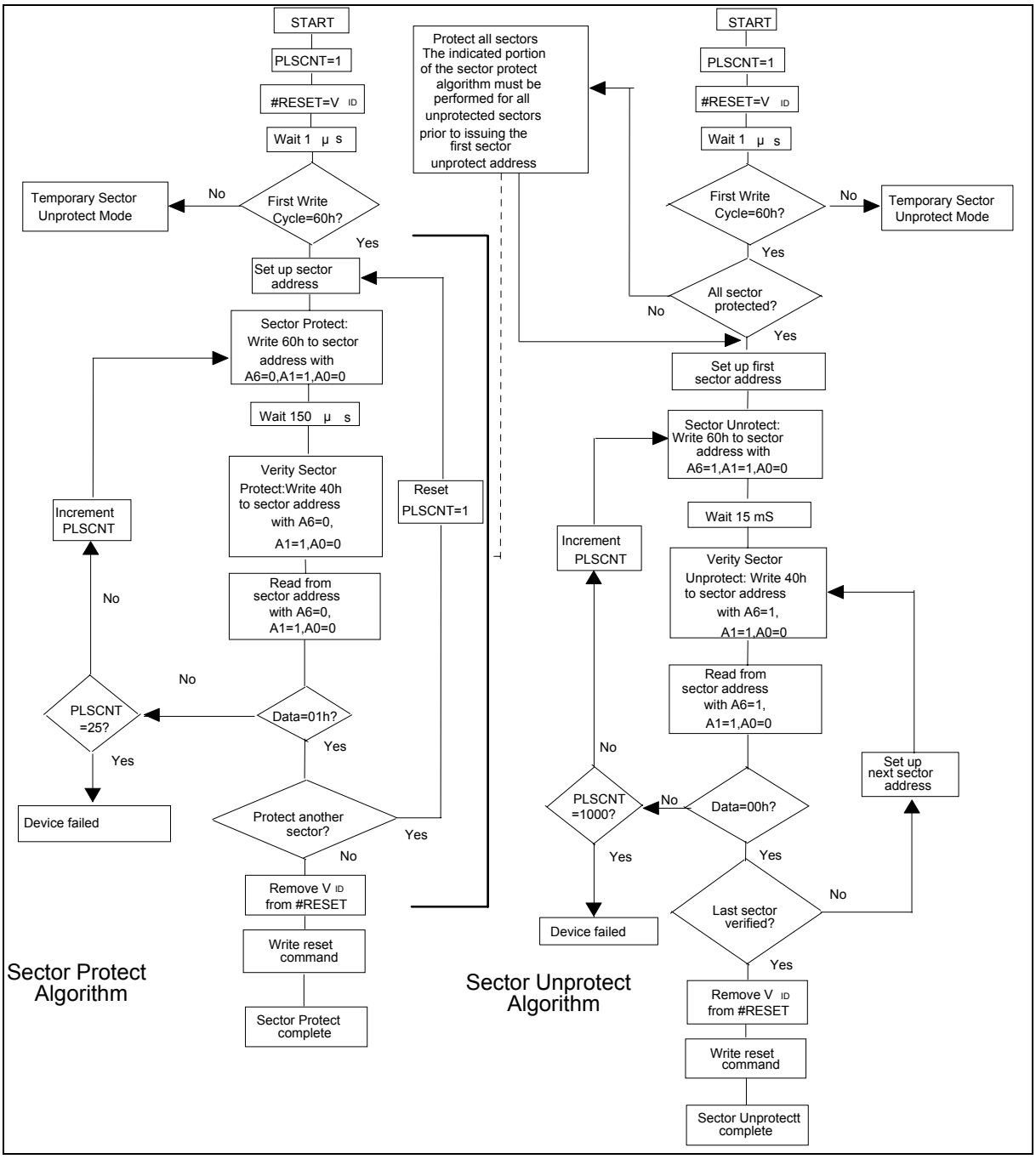
8.10 Temporary Sector Unprotect Algorithm



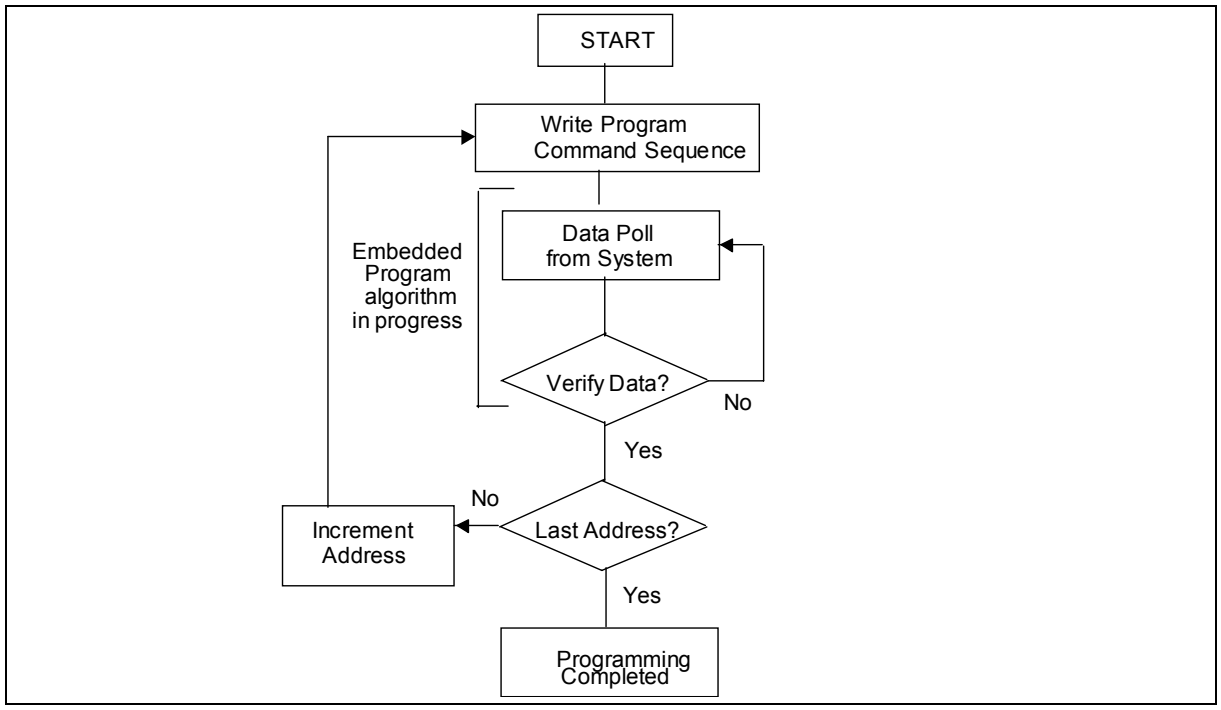
Notes:

1. All protected sectors unprotected.
2. All previously protected sectors are protected once again

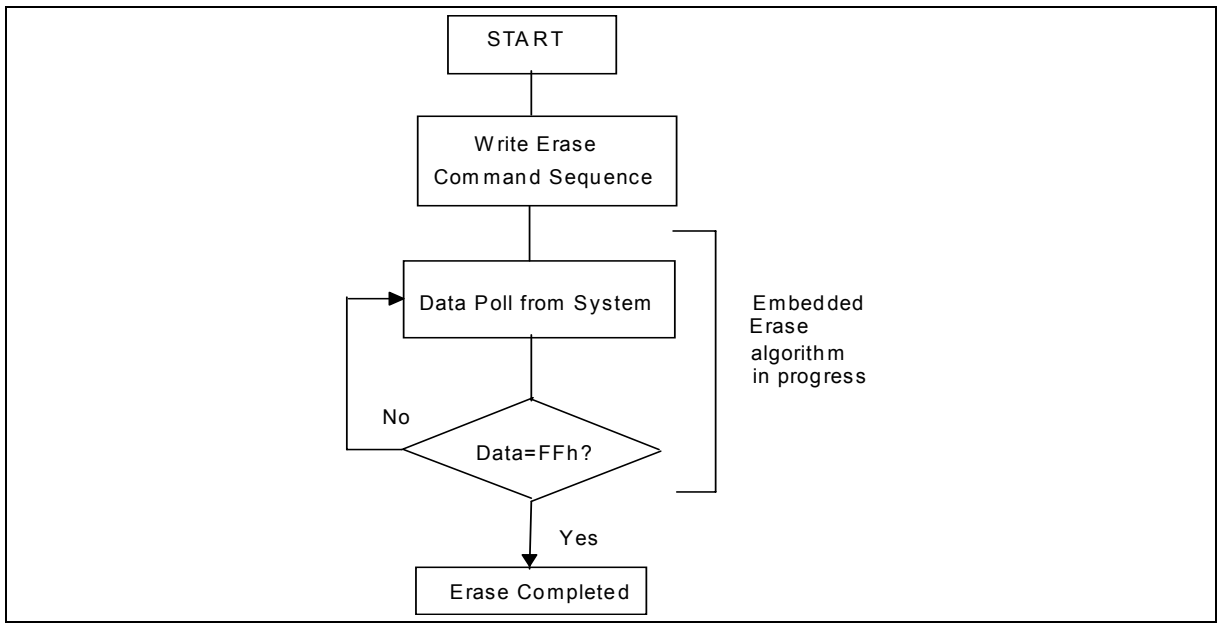
8.11 In-System Sector Protect/Unprotect Algorithms



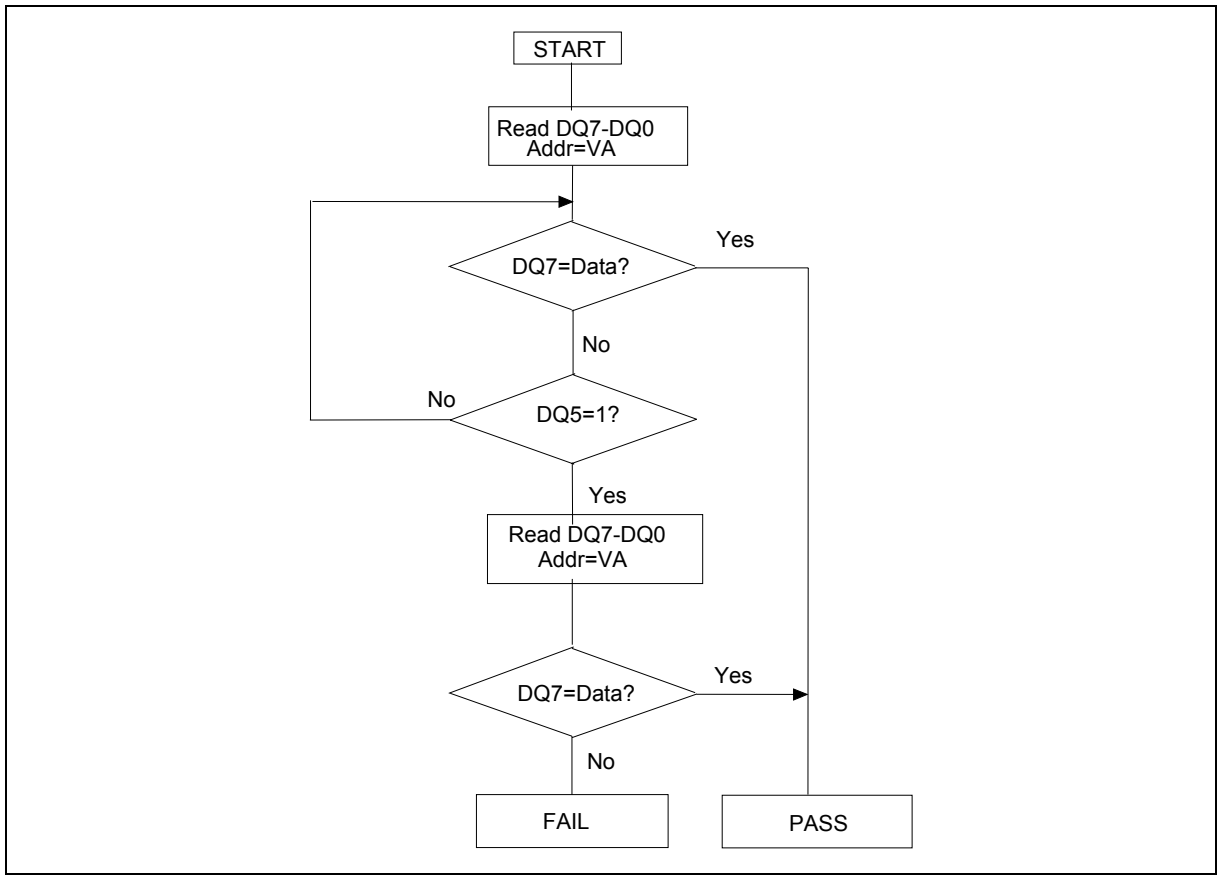
8.12 Program Algorithm



8.13 Erase Algorithm



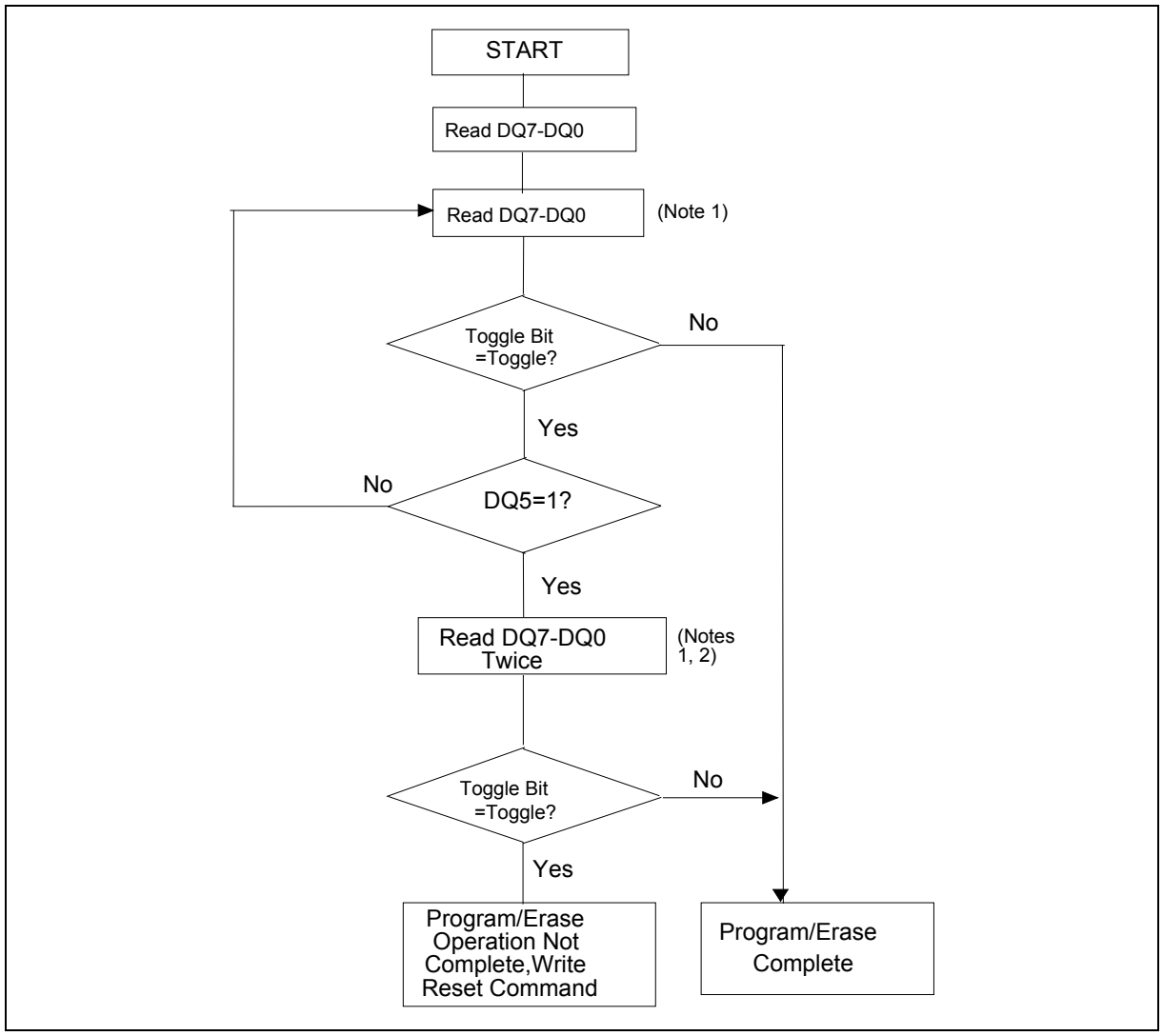
8.14 Data Polling Algorithm



Notes:

1. VA = Valid address for programming. During a sector erase operation; a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.
2. DQ7 should be rechecked even if DQ5 = “1” because DQ7 may change simultaneously with DQ5.

8.15 Toggle Bit Algorithm



Notes:

1. Read toggle bit twice to determine whether or not it is toggling.
2. Recheck toggle bit because it may stop toggling as DQ5 changes to "1."

9. ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Storage Temperature Plastic Packages	-65 to +150	°C
Ambient Temperature with Power Applied	-65 to +125	°C
Voltage with Respect to Ground , V_{DD} (Note1)	-0.5 to +4.0	V
A9, #OE, and #RESET (Note 2)	-0.5 to V_{DD} (Max.)	V
All other pins (Note 1)	-0.5 to V_{DD} +0.5	V
Output Short Circuit Current (Note 3)	200	mA

Notes:

1. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to -2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{DD} +0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{DD} +2.0 V for periods up to 20 ns.
2. Minimum DC input voltage on pins A9, #OE, and #RESET is -0.5 V. During voltage transitions, A9, #OE, and #RESET may overshoot V_{SS} to -2.0 V for periods of up to 20 ns. Maximum DC input voltage on pin A9 is V_{DD} (Max.) which may overshoot to +14.0 V for periods up to 20 ns. Maximum DC input voltage is +9.5 V which may overshoot to +12.0 V for periods up to 20 nS.
3. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

9.2 Operating Ranges

PARAMETER	RATING	UNIT
Industrial (I) Devices Ambient Temperature (TA)	-40 to +85	°C
Commercial Devices Ambient Temperature (TA)	0 to +70	°C
VDD Supply Voltages VDD for standard voltage range	2.7 to 3.6	V

Operating ranges define those limits between which the functionality of the device is guaranteed.

9.3 DC CHARACTERISTICS

PARAMETER	SYM.	TEST CONDITIONS		LIMITS			UNIT
				MIN.	TYP.	MAX.	
Input Load Current	ILI	VIN = VSS to VDD, VDD = VDD (Max.)		-	-	± 1.0	μA
A9 Input Load Current	ILIT	VDD = VDD (Max.), A9 = VID (Max.)		-	-	35	μA
Output Leakage Current	ILO	VOUT = VSS to VDD , VDD = VDD (Max.)		-	-	± 1.0	μA
VDD Active Read Current (Note 1,2)	ICC1	#CE = VIL , #OE = VIH Byte Mode	10 MHz		15	25	mA
			5 MHz	-	9	16	mA
			1 MHz		2	4	mA
		#CE = VIL , #OE = VIH Word Mode	10 MHz		18	25	mA
			5 MHz		9	16	mA
			1 MHz		2	4	mA
VDD Active Current (Note 2,3,4)	ICC2	#CE = VIL , #OE = VIH		-	20	30	mA
VDD Standby Current (Note 2,5)	ICC3	#RESET , #CE = VDD ± 0.3V		-	0.2	5	μA
VDD Reset Current (Note 2,5)	ICC4	#RESET = VSS ± 0.3V		-	0.2	5	μA
Automatic Sleep Mode Current (Note 2,4,5,6)	ICC5	VIH = VDD ± 0.3V, VIL = VSS ± 0.3V		-	0.2	5	μA
Input Low Voltage	VIL			-0.5	-	0.8	V
Input High Voltage	VIH			0.7 x VDD	-	VDD+0.3	V
Voltage for Auto-select and Temporary Sector Unprotected	VID	VDD =3.0V ± 10%		8.5	-	11.5	V
Output Low Voltage	VOL	IOL = 4.0 mA, VDD = VDD (Min.)		-	-	0.45	V
Output High Voltage	VOH1	IOL = -2.0 mA, VDD = VDD (Min.)		2.4	-	-	V
	VOH2	IOH = -100 μA, VDD = VDD (Min.)		VDD -0.4	-	-	V

Notes:

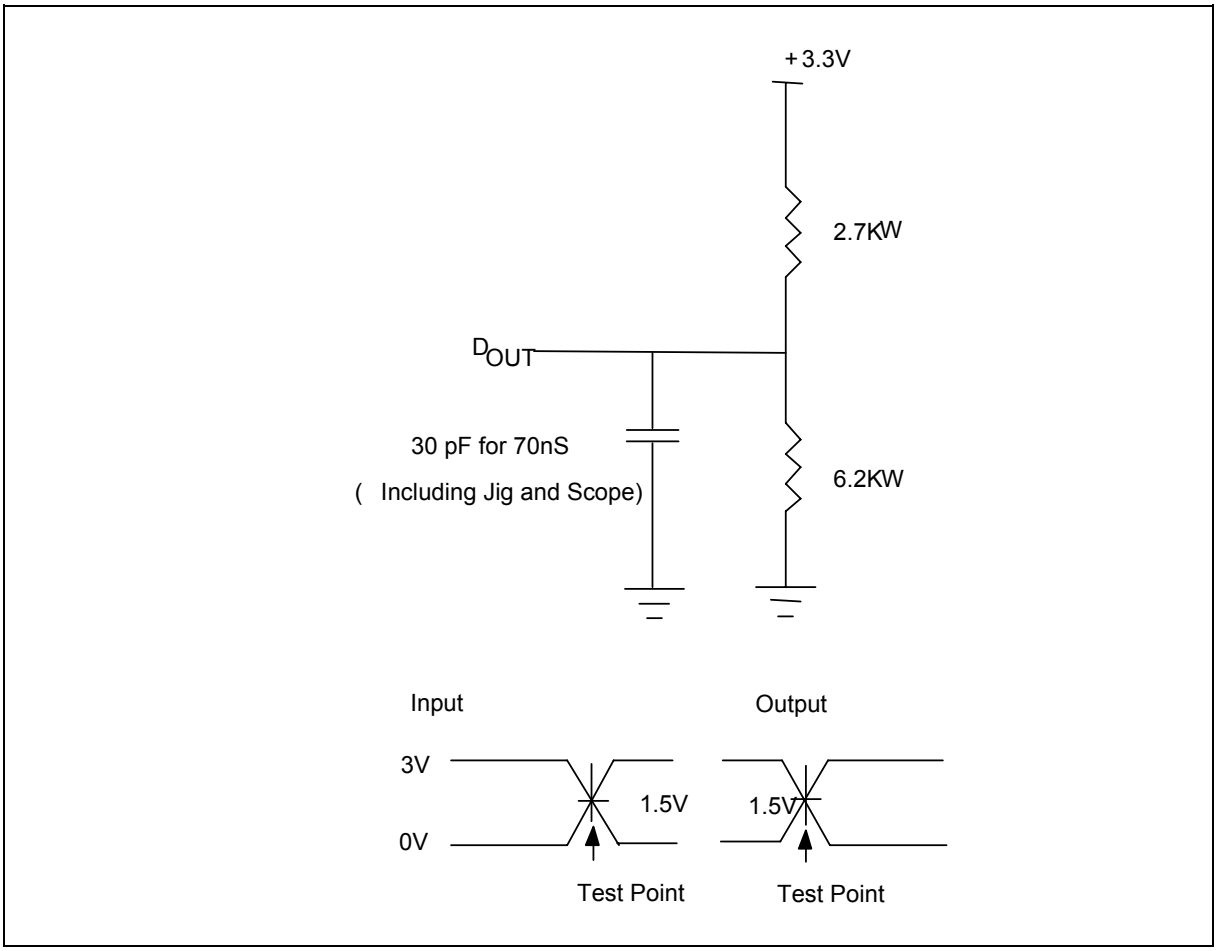
1. The I_{CC} current is typically less than 2 mA/MHz, with #OE at V_{IH}. Typical V_{DD} is 3.0V.
2. Maximum I_{CC} specifications are tested with $V_{DD} = V_{DD}$ max.
3. I_{CC} active while Embedded Erase or Embedded Program is in progress.
4. Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns. Typical sleep mode current is 200 nA.
5. For temperature >70 degree C, Vih(Max.)=Vdd+0.1V and Vil(Min)=Vss-0.1V.
6. Not 100% tested

9.4 AC CHARACTERISTICS

9.4.1 Test Condition

Test Condition	70nS	90nS	Unit
Output Load	1 TTL gate		
Output Load Capacitance, CL (including jig capacitance)	30	100	pF
Input Rise and Fall Times	5		ns
Input Pulse Levels	0 - 3.0		V
Input timing measurement reference levels	1.5		V
Output timing measurement reference levels	1.5		V

9.4.2 AC Test Load and Waveforms



9.4.3 Read-Only Operations

PARAMETER		SYM.	TEST Setup	70nS		90nS		Unit
				Min.	Max.	Min.	Max.	
Read Cycle Time		TRC		70	-	90	-	ns
Address to Output Delay		TACC	#CE = VIL, #OE = VIL	-	70	-	90	ns
Chip Enable to Output Delay		TCE	#OE = VIL	-	70	-	90	ns
Output Enable Access Time		TOE		-	30	-	35	ns
Chip Enable to Output High Z		TDF		-	25	-	30	ns
Output Enable to Output High Z		TDF		-	25	-	30	ns
Output Hold Time From Address. #OE or #CE Whichever Occurs First		TOH		0	-	0	-	ns
Output Enable Hold Time	Read	TOEH		0	-	0	-	ns
	Toggle and #Data polling			10	-	10	-	ns

Note : Not 100 % tested

9.4.4 Read-Only Operations

Test Condition	70nS	90nS	Unit
Output Load	1 TTL gate		
Output Load Capacitance, CL (including jig capacitance)	30	100	pF
Input Rise and Fall Times	5		ns
Input Pulse Levels	0 - 3.0		V
Input timing measurement reference levels	1.5		V
Output timing measurement reference levels	1.5		V

Note : Not 100 % tested

9.4.5 Hardware Reset (#RESET)

PARAMETER	SYM.	MIN.	MAX.	UNIT
#RESET PIN Low (During Embedded Algorithms) to Read or Write	T_{READY}	-	20	us
#RESET Pin Low (Not During Embedded Algorithms) to Read or Write	T_{READY}	-	500	ns
#RESET Pulse Width	T_{Rp}	500	-	ns
#RESET High Time Before Read	T_{RH}	50	-	ns
#RESET Low to Standby Mode	T_{RPD}	20	-	us
RY/#BY Recovery Time	T_{RB}	0	-	ns

Note: Not 100 % tested

9.4.6 Word/Byte Configuration (#BYTE)

Test Condition	70nS	90nS	Unit
Output Load	1 TTL gate		
Output Load Capacitance, CL (including jig capacitance)	30	100	pF
Input Rise and Fall Times	5		ns
Input Pulse Levels	0 - 3.0		V
Input timing measurement reference levels	1.5		V
Output timing measurement reference levels	1.5		V

9.4.7 Erase and Program Operation

PARAMETER		SYM.	70nS			90nS			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Write Cycle Timing		T_{WC}	70	-	-	90	-	-	ns
Address setup Time		T_{AS}	0	-	-	0	-	-	ns
Address Hold Time		T_{AH}	45	-	-	45	-	-	ns
Data Setup Time		T_{DS}	35	-	-	45	-	-	ns
Data Hold Time		T_{DH}	0	-	-	0	-	-	ns
Output Enable Setup Time		T_{OES}	0	-	-	0	-	-	ns
Read Recovery Time Before Write (#OE High to #WE Low)		T_{GHWL}	0	-	-	0	-	-	ns
#CE Setup Time		T_{CS}	0	-	-	0	-	-	ns
#CE HOLD Time		T_{CH}	0	-	-	0	-	-	ns
Write Pulse Width		T_{WP}	35	-	-	35	-	-	ns
Write Pulse Width High		T_{WPH}	30	-	-	30	-	-	ns
Programming Time	Byte	T_{PB}	-	5	150	-	5	150	us
	Word	T_{PW}	-	7	210	-	7	210	us
Sector Erase Time		T_{SE}	-	0.7	10	-	0.7	10	sec
VDD Setup Time (Note 1)		T_{VCS}	50	-	-	50	-	-	us
Write Recovery Time from RY/#BY		T_{RB}	0	-	-	0	-	-	ns
Program/Erase Valid to RY/#BY Delay		T_{BUSY}	30	-	90	-	-	90	ns

Notes: Not 100 % tested

9.4.8 Temporary Sector Unprotect

PARAMETER	SYM.	MIN.	MAX.	UNIT
VID Rise and Fall Time (See Note)	T_{VIDR}	500	-	ns
#RESET setup Time for Temporary Sector Unprotect	T_{RSP}	4	-	us
#RESET Hold Time from RY/#BY High for Temporary Sector Unprotect	T_{RRB}	4	-	s

Note: Not 100 % tested

9.4.9 Alternate #CE Controlled Erase and Program Operation

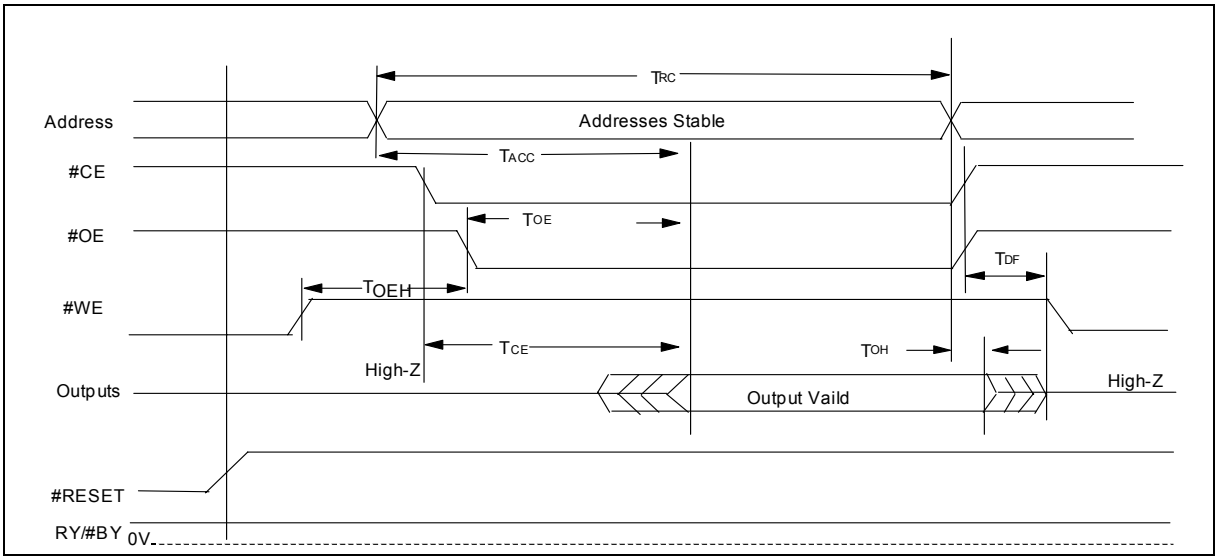
PARAMETER		SYM.	70nS			90nS			Unit
			Min	Typ (Note 3)	Max (Note 4)	Min	Typ (Note 3)	Max (Note 4)	
Write Cycle Time (Note 1)		T_{WC}	70	-	-	90	-	-	ns
Address Setup Time		T_{AS}	0	-	-	0	-	-	ns
Address Hold Time		T_{AH}	45	-	-	45	-	-	ns
Data Setup Time		T_{DS}	35	-	-	45	-	-	ns
Data Hold Time		T_{DH}	0	-	-	0	-	-	ns
Output Enable Setup Time		T_{OES}	0	-	-	0	-	-	ns
Read Recover Time Before Write (#OE High to #WE Low)		T_{GHEL}	0	-	-	0	-	-	ns
#WE Setup Time		T_{WS}	0	-	-	0	-	-	ns
#WE Hold Time		T_{WH}	0	-	-	0	-	-	ns
#CE Pulse Width		T_{CP}	35	-	-	35	-	-	ns
#CE Pulse Width High		T_{CPH}	30	-	-	30	-	-	ns
Programming Time (Note 6)	Byte	T_{PB}	-	5	-	-	5	-	us
	Word	T_{PW}	-	7	-	-	7	-	
Sector Erase Time (Note 2)		T_{SE}	-	0.7	-	-	0.7	-	sec
Chip Erase Time (Note 2)		T_{CE}	-	25	-	-	25	-	sec
Chip Program Time (Note 5)	Byte	T_{CPB}	-	11	-	-	11	-	sec
	Word	T_{CPW}	-	7.2	-	-	7.2	-	

Notes :

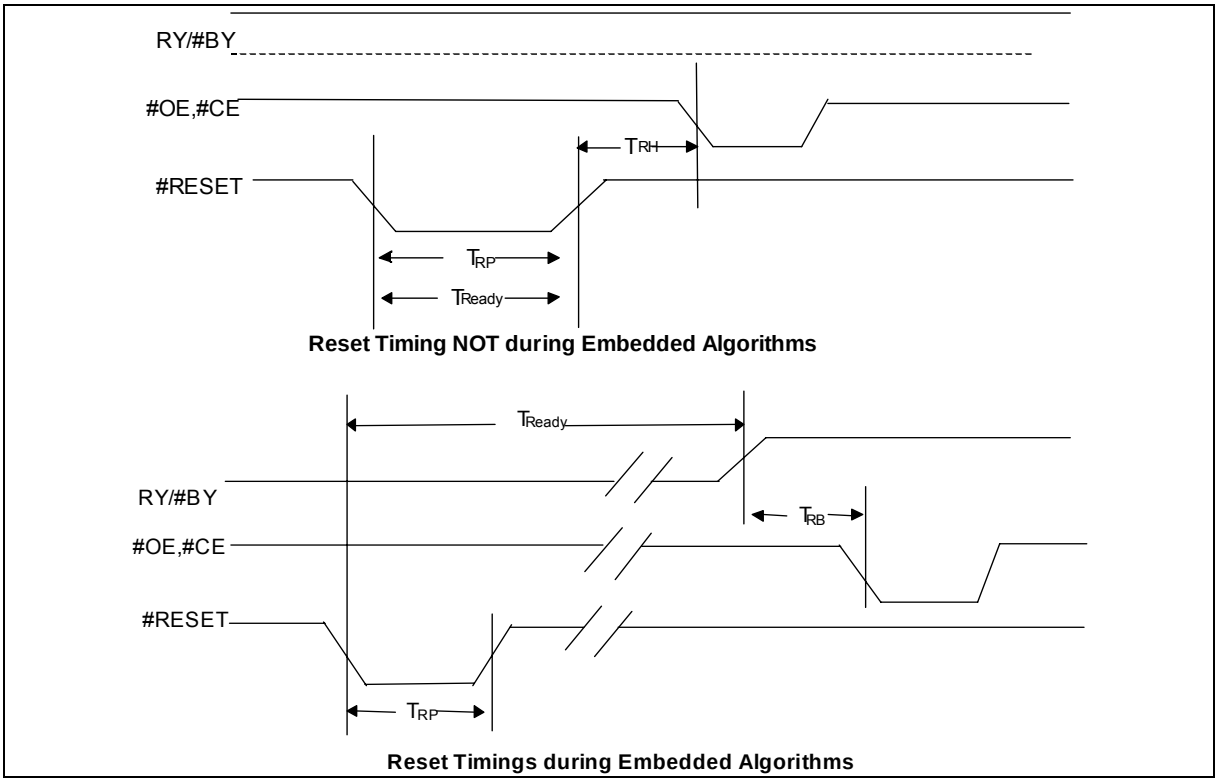
1. Not 100 % tested.
2. In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.
3. Typical program and erase time assume the following conditions :25℃,3.0 V V_{DD}, 10,000 cycles .Additionally, programming typicals assume checkerboard pattern.
4. Under worst case conditions of 90℃, V_{DD} =2.7V, 10,000 cycles.
5. The typical chip programming time is considerably less than the maximun chip programming time listed,since most bytes program faster than maximun program times listed.
6. System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command.
7. The device has a minimum erase and program cycle endurance of 10,000 cycles.

10. TIMING WAVEFORMS

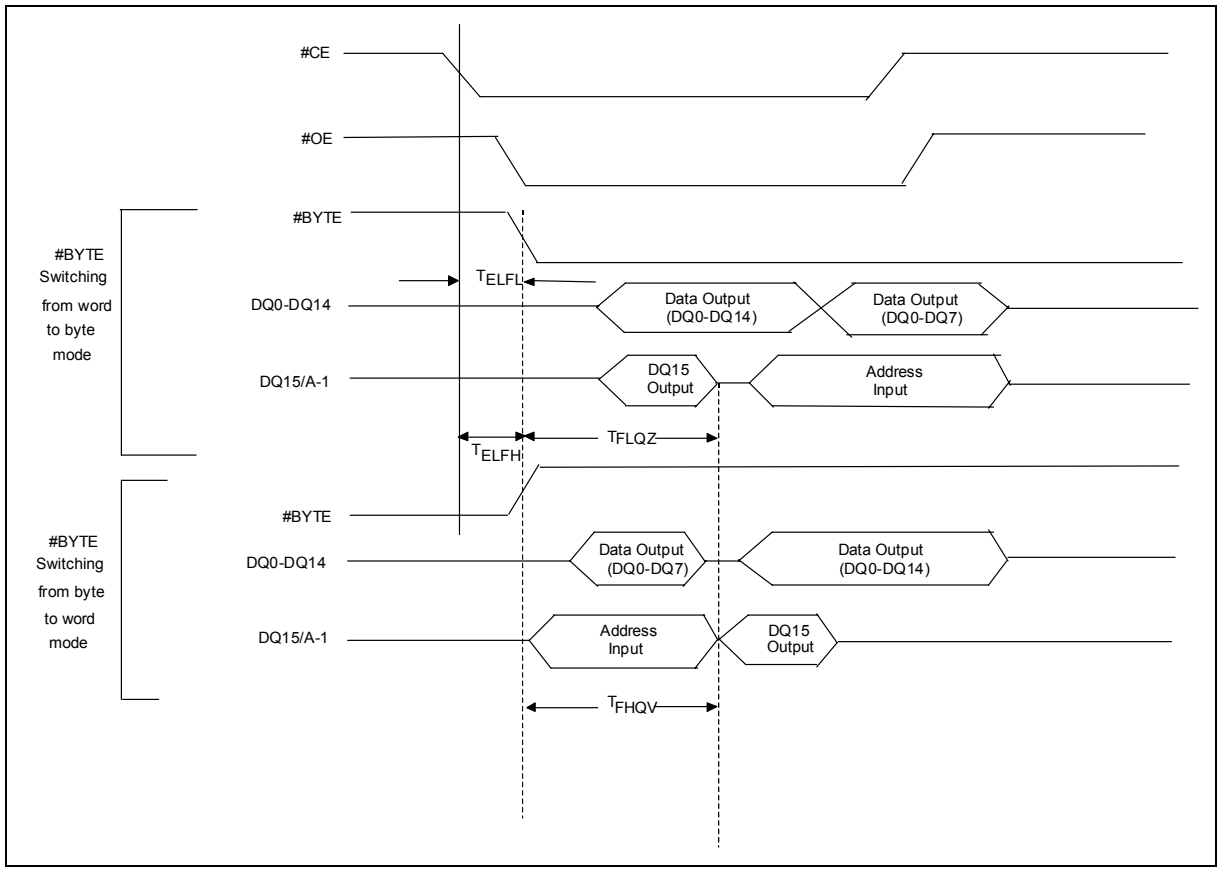
10.1 AC Read Waveform



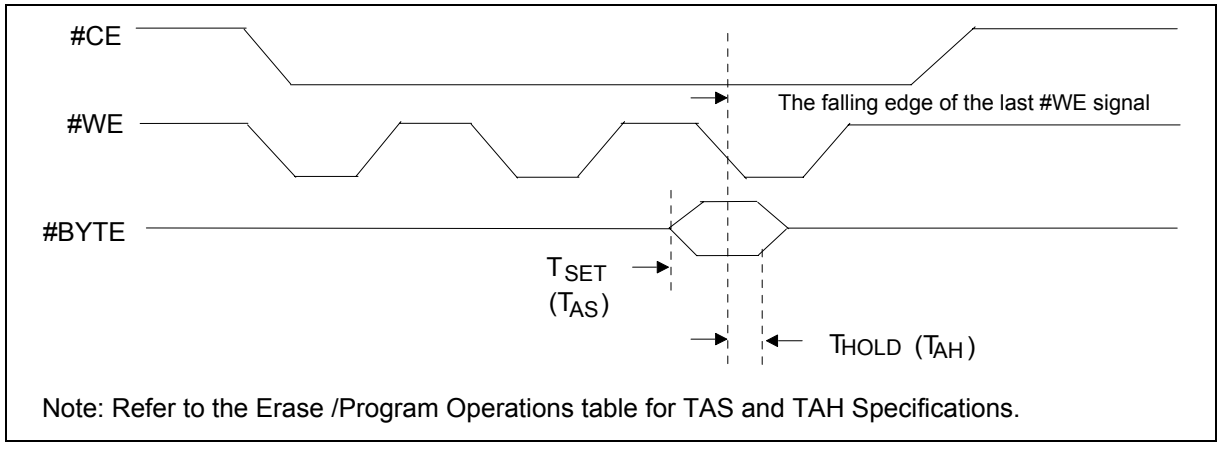
10.2 Reset Waveform



10.3 #BYTE Waveform for Read Operation

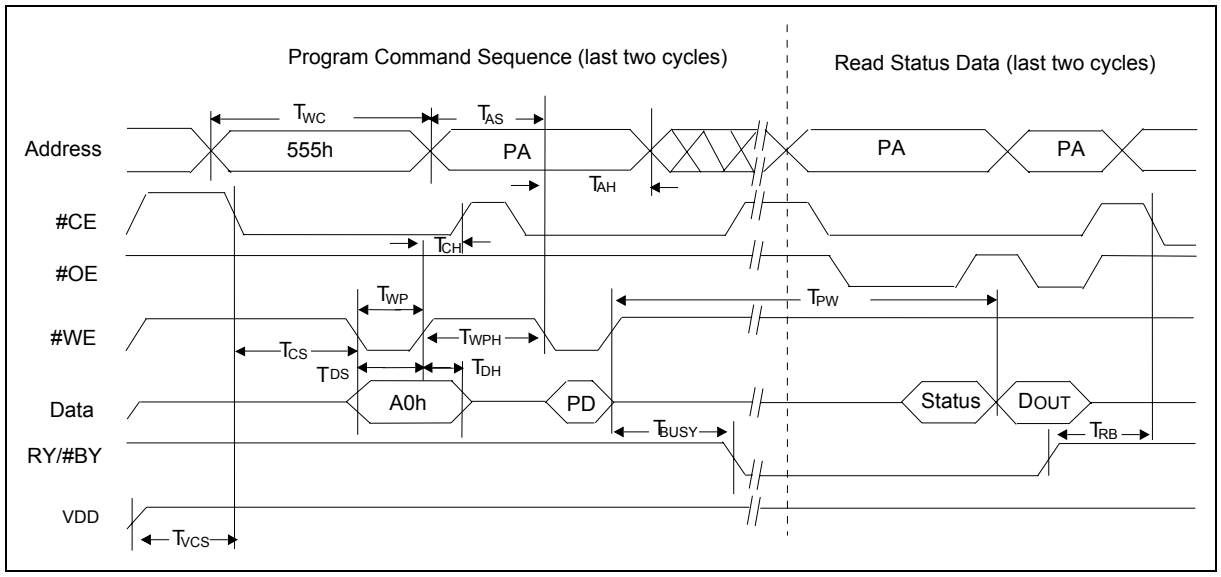


10.4 #BYTE Waveform for Write Operation



Note: Refer to the Erase /Program Operations table for TAS and TAH Specifications.

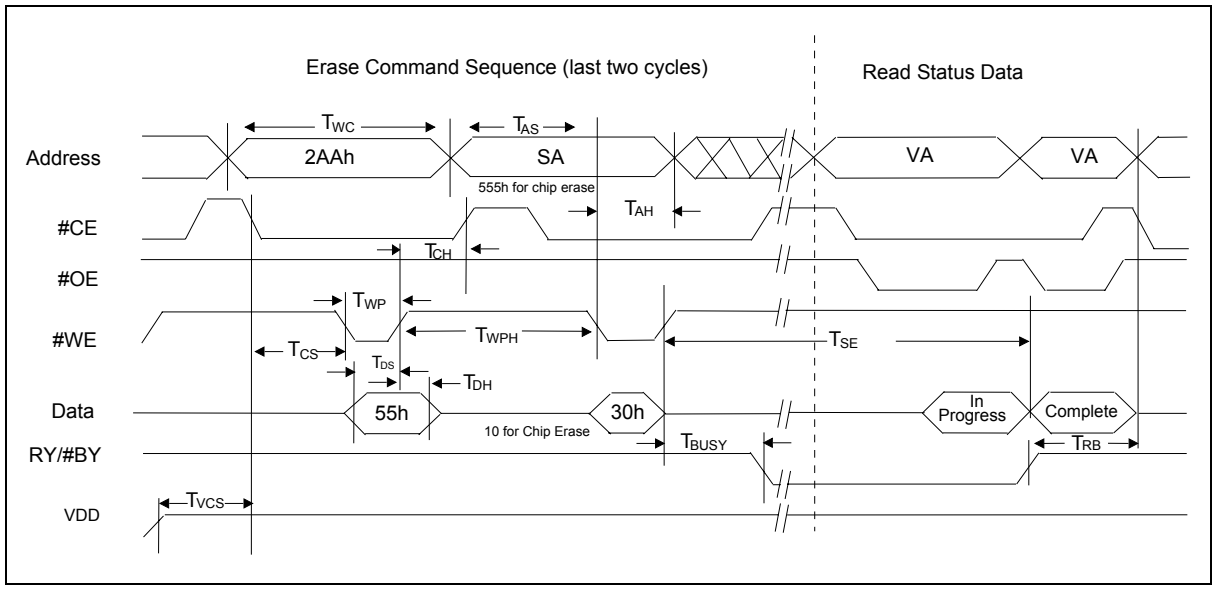
10.5 Programming Waveform



Notes :

1. PA=program address ,PD=program data,DOUT is the true data at the program address
2. Illustration shows device in word mode

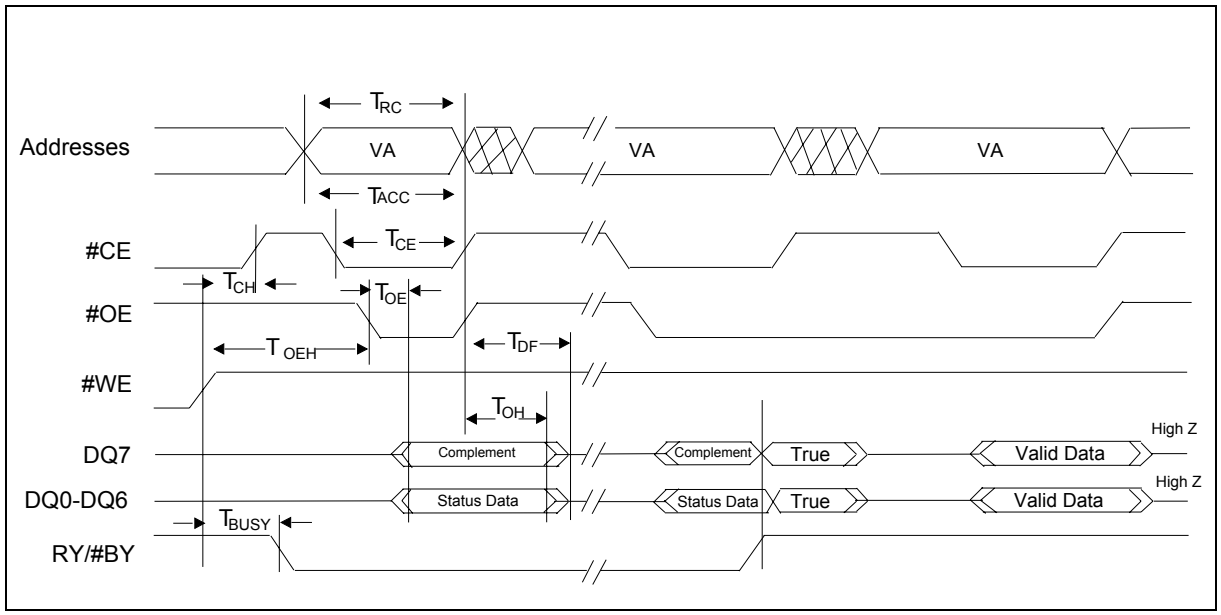
10.6 Chip/Sector Erase Waveform



Notes :

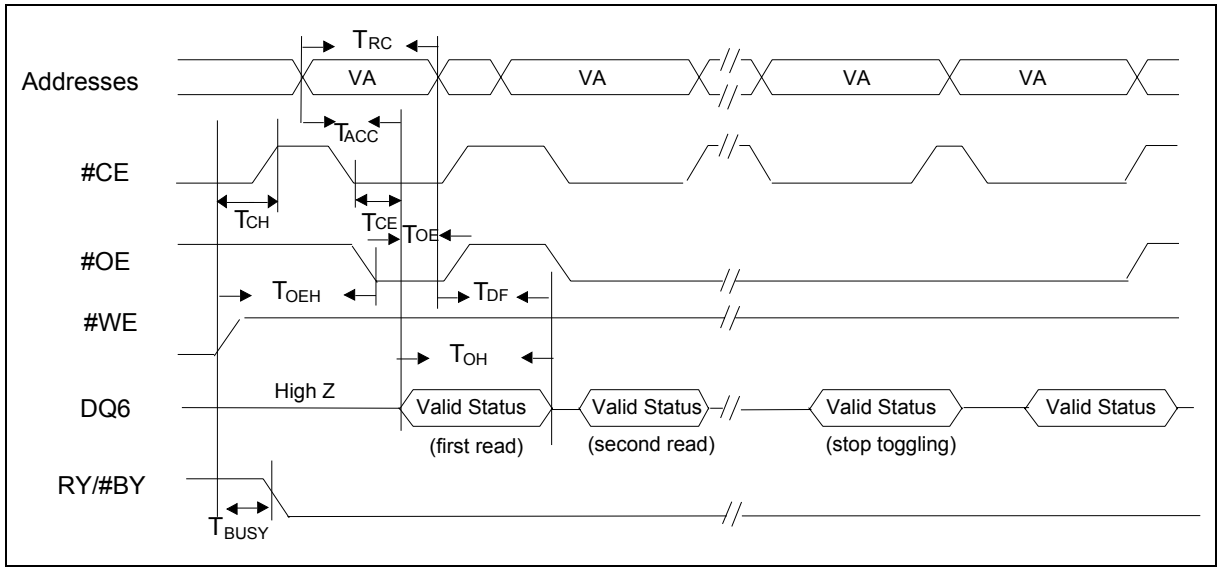
1. SA= sector address (for Sector Erase), VA= Valid Address for reading status data (see “Write operation Status”).
2. These waveforms are for the word mode

10.7 #Data Polling Waveform (During Embedded Algorithms)



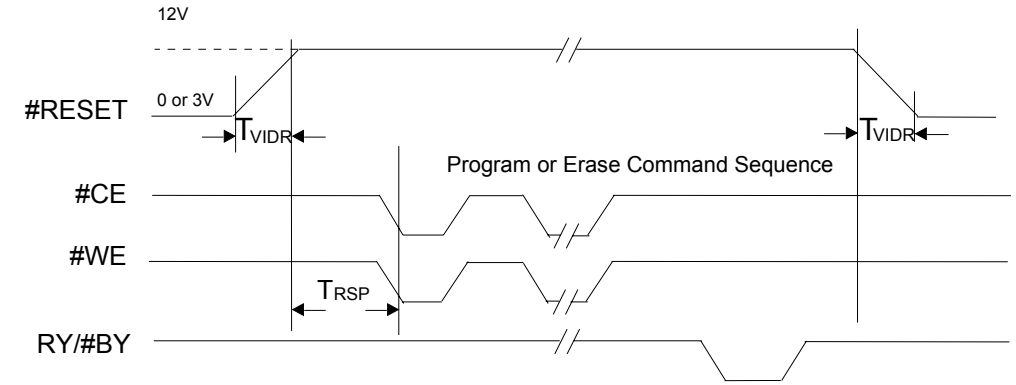
Note : VA= Valid Address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.

10.8 Toggle Bit Waveform (During Embedded Algorithms)

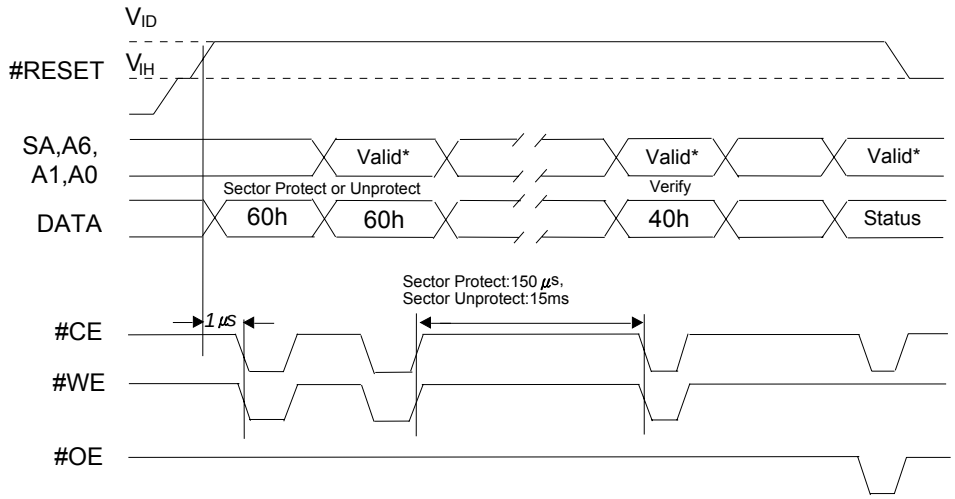


Note : VA= Valid address;not requires for DQ6. Illustration shows status cycle after command sequence, last status read cycle, and array data read cycle.

10.9 Temporary Sector Unprotect Timing Diagram

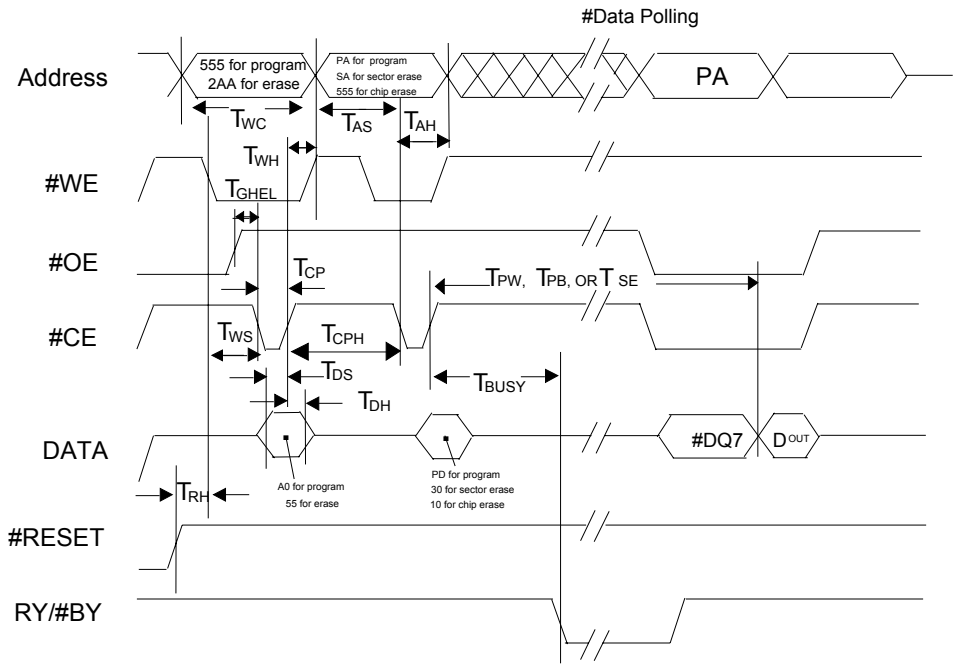


10.10 Sector Protect and Unprotect Timing Diagram



Note: For sector protect, A6=0, A1=1, A0=0.
For sector unprotect, A6=1, A1=1, A0=0.

10.11 Alternate #CE Controlled Write (Erase/Program) Operation Timing



Notes :

1. Firgure indicates last two bus cycles of a program or erase operation.
2. PA= program address, SA= sector address, PD= program data.
3. #DQ7 is the complement of the data written to the device. DOUT is the data written to the device.
4. Waveforms are for the word mode.

11. LATCHUP CHARACTERISTICS

PARAMETER	MIN	MAX
Input voltage with respect to Vss on all pins except I/O pins (including A9, #OE, and #RESET)	-1.0 V	11.5 V
Input voltage with respect to Vss on all I/O pins	-1.0 V	V_{DD} +1.0 V
V_{DD} Current	-100 mA	+100 mA

Note : Includes all pins except VDD. Test conditions: VDD = 3.0 V, one pin at a time.

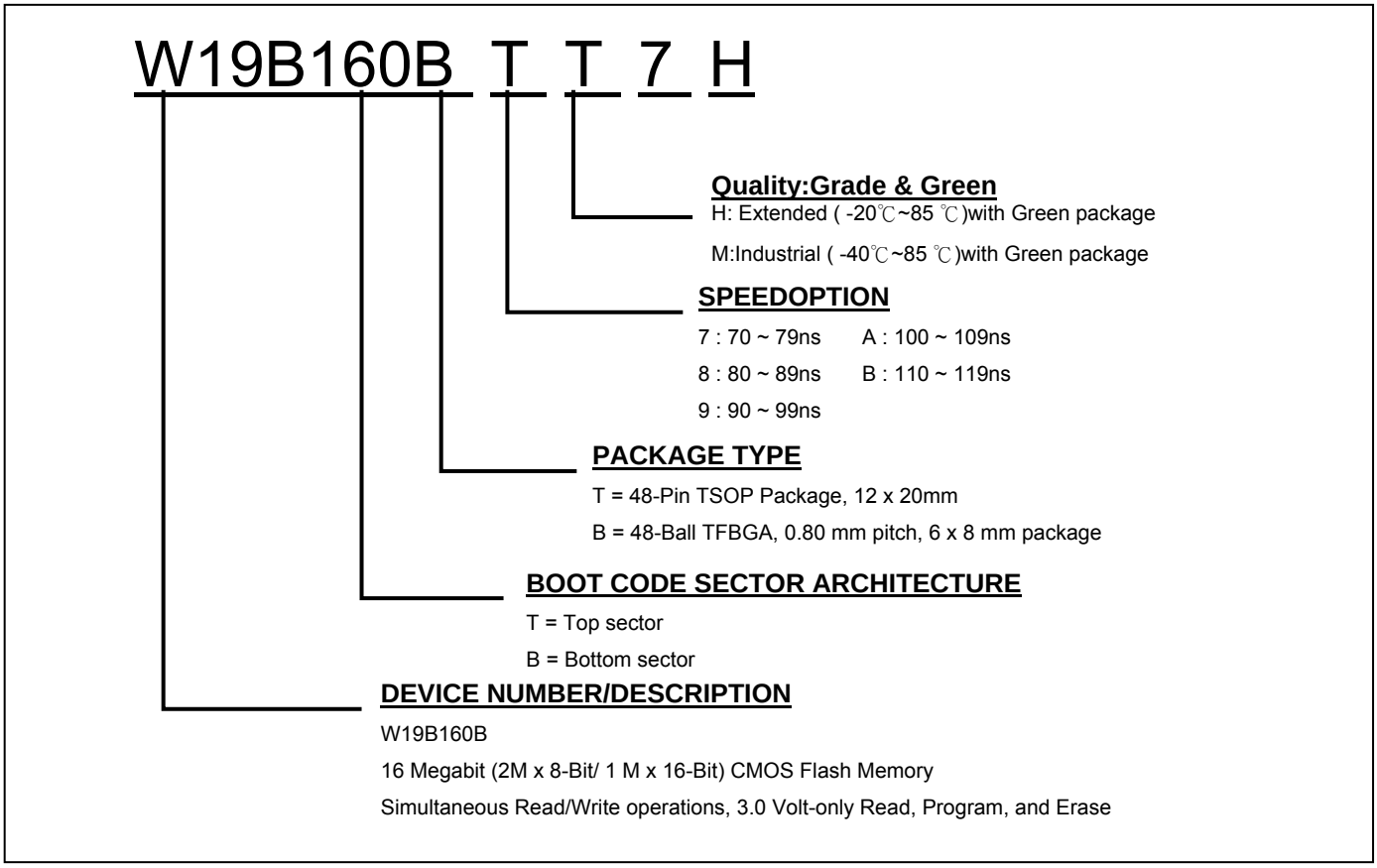
12. CAPACITANCE

PARAMETER	SYM.	TEST SETUP	TYP	MAX	UNIT
Input Capacitance	V_{IN}	V_{IN} = 0	6	7.5	pF
Output Capacitance	V_{OUT}	V_{OUT} = 0	8.5	12	pF
Control Pin Capacitance	V_{IN2}	V_{IN} = 0	7.5	9	pF

Notes :

1. Sampled, not 100 % tested.
2. Test condition TA = 25℃, f = 1.0 MHz.

13. ORDERING INFORMATION

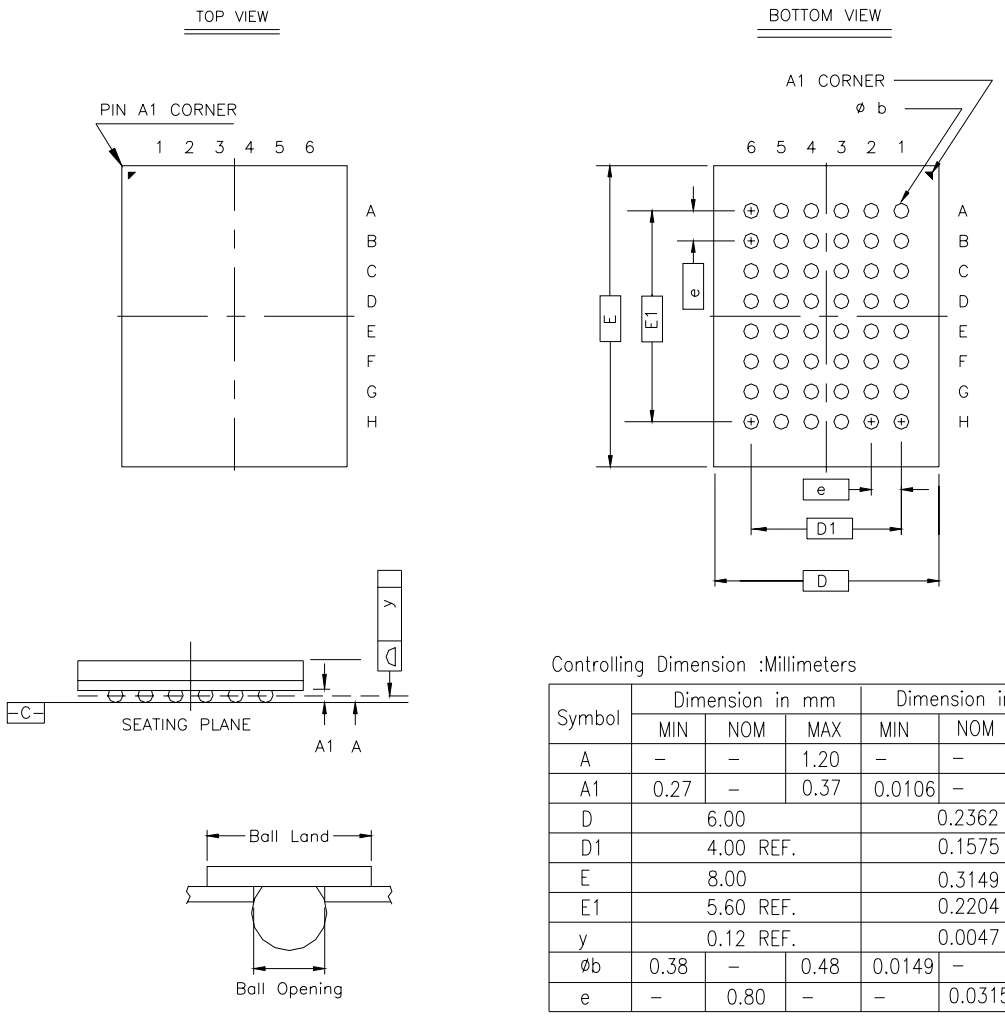


Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

14. PACKAGE DIMENSIONS

TFBGA48ball (6X8 mm^2, Ø=0.40mm)

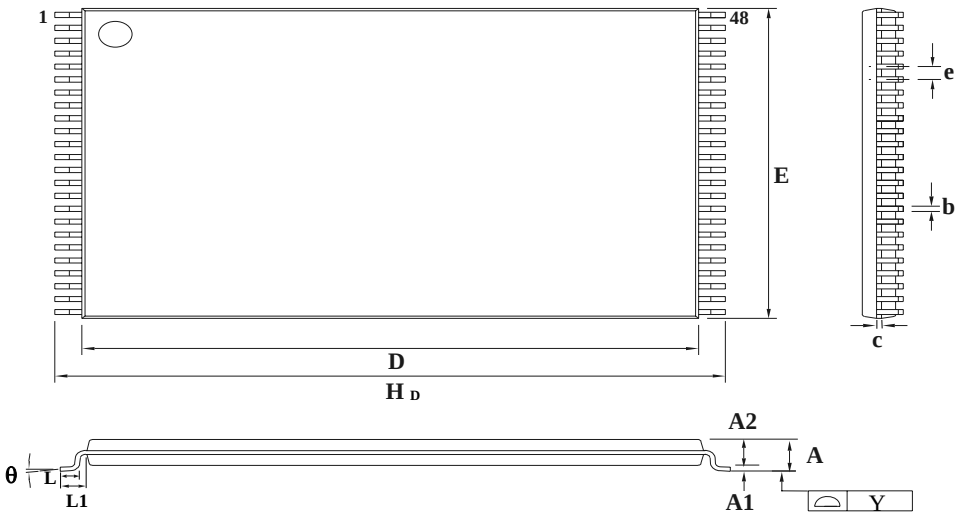


Controlling Dimension :Millimeters

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	–	–	1.20	–	–	0.0472
A1	0.27	–	0.37	0.0106	–	0.0146
D	6.00			0.2362		
D1	4.00 REF.			0.1575 REF.		
E	8.00			0.3149		
E1	5.60 REF.			0.2204 REF.		
y	0.12 REF.			0.0047 REF.		
øb	0.38	–	0.48	0.0149	–	0.0188
e	–	0.80	–	–	0.0315	–

Note: Ball Land: 0.50mm / Ball opening: 0.35mm

48-Pin Standard Thin Small Outline Package (measured in millimeters)



Symbol	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	——	——	1.20	——	——	0.047
A1	0.05	——	——	0.002	——	——
A2	0.95	1.00	1.05	0.037	0.039	0.041
D	18.3	18.4	18.5	0.720	0.724	0.728
H D	19.8	20.0	20.2	0.780	0.787	0.795
E	11.9	12.0	12.1	0.468	0.472	0.476
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.10	——	0.21	0.004	——	0.008
e	——	0.50	——	——	0.020	——
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	——	0.80	——	——	0.031	——
Y	——	——	0.10	——	——	0.004
θ	0	——	5	0	——	5

15. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	April/12/2007	ALL	Initial Issued
A2	July/17/2007	ALL	48-Pin Standard Thin Small Outline Package/VID Spec to 11.5volt
A3	Oct./01/2007	34-38	1. Reduced T_{BUSY} form 90nS to 30nS 2. Reduced I_{CC1} form 30/35mA to 25mA 3. Removed max of T_{CPB}/ T_{CPW} 4. Removed max of T_{PW}
A4	Oct./17/2007	26,46	Updated frame setting and package material as Green
A5	Jan./04/2008	32,36-41	Added note of ICC3-5, 90nS/Read only spec, and max. of t_{PW}/t_{PB}

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Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.