Fast Logic

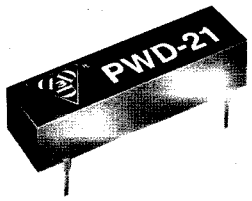
Pulse Width Discriminator

SERIES: PWD-21
TTL Interfaced

data delay devices, inc.

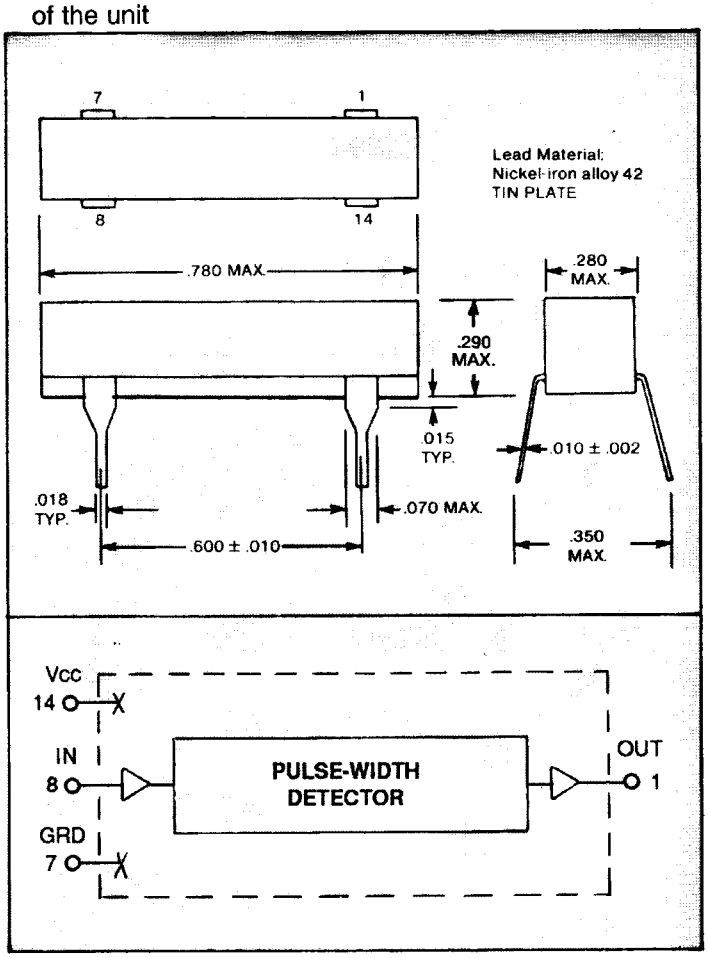
Features:

- **Auto-Insertable.**
- **Completely Interfaced with TTL and DTL application.**
- **No external components required.**
- **P.C. board space economy achieved.**
- **Fits standard 14 pins DIP socket.**



Specifications:

- **Pulse-width tolerance:** ±5% or better 2 ns whichever is greater.
- **Rise-time:** 2 ns typically.
- **Temperatrure coefficient:** 100 PPM/°C.
- **Temperature range:** 0°C to 70° C standard.
- **Minimum pulse rep. rate** = 2.5 x pulse-width of the unit
- **Supply voltage:** 4.75 to 5.25 Vdc.
- **Supply current:**
  I_{CCL}: 32 ma.
  I_{CCH}: 7 ma.
- **DC Parameters:** See TTL-Fast Schottky Logic Table on Page 6.



Part No.	Pulse Widths (ns)		
	Nominal	Suppress	Pass
PWD-21-5	5	≤4	≥6
PWD-21-10	10	≤9	≥11
PWD-21-15	15	≤14	≥16
PWD-21-20	20	≤19	≥21
PWD-21-25	25	≤24	≥26
PWD-21-30	30	≤29	≥31
PWD-21-35	35	≤34	≥36
PWD-21-40	40	≤39	≥41
PWD-21-45	45	≤43.5	≥46.5
PWD-21-50	50	≤48.5	≥51.5
PWD-21-60	60	≤58	≥62
PWD-21-70	70	≤68	≥72
PWD-21-75	75	≤73	≥77
PWD-21-80	80	≤78	≥82
PWD-21-90	90	≤88	≥92
PWD-21-100	100	≤98	≥102
PWD-21-125	125	≤123	≥127
PWD-21-150	150	≤147	≥153
PWD-21-175	175	≤172	≥178
PWD-21-200	200	≤196	≥204
PWD-21-250	250	≤245	≥255
PWD-21-300	300	≤294	≥306
PWD-21-400	400	≤392	≥408
PWD-21-500	500	≤490	≥510

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