

Notice: This is not a final specification.  
Some parametric limits are subject to change.

## M6MGE13VW34DWG-P

**134,217,728-BIT (8,388,608-WORD BY 16-BIT) CMOS FLASH MEMORY &  
33,554,432-BIT (2,097,152-WORD BY 16-BIT) CMOS MOBILE RAM**  
Stacked-CSP ( Chip Scale Package)

### Description

The M6MGE13VW34DWG-P is a Stacked Chip Scale Package (S-CSP) that contains 128M-bit Flash memory and 32M-bit Mobile RAM in a 72-pin Stacked CSP with leaded solder ball.

128M-bit Flash memory is a 8,388,608 words, single power supply and high performance non-volatile memory fabricated by CMOS technology for the peripheral circuit and DINOR IV (Divided bit-line NOR IV) architecture for the memory cell. All memory blocks are locked and can not be programmed or erased, when F-WP# is Low. Using Software Lock Release function, program or erase operation can be executed.

32M-bit Mobile RAM is a 2,097,152 words high density RAM fabricated by CMOS technology for the peripheral circuit and DRAM cell for the memory array. The interface is compatible to an asynchronous SRAM.

The cells are automatically refreshed and the refresh control is not required for system. The device also has the partial block refresh scheme and the power down mode by writing the command.

The M6MGE13VW34DWG-P is suitable for a high performance cellular phone and a mobile PC that are required to be small mounting area, weight and small power dissipation.

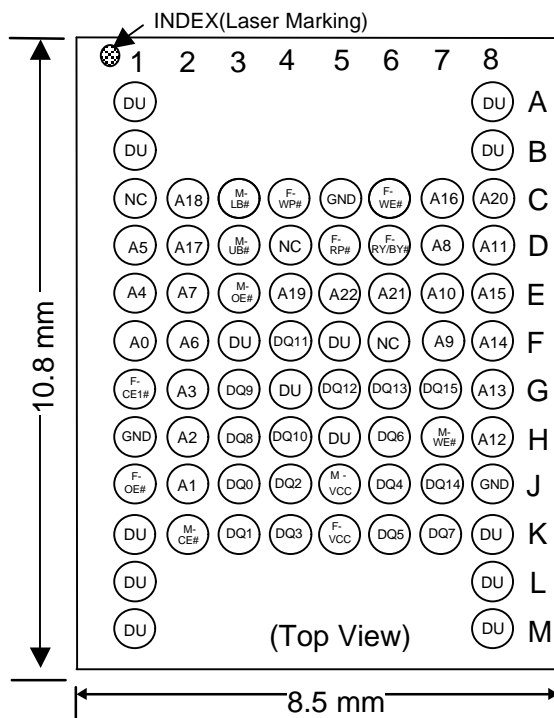
### Features

Access Time	Random Access/ Page Access
	Flash 70ns (Max.)
	Mobile RAM 80ns (Max.)
Supply Voltage	F-VCC=2.7 ~ 3.0V
	M-VCC=2.7 ~ 3.0V
Ambient Temperature	Ta= -40 ~ 85 degree
Package	72pin S-CSP, Ball pitch 0.80mm Outer-ball:Sn - Pb

### Application

Mobile communication products

### PIN CONFIGURATION (TOP VIEW)



F-VCC : VCC for Flash  
M-VCC : VCC for Mobile RAM  
GND : GND for Flash / Mobile RAM  
A0-A20 : Common address for Flash/Mobile RAM  
A21/A22 : Address for Flash  
DQ0-DQ15 : Data I/O  
F-CE1# : Flash chip enable  
F-OE# : Output enable for Flash Memory  
F-WE# : Write enable for Flash Memory

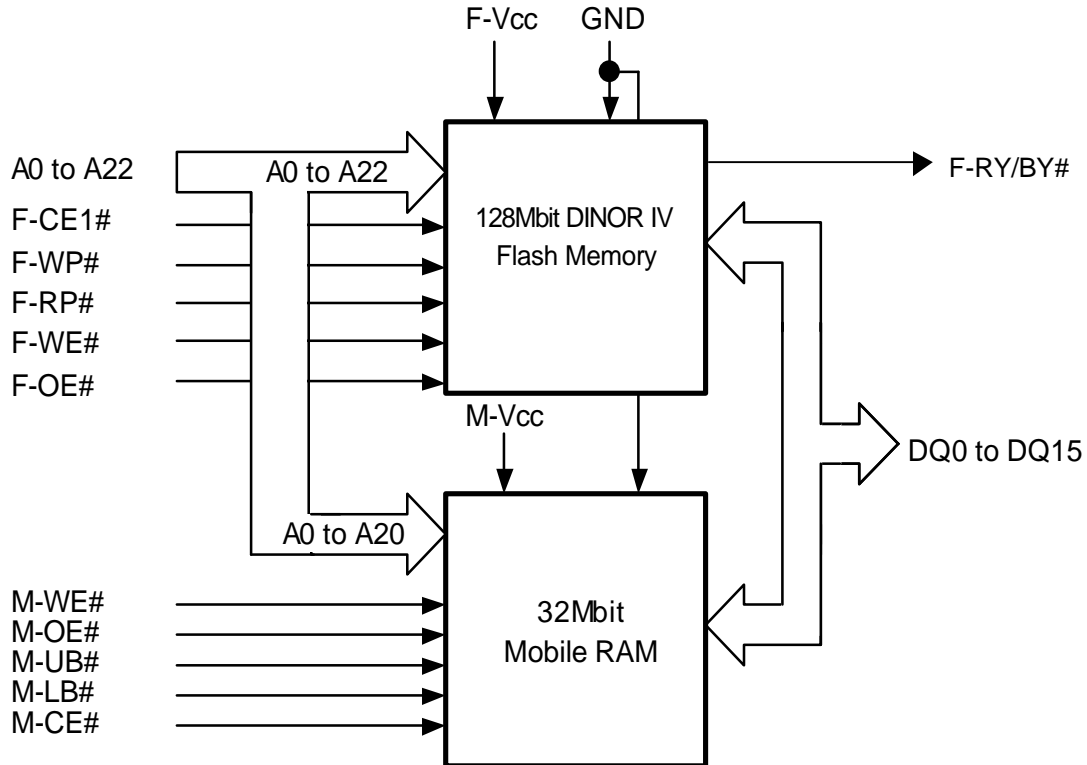
F-RP# : Reset power down for Flash  
F-WP# : Write protect for Flash  
F-RY/BY# : Flash Memory Ready /Busy  
M-CE# : Mobile RAM chip enable  
M-OE# : Output enable for Mobile RAM  
M-WE# : Write enable for Mobile RAM  
M-LB# : Lower byte control for Mobile RAM  
M-UB# : Upper byte control for Mobile RAM  
NC : Non Connection  
DU : Don't Use

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### MCP Block Diagram



Note: In the Flash Memory part they mean OE# and WE# are F-OE# and F-WE#.  
In the Mobile RAM part UB# , LB# , OE# and WE# are M-UB# , M-LB# , M-OE# and M-WE# , respectively.

### Capacitance

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
CIN	Input capacitance A21-A0, F-OE#, F-WE#, F-CE1#, F-CE2#, F-WP#, F-RP#, M-OE#, M-WE#, M-CE#, M-LB#, M-UB#	Ta=25°C, f=1MHz, Vin=Vout=0V			26	pF
COUT	Output Capacitance DQ15-DQ0, F-RY/BY#				34	pF

# Preliminary

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