HD404618 Series

4-Bit Single-Chip Microcomputer

HITACHI

Rev. 6.0
Sept. 1998

Description

The HD404618 Series is designed with the powerful and efficient architecture of the HMCS400 family. The MCU incorporates a high-precision dual-tone multifrequency (DTMF) circuit, LCD driver/controller, voltage comparator, and 32-kHz watch oscillator circuit.

The HD404618 Series includes five chips: the HD404612 with 2-kword ROM; the HD404614 with 4-kword ROM; the HD404616 with 6-kword ROM; the HD404618 with 8-kword ROM; the HD4074618 with 8-kword PROM.

The HD4074618, incorporating PROM, is a ZTAT™ microcomputer that can dramatically shorten system development periods and smooth the process from debugging to mass production.

ZTAT™ : Zero Turn Around time ZTAT is a trademark of Hitachi Ltd.

Features

- 2048-word × 10-bit ROM (HD404612)
- 4096-word × 10-bit ROM (HD404614)
- 6144-word × 10-bit ROM (HD404616)
- 8192-word × 10-bit ROM (HD404618, HD4074618)
- 1184-digit × 4-bit RAM
- 30 I/O pins
  - 10 high-current output pins
  - CMOS I/O pin circuit configuration
  - Input/output pull-up MOS can be selected by software
- On-chip DTMF generator
- LCD controller/driver (32 segments × 4 commons)
- Three timer/counters
- Clock-synchronous 8-bit serial interface
- Six interrupt sources
  - Two by external sources
  - Four by internal sources

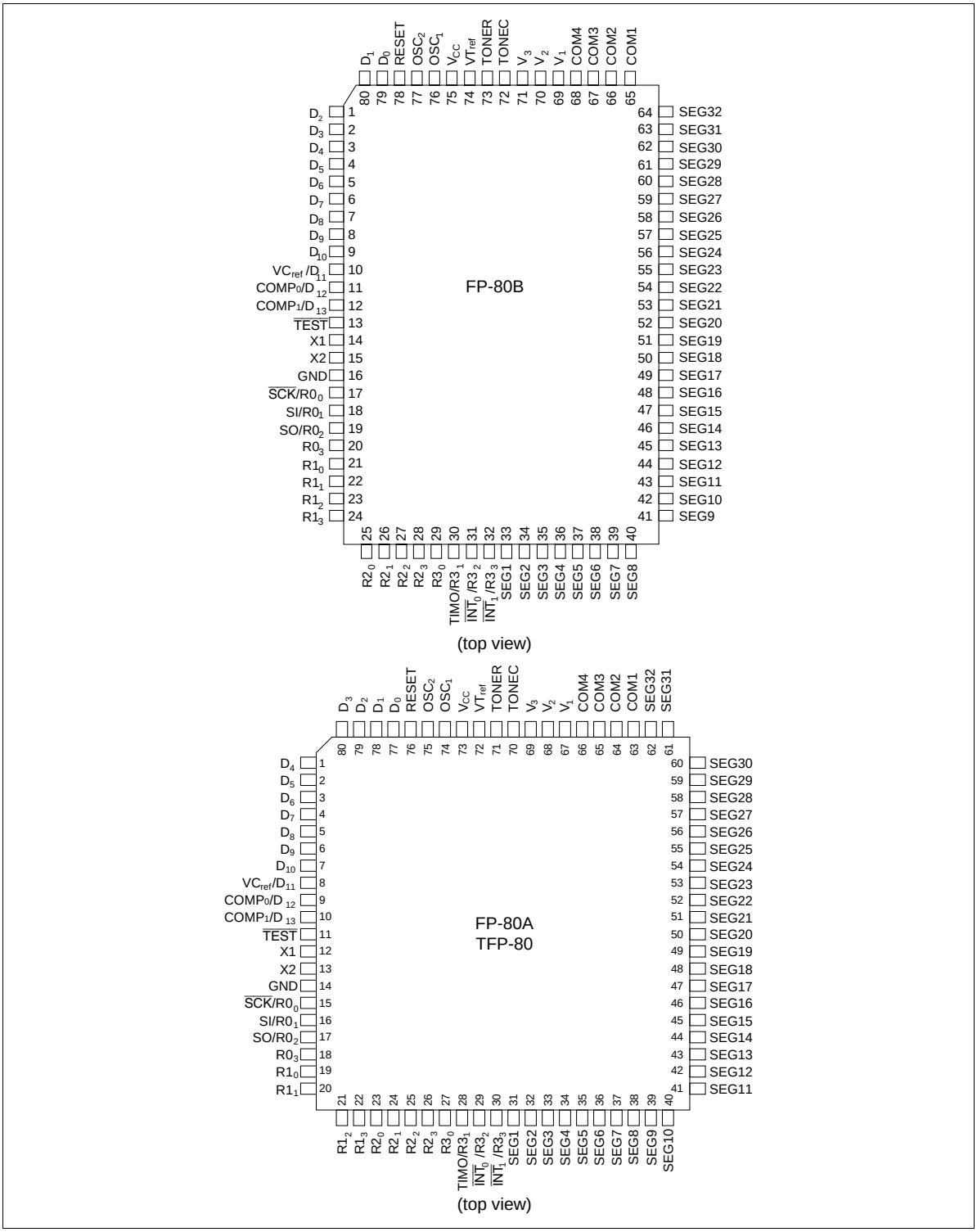
Hitachi semiconductor

- Subroutine stack up to 16 levels, including interrupts
- Instruction cycle time
  - 10 µs (f_{OSC} = 400 kHz)
  - 5 µs (f_{OSC} = 800 kHz)
- Four low-power dissipation modes
  - Stop mode
  - Standby mode
  - Watch mode
  - Subactive mode
- Built-in oscillator
  - Crystal or ceramic oscillator (an external clock also possible)
- Voltage comparator (2 channels)
- Two operating modes
  - MCU mode
  - PROM mode (HD4074618)
- Package
  - 80-pin plastic flat package (FP-80B) (FP-80A)
  - 80-pin plastic thin flat package (TFP-80)

Ordering Information

Type	Product Name	Model Name	ROM (Word)	Package
Mask ROM	HD404612	HD404612FS	2,048	FP-80B
		HD404612H		FP-80A
		HD404612TF		TFP-80
	HD404614	HD404614FS	4,096	FP-80B
		HD404614H		FP-80A
		HD404614TF		TFP-80
	HD404616	HD404616FS	6,144	FP-80B
		HD404616H		FP-80A
		HD404616TF		TFP-80
	HD404618	HD404618FS	8,192	FP-80B
		HD404618H		FP-80A
		HD404618TF		TFP-80
ZTAT™	HD4074618	HD4074618FS	8,192	FP-80B
		HD4074618H		FP-80A
		HD4074618TF		TFP-80

Pin Arrangement



Pin Description

Pin Number				Pin Number			
FP-80B	FP-80A, TFP-80	Pin Name	I/O	FP-80B	FP-80A, TFP-80	Pin Name	I/O
1	79	D_2	I/O	33	31	SEG1	O
2	80	D_3	I/O	34	32	SEG2	O
3	1	D_4	I/O	35	33	SEG3	O
4	2	D_5	I/O	36	34	SEG4	O
5	3	D_6	I/O	37	35	SEG5	O
6	4	D_7	I/O	38	36	SEG6	O
7	5	D_8	I/O	39	37	SEG7	O
8	6	D_9	I/O	40	38	SEG8	O
9	7	D_{10}	I	41	39	SEG9	O
10	8	D_{11}/VC_{ref}	I	42	40	SEG10	O
11	9	$D_{12}/COMP_0$	I	43	41	SEG11	O
12	10	$D_{13}/COMP_1$	I	44	42	SEG12	O
13	11	$\overline{TEST}$	I	45	43	SEG13	O
14	12	X1	I	46	44	SEG14	O
15	13	X2	O	47	45	SEG15	O
16	14	GND		48	46	SEG16	O
17	15	$R0_0/\overline{SCK}$	I/O	49	47	SEG17	O
18	16	$R0_1$/SI	I/O	50	48	SEG18	O
19	17	$R0_2$/SO	I/O	51	49	SEG19	O
20	18	$R0_3$	I/O	52	50	SEG20	O
21	19	$R1_0$	I/O	53	51	SEG21	O
22	20	$R1_1$	I/O	54	52	SEG22	O
23	21	$R1_2$	I/O	55	53	SEG23	O
24	22	$R1_3$	I/O	56	54	SEG24	O
25	23	$R2_0$	I/O	57	55	SEG25	O
26	24	$R2_1$	I/O	58	56	SEG26	O
27	25	$R2_2$	I/O	59	57	SEG27	O
28	26	$R2_3$	I/O	60	58	SEG28	O
29	27	$R3_0$	I/O	61	59	SEG29	O
30	28	$R3_1$/TIMO	I/O	62	60	SEG30	O
31	29	$R3_2/\overline{INT_0}$	I/O	63	61	SEG31	O
32	30	$R3_3/\overline{INT_1}$	I/O	64	62	SEG32	O

Pin Number				Pin Number			
FP-80B	FP-80A, TFP-80	Pin Name	I/O	FP-80B	FP-80A, TFP-80	Pin Name	I/O
65	63	COM1	O	73	71	TONER	O
66	64	COM2	O	74	72	VT_{ref}	
67	65	COM3	O	75	73	V_{CC}	
68	66	COM4	O	76	74	OSC_1	I
69	67	V_1		77	75	OSC_2	O
70	68	V_2		78	76	RESET	I
71	69	V_3		79	77	D_0	I/O
72	70	TONEC	O	80	78	D_1	I/O

Note: I/O: Input/output pin, I: Input pin, O: Output pin

Pin Functions

Power Supply

V_{CC}: Apply power voltage to this pin.

GND: Connect to ground.

$\overline{TEST}$: Used for test purposes only. Connect it to V_{CC}.

RESET: Resets the MCU.

Oscillators

OSC_1, OSC_2: Used as pins for the internal oscillator circuit. They can be connected to a ceramic resonator, or OSC_1 can be connected to an external oscillator circuit.

X1, X2: Used for a 32.768-kHz crystal oscillator that acts as a clock.

Ports

D_0–D_{13} (D Port): Input/output port addressable by individual bits. D_0–D_9 are I/O pins and D_{10}–D_{13} are input pins. D_0–D_9 are high current output pins (15 mA, max.). D_{11}–D_{13} are also available as voltage comparators.

R0–R3 (R Ports): Input/output ports addressable in 4-bit units. $R0_0$, $R0_1$, $R0_2$, $R3_1$, $R3_2$, and $R3_3$, are multiplexed with $\overline{SCK}$, SI, SO, TIMO, $\overline{INT}_0$, and $\overline{INT}_1$, respectively.

Interrupts

$\overline{INT_0}$, $\overline{INT_1}$: Input external interrupts to the MCU. $\overline{INT_1}$ is also used as an external event input for timer B. $\overline{INT_0}$ and $\overline{INT_1}$ are multiplexed with $R3_2$ and $R3_3$, respectively.

Serial Communications Interface

$\overline{SCK}$: Input/output serial clock pin multiplexed with $R0_0$.

SI: Serial receive data input pin multiplexed with $R0_1$.

SO: Serial transmit data output pin multiplexed with $R0_2$.

Timers

TIMO: Outputs a variable-duty square wave. It is multiplexed with $R3_1$.

LCD Driver/Controller

V_1, V_2, V_3: Power supply pins for the LCD driver. Internal resistors provide the voltage level for each pin. The voltage condition is $V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq GND$.

COM1–COM4: Common signal output pins for LCD display.

SEG1–SEG32: Segment signal output pins for LCD display.

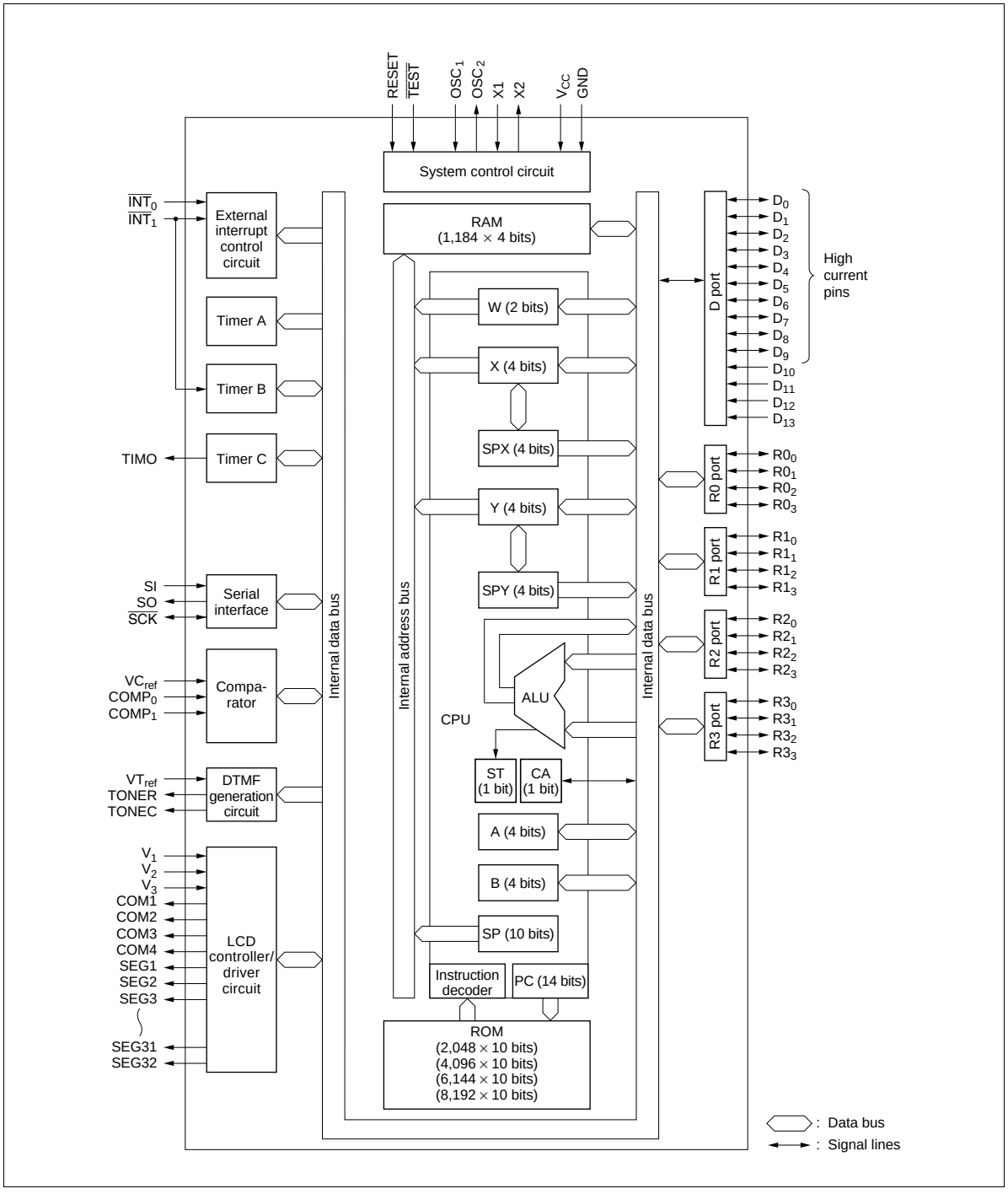
DTMF Generator

TONER, TONEC, VT_{ref}: DTMF signal pins. TONER and TONEC transmit signals for row and column, respectively. VT_{ref} is a reference voltage for DTMF signals. Apply condition $V_{CC} \geq VT_{ref} \geq GND$ to VT_{ref}.

Voltage Comparator

COMP0, COMP1, VC_{ref}: COMP0 and COMP1 are analog inputs for the voltage comparator. VC_{ref} is a reference voltage pin that inputs the threshold voltage of the analog input pin.

Block Diagram



Memory Map

ROM Memory Map

The ROM memory map is shown in figure 1, and the ROM is described below.

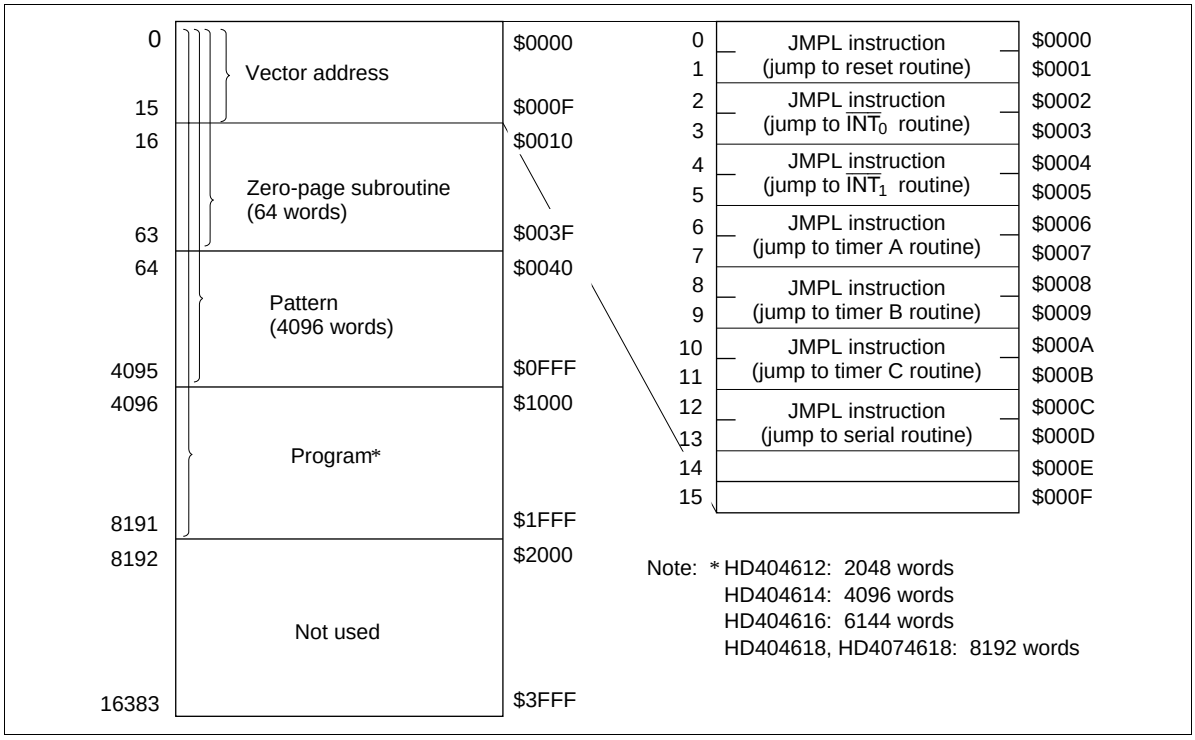


Figure 1 ROM Memory Map

Vector Address Area ($0000–$000F): Reserved for JMPL instructions that branch to the start addresses of the reset and interrupt routines. After an MCU reset or interrupt execution, the program starts from the vector address.

Zero-Page Subroutine Area ($0000–$003F): Reserved for subroutines. The program branches to a subroutine in this area in response to the CAL instruction.

Pattern Area ($0000–$0FFF): Contains ROM data that can be referenced with the P instruction.

Program Area ($0000–$07FF (HD404612), $0000–$0FFF (HD404614), $0000–$17FF (HD404616), $0000–$1FFF (HD404618, HD4074618)): Used for program coding.

RAM Memory Map

The MCU contains a 1,184-digit × 4-bit RAM area consisting of a data area and a stack area. In addition, interrupt control bits and special registers are mapped onto the same RAM memory space outside this area. The RAM memory map is shown in figure 2, and described below.

Interrupt Control Bits Area ($000–$003): Used for interrupt control bits and the bit register (figure 3). The register flag area consists of LSON, WDON, TGSP, and DTON flags. Both areas can be accessed only by RAM bit manipulation instructions. In addition, note that the interrupt request flag cannot be set by software, the RSP bit is used only to reset the stack pointer. Limitations on using the instructions are shown in figure 4.

Register Flag Area ($020–$023): Consist of the LSON, WDON, TGSP, and DTON flags which are bit registers accessible by RAM bit manipulation instructions.

The WDON flag can only be set, only by the SEM/SEMD instruction.

The TGSP flag can be set and reset by the SEM/SEMD and REM/REMD instructions.

The DTON flag can be set, reset, and tested by the SEM/SEMD, REM/REMD, and TMD instructions. Note that the DTON flag is active only in subactive mode, and is normally reset in active mode.

Special Function Registers Area ($004–$01F, $024–$03F): Used as mode or data registers for serial interface, timer/counters, LCD, and DTMF, and as data control registers for I/O ports. These registers are classified into three types: write-only, read-only, and read/write as shown in figure 2.

The SEM/REM and SEMD/REMD instructions can be used for the LCD control register (LCR), but RAM bit manipulation instructions cannot be used for other registers.

LCD Data Area ($050–$06F): Used for storing LCD data which is automatically output to LCD segments as display data. Data 1 lights the corresponding LCD segment; data 0 extinguishes it. This area can be used as data area.

Data Area ($040–$2CF, $100–$2CF; Bank 0, 1): The memory registers (MR), which consist of 16 digits ($040–$04F), can be accessed by the LAMR and XMRA instructions (see figure 5). In the 464 digits from $100–$2CF, a bank can be selected by the V register (see section on V register).

Stack Area ($3C0–$3FF): Used for saving the contents of the program counter (PC), status flag (ST), and carry flag (CA) at subroutine call (CAL or CALL instruction) and interrupt processing. This area can be used as a 16-level nesting subroutine stack in which one level requires four digits. The data to be saved and the save conditions are shown in figure 5.

The program counter is restored by either the RTN or RTNI instruction, but the status and carry flags can only be restored by the RTNI instruction. Any unused space in this area is used for data storage.

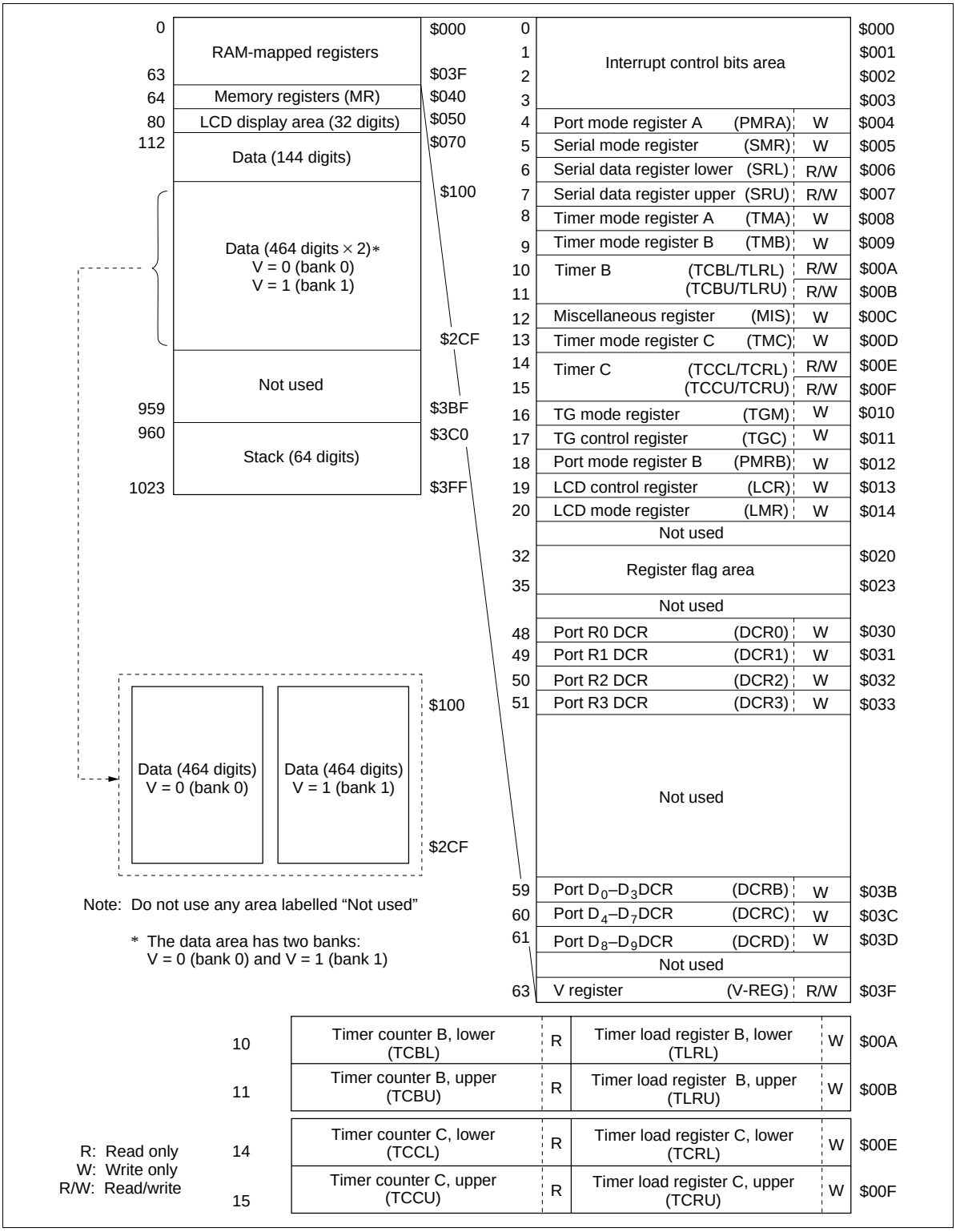


Figure 2 RAM Memory Map

	Bit 3	Bit 2	Bit 1	Bit 0	
0	IM0 (IM of $\overline{INT_0}$)	IF0 (IF of $\overline{INT_0}$)	RSP (Reset SP bit)	IE (Interrupt enable flag)	$000
1	IMTA (IM of timer A)	IFTA (IF of timer A)	IM1 (IM of $\overline{INT_1}$)	IF1 (IF of $\overline{INT_1}$)	$001
2	IMTC (IM of timer C)	IFTC (IF of timer C)	IMTB (IM of timer B)	IFTB (IF of timer B)	$002
3	Not used	Not used	IMS (IM of serial)	IFS (IF of serial)	$003
32	DTON Direct transfer on flag	TGSP (Tone generator speed flag)	WDON (Watchdog on flag)	LSON (Low speed on flag)	$020
	Not Used				$021
35					$023

IF: Interrupt request flag
IM: Interrupt mask
IE: Interrupt enable flag
SP: Stack pointer
Note: Bits in the interrupt control bits area and register flag area are set by the SEM or SEMD instruction, reset by the REM or REMD instruction, and tested by the TM or TMD instruction. Other instructions have no effect.

Figure 3 Configuration of Interrupt Control Bits and Register Flag Areas

	SEM/SEMD	REM/REMD	TM/TMD
IF	Not executed	Allowed	Allowed
RSP	Not executed	Allowed	Inhibited
WDON	Allowed	Not executed	Inhibited
TGSP	Allowed	Allowed	Inhibited
DTON	Not executed in active mode	Allowed	Allowed
	Used in subactive mode		

Note: WDON is always reset in active mode.
DTON is always reset in active mode.
If the TM or TMD instruction is executed for the inhibited bits or non-existing bits, the value in ST becomes invalid.

Figure 4 Usage Limitations of RAM Bit Manipulation Instructions

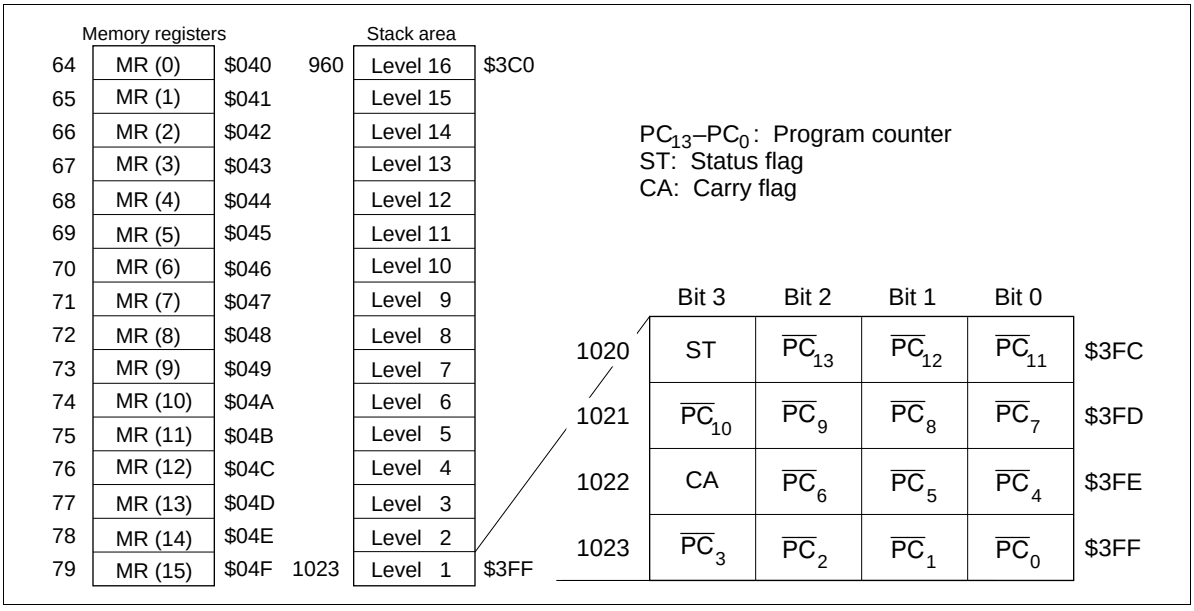


Figure 5 Configuration of Memory Registers and Stack Area, and Stack Position

Functional Description

Registers and Flags

The MCU has ten registers and two flags for CPU operations. They are illustrated in figure 6 and described below.

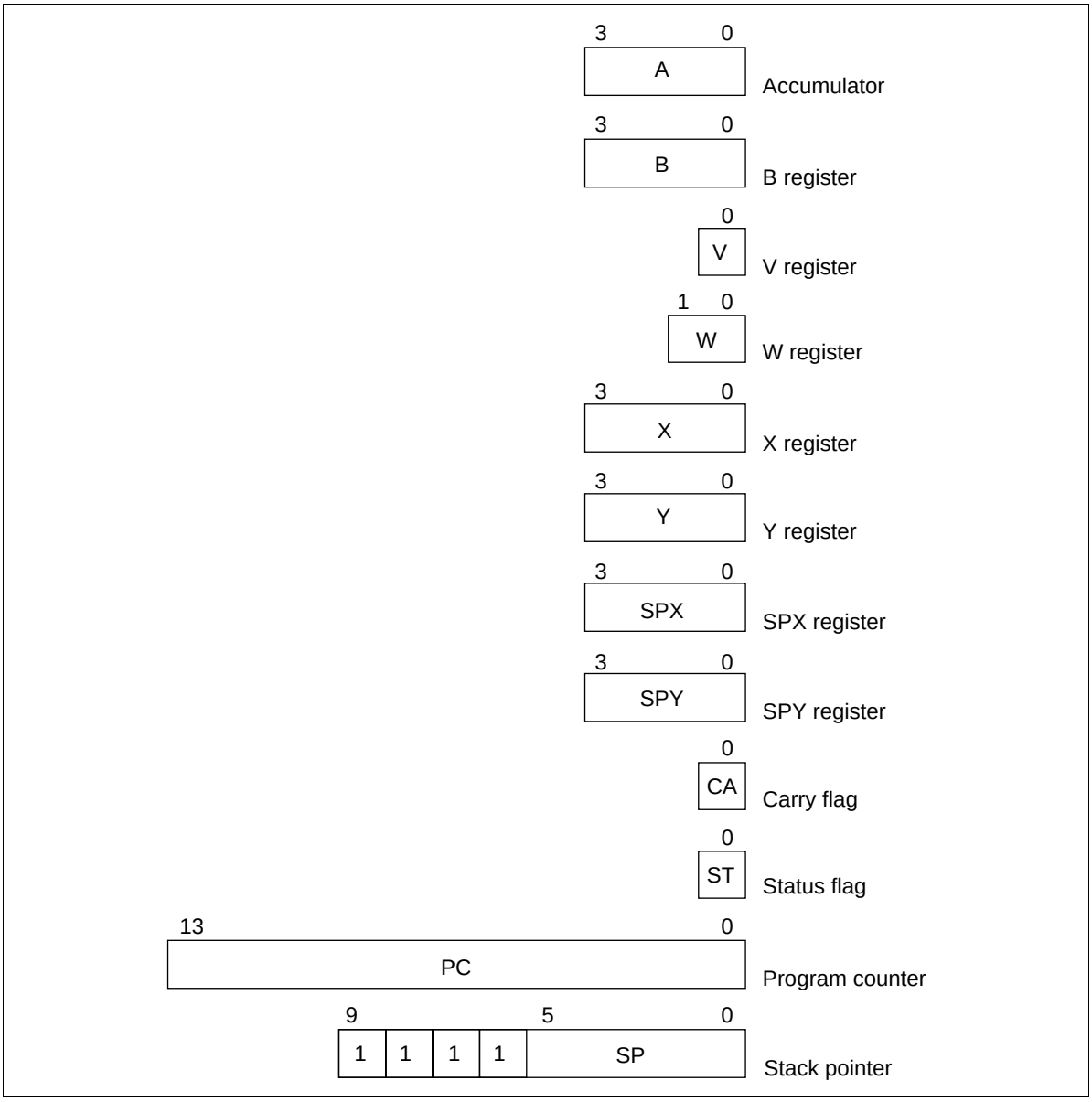


Figure 6 Registers and Flags

Accumulator (A), B Register (B): Four-bit registers used to hold results from the arithmetic logic unit (ALU) and transfer data between memory, I/O, and other registers.

V Register (V): Used for RAM address expansion and selecting the bank of RAM addresses $100–$2CF (464 digits). Thus, when accessing locations $100–$2CF, specify the value of the V register (V = $0 for bank 0, V = $1 for bank 1). Locations $000–$0FF and $3C0–$3FF can be accessed independent of the V register. The V register is located at RAM address $03F.

W Register (W), X Register (X), Y Register (Y): Two-bit (W) and four-bit (X and Y) registers used for indirect RAM addressing. The Y register is also used for D-port addressing.

SPX Register (SPX), SPY Register (SPY): Four-bit registers used to supplement the X and Y registers.

Carry Flag (CA): One-bit flag that stores any ALU overflow generated by an arithmetic operation. CA is affected by the SEC, REC, ROTL, and ROTR instructions. During an interrupt, a carry is pushed onto the stack and popped from the stack by the RTNI instruction–but not by the RTN instruction.

Status Flag (ST): One-bit flag that latches any overflow generated by an arithmetic or compare instruction, not-zero decision from the ALU, or result of a bit test. ST is used as a branch condition of the BR, BRL, CAL, or CALL instruction. The contents of ST remain unchanged until the next arithmetic, compare, or bit test instruction is executed, but become 1 after the BR, BRL, CAL, or CALL instruction is read, regardless of whether the instruction is executed or skipped. During an interrupt, the contents of ST are pushed onto the stack and popped from the stack by the RTNI instruction, but not by the RTN instruction.

Program Counter (PC): A 14-bit counter that points to the ROM address of the instruction being executed.

Stack Pointer (SP): Ten-bit pointer that contains the address of the stack area to be used next. The SP is initialized to $3FF by MCU reset, is decremented by 4 when data is pushed onto the stack, and is incremented by 4 when data is popped from the stack. Since the top four bits of the SP are fixed at 1111, a stack of up to 16 levels can be used.

The SP can also be initialized to $3FF in another way: by resetting the RSP bit with the REM or REMD instruction.

Reset

The MCU is reset by inputting a high-level voltage to the RESET pin. At power-on or when stop mode is cancelled, RESET must be high for at least one t_{RC} to enable the oscillator to stabilize.

During operation, RESET must be high for at least two instruction cycles.

I/O pins go to high-impedance at power-on.

Initial values after MCU reset are shown in table 1.

Table 1 Initial Values After MCU Reset

Item		Abbr.	Initial Value	Contents
Program counter		(PC)	$0000	Indicates program execution point from start address of ROM area
Status flag		(ST)	1	Enables conditional branching
Stack pointer		(SP)	$3FF	Stack level 0
V register (bank register)		(V)	0	Bank 0 (memory)
Interrupt flags/mask	Interrupt enable flag	(IE)	0	Inhibits all interrupts
	Interrupt request flag	(IF)	0	Indicates there is no interrupt request
	Interrupt mask	(IM)	1	Prevents (masks) interrupt request
I/O	Port data register	(PDR)	All bits 1	Enables output at level 1
	Data control register	(DCR)	All bits 0	Turns output buffer off (to high impedance)
	Port mode register A	(PMRA)	0000	Refer to description of port mode register A
	Port mode register B	(PMRB)	0000	Refer to description of port mode register B
Timer/ counters, serial interface	Timer mode register A	(TMA)	0000	Refer to description of timer mode register A
	Timer mode register B	(TMB)	0000	Refer to description of timer mode register B
	Timer mode register C	(TMC)	0000	Refer to description of timer mode register C
	Serial mode register	(SMR)	0000	Refer to description of serial mode register
	Prescaler S		$000	—
	Prescaler W		$00	—
	Timer counter A	(TCA)	$00	—

Table 1 Initial Values After MCU Reset (cont)

Item		Abbr.	Initial Value	Contents
Timer/ counters, serial interface	Timer counter B	(TCB)	$00	—
	Timer counter C	(TCC)	$00	—
	Timer load register B	(TLR)	$00	—
	Timer load register C	(TCR)	$00	—
	Octal counter		000	—
LCD	LCD control register	(LCR)	000	Refer to description of LCD control register
	LCD mode register	(LMR)	0000	Refer to description of LCD duty cycle/clock control
DTMF generator	Tone generator control register	(TGC)	000	Refer to description of tone generator control register
	Tone generator mode register	(TGM)	0000	Refer to description of generator mode register
Bit registers	Low speed on flag	(LSON)	0	Refer to description of operating modes
	Watchdog timer on flag	(WDON)	0	Refer to description of timer C
	Tone generator speed flag	(TGSP)	0	Refer to description of DTMF generation circuit
	Direct transfer on flag	(DTON)	0	Refer to description of operating modes
Miscellaneous register		(MIS)	000	—

Item	Abbr.	Status after Cancellation of Stop Mode by MCU Reset	Status after Cancellation of All Other Modes by MCU Reset
Carry flag	(CA)	Pre-MCU-reset values are not guaranteed; values must be initialized by program	Pre-MCU-reset values are not guaranteed; values must be initialized by program
Accumulator	(A)		
B register	(B)		
W register	(W)		
X/SPX register	(X/SPX)		
Y/SPY register	(Y/SPY)		
Serial data register	(SR)		
RAM		Pre-MCU-reset (pre-STOP-instruction) values are retained	

Interrupts

The MCU has six interrupt sources: two external signals ($\overline{INT_0}$ and $\overline{INT_1}$), three timer/counters (timers A, B, and C), and serial interface (serial).

An interrupt request flag (IF), interrupt mask (IM), and vector address are provided for each interrupt source, and an interrupt enable flag (IE) controls the entire interrupt process.

Interrupt Control Bits and Interrupt Servicing: Locations $000 through $003 in RAM space are reserved for interrupt control bits which can be accessed by RAM bit manipulation instructions.

The interrupt request flag (IF) cannot be set by software. MCU reset initializes the interrupt enable flag (IE) and the IF to 0 and the interrupt mask (IM) to 1.

Figure 7 is a block diagram of the interrupt control circuit. Table 2 lists interrupt priorities and vector addresses, and table 3 lists the interrupt processing conditions for the six interrupt sources.

An interrupt request occurs when the IF is set to 1 and IM to 0. If the IE is 1 at that point, the interrupt is processed. A priority programmable logic array (PLA) generates the vector address assigned to that interrupt source.

Figure 8 shows the interrupt processing sequence, and figure 9 shows an interrupt processing flowchart. After an interrupt is acknowledged, the previous instruction is completed in the first cycle. The IE is reset in the second cycle, the carry flag, status flag, and program counter values are pushed onto the stack during the second and third cycles, and the program jumps to the vector address to execute the instruction in the third cycle.

Program the JMPL instruction at each vector address to branch the program to the start address of the interrupt program, and reset the IF by a software instruction within the interrupt program.

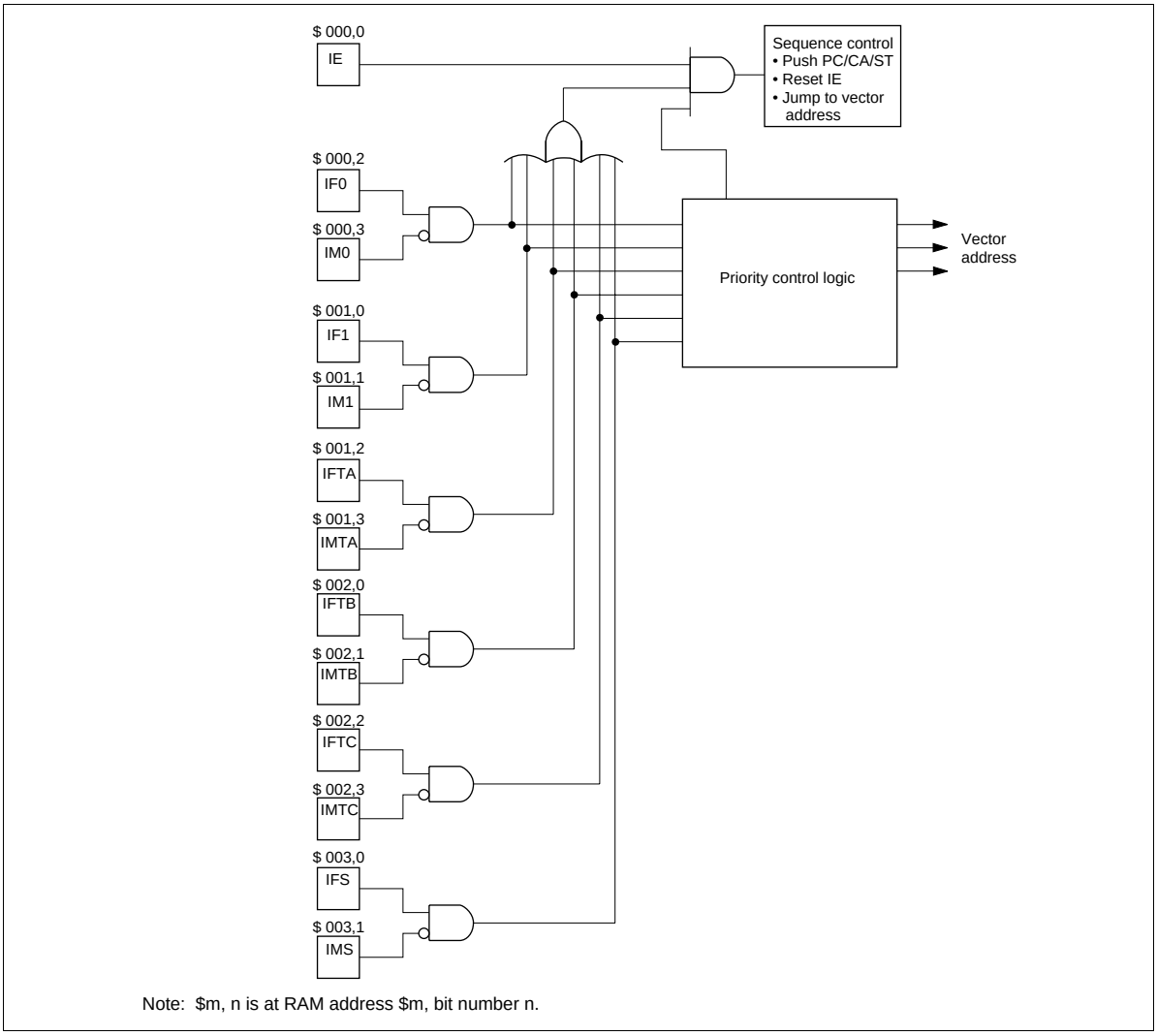


Figure 7 Block Diagram of Interrupt Control Circuit

Table 2 Vector Addresses and Interrupt Priorities

Reset/Interrupt	Priority	Vector Address
RESET		$0000
$\overline{INT}_0$	1	$0002
$\overline{INT}_1$	2	$0004
Timer A	3	$0006
Timer B	4	$0008
Timer C	5	$000A
Serial	6	$000C

Table 3 Interrupt Processing and Activation Conditions

	Interrupt Source					
Interrupt Control Bit	**$\overline{INT_0}$**	**$\overline{INT_1}$**	**Timer A**	**Timer B**	**Timer C**	**Serial**
IE	1	1	1	1	1	1
IF0·$\overline{IM0}$	1	0	0	0	0	0
IF1·$\overline{IM1}$	*	1	0	0	0	0
IFTA·$\overline{IMTA}$	*	*	1	0	0	0
IFTB·$\overline{IMTB}$	*	*	*	1	0	0
IFTC·$\overline{IMTC}$	*	*	*	*	1	0
IFS·$\overline{IMS}$	*	*	*	*	*	1

Note: Bits marked by * can be either 0 or 1. Their values have no effect on operation.

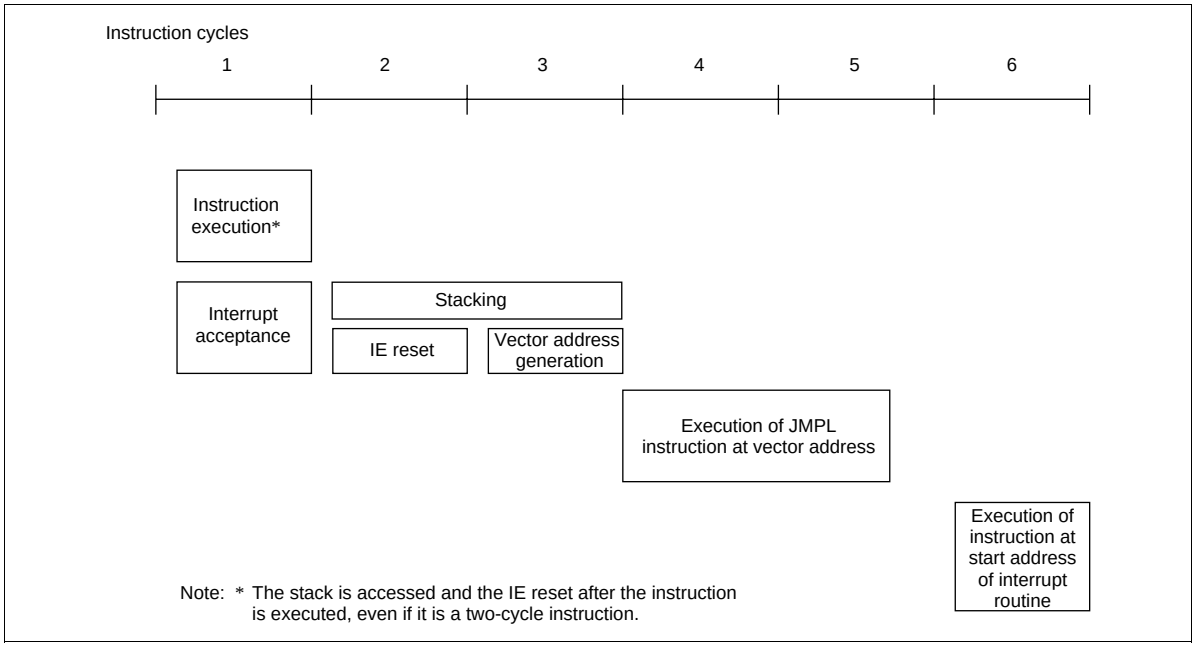


Figure 8 Interrupt Processing Sequence

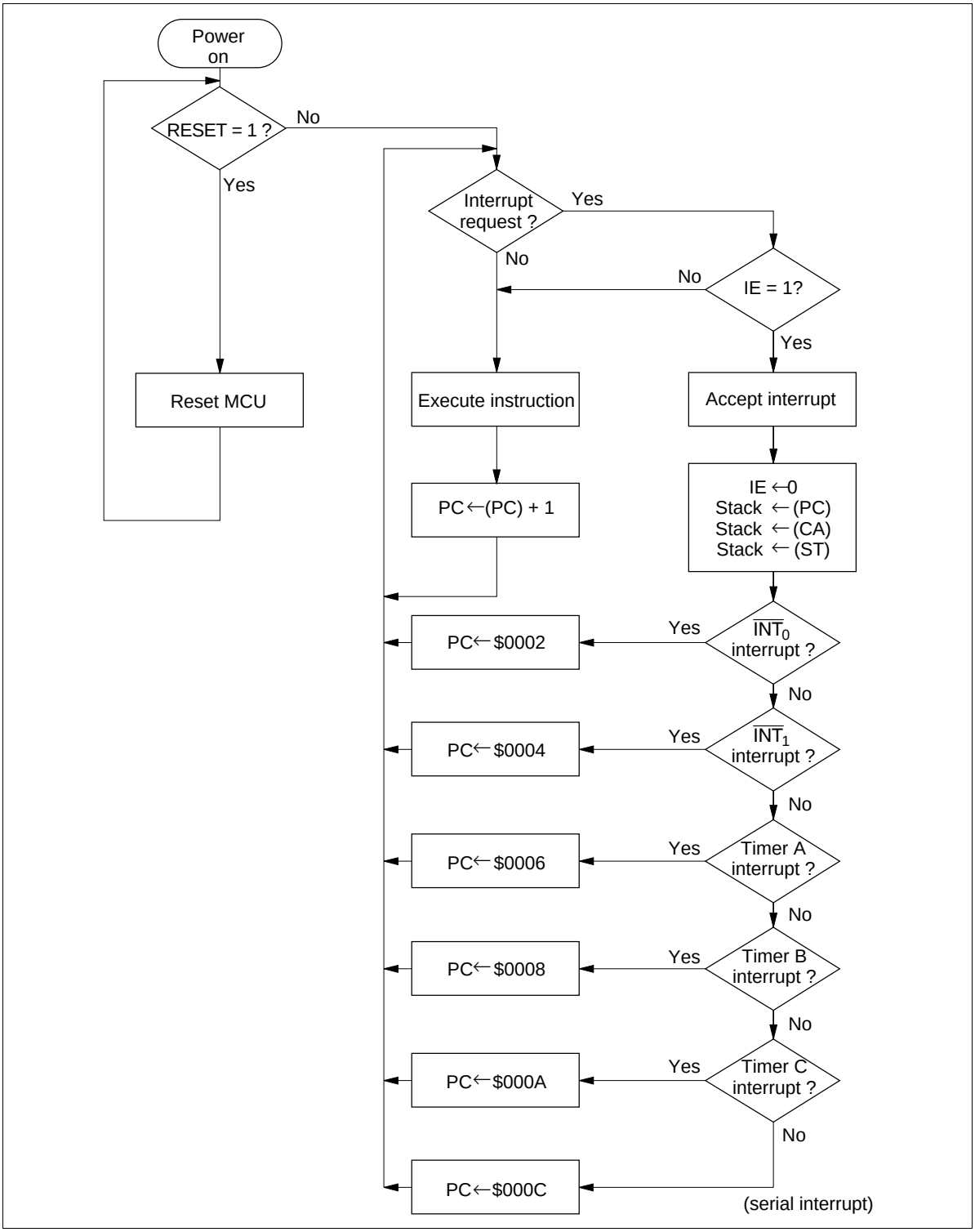


Figure 9 Interrupt Processing Flowchart

Interrupt Enable Flag (IE: $000, Bit 0): Controls the entire interrupt process. It is reset by the interrupt processing and set by the RTNI instruction, as shown in table 4.

Table 4 Interrupt Enable Flag

IE	Interrupt Enabled/Disabled
0	Disabled
1	Enabled

External Interrupts ($\overline{INT_0}$, $\overline{INT_1}$): Specified by port mode register A (PMRA: $004).

The $\overline{INT_1}$ input can be used as a clock signal input to timer B. Timer B increments at each falling edge of the $\overline{INT_1}$ input. When using $\overline{INT_1}$ as a timer B external event input, external interrupt mask IM1 must be set to prevent the $\overline{INT_1}$ interrupt request from being accepted (see table 6).

To detect the edge of $\overline{INT_0}$ or $\overline{INT_1}$, more than two instruction cycle times are required ($2t_{cyc}$ or $2t_{subcyc}$).

External Interrupt Request Flags (IF0: $000, Bit 2; IF1: $001, Bit 0): Set at the falling edge of the $\overline{INT_0}$ and $\overline{INT_1}$ inputs as shown in table 5.

Table 5 External Interrupt Request Flags

IF0, IF1	Interrupt Request
0	No
1	Yes

External Interrupt Masks (IM0: $000, Bit 3; IM1: $001, Bit 1): Prevent (mask) interrupt requests caused by the corresponding external interrupt request flags, as shown in table 6.

Table 6 External Interrupt Masks

IM0, IM1	Interrupt Request
0	Enabled
1	Disabled (masked)

Timer A Interrupt Request Flag (IFTA: $001, Bit 2): Set by overflow output from timer A as shown in table 7.

Table 7 Timer A Interrupt Request Flag

IFTA	Interrupt Request
0	No
1	Yes

Timer A Interrupt Mask (IMTA: $001, Bit 3): Prevents (masks) an interrupt request caused by the timer A interrupt request flag, as shown in table 8.

Table 8 Timer A Interrupt Mask

IMTA	Interrupt Request
0	Enabled
1	Disabled (masked)

Timer B Interrupt Request Flag (IFTB: $002, Bit 0): Set by overflow output from timer B as shown in table 9.

Table 9 Timer B Interrupt Request Flag

IFTB	Interrupt Request
0	No
1	Yes

Timer B Interrupt Mask (IMTB: $002, Bit 1): Prevents (masks) an interrupt request caused by the timer B interrupt request flag, as shown in table 10.

Table 10 Timer B Interrupt Mask

IMTB	Interrupt Request
0	Enabled
1	Disabled (masked)

Timer C Interrupt Request Flag (IFTC: $002, Bit 2): Set by overflow output from timer C as shown in table 11.

Table 11 Timer C Interrupt Request Flag

IFTC	Interrupt Request
0	No
1	Yes

Timer C Interrupt Mask (IMTC: $002, Bit 3): Prevents (masks) an interrupt request caused by the timer C interrupt request flag, as shown in table 12.

Table 12 Timer C Interrupt Mask

IMTC	Interrupt Request
0	Enabled
1	Disabled (masked)

Serial Interrupt Request Flag (IFS: $003,Bit 0): Set when the octal counter counts the eighth transmit clock signal or when data transmit is discontinued by resetting the octal counter, as shown in table 13.

Table 13 Serial Interrupt Request Flag

IFS	Interrupt Request
0	No
1	Yes

Serial Interrupt Mask (IMS: $003, Bit 1): Prevents (masks) an interrupt request caused by the serial interrupt request flag, as shown intable 14.

Table 14 Serial Interrupt Mask

IMS	Interrupt Request
0	Enabled
1	Disabled (masked)

Operating Modes

The MCU has five operating modes that are specified by how the clock is used. The functions available in each mode are listed in table 15, and operations are shown in table 16. Transitions between operating modes are shown in figure 10. Table 17 provides additional information for table 15.

Table 15 Functions Available in Each Operating Mode

		Mode Name				
		Active	**Standby**	**Stop**	**Watch**	**Subactive*4**
Activation method		Reset cancellation, interrupt request	SBY instruction	TMA3 = 0, STOP instruction	TMA3 = 1, STOP instruction	$\overline{INT}_0$ or timer A interrupt request from watch mode
Status	System oscillator	Operating	Operating	Stopped	Stopped	Stopped
	Subsystem oscillator	Operating	Operating	Operating*1	Operating	Operating
	Instruction execution ($ø_{CPU}$)	Operating	Stopped	Stopped	Stopped	Operating
	Peripheral function interrupt($ø_{PER}$)	Operating	Operating	Stopped	Stopped	Operating
	Clock function interrupt ($ø_{CLK}$)	Operating	Operating	Stopped	Operating*2	Operating*2
	RAM	Operating	Retained	Retained	Retained	Operating
	Registers/ flags	Operating	Retained	Reset	Retained	Operating
	I/O	Operating	Retained	High impedance*3	Retained*3	Operating*3
Cancellation method		RESET input, STOP/SBY instruction	RESET input, interrupt request	RESET input	RESET input, $\overline{INT}_0$ or timer A interrupt request	RESET input, STOP/SBY instruction

Notes: 1. To reduce current dissipation, stop all oscillation in external circuits.
2. Refer to the Interrupt Frame section for details.
3. Refer to table 17.
4. Subactive mode is an optional function, specify it on the function option list.
5. In the watch and subactive modes, the MCU requires a 32.768-kHz crystal oscillator.

		System Clock ($ø_{CPU}$)	
		Operating	**Stopped**
Non-time-base peripheral function clock ($ø_{PER}$)	Operating	Active mode	Standby mode
		Subactive mode	
	Stopped	—	Watch mode (TMA3 = 1)
			Stop mode (TMA3 = 0)

Table 16 Operations in Low-Power Dissipation Modes

Function	Stop Mode	Watch Mode*[3]	Standby Mode	Subactive Mode*[2, 3]
CPU	Reset	Retained	Retained	OP
RAM	Retained	Retained	Retained	OP
Timer A	Reset	OP	OP	OP
Timer B	Reset	Stopped	OP	OP
Timer C	Reset	Stopped	OP	OP
Serial interface	Reset	Stopped*[4]	OP	OP
LCD	Reset	OP	OP	OP
DTMF	Reset	Reset	Stopped	Reset
I/O	Reset*[1]	Retained	Retained	OP

Notes: OP indicates operating.

1. Output pins are at high impedance.
2. Subactive mode is an optional function specified on the function option list.
3. In the watch and subactive modes, the MCU requires a 32.768 kHz crystal oscillator.
4. Transmission/reception is activated if a clock is input in external clock mode. (However, interrupts stop.)

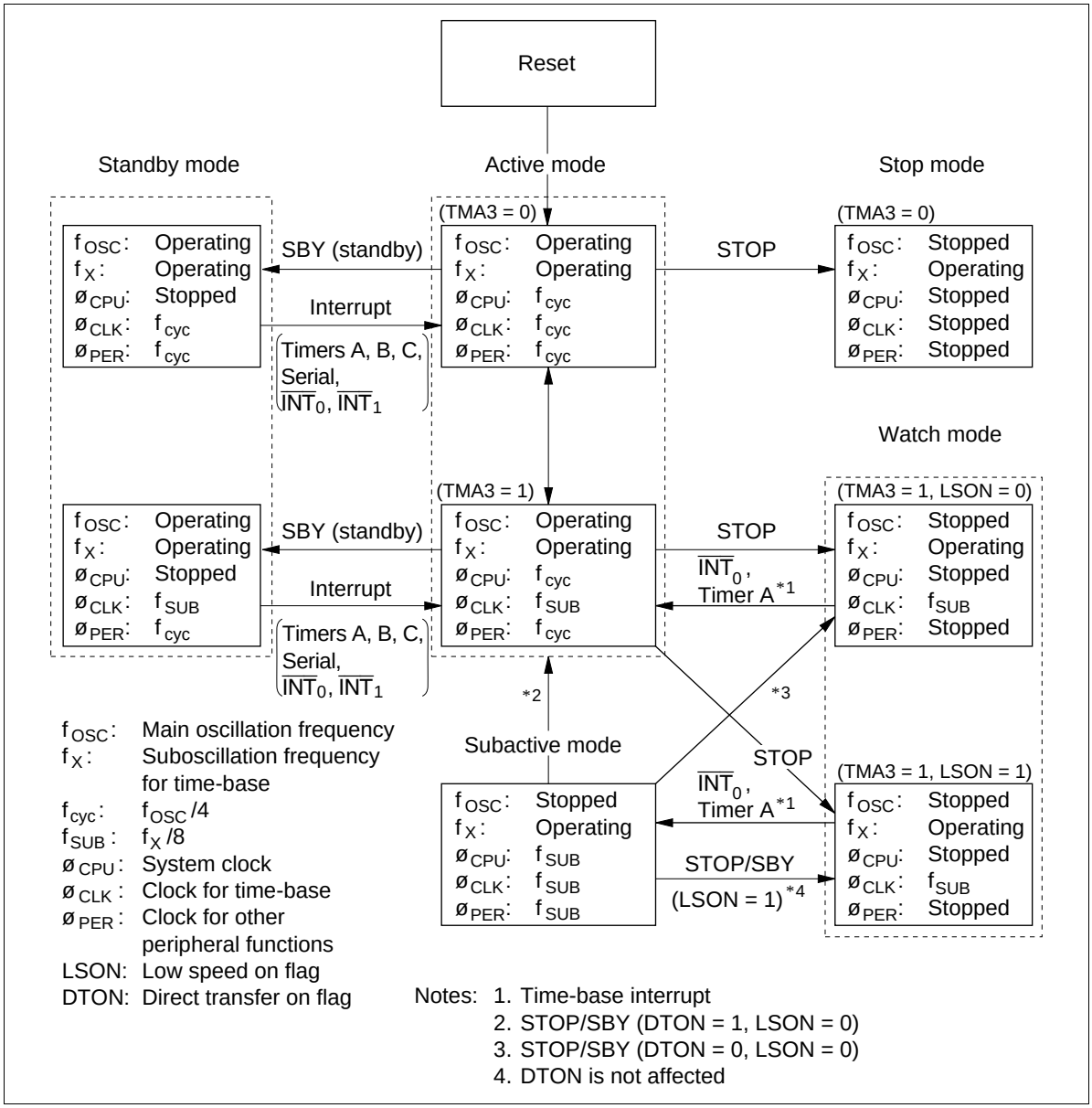


Figure 10 MCU Status Transitions

Table 17 I/O Status in Low-Power Dissipation Modes

	Output		Input
	Standby Mode, Watch Mode	**Stop Mode**	**Active Mode, Subactive Mode**
D_0–D_9	Retained	High impedance	Input enabled
D_{10}–D_{13}	—	—	Input enabled
R0–R3	Retained	High impedance	Input enabled

Active Mode: The MCU operates according to the clock generated by the system oscillators OSC_1 and OSC_2.

Standby Mode: The MCU enters standby mode when the SBY instruction is executed from active mode. In this mode, the oscillators, interrupts, timer/counters, and serial interface continue to operate, but all instruction execution-related clocks stop. The stopping of these clocks stops the CPU, retaining all RAM and register contents and maintaining the current I/O pin status.

Standby mode is terminated by a RESET input or an interrupt request. If it is terminated by RESET input, the MCU is reset as well. After an interrupt request, the MCU enters active mode and resumes, executing the next instruction after the SBY instruction. If the interrupt enable flag is 1, that interrupt is then processed; if it is 0, the interrupt request is left pending and normal instruction execution continues. A flowchart of operation in standby mode is shown in figure 11.

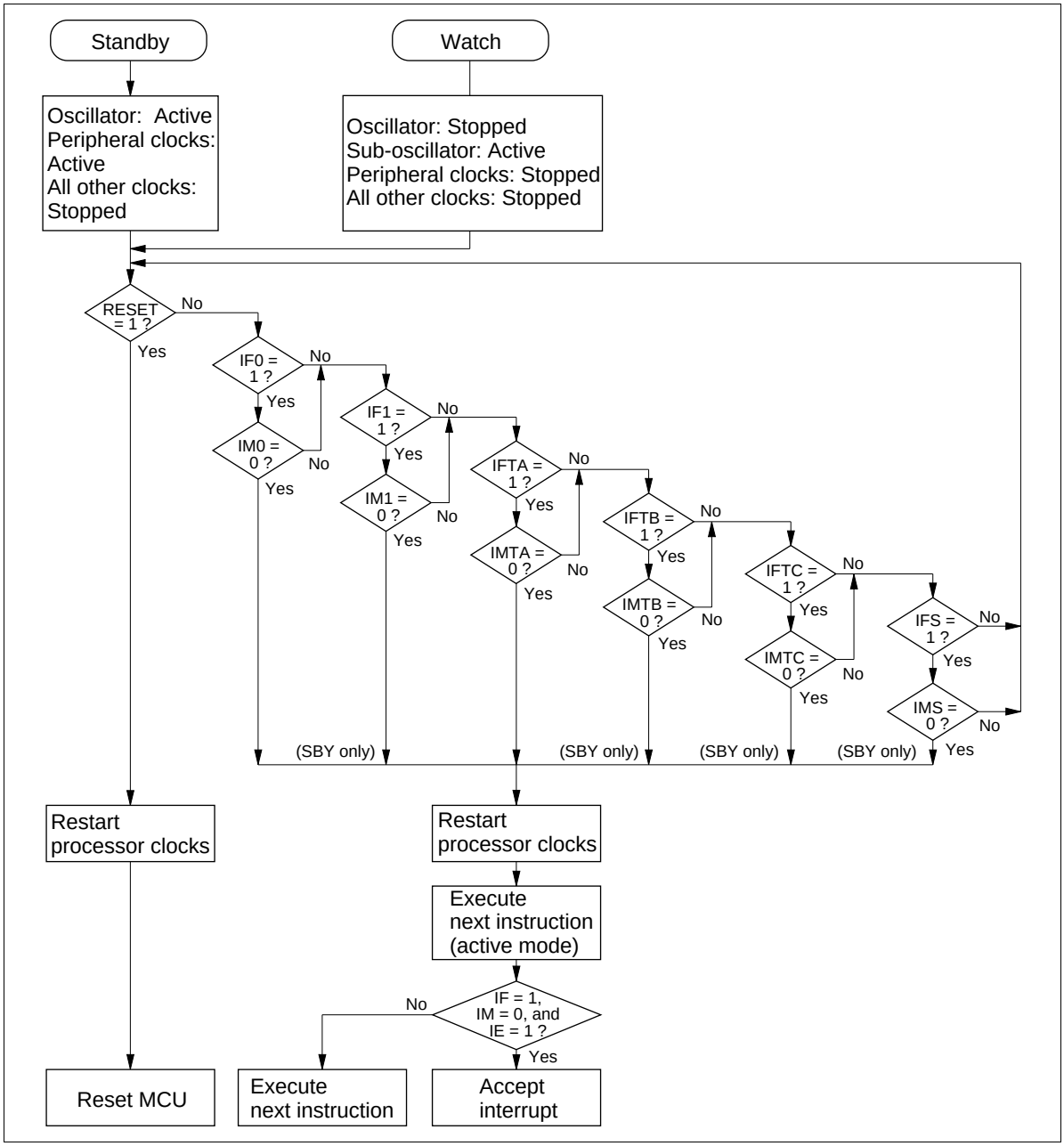


Figure 11 MCU Operation Flowchart in Watch and Standby Modes

Stop Mode: The MCU enters stop mode if the STOP instruction is executed in active mode when TMA3 = 0. In this mode, the system oscillator stops, which stops all MCU functions as well.

Stop mode is terminated by a RESET input as shown in figure 12. RESET must be high for at least one t_{RC} to stabilize oscillation (refer to the AC Characteristics section). When the MCU restarts after stop mode is cancelled, all RAM contents are retained, but the accuracy of the contents of the accumulator, B register, W register, X/SPX register, Y/SPY register, carry flag, and serial data register cannot be guaranteed.

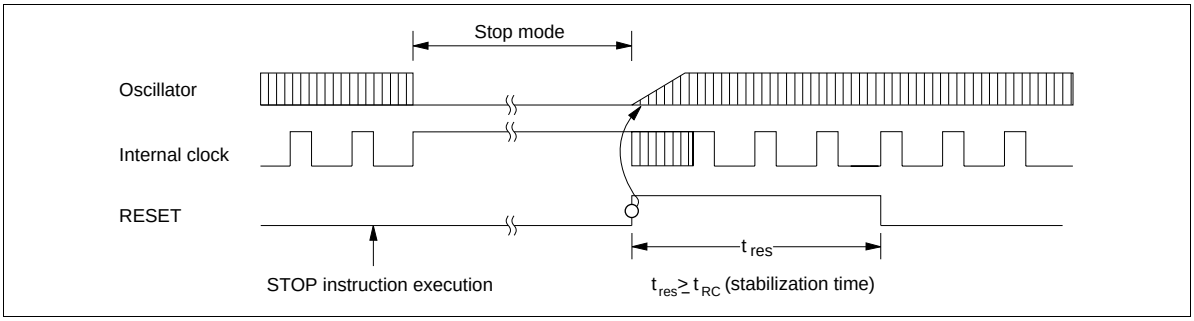


Figure 12 Timing of Stop Mode Cancellation

Watch Mode: The MCU enters watch mode if the STOP instruction is executed in active mode when TMA3 = 1, or if the STOP or SBY instruc-tion is executed in subactive mode.

Watch mode is terminated by a RESET input or a timer-A/$\overline{INT_0}$ interrupt request. For details of RESET input, refer to the Stop Mode section. When terminated by a timer-A/$\overline{INT_0}$ interrupt request, the MCU enters active mode if LSON is 0, or subactive mode if LSON is 1. After an interrupt request is generated, the time required to enter active mode is t_{RC} for a timer A interrupt, and T_X (where $T + t_{RC} < T_X < 2T + t_{RC}$) for an $\overline{INT_0}$ interrupt, as shown in figure 13.

Operation during mode transition is the same as that at standby mode cancellation (figure 12).

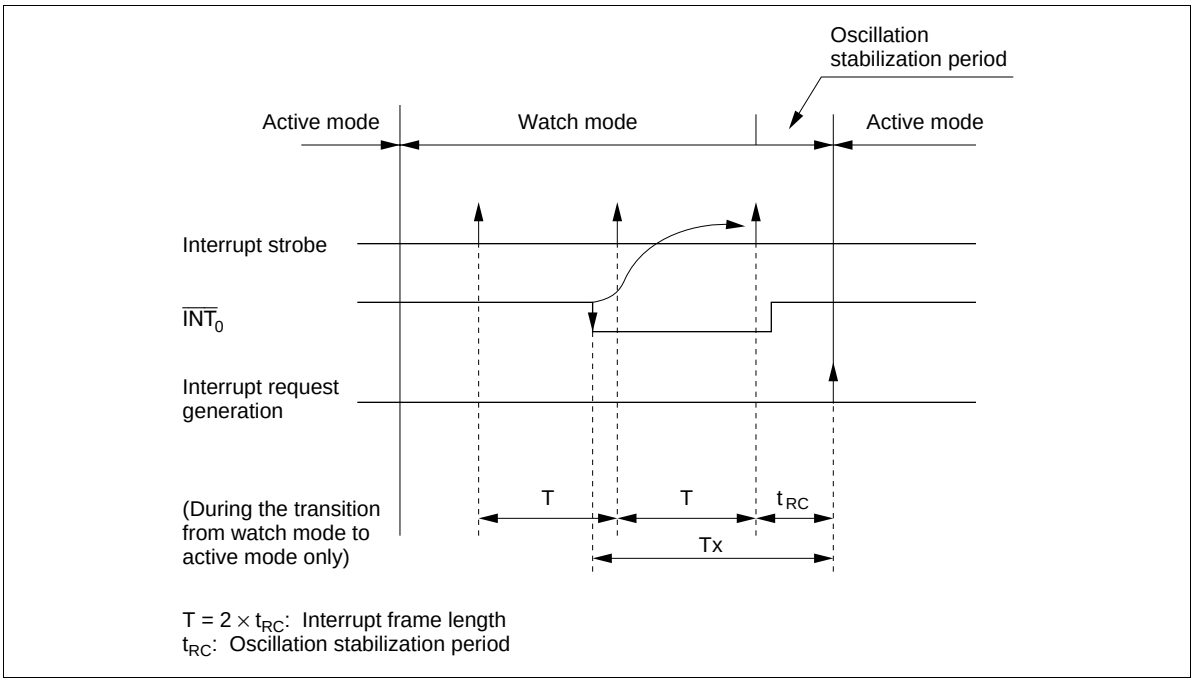


Figure 13 Interrupt Frame

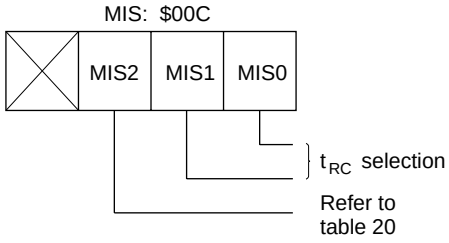
Subactive Mode: The CPU operates with a clock generated by the X1 and X2 oscillation circuits. Functions that can operate in subactive mode are listed in table 16. When the STOP or SBY instruction is executed in subactive mode, the MCU enters either watch or active mode, depending on the statuses of

LSON and DTON. The DTON flag can only be set in subactive mode; it is automatically reset after a transition to active mode.

Subactive mode is an optional function that the user must specify on the function option list.

Interrupt Frame: In watch and subactive modes, $Ø_{CLK}$ is supplied for timer A and the $\overline{INT_0}$ circuit. Prescaler W and timer A operate as time bases to generate interrupt frame timing. Three interrupt frame cycles (T) can be selected by the settings of the miscellaneous register, as shown in figure 14.

In watch and subactive modes, timer A and $\overline{INT_0}$ interrupts are generated in synchronism with the interrupt frame. An interrupt request is generated at the interrupt strobe timing, except when the MCU enters active mode from watch mode. The $\overline{INT_0}$ falling edge is acknowledged regardless of the interrupt frame, but the interrupt is executed simultaneously with the next interrupt strobe. Timer A generates an overflow and interrupt request at the timing of an interrupt strobe.



MIS		T *1	t_{RC} *1	Oscillation circuit condition
Bit 1	Bit 0			
0	0	0.24414 ms	0.12207 ms	External clock input
			0.24414 ms *2	
0	1	15.625 ms	7.8125 ms	400/800-kHz ceramic oscillator
1	0	62.5 ms	31.25 ms	
1	1	Not used		—

Notes: 1. The value of t_{RC} applies only when using a 32.768-kHz oscillator.
2. Only direct transfer.

Figure 14 Miscellaneous Register

Direct Transfer: By controlling the DTON, the MCU would be placed directly from subactive to active mode. The detailed procedure is as follows:

- Set the DTON flag in subactive mode while LSON = 0.
- Execute the STOP or SBY instruction.
- After the oscillation stabilization time (a fixed value), the MCU will move automatically from subactive to active mode.

Note that DTON ($020, bit 3) is valid only in subactive mode. When the MCU is in active mode, this flag is always at reset.

The transition time (t_D) from subactive to active mode is $t_{RC} < t_D < T + t_{RC}$.

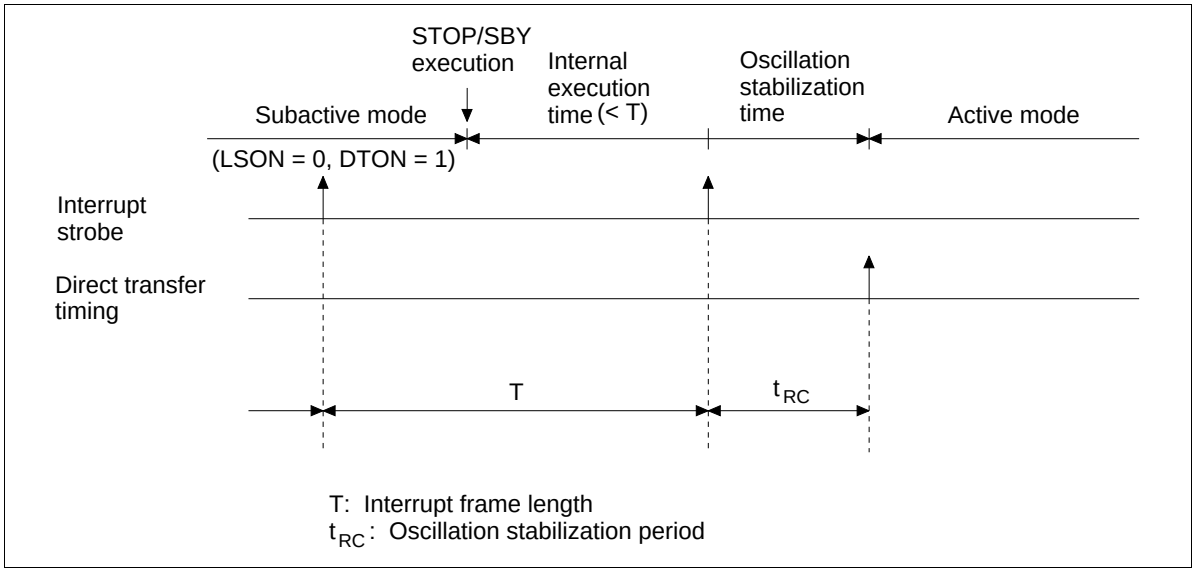


Figure 15 Direct Transfer Timing

MCU Operating Sequence: The MCU operates in the sequence shown in figures 16 to 18. It is reset by an asynchronous RESET input, regardless of its state.

The low-power mode operation sequence is shown in figure 18. With the IE flag cleared and an interrupt flag set together with its interrupt mask cleared, if a STOP/SBY instruction is executed, the instruction is cancelled (regarded as an NOP) and the following instruction is executed. Before executing a STOP/SBY instruction, make sure all interrupt flags are cleared or all interrupts are masked.

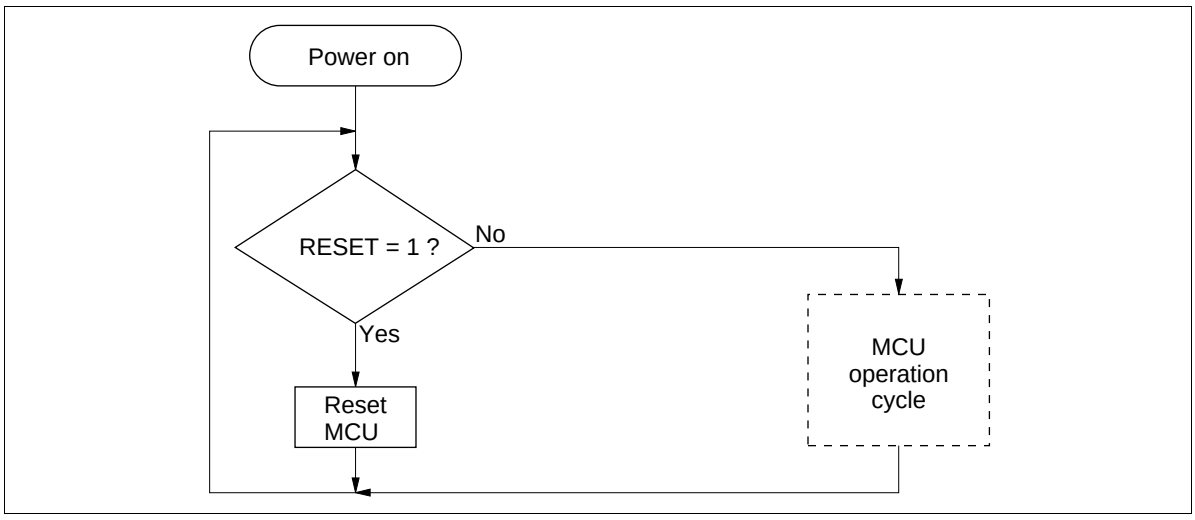


Figure 16 MCU Operating Sequence (power on)

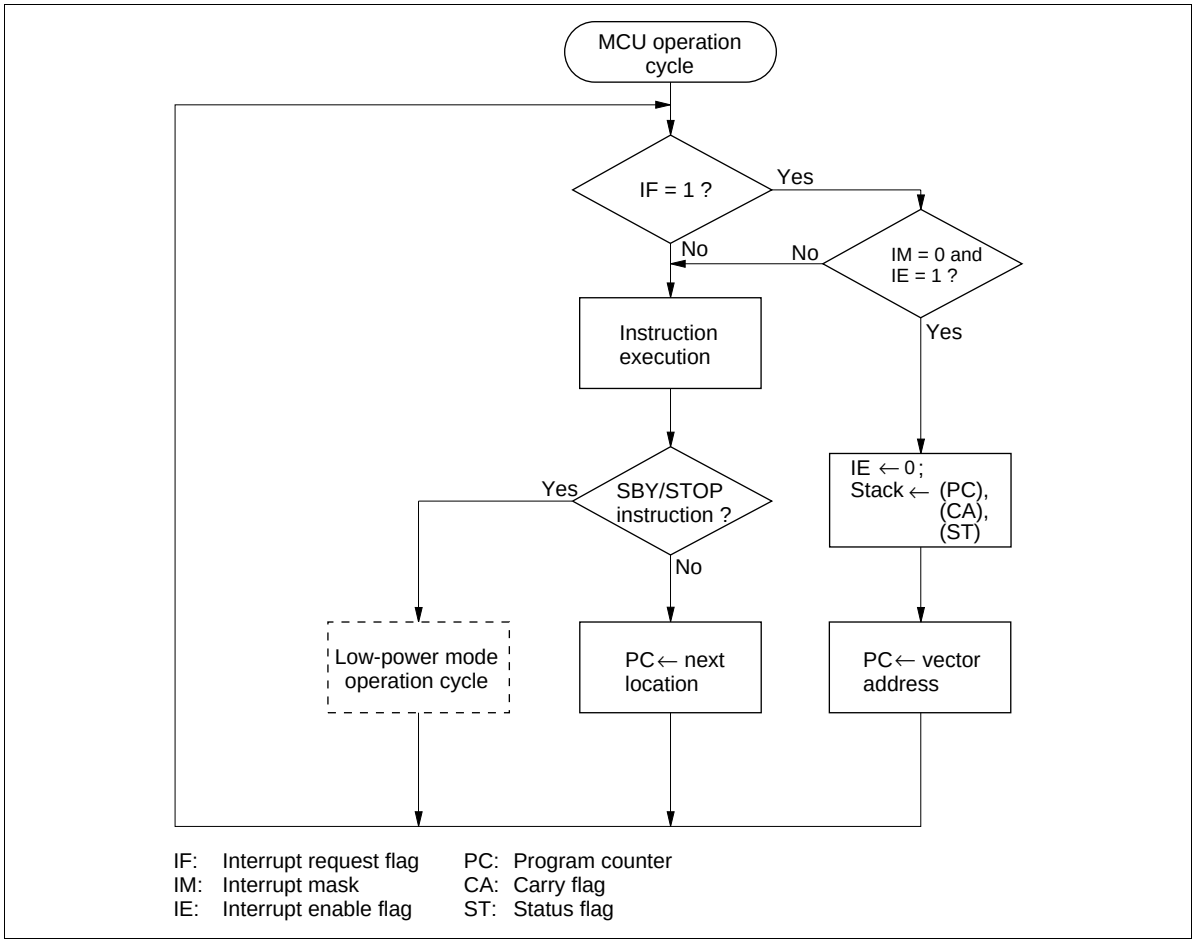


Figure 17 MCU Operating Sequence (MCU operation cycle)

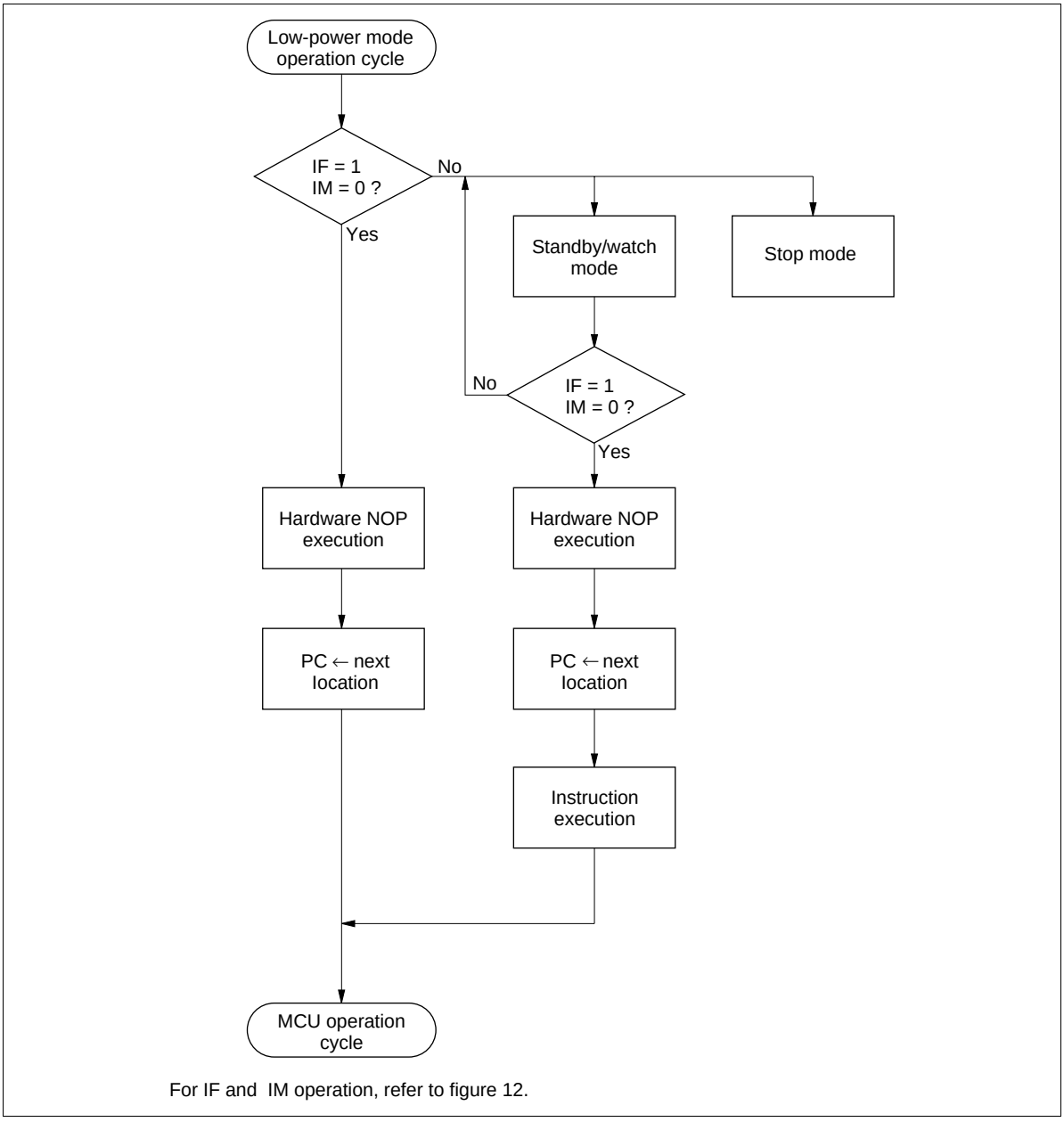


Figure 18 MCU Operating Sequence (low-power mode operation)

Notes on Use:

- In subactive mode, the timer A interrupt request or the external interrupt request ($\overline{INT}_0$) occurs in synchronism with the interrupt strobe.

  If the STOP or SBY instruction is executed at the same time with the interrupt strobe, these interrupt requests will be cancelled and the corresponding interrupt request flags (IFTA, IF0) will not be set.

  In subactive mode, do not use the STOP or SBY instruction at the time of the interrupt strobe.

- When the MCU is in watch mode or subactive mode, if the high level period before the falling edge of $\overline{INT_0}$ is shorter than the interrupt frame, $\overline{INT_0}$ is not detected. Also, if the low level period after the falling edge of $\overline{INT_0}$ is shorter than the interrupt frame, $\overline{INT_0}$ is not detected.

  Edge detection is shown in figure 19. The level of the $\overline{INT_0}$ signal is sampled by a sampling clock. When this sampled value changes to low from high, a falling edge is detected.

  In figure 20, the level of the $\overline{INT_0}$ signal is sampled by an interrupt frame. In (a) the sampled value is low at point A, and also low at point B. Therefore, a falling edge is not detected. In (b), the sampled value is high at point A, and also high at point B. A falling edge is not detected in this case either.
- When the MCU is in watch mode or subactive mode, keep the high level and low level period of $\overline{INT_0}$ longer than interrupt frame.

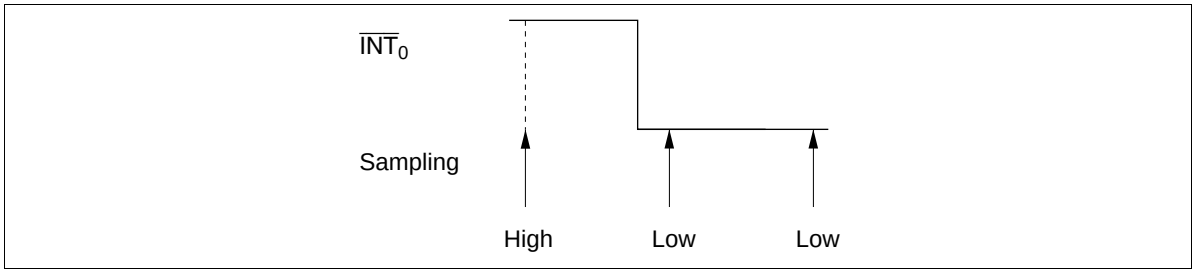


Figure 19 Edge Detection

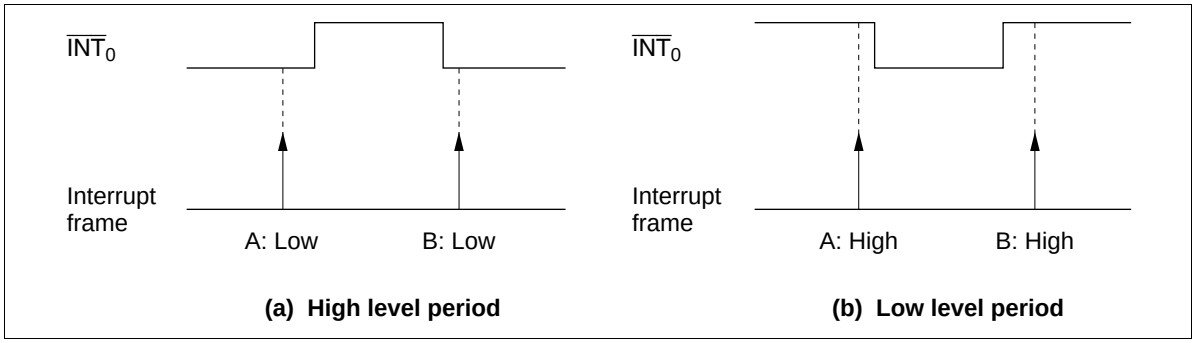


Figure 20 Sampling Example

Internal Oscillator Circuit

Figure 21 shows a block diagram of the internal oscillator circuit. A ceramic oscillator can be connected to OSC_1 and OSC_2, and a 32.768-kHz crystal oscillator can be connected to X1 and X2. The system oscillator can also be operated by an external clock.

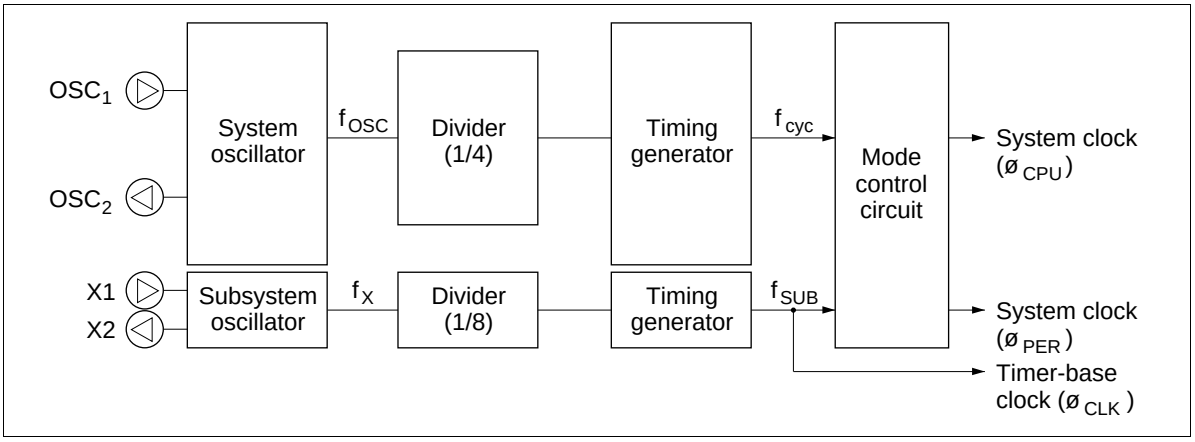


Figure 21 Internal Oscillator Circuit

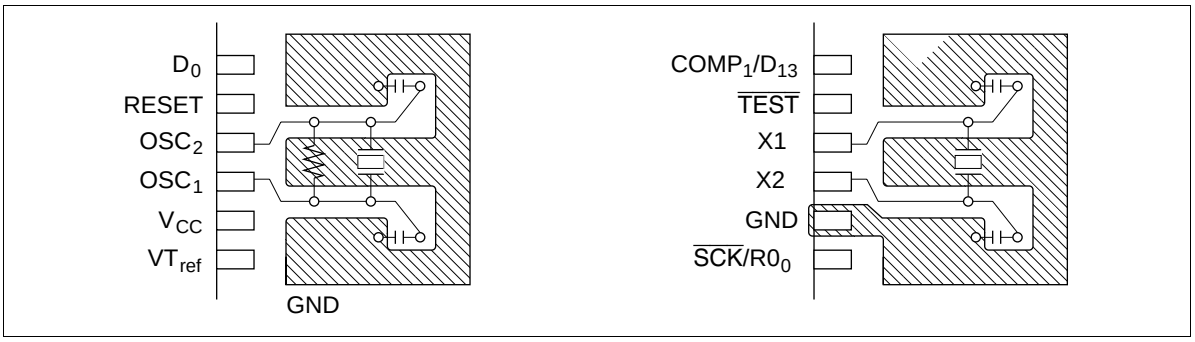
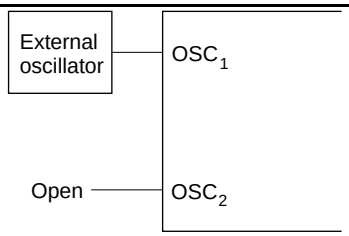
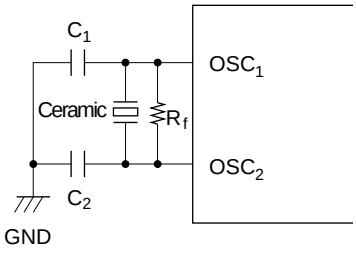
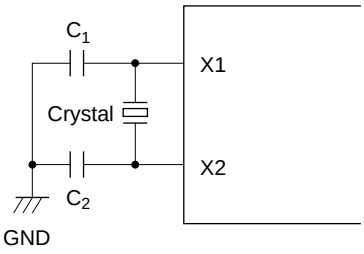
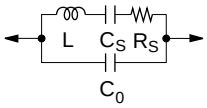


Figure 22 Layout of Crystal and Ceramic Oscillators

Table 18 Oscillator Circuit Examples

Circuit Configuration		Circuit Constants
External clock operation (OSC_1, OSC_2)		
Ceramic oscillator (OSC_1, OSC_2)		Ceramic oscillator: CSB400P22, CSB400P (Murata) R_f = 1 MΩ ± 20% $C_1 = C_2$ = 220 pF ± 5% Ceramic oscillator: CSB800J122, CSB800J(Murata) R_f = 1 MΩ ± 20% $C_1 = C_2$ = 220 pF ± 5%
Crystal oscillator	 	Crystal: 32.768 kHz: MX38T (Nippon Denpa Kogyo) R_s = 14 kΩ C_0 = 1.5 pF C_1 = 20 pF ± 20% C_2 = 20 pF ± 20%

Notes: 1. The circuit constants given above are recommended values provided by the oscillator manufacturer. Since they may be affected by stray capacitances from the oscillator or board, consult the crystal or ceramic oscillator manufacturer to determine the actual circuit parameters required.

2. Wiring between the OSC_1/OSC_2 pins (X1, X2 pins) and other elements must be as short as possible, and must not cross other wiring. Refer to the recommended layout of the crystal and ceramic oscillator in figure 22.

3. If a 32.768-kHz crystal oscillator is not used, fix the X1 pin to V_{CC} and leave the X2 pin open.

Input/Output

The MCU provides 26 input/output pins and 4 input pins, including 10 high-current pins (15 mA, max.). A program-controlled pull-up MOS transistor is provided for each input/output pin.

The output buffer is turned on and off by the data control register (DCR) during input through an input/output pin.

I/O pin circuit types are shown in table 19.

D Ports (D_0–D_{13}): Consist of ten 1-bit input/output pins and four input pins. Pins D_0–D_9 are high-current I/O pins (15 mA, max.). The sum current of the pins can go up to 100 mA. These pins are set by the SED and SEDD instructions, reset by the RED and REDD instructions, and tested by the TD and TDD instructions. Output data is stored in the port data register.

The on/off status of the output buffer is controlled by D port data control registers (DCRB, DCRC, and DCRD) that are mapped to the memory address area. Pins D_{10}–D_{13} are input-only pins.

Two operating modes are available to pins D_{12} and D_{13}: digital input mode and analog input mode. The operating modes are set by bits 0 and 1 of port mode register B (PMRB). In the digital input mode, these pins can be used as input pins with the same input characteristics as the I/O pins. In the analog input mode, the result of a comparison with the reference voltage can be read as input data. The reference voltage is input by the D_{11}/VC_{ref} pin.

R Ports: Consist of sixteen 4-bit I/O ports. Data is input to these ports by the LAR and LBR instructions and output from them by the LRA and LRB instructions.

The on/off status of the output buffers of the R ports are controlled by R port data control registers (DCR0–DCR3) that are mapped to memory addresses.

Pins $R0_0$, $R0_1$, and $R0_2$ are multiplexed with pins $\overline{SCK}$, SI, and SO, respectively.

Pins $R3_1$, $R3_2$, and $R3_3$ are multiplexed with TIMO, $\overline{INT}_0$, and $\overline{INT}_1$, respectively. Refer to figure 24.

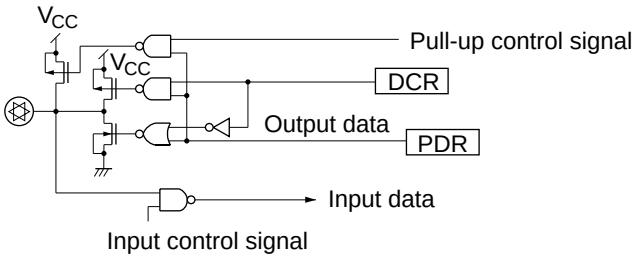
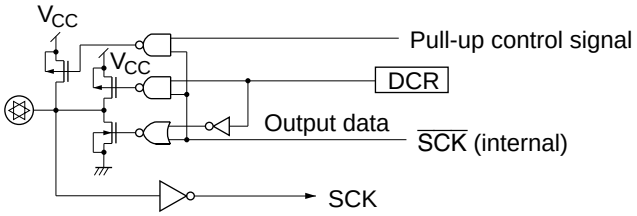
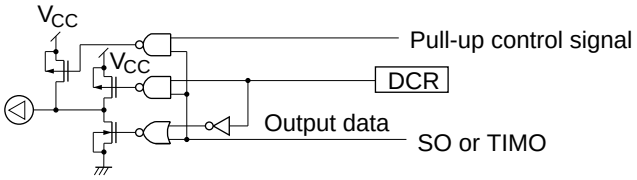
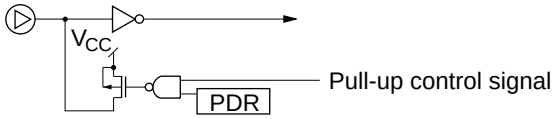
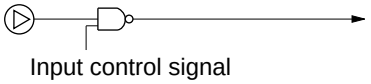
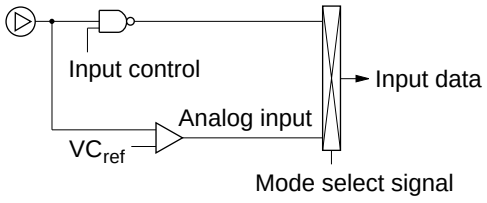
Pull-Up MOS Transistor Control: A program-controlled pull-up MOS transistor is provided for each input/output pin.

The on/off status of all these transistors is controlled by bit 3 of port mode register B (PMRB), and the on/off status of an individual transistor can also be controlled by the port data register (PDR) of the corresponding pin. This enables on/off control of each individual pin. Refer to table 20.

The on/off status of each transistor and the peripheral function mode of each pin can be set independently.

How to Deal with Unused I/O Pins: I/O pins that are not needed by the user system must be connected to V_{CC} to prevent LSI malfunctions due to noise. These pins must either be pulled up to V_{CC} by their pull-up transistors or by resistors of about 100 kΩ.

Table 19 Circuit Configurations of I/O Pins

I/O Pin Type	Circuit	Applicable Pins
Common I/O pin (with pull-up MOS transistor)		D_0–D_9 $R0_0$–$R0_3$ $R1_0$–$R1_3$ $R2_0$–$R2_3$ $R3_0$–$R3_3$
		$\overline{SCK}$
Output pin (with pull-up MOS transistor)		SO, TIMO
Input pin		$\overline{INT_0}$, $\overline{INT_1}$ SI
		D_{10} D_{11}/VC_{ref}
		$D_{12}/COMP_0$ $D_{13}/COMP_1$ (multiplexed with analog inputs)

Note: Refer to table 20, note 3 concerning $R0_2$/SO.

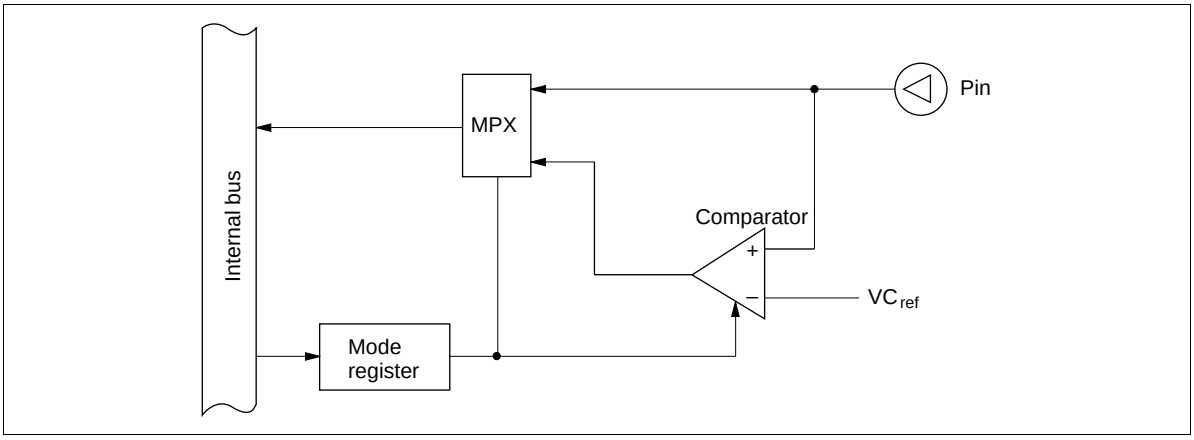
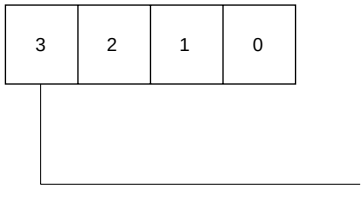


Figure 23 Configuration of D_{12} and D_{13}

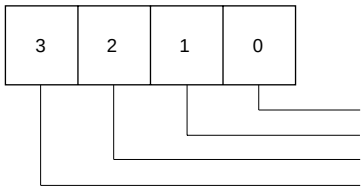
Serial mode register: $005 (SMR)



SMR Bit 3	Port selection
0	$R0_0$
1	$\overline{SCK}$

$R0_0$ /$\overline{SCK}$ pin mode selection

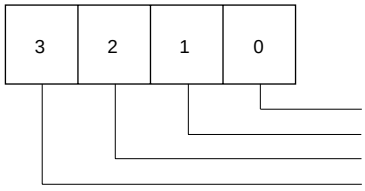
Port mode register A: $004 (PMRA)



$R0_2$ /SO pin mode selection
$R0_1$ /SI pin mode selection
$R3_2$ /$\overline{INT_0}$ pin mode selection
$R3_3$ /$\overline{INT_1}$ pin mode selection

PMRA Bit 3	Port selection	PMRA Bit 2	Port selection	PMRA Bit 1	Port selection	PMRA Bit 0	Port selection
0	$R3_3$	0	$R3_2$	0	$R0_1$	0	$R0_2$
1	$\overline{INT_1}$	1	$\overline{INT_0}$	1	SI	1	SO

Port mode register B: $012 (PMRB)



D_{12} /COMP0 pin mode selection
D_{13} /COMP1 pin mode selection
$R3_1$/TIMO pin mode selection
Pull-up MOS on/off selection

PMRB Bit 3	Pull-up MOS on/off	PMRB Bit 2	Port selection	PMRB Bit 1	Port selection	PMRB Bit 0	Port selection
0	Off	0	$R3_1$	0	D_{13}	0	D_{12}
1	On	1	TIMO	1	$COMP_1$	1	$COMP_0$

Figure 24 I/O Switching Mode Registers

Table 20 Programmable I/O Circuits

PMRB Bit 3 (PMRB3)		0				1			
DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS Buffer	PMOS (A)	—	—	—	On	—	—	—	On
	NMOS (B)	—	—	On	—	—	—	On	—
Pull-up MOS Transistor		—	—	—	—	—	On	—	On

Notes: 1. —: Off

2. Various I/O methods can be selected by different combinations of settings of the above mode registers (PMRB3, DCR, PDR).
3. The PMOS (A) transistor of the $R1_2$/SO pin can be turned off by setting bit 2 of the miscellaneous register (MIS) to 1.

MIS	
Bit 2	**$R0_2$/SO Pin PMOS (A)**
0	On
1	Off

4. The relationships between DCRs and pins are as shown below.

DCR	Bit 3	Bit 2	Bit 1	Bit 0
DCR0	$R0_3$	$R0_2$	$R0_1$	$R0_0$
DCR1	$R1_3$	$R1_2$	$R1_1$	$R1_0$
DCR2	$R2_3$	$R2_2$	$R2_1$	$R2_0$
DCR3	$R3_3$	$R3_2$	$R3_1$	$R3_0$
DCRB	D_3	D_2	D_1	D_0
DCRC	D_7	D_6	D_5	D_4
DCRD	—	—	D_9	D_8

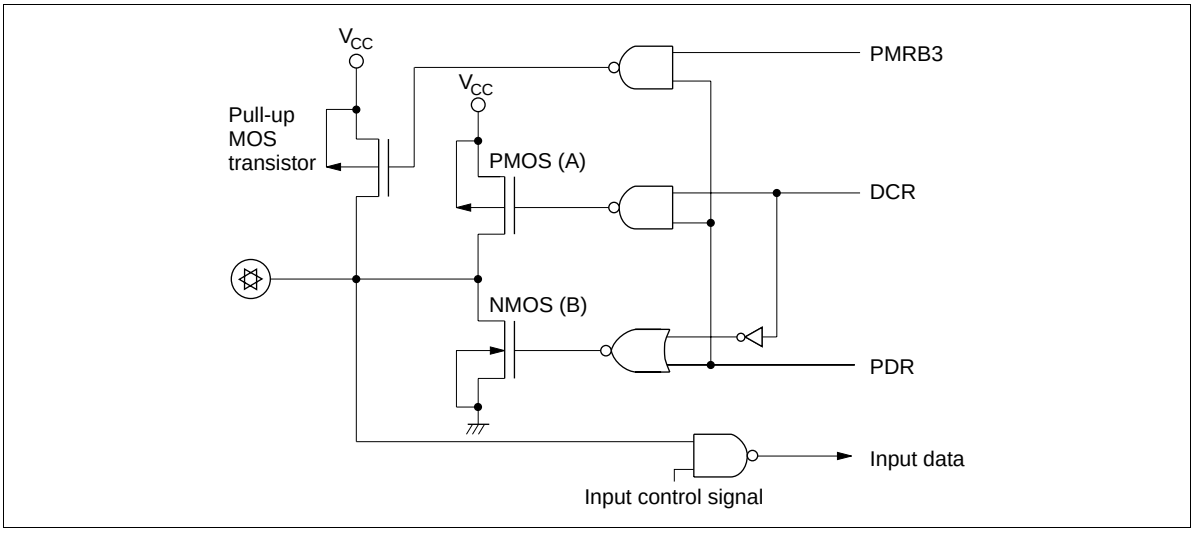


Figure 25 I/O Buffer Configuration

Timers

The MCU has two prescalers (S and W) and three timer/counters (A, B, and C). Figures 26, 27 and 28 show their diagrams.

Prescaler S: Eleven-bit counter that inputs the system clock signal. After being initialized to $000 by MCU reset, prescaler S divides the system clock. Prescaler S keeps counting, except at MCU reset and in the stop and watch modes. Of the prescaler S outputs, timer A input clock, timer B input clock, timer C input clock, and serial interface transmit clock are selected by timer mode register A (TMA), timer mode register B (TMB), timer mode register C (TMC), and the serial mode register (SMR), respectively.

Prescaler W: Five-bit counter that inputs the X1 input clock signal divided by eight. Prescaler W output can be selected as a timer A input clock by timer mode register A (TMA).

Timer A: Eight-bit timer that can be used as a clock time-base (figure 26). It is initialized to $00 and incremented at each clock input. If an input clock is applied to timer A after it has reached $FF, an overflow that sets the timer A interrupt request flag (IFTA: $001, bit 2) is generated, and timer A restarts from $00.

Timer A is used to generate regular interrupts (every 256 clocks) for measuring times between events. It can also be used as a clock time-base when bit 3 of timer mode register A (TMA) is set to 1. The timer is driven by the 32-kHz oscillator clock frequency divided by prescaler W, and the clock input to timer A is controlled by TMA. In this case, prescaler W and timer A can be initialized to $00 by software.

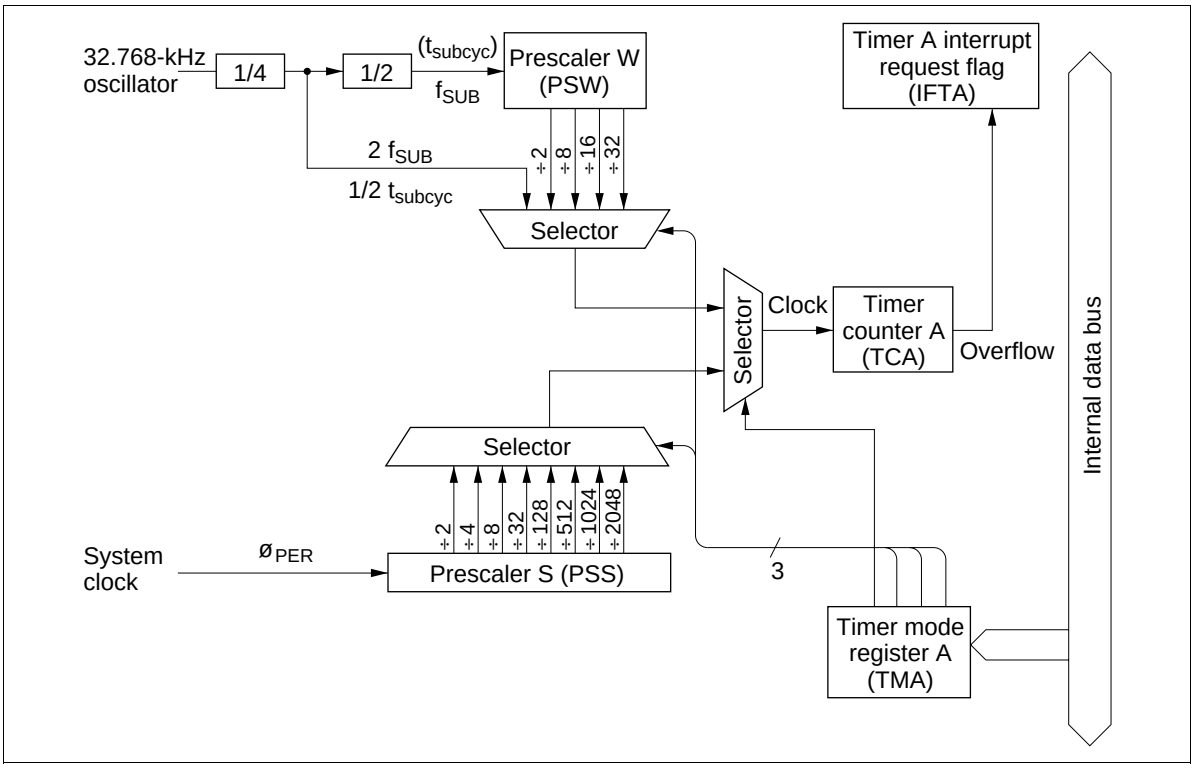


Figure 26 Timer A Block Diagram

Timer B (TCBL and TLRL: $00A, TCBU and TLRU: $00B): Eight-bit write-only timer load register (TLRL and TLRU) and read-only timer counter (TCBL and TCBU) located at the same addresses. The eight-bit configuration consists of lower and upper 4-bit digits located at sequential addresses. A block diagram of timer B is shown in figure 27.

Timer counter B is initialized by writing to timer load register B (TLR). In this case, the lower digit must be written to first. The contents of TLR are loaded into the timer counter at the same time the upper digit is written to, initializing the timer counter. TLR is initialized to $00 by MCU reset.

The count of timer B is obtained by reading timer counter B. In this case, the upper digit must be read first; the count is latched when the upper digit is read.

An auto-reload function, input clock source, and prescaler division ratio of timer B depend on the state of timer mode register B (TMB). When an external event input is used as the input clock source of TMB, the $R3_3/\overline{INT}_1$ pin must be set to $\overline{INT}_1$ by setting port mode register A (PMRA: $004).

Timer B is initialized to the value set in TMB by software, and is then incremented by one each clock input. If an input is applied to timer B after it has reached $FF, an overflow is generated. In this case, if the auto-reload function is enabled, timer B is initialized to its initial value; if auto-reload is disabled, the timer is initialized to $00. The overflow sets the timer B interrupt request flag (IFTB: $002, bit 0).

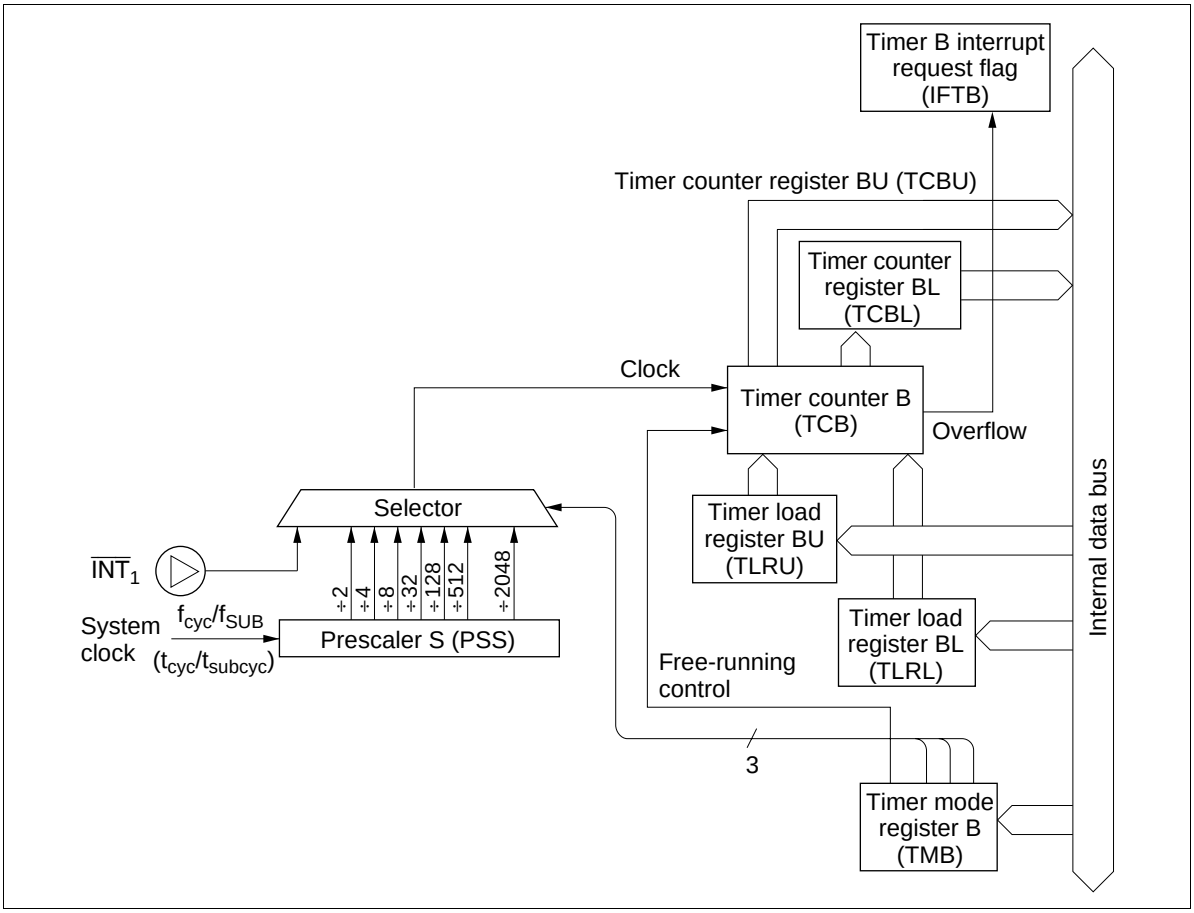


Figure 27 Timer B Block Diagram

Timer C (TCCL and TCRL: $00E, TCCU and TCRU: $00F): Eight-bit write-only timer load register (TCRL and TCRU) and read-only timer counter (TCCL and TCCU) located at the same addresses. The eight-bit configuration consists of lower and upper 4-bit digits located at sequential addresses. The operation of timer C is basically the same as that of timer B.

The auto-reload function and prescaler division ratio of timer C depend on the state of timer mode register C (TMC). Timer C is initialized to the value set in TMC by software, and is then incremented by one at each clock input. If an input is applied to timer C after it has reached $FF, an overflow is generated. In this case, if the auto-reload function is enabled, timer C is initialized to its initial value; if auto-reload is disabled, the timer is initialized to $00. The overflow sets the timer C interrupt request flag (IFTC: $002, bit 2).

Timer C also functions as a watchdog timer. If a program routine runs out of control and an overflow is generated while the watchdog on (WDON) flag is set, the MCU is reset. This error can be detected by having the program control timer C reset before timer C reaches $FF.

The WDON can only have 1 written to it ; it is cleared to 0 only by MCU reset.

Timer Mode Register A (TMA: $008): Four-bit write-only register that controls timer A as shown in table 21.

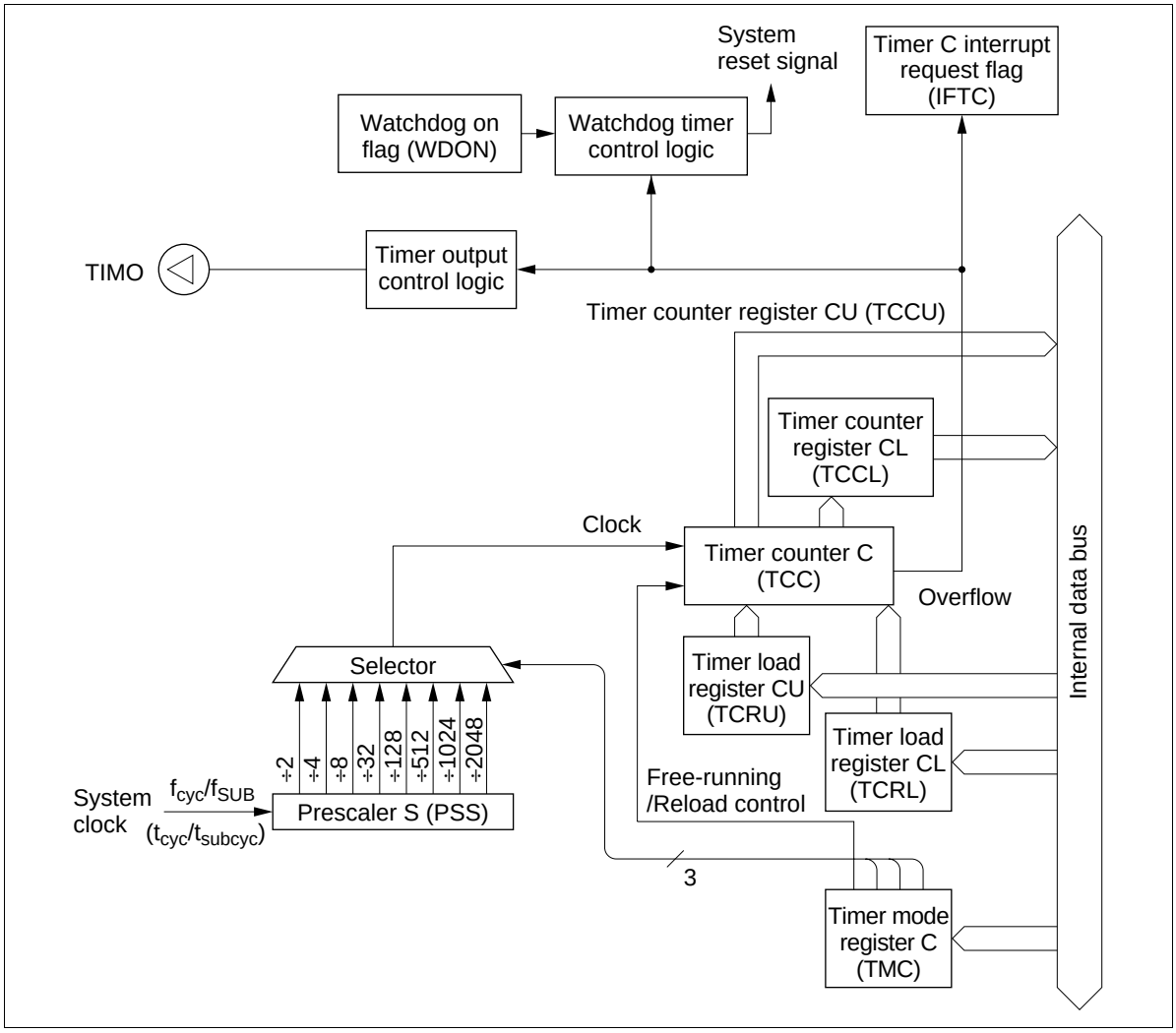


Figure 28 Timer C Block Diagram

Table 21 Timer Mode Register A

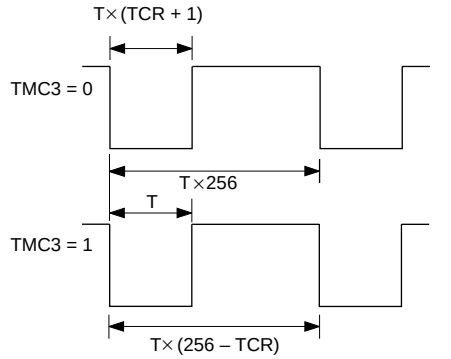
TMA					
Bit 3	**Bit 2**	**Bit 1**	**Bit 0**	**Source Prescaler, Input Clock Period, Operating Mode**	
0	0	0	0	PSS, 2048 t_{cyc}	Timer A mode
			1	PSS, 1024 t_{cyc}	
		1	0	PSS, 512 t_{cyc}	
			1	PSS, 128 t_{cyc}	
	1	0	0	PSS, 32 t_{cyc}	
			1	PSS, 8 t_{cyc}	
		1	0	PSS, 4 t_{cyc}	
			1	PSS, 2 t_{cyc}	
1	0	0	0	PSW, 32 t_{subcyc}	Time-base mode
			1	PSW, 16 t_{subcyc}	
		1	0	PSW, 8 t_{subcyc}	
			1	PSW, 2 t_{subcyc}	
	1	0	0	PSW, 1/2 t_{subcyc}	
			1	Not used	
		1	0	PSW, TCA reset	
			1		

Notes: 1. t_{subcyc} = 244.14 µs (when 32.768-kHz crystal oscillator is used)

2. Timer counter overflow output period(s) = input clock period(s) × 256
3. If PSW or TCA reset is selected while the LCD is operating, LCD operation halts (power switch goes off).

   When LCD is connected for display, the PSW and TCA reset periods must be set in the program to the minimum.
4. In time base mode, the timer counter overflow output cycle must be greater than half of the interrupt frame period (T/2 = t_{RC}).

   If 1/2 t_{subcyc} is selected, t_{RC} must be 7.8125 ms ((MIS1, MIS0) = (0, 1), see figure 14).
5. The division ratio must not be modified during time-base mode operation, otherwise an overflow cycle error will occur.



T: Period of clock input to the counter (table 23)
TCR: Value of timer load register C (0–255)

Note: This waveform is always fixed low when TCR = $FF.

Figure 29 Variable-Duty Pulse Output Waveform

Timer Mode Register B (TMB: $009): Four-bit write-only register that selects the auto-reload function, the prescaler division ratio, and input clock source as shown in table 22. Timer mode register B is initialized to $0 by MCU reset.

Writing to this register is valid from the second instruction execution cycle. Timer B initialization set by writing to TMB must be done after a mode change becomes valid.

Table 22 Timer Mode Register B

TMB	
Bit 3	**Auto-Reload Function**
0	Disabled
1	Enabled

TMB			
Bit 2	**Bit 1**	**Bit 0**	**Prescaler Division Ratio, Clock Input Source**
0	0	0	÷ 2048
0	0	1	÷ 512
0	1	0	÷ 128
0	1	1	÷ 32
1	0	0	÷ 8
1	0	1	÷ 4
1	1	0	÷ 2
1	1	1	$\overline{INT}_1$ (external event input)

Timer Mode Register C (TMC: $00D): Four-bit write-only register that selects the auto-reload function and prescaler division ratio as shown in table 23. Timer mode register C is initialized to $0 by MCU reset.

Writing to this register is valid from the second instruction execution cycle. Timer C initialization set by writing to TMC must be done after a mode change becomes valid.

Table 23 Timer Mode Register C

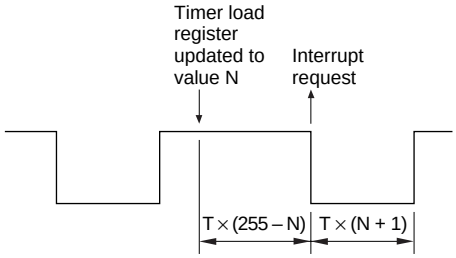
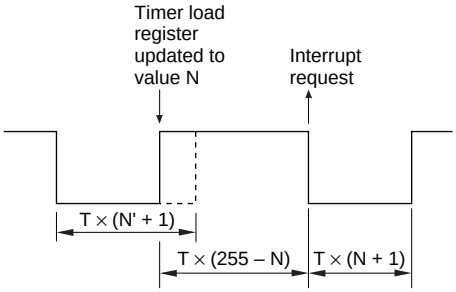
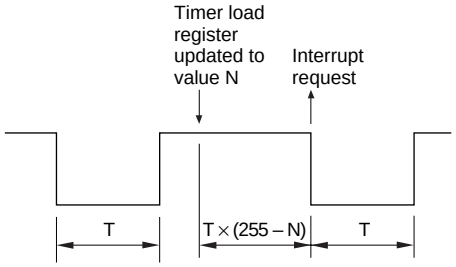
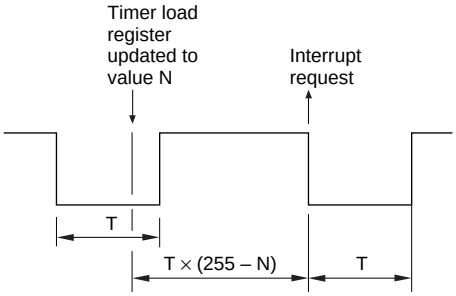
TMC	
Bit 3	**Auto-Reload Function**
0	Disabled
1	Enabled

TMC			
Bit 2	**Bit 1**	**Bit 0**	**Prescaler Division Ratio, Clock Input Source**
0	0	0	÷ 2048
0	0	1	÷ 1024
0	1	0	÷ 512
0	1	1	÷ 128
1	0	0	÷ 32
1	0	1	÷ 8
1	1	0	÷ 4
1	1	1	÷ 2

Note on Use

When using the timer output as PWM output, note the following point. From the update of the timer write register untill the occurrence of the overflow interrupt, the PWM output differs from the period and duty settings, as shown in table 24. The PWM output should therefore not be used until after the overflow interrupt following the update of the timer write register. After the overflow, the PWM output will have the set period and duty cycle.

Table 24 PWM Output Following Update of Timer Write Register

	PWM Output	
Mode	**Timer Load Register is Updated during High PWM Output**	**Timer Load Register is Updated during Low PWM Output**
Free running		
Reload		

Serial Interface

The MCU has a clock-synchronous serial interface which transmits and receives 8-bit data.

The serial interface consists of a serial data register (SR), serial mode register (SMR), port mode register A (PMRA), octal counter, and multiplexers (see figure 30). The $R0_0/\overline{SCK}$ pin and the transmit clock are controlled by writing to the SMR. The transmit clock shifts the contents of the SR, which can be read and written to by software.

The serial interface is activated by the STS instruction. The octal counter is reset to 000 by this instruction, starts counting at the falling edge of the transmit clock ($\overline{SCK}$), and it increments at the rising edge of the clock. A serial interrupt request flag is set when the eighth transmit clock signal is input (the serial interface is reset) or when serial transmission is discontinued (the octal counter is reset).

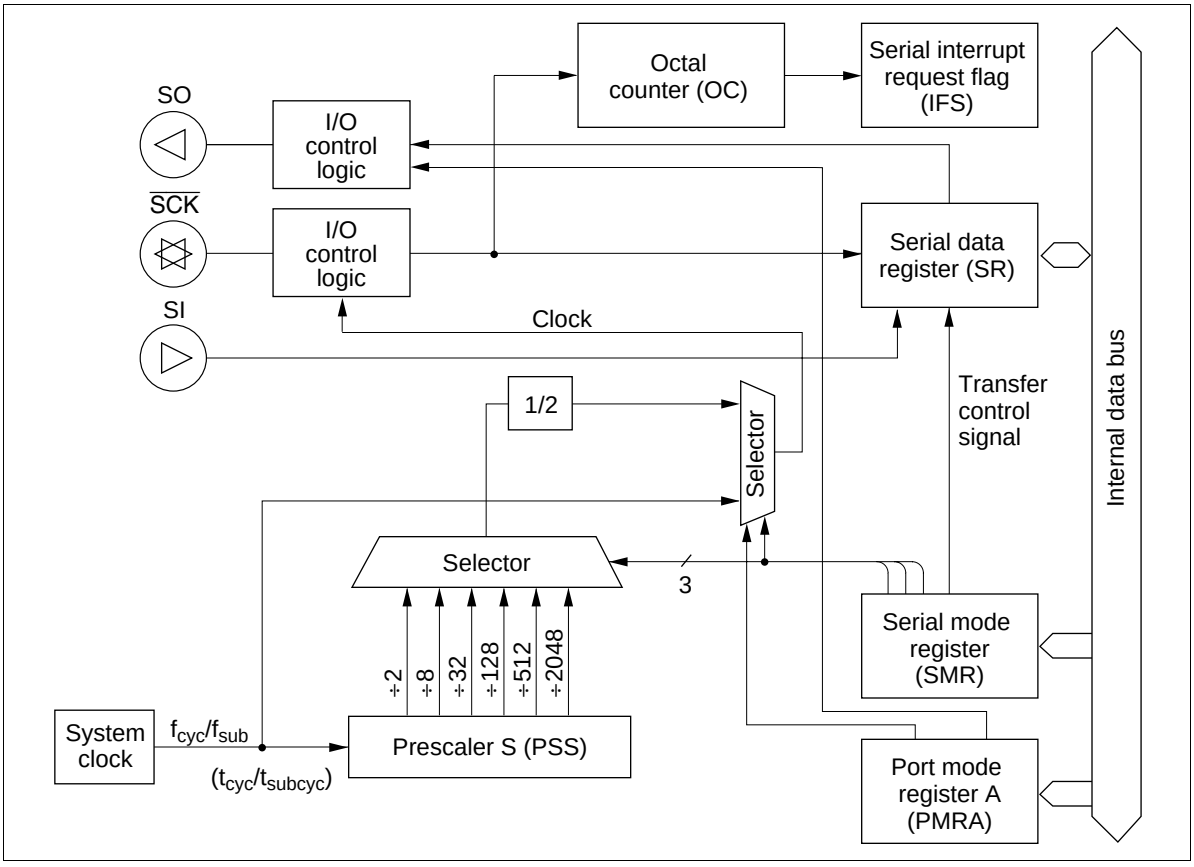


Figure 30 Serial Interface Block Diagram

Serial Mode Register (SMR: $005): Four-bit write-only register that controls the $R0_0/\overline{SCK}$ pin, prescaler division ratio, and transmit clock source (table 25 and figure 31). Writing to this register initializes the serial interface.

A write signal input to the serial mode register discontinues the input of the transmit clock to the serial data register and octal counter. Therefore, if a write is performed during data transmission, the octal counter is reset to 000 to stop transmission, and at the same time, the serial interrupt request flag is set.

Write operations are valid from the second instruction execution cycle, so the STS instruction must be executed after at least two cycles have been executed. The serial mode register is initialized to $0 by MCU reset.

Table 25 Serial Mode Register

SMR	
Bit 3	**$R0_0$/$\overline{SCK}$ Pin**
0	$R0_0$ port input/output pin
1	$\overline{SCK}$ input/output pin

SMR			Transmit Clock			
Bit 2	**Bit 1**	**Bit 0**	**$R0_0$/$\overline{SCK}$ Pin**	**Clock Source**	**Prescaler Division Ratio**	**System Clock Division Ratio**
0	0	0	$\overline{SCK}$ output	Prescaler	÷ 2048	÷ 4096
0	0	1	$\overline{SCK}$ output	Prescaler	÷ 512	÷ 1024
0	1	0	$\overline{SCK}$ output	Prescaler	÷ 128	÷ 256
0	1	1	$\overline{SCK}$ output	Prescaler	÷ 32	÷ 64
1	0	0	$\overline{SCK}$ output	Prescaler	÷ 8	÷ 16
1	0	1	$\overline{SCK}$ output	Prescaler	÷ 2	÷ 4
1	1	0	$\overline{SCK}$ output	System clock	—	÷ 1
1	1	1	$\overline{SCK}$ input	External clock	—	—

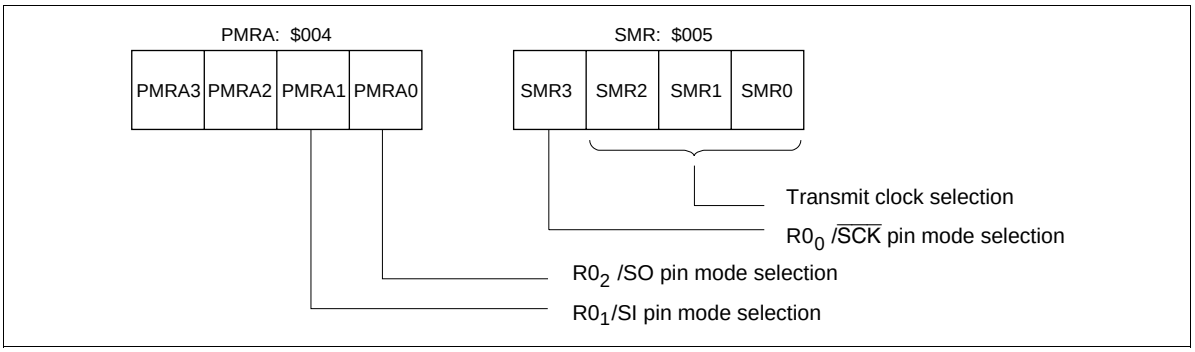


Figure 31 Configurations and Functions of the Mode Registers

Serial Data Register (SRL: $006, SRU: $007): Eight-bit read/write register separated into upper and lower digits located at sequential addresses.

Data in this register is output from the SO pin, LSB first, in synchronism with the falling edge of the transmit clock, and data is input LSB first through the SI pin at the rising edge of the transmit clock. Input/output timing is shown in figure 32.

Data cannot be read or written during serial data transmission. If a read/write occurs during transmission, the accuracy of the resultant data cannot be guaranteed.

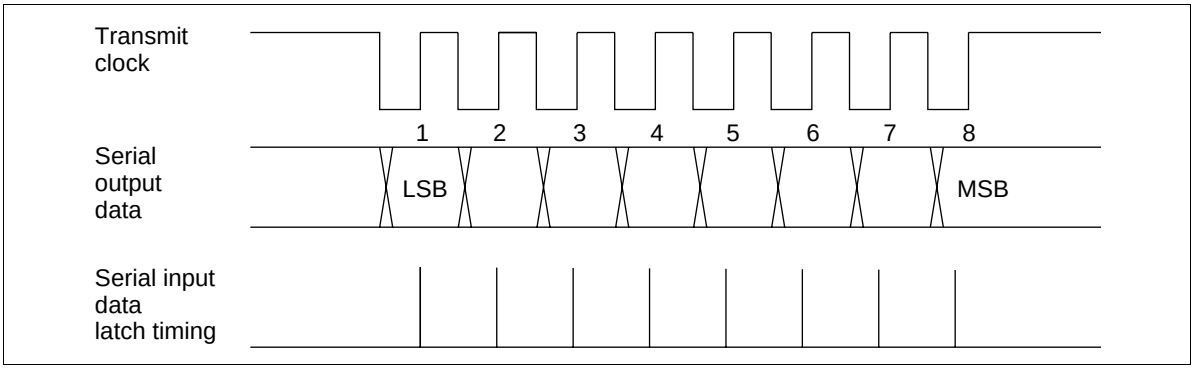


Figure 32 Serial Interface Timing

Selecting and Changing Operating Mode: Table 26 lists the serial interface operating modes. To select an operating mode, use one of these combinations of PMR and SMR settings; to change the operating mode, always initialize the serial interface internally by writing to the SMR.

Table 26 Serial Interface Operating Modes

SMR	PMRA		
Bit 3	**Bit 1**	**Bit 0**	**Operating Mode**
1	0	0	Continuous clock output mode
1	0	1	Transmit mode
1	1	0	Receive mode
1	1	1	Transmit/receive mode

Serial Interface Operation: Three operating modes are provided for the serial interface; transitions between them are shown in figure 33.

In STS waiting state, the serial interface is initialized and the transmit clock is ignored. If the STS instruction is then executed, the serial interface enters transmit clock wait state.

In transmit clock wait state, input of the transmit clock increments the octal counter, shifts the serial clock register, and activates serial transmission. However, note that if clock output mode is selected, the transmit clock is continuously output but data is not transmitted.

During transmission, the input of eight clocks or the execution of the STS instruction sets the octal counter to 000, and the serial interface enters transmit clock wait state. If the state changes from transmit to another state, the serial interrupt request flag is set by the octal counter reaching 000.

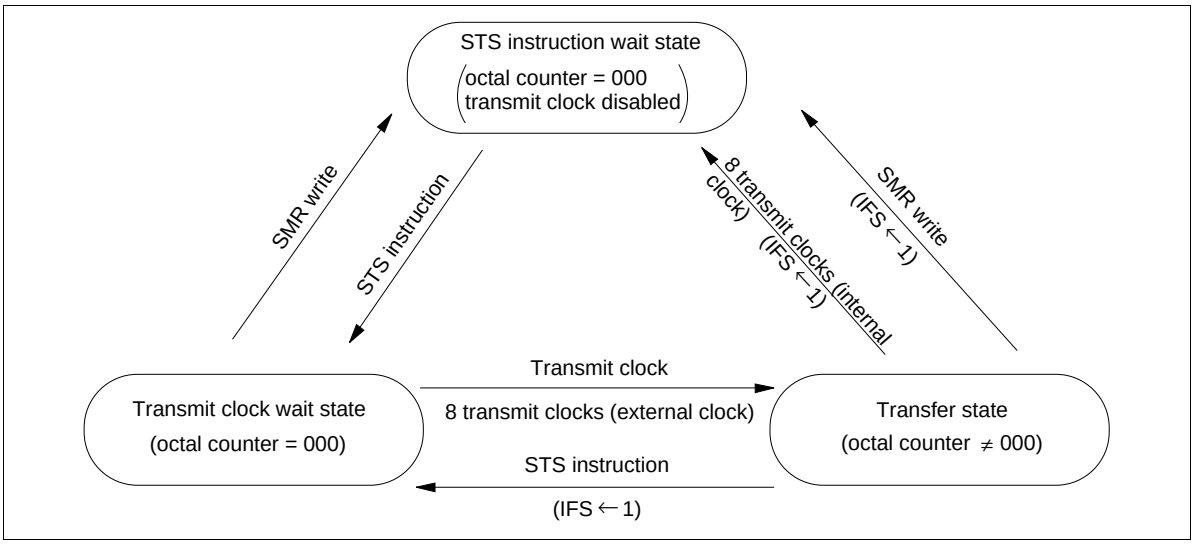


Figure 33 Serial Interface Mode Transitions

In this state, if the internal clock has been selected, the transmit clock is output in answer to the execution of the STS instruction, but serial transmission is inhibited after the eighth clock is output.

If port mode register A (PMRA) is written to in transmit clock wait state or during transmission, the serial mode register (SMR) must be written to, to initialize the serial interface. The serial interface then enters STS wait state.

If the serial interface shifts from transfer state to another state, the octal counter returns to 000, setting the serial interrupt request flag.

Transmit Clock Error Detection: The serial interface will malfunction if a spurious pulse caused by external noise conflicts with a normal transmit clock during transmission. A transmit clock error of this type can be detected as shown in figure 34.

If more than eight transmit clocks are input in transmit clock wait state, the serial interface state changes to transfer, transmit clock wait, then back to transfer.

If the serial interface is set to STS wait state by writing data to the SMR after the serial interrupt request flag has been reset, the flag is set again.

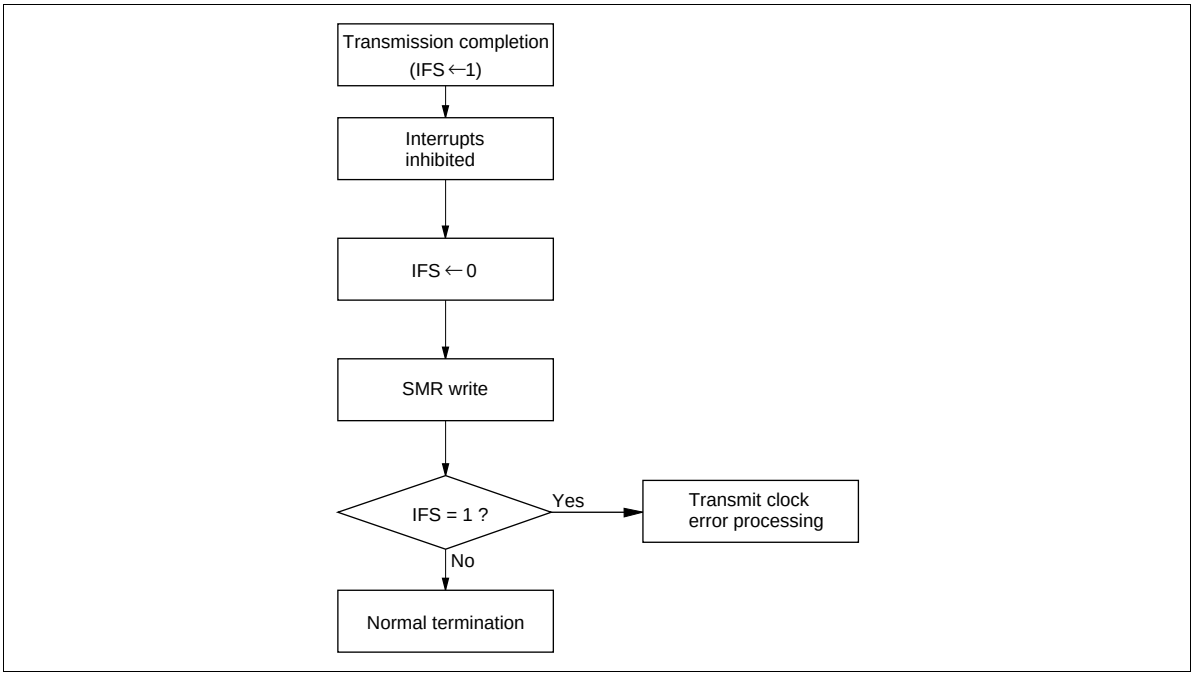


Figure 34 Transmit Clock Error Detection

Note on Use: The serial interrupt request flag might not be set if the status is changed from transfer by the execution of an SMR write or STS instruction during the first period that the transmit clock is low. To prevent this, program a check that the SCK pin is at 1 (by executing an input instruction for the R1 port) before the execution of an SMR write or STS instruction, to ensure that the serial interrupt request flag is set.

Liquid Crystal Display (LCD)

The MCU has an LCD controller and driver which drive 4 common signal pins and 32 segment signal pins. The controller consists of a RAM area in which display data is stored, a display control register (LCR), and a duty/clock control register (LMR), as shown in figure 37.

Four duties and the LCD clock are program-controllable, and a built-in dual-port RAM ensures that display data can be automatically transmitted to the segment signal pins without program intervention. If a 32-kHz oscillation clock is selected as the LCD clock source, the LCD can be used even in watch mode, in which the system clock stops.

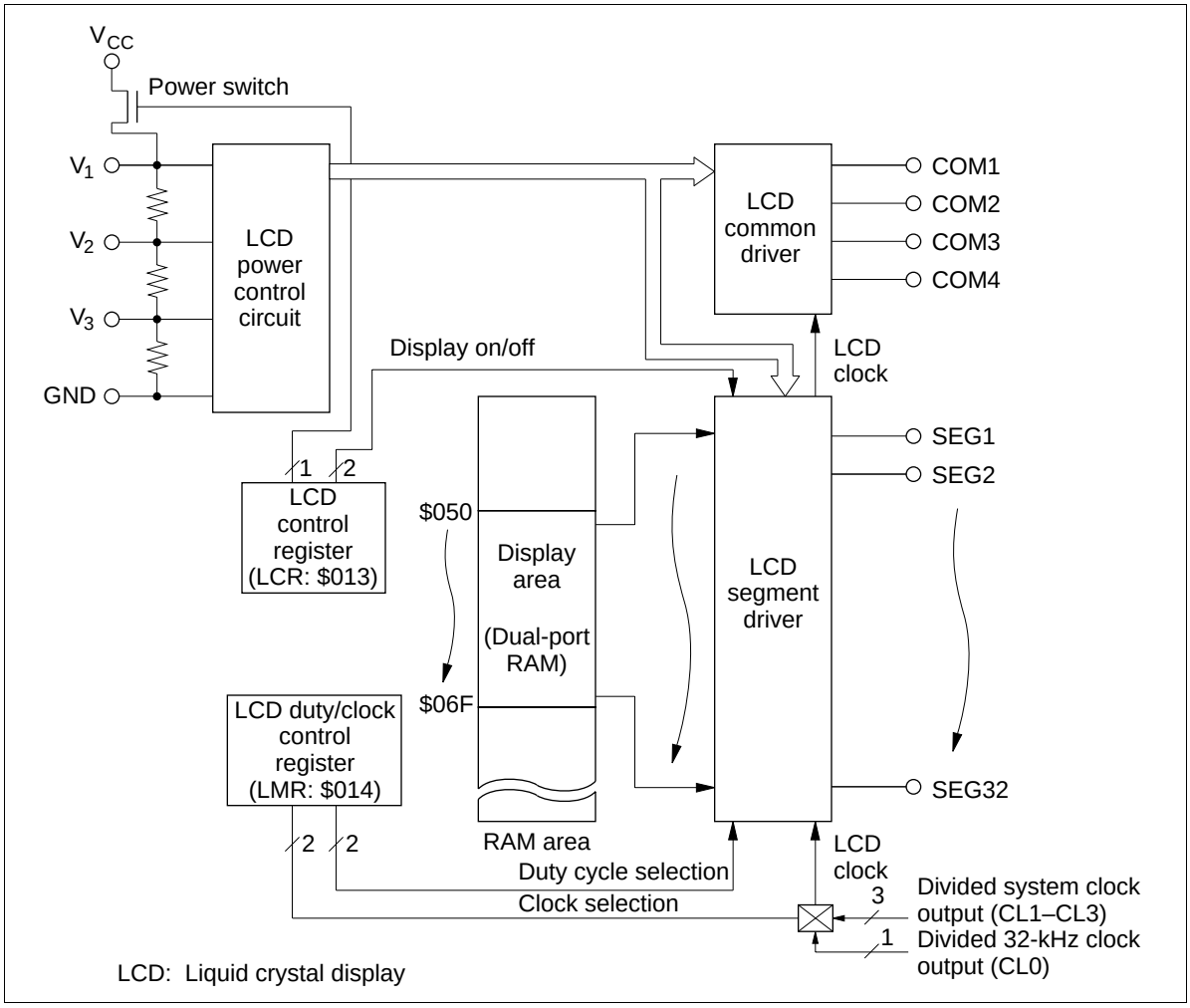


Figure 35 Liquid Crystal Display Block Diagram

LCD Data Area and Segment Data ($050– $06F): Figure 36 shows the configuration of LCD RAM area. Each bit of the storage area corresponds to one of four types of duties. If data is written to an area corresponding to a certain duty cycle, it is automatically output to the corresponding segments as display data.

	Bit 3	Bit 2	Bit 1	Bit 0	
80	SEG1	SEG1	SEG1	SEG1	$050
81	SEG2	SEG2	SEG2	SEG2	$051
82	SEG3	SEG3	SEG3	SEG3	$052
83	SEG4	SEG4	SEG4	SEG4	$053
84	SEG5	SEG5	SEG5	SEG5	$054
85	SEG6	SEG6	SEG6	SEG6	$055
86	SEG7	SEG7	SEG7	SEG7	$056
87	SEG8	SEG8	SEG8	SEG8	$057
88	SEG9	SEG9	SEG9	SEG9	$058
89	SEG10	SEG10	SEG10	SEG10	$059
90	SEG11	SEG11	SEG11	SEG11	$05A
91	SEG12	SEG12	SEG12	SEG12	$05B
92	SEG13	SEG13	SEG13	SEG13	$05C
93	SEG14	SEG14	SEG14	SEG14	$05D
94	SEG15	SEG15	SEG15	SEG15	$05E
95	SEG16	SEG16	SEG16	SEG16	$05F
	COM4	COM3	COM2	COM1	

	Bit 3	Bit 2	Bit 1	Bit 0	
96	SEG17	SEG17	SEG17	SEG17	$060
97	SEG18	SEG18	SEG18	SEG18	$061
98	SEG19	SEG19	SEG19	SEG19	$062
99	SEG20	SEG20	SEG20	SEG20	$063
100	SEG21	SEG21	SEG21	SEG21	$064
101	SEG22	SEG22	SEG22	SEG22	$065
102	SEG23	SEG23	SEG23	SEG23	$066
103	SEG24	SEG24	SEG24	SEG24	$067
104	SEG25	SEG25	SEG25	SEG25	$068
105	SEG26	SEG26	SEG26	SEG26	$069
106	SEG27	SEG27	SEG27	SEG27	$06A
107	SEG28	SEG28	SEG28	SEG28	$06B
108	SEG29	SEG29	SEG29	SEG29	$06C
109	SEG30	SEG30	SEG30	SEG30	$06D
110	SEG31	SEG31	SEG31	SEG31	$06E
111	SEG32	SEG32	SEG32	SEG32	$06F
	COM4	COM3	COM2	COM1	

Figure 36 Configuration of LCD RAM Area

LCD Control Register (LCR: $013): Three-bit write-only register which controls LCD blanking, the turning on and off of the LCD's power supply division resistor, and display in watch and subactive modes (see table 27).

- Blank/display

  Blank: Segment signals are turned off regardless of LCD RAM data setting.

  Display: LCD RAM data is output as segment signals.

- Power switch on/off

  Off: The power switch is off.

  On: The power switch is on and V_1 is V_{CC}.

- Watch/subactive mode display

  Off: In watch and subactive modes, all common and segment pins are grounded and the liquid crystal power switch is turned off.

  On: In watch and subactive modes, LCD RAM data is output as segment signals.

Table 27 LCD Control Register

LCR Bit 2	Display in Watch Mode or Subactive Mode	LCR Bit 1	Power Switch On/Off	LCR Bit 0	Blank/Display
0	Off	0	Off	0	Blank
1	On	1	On	1	Display

Note: When using an LCD in watch mode or subactive mode, use the divided output of a 32-kHz oscillator as the LCD clock and set bit 2 of the LCR to 1. If using the divided output of the system clock as the LCD clock, always set bit 2 of the LCR to 0.

LCD Duty/Clock Control Register (LMR: $014): Four-bit write-only register which selects the display duty and LCD clock source, as shown in table 28.

Table 28 LCD Duty/Clock Control Register

LMR Bit 3	Bit 2	Bit 1	Bit 0	Duty Selection/Input Clock Selection
—	—	0	0	1/4 duty cycle
—	—	0	1	1/3 duty cycle
—	—	1	0	1/2 duty cycle
—	—	1	1	Static
0	0	—	—	CL0 (32.768/64 kHz when using 32.768-kHz oscillator)
0	1	—	—	CL1 (f_{cyc}/256)
1	0	—	—	CL2 (f_{cyc}/2048)
1	1	—	—	CL3 (refer to table 29)

Note: f_{cyc} is the divided system clock output.

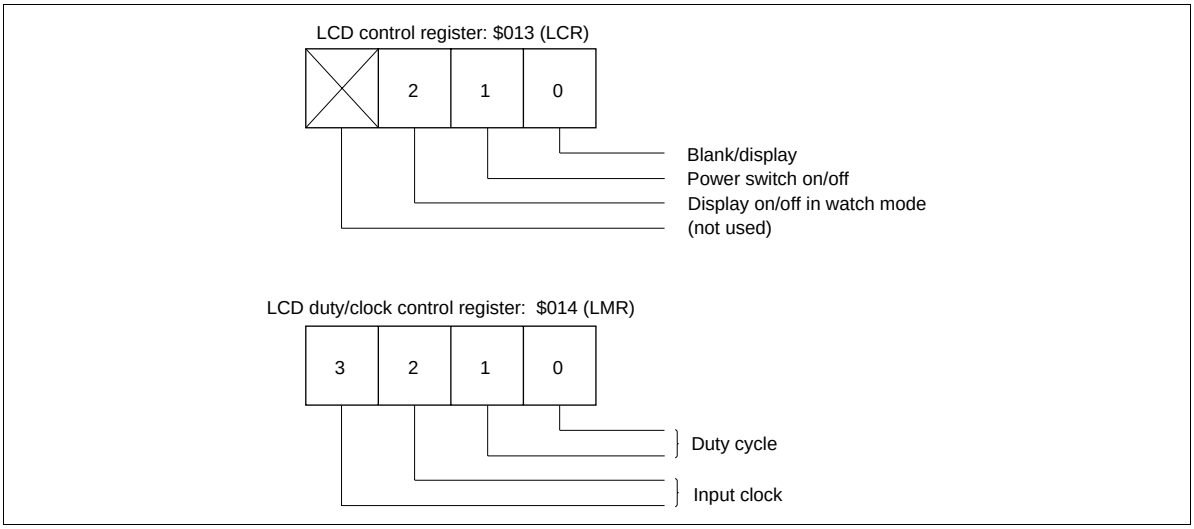


Figure 37 LCD Control and LCD Mode Registers

Table 29 LCD Frame Periods for Different Duties

Static Duty	**LMR**							
Instruction cycle time	**Bit 3 0**	**Bit 2 0**	**Bit 3 0**	**Bit 2 1**	**Bit 3 1**	**Bit 2 0**	**Bit 3 1**	**Bit 2 1**
	CL0		**CL1**		**CL2**		**CL3***	
10 µs	512 Hz		390.6 Hz		48.8 Hz		24.4 Hz/64 Hz	
5 µs	512 Hz		781.2 Hz		97.6 Hz		48.8 Hz/64 Hz	
1/2 Duty	**LMR**							
Instruction cycle time	**Bit 3 0**	**Bit 2 0**	**Bit 3 0**	**Bit 2 1**	**Bit 3 1**	**Bit 2 0**	**Bit 3 1**	**Bit 2 1**
	CL0		**CL1**		**CL2**		**CL3***	
10 µs	256 Hz		195.3 Hz		24.4 Hz		12.2 Hz/32 Hz	
5 µs	256 Hz		390.6 Hz		48.8 Hz		24.4 Hz/32 Hz	
1/3 Duty	**LMR**							
Instruction cycle time	**Bit 3 0**	**Bit 2 0**	**Bit 3 0**	**Bit 2 1**	**Bit 3 1**	**Bit 2 0**	**Bit 3 1**	**Bit 2 1**
	CL0		**CL1**		**CL2**		**CL3***	
10 µs	170.6 Hz		130.2 Hz		16.3 Hz		8.1 Hz/21.3 Hz	
5 µs	170.6 Hz		260.4 Hz		32.6 Hz		16.2 Hz/21.3 Hz	
1/4 Duty	**LMR**							
Instruction cycle time	**Bit 3 0**	**Bit 2 0**	**Bit 3 0**	**Bit 2 1**	**Bit 3 1**	**Bit 2 0**	**Bit 3 1**	**Bit 2 1**
	CL0		**CL1**		**CL2**		**CL3***	
10 µs	128 Hz		97.7 Hz		12.2 Hz		6.1 Hz/16 Hz	
5 µs	128 Hz		195.4 Hz		24.4 Hz		12.2 Hz/16 Hz	

Note: * The division ratio depends on the value of bit 3 of timer mode register A (TMA3): The first value is for TMA3 = 0 and the second is for TMA3 = 1.

When TMA3 = 0, CL3 = $f_{cyc} \times$ duty cycle/4096.

When TMA3 = 1, CL3 = 32.768 kHz $\times$ duty cycle/512

Large Liquid-Crystal Panel Drive and V_{LCD}: To drive a large-capacity LCD, decrease the resistance of the built-in division resistors by attaching external resistors in parallel, as shown in figure 38.

The size of these resistors cannot be simply calculated from the LCD load capacitance because the matrix configuration of the LCD complicates the paths of charge/discharge currents flowing through the capacitors. The resistance will also vary with lighting conditions. This size must be determined by trial and error, taking into account the power dissipation of the device using the LCD, but a resistance of 1 to 10 kΩ would usually be suitable. (Another effective method is to attach capacitors of 0.1 to 0.3 μF.)

Always turn off the power switch (set bit 1 of the LCR to 0) before changing the liquid crystal drive voltage (V_{LCD}).

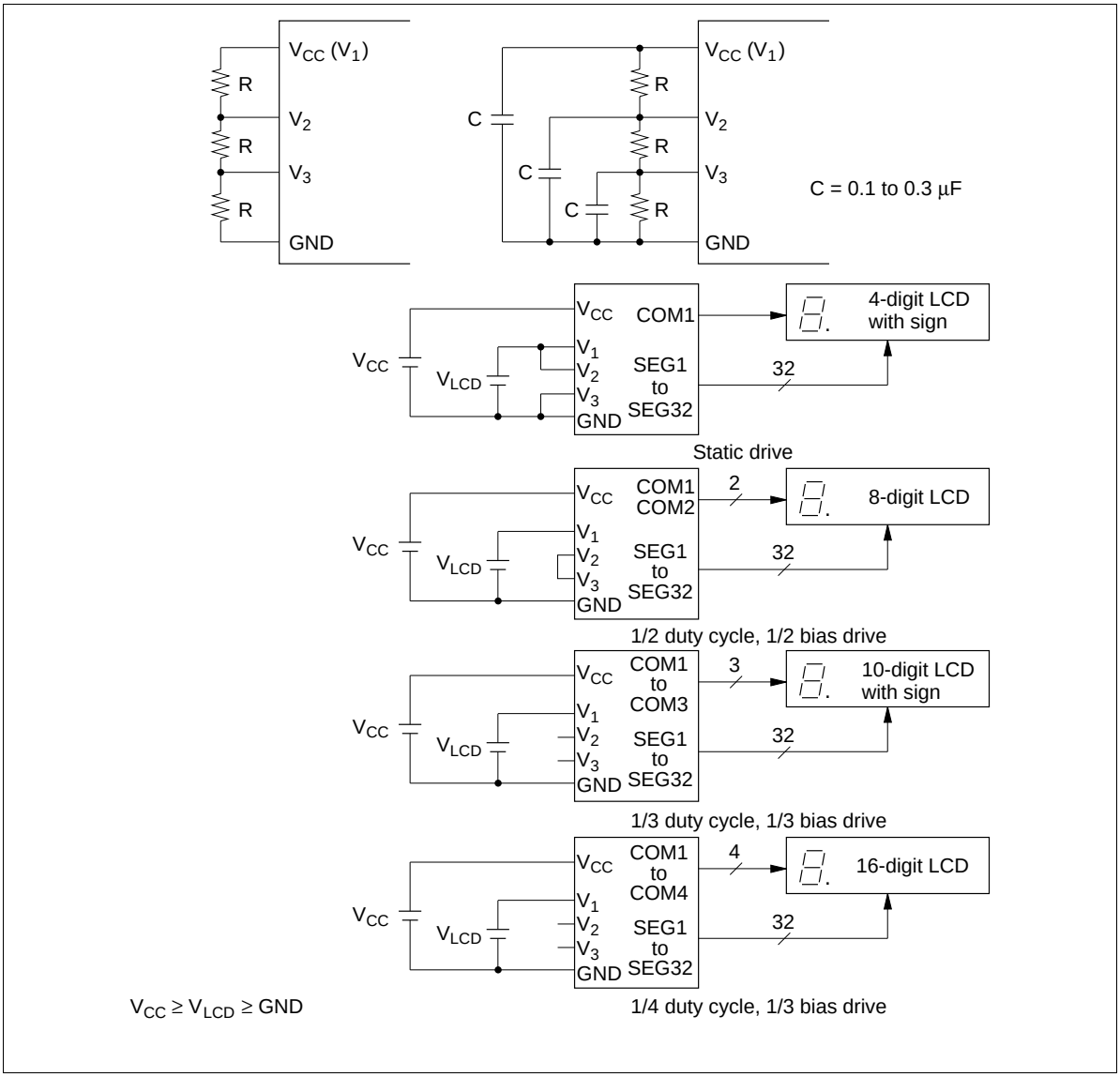


Figure 38 LCD Connection Examples

DTMF Generation Circuit

The MCU has a dual-tone multifrequency (DTMF) generation circuit.

The DTMF signal consists of two sine waves to access the switching system.

Figure 39 shows the DTMF keypad and frequencies. Pressing a key generates a tone corresponding to its frequency. Figure 40 shows a block diagram of the DTMF circuit.

The MCU uses an oscillation frequency reduced to 400 kHz, an eighth of the conventionally used frequency, for low-power consumption. This, however, causes a potential frequency deviation. The MCU provides transformed programmable dividers in addition to sine wave counters and a control register to reduce frequency deviation.

The DTMF generation circuit is controlled by the following three registers.

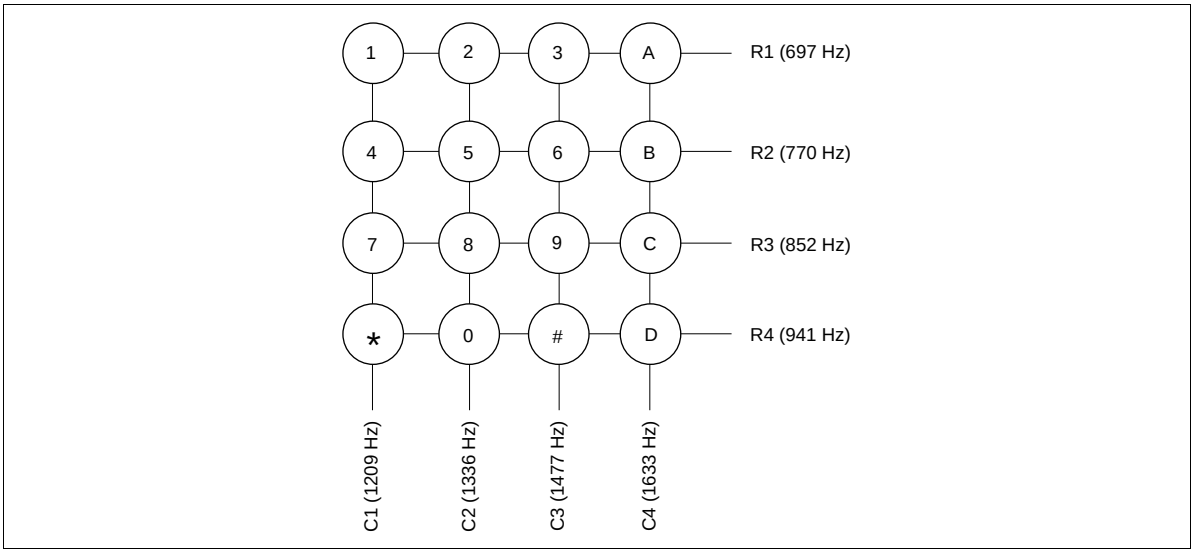


Figure 39 DTMF Keypad and Frequencies

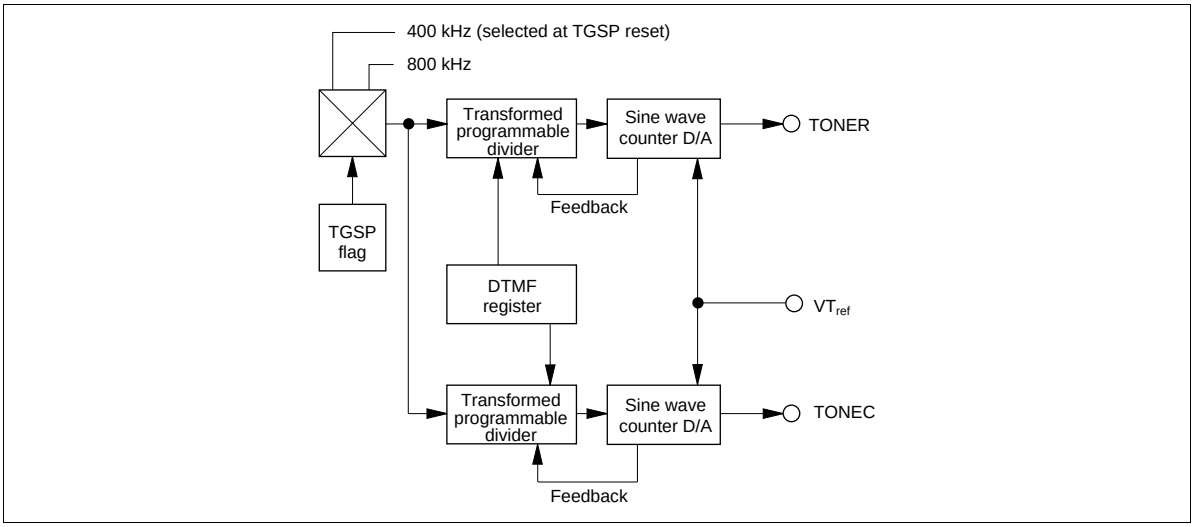


Figure 40 DTMF Circuit Block Diagram

Tone Generator Mode Register (TGM: $010): Four-bit write-only register which controls output frequencies (see table 30). It is cleared to $0 by MCU reset.

Table 30 Tone Generator Mode Register

TGM

Bit 3	Bit 2	Bit 1	Bit 0	Output Frequencies	
Option (TONER output is not affected)		0	0	f_{R1} (697 Hz)	Output through TONER pin
		0	1	f_{R2} (770 Hz)	
		1	0	f_{R3} (852 Hz)	
		1	1	f_{R4} (941 Hz)	
0	0	Option (TONEC output is not affected)		f_{C1} (1,209 Hz)	Output through TONEC pin
0	1			f_{C2} (1,336 Hz)	
1	0			f_{C3} (1,477 Hz)	
1	1			f_{C4} (1,633 Hz)	

Tone Generator Control Register (TGC: $011): Three-bit write-only register which controls the start and stop of DTMF signal output (see table 31). It is cleared to $0 by MCU reset.

Table 31 Tone Generator Control Register

TGC	
Bit 1	**DTMF Enable Bit**
0	DTMF disabled
1	DTMF enabled

TGC	
Bit 2	**TONER Output Control (row)**
0	Stopped
1	TONER output (active)

TGC	
Bit 3	**TONEC Output Control (column)**
0	Stopped
1	TONEC output (active)

Tone Generator Speed Flag (TGSP: $020,Bit 2): One-bit register which can be set and reset by the SEM/REM and SEMD/REMD instructions. The DTMF generation circuit generates output frequencies with a 400-kHz clock (table 30). With an 800-kHz clock, the DTMF generation circuit generates these same frequencies by pulling the TGSP flag high.

DTMF Output: The sine waves of the row-group and column-group are individually converted from digital to analog in the D/A conversion circuit, which provides high-precision ladder resistance. The DTMF output pins, TONER and TONEC, transmit the sine waves of the row-group and column-group, respectively. Figure 41 shows thetone output equivalent circuit. Figure 42 shows the output waveform. One cycle of this wave consists of 32 time slots, making the output waveform stable with little distortion. Table 32 lists the frequency deviation of the MCU from standard DTMF signals.

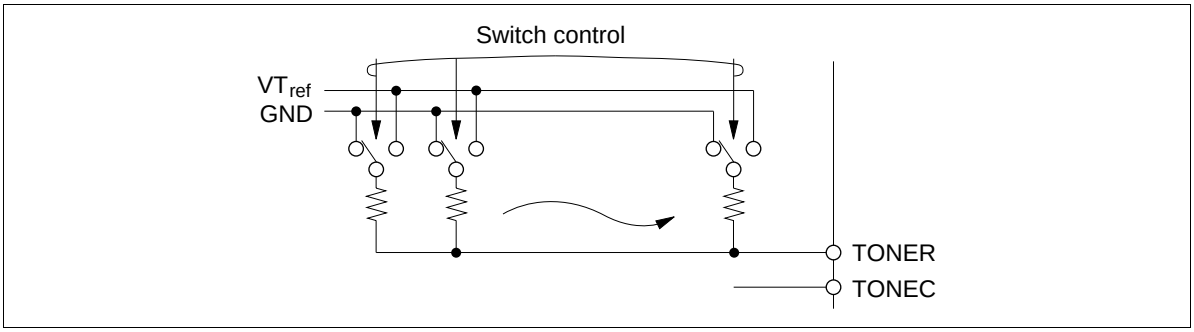


Figure 41 Tone Output Equivalent Circuit

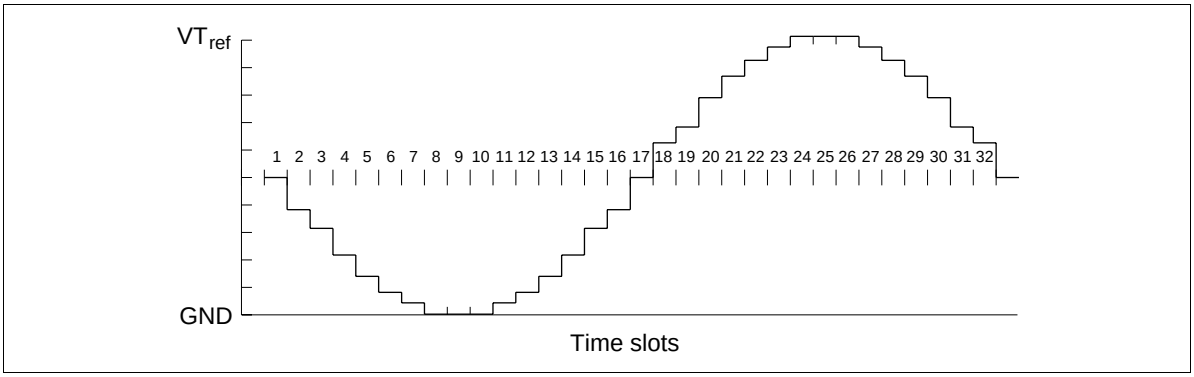


Figure 42 Waveform of Tone Output

Table 32 Frequency Deviation of the MCU from Standard DTMF Signals

Standard	DTMF (Hz)	MCU (Hz)	Deviation from Standard (%)
R1	697	694.44	–0.37
R2	770	769.23	–0.10
R3	852	851.06	–0.11
R4	941	938.97	–0.22
C1	1,209	1,212.12	0.26
C2	1,336	1,333.33	–0.20
C3	1,477	1,481.48	0.30
C4	1,633	1,639.34	0.39

Note: This frequency deviation value does not include the frequency deviation due to the oscillator element. Also note that in this case the ratio of the high level and low level widths in the oscillator waveform due to the oscillator element will be 50% : 50%.

Programmable ROM

The HD4074618 is a ZTAT™ microcomputer with built-in PROM that can be programmed in PROM mode.

PROM Mode Pin Description

Pin Number		MCU Mode		PROM Mode		Pin Number		MCU Mode		PROM Mode	
FP-80B	FP-80A, TFP-80	Pin Name	I/O	Pin Name	I/O	FP-80B	FP-80A, TFP-80	Pin Name	I/O	Pin Name	I/O
1	79	D_2	I/O	O_2	I/O	28	26	$R2_3$	I/O	A_{12}	I
2	80	D_3	I/O	O_3	I/O	29	27	$R3_0$	I/O	A_{13}	I
3	1	D_4	I/O	O_4	I/O	30	28	$R3_1$/TIMO	I/O	A_{14}	I
4	2	D_5	I/O	O_5	I/O	31	29	$R3_2/\overline{INT_0}$	I/O	$\overline{CE}$	I
5	3	D_6	I/O	O_6	I/O	32	30	$R3_3/\overline{INT_1}$	I/O	$\overline{OE}$	I
6	4	D_7	I/O	O_7	I/O	33	31	SEG1	O		
7	5	D_8	I/O			34	32	SEG2	O		
8	6	D_9	I/O			35	33	SEG3	O		
9	7	D_{10}	I	V_{PP}		36	34	SEG4	O		
10	8	D_{11}/VC_{ref}	I	A_9	I	37	35	SEG5	O		
11	9	$D_{12}/COMP_0$	I	$\overline{M0}$	I	38	36	SEG6	O		
12	10	$D_{13}/COMP_1$	I	$\overline{M1}$	I	39	37	SEG7	O		
13	11	$\overline{TEST}$	I	$\overline{TEST}$	I	40	38	SEG8	O		
14	12	X1	I	GND		41	39	SEG9	O		
15	13	X2	O			42	40	SEG10	O		
16	14	GND		GND		43	41	SEG11	O		
17	15	$R0_0/\overline{SCK}$	I/O	A_1	I	44	42	SEG12	O		
18	16	$R0_1$/SI	I/O	A_2	I	45	43	SEG13	O		
19	17	$R0_2$/SO	I/O	A_3	I	46	44	SEG14	O		
20	18	$R0_3$	I/O	A_4	I	47	45	SEG15	O		
21	19	$R1_0$	I/O	A_5	I	48	46	SEG16	O		
22	20	$R1_1$	I/O	A_6	I	49	47	SEG17	O		
23	21	$R1_2$	I/O	A_7	I	50	48	SEG18	O		
24	22	$R1_3$	I/O	A_8	I	51	49	SEG19	O		
25	23	$R2_0$	I/O	A_0	I	52	50	SEG20	O		
26	24	$R2_1$	I/O	A_{10}	I	53	51	SEG21	O		
27	25	$R2_2$	I/O	A_{11}	I	54	52	SEG22	O		

Pin Number		MCU Mode		PROM Mode		Pin Number		MCU Mode		PROM Mode	
FP-80B	FP-80A, TFP-80	Pin Name	I/O	Pin Name	I/O	FP-80B	FP-80A, TFP-80	Pin Name	I/O	Pin Name	I/O
55	53	SEG23	O			68	66	COM4	O		
56	54	SEG24	O			69	67	V_1			
57	55	SEG25	O			70	68	V_2			
58	56	SEG26	O			71	69	V_3		V_{CC}	
59	57	SEG27	O			72	70	TONEC	O		
60	58	SEG28	O			73	71	TONER	O		
61	59	SEG29	O			74	72	VT_{ref}		V_{CC}	
62	60	SEG30	O			75	73	V_{CC}		V_{CC}	
63	61	SEG31	O			76	74	OSC_1	I	V_{CC}	
64	62	SEG32	O			77	75	OSC_2	O		
65	63	COM1	O			78	76	RESET	I	RESET	I
66	64	COM2	O			79	77	D_0	I/O	O_0	I/O
67	65	COM3	O			80	78	D_1	I/O	O_1	I/O

Programming the Built-in PROM

The MCU's built-in PROM is programmed in PROM mode which is set by pulling $\overline{\text{TEST}}$, $\overline{M_0}$, and $\overline{M_1}$ low, and RESET high, as shown in figure 43. In PROM mode, the MCU does not operate, but it can be programmed in the same way as any other commercial 27256 EPROM using a standard PROM programmer and a 80-to-28-pin socket adaptor. Recommended PROM programmers and socket adapters are listed in table 34.

Since an HMCS400-series instruction is ten bits long, the HMCS400-series MCU has a built-in conversion circuit to enable use of a general-purpose PROM programmer. This circuit splits each instruction into a lower 5 bits and an upper 5 bits that are read from or written to consecutive addresse. This means that if, for example, 8 kwords of built-in PROM are to be programmed by a general-purpose PROM programmer, a 16-kbyte address space ($0000–$3FFF) must be specified.

Programming and Verification: The built-in PROM of the MCU can be programmed at high-speed programming sequence without risk of voltage stress or damage to data reliability.

For details of PROM programming, refer to the notes on PROM Programming section.

Warnings

1. Always specify addresses $0000 to $3FFF when programming with a PROM programmer. If address $4000 or higher is accessed, the PROM may not be programmed or verified correctly. Set all data in unused addresses to $FF.

   Note that the plastic-package version cannot be erased and reprogrammed.
2. Make sure that the PROM programmer, socket adapter, and LSI are aligned correctly (their pin 1 positions match), otherwise overcurrents may damage the LSI. Before starting programming, make sure that the LSI is firmly fixed in the socket adapter and the socket adapter is firmly fixed onto the programmer.
3. PROM programmers have two voltages (V_{pp}): 12.5 V and 21 V. Remember that ZTAT™ devices require a V_{PP} of 12.5 V—the 21-V setting will damage them. 12.5 V is the Intel's 27256 setting.

Table 33 PROM Mode Selection

	Pin			
Mode	$\overline{\text{CE}}$	$\overline{\text{OE}}$	V_{PP}	O_0–O_7
Programming	Low	High	V_{PP}	Data input
Verification	High	Low	V_{PP}	Data output
Programming inhibition	High	High	V_{PP}	High impedance

Table 34 Recommended PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapter		
Manufacturer	**Model Name**	**Manufacturer**	**Model Name**	**Package**
DATA I/O Corp.	121B 29B	Hitachi	HS460ESF01H	FP-80B
			HS460ESH01H	FP-80A
			HS461EST01H	TFP-80
AVAL Corp.	PKW-1000	Hitachi	HS460ESF01H	FP-80B
			HS460ESH01H	FP-80A
			HS461EST01H	TFP-80

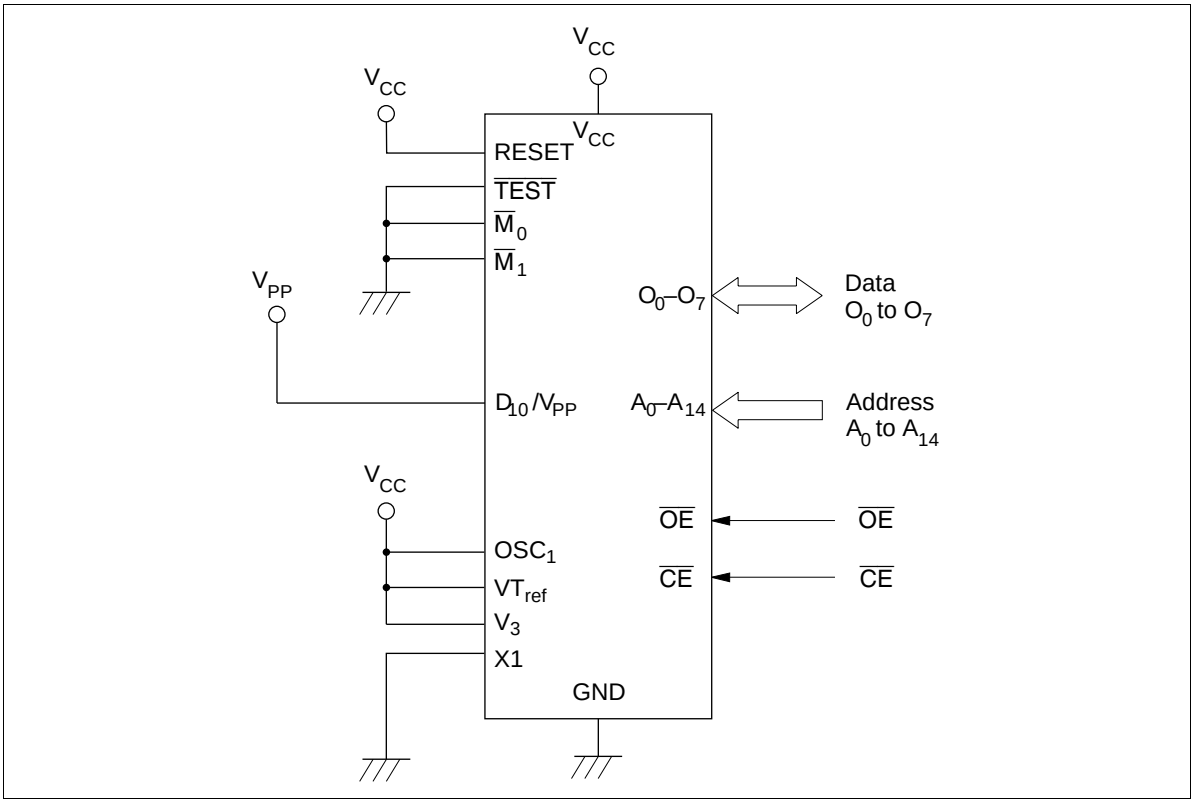


Figure 43 Connections for PROM Mode

Addressing Modes

RAM Addressing Modes

The MCU has three RAM addressing modes, as shown in figure 44 and described below.

Register Indirect Addressing Mode: The contents of the W, X, and Y registers (10 bits in total) are used as a RAM address.

Direct Addressing Mode: A direct addressing instruction consists of two words. The first word contains the opcode, and the contents of the second word (10 bits) are used as a RAM address.

Memory Register Addressing Mode: The memory registers (MR), consisting of 16 digits from $040 to $04F, are accessed with the LAMR and XMRA instructions.

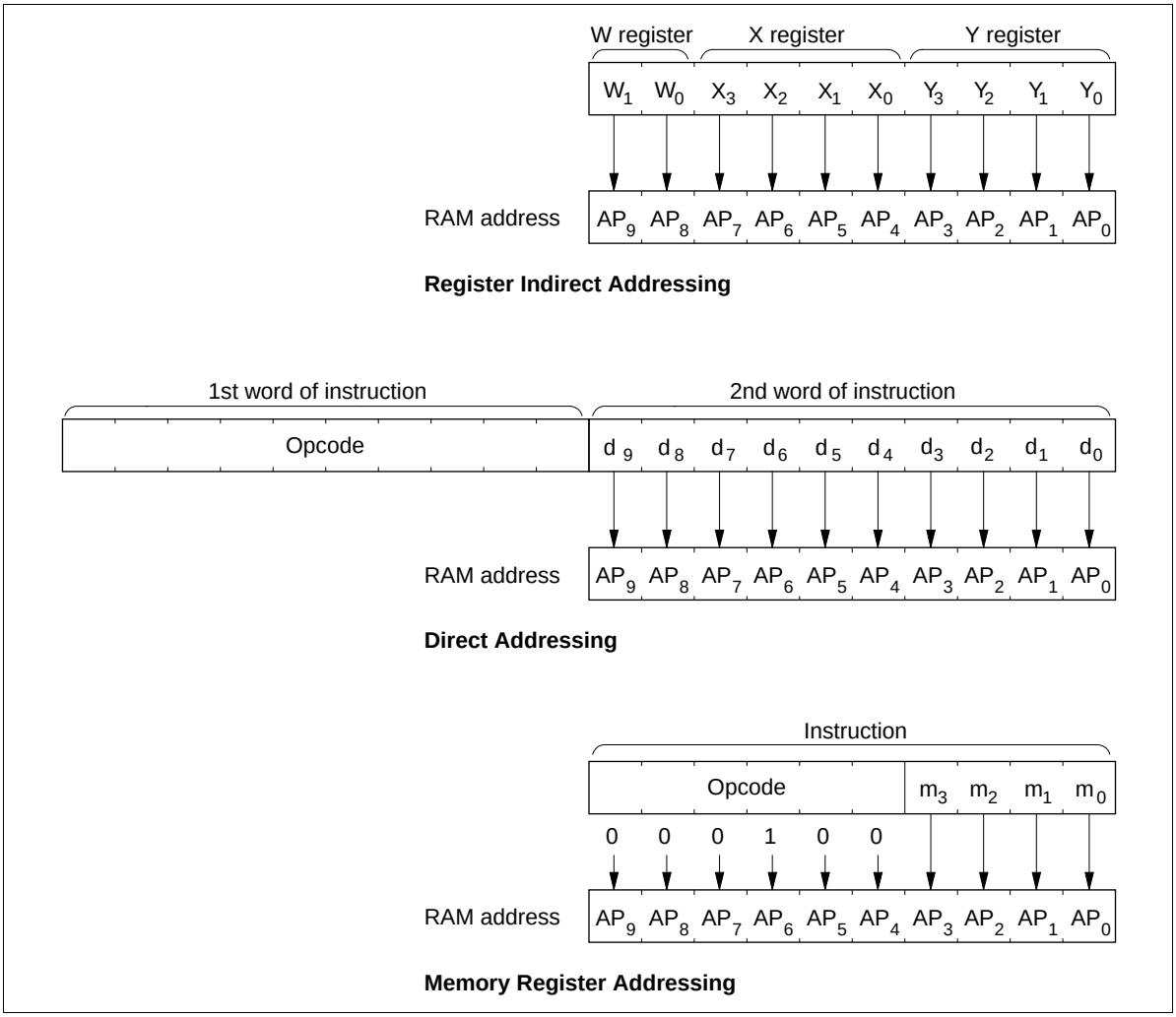


Figure 44 RAM Addressing Modes

ROM Addressing Modes and the P Instruction

The MCU has four ROM addressing modes, as shown in figure 45 and described below.

Direct Addressing Mode: A program can branch to any address in the ROM memory space by executing the JMPL, BRL, or CALL instruction. Each of these instructions replaces the 14 program counter bits (PC_{13}–PC_0) with 14-bit immediate data.

Current Page Addressing Mode: The MCU has 32 pages of ROM with 256 words per page. A program can branch to any address in the current page by executing the BR instruction. This instruction replaces the eight low-order bits of the program counter (PC_7–PC_0) with eight-bit immediate data. If the BR instruction is on a page boundary (address 256n + 255), executing that instruction transfers the PC contents to the next physical page, as shown in figure 46. This means that the execution of the BR instruction on a page boundary will make the program branch to the next page.

Note that the HMCS400-series cross macro-assembler has an automatic paging feature for ROM pages.

Zero-Page Addressing Mode: A program can branch to the zero-page subroutine area located at $000–$003F by executing the CAL instruction. When the CAL instruction is executed, 6 bits of immediate data are placed in the six low-order bits of the program counter (PC_5–PC_0), and 0s are placed in the eight high-order bits (PC_{13}–PC_6).

Table Data Addressing Mode: A program can branch to an address determined by the contents of four-bit immediate data, the accumulator, and the B register by executing the TBR instruction.

P Instruction: ROM data addressed in table data addressing mode can be referenced with the P instruction as shown in figure 47. If bit 8 of the ROM data is 1, eight bits of ROM data are written to the accumulator and the B register. If bit 9 is 1, eight bits of ROM data are written to the R1 and R2 port output registers. If both bits 8 and 9 are 1, ROM data is written to the accumulator and the B register, and also to the R1 and R2 port output registers at the same time.

The P instruction has no effect on the program counter.

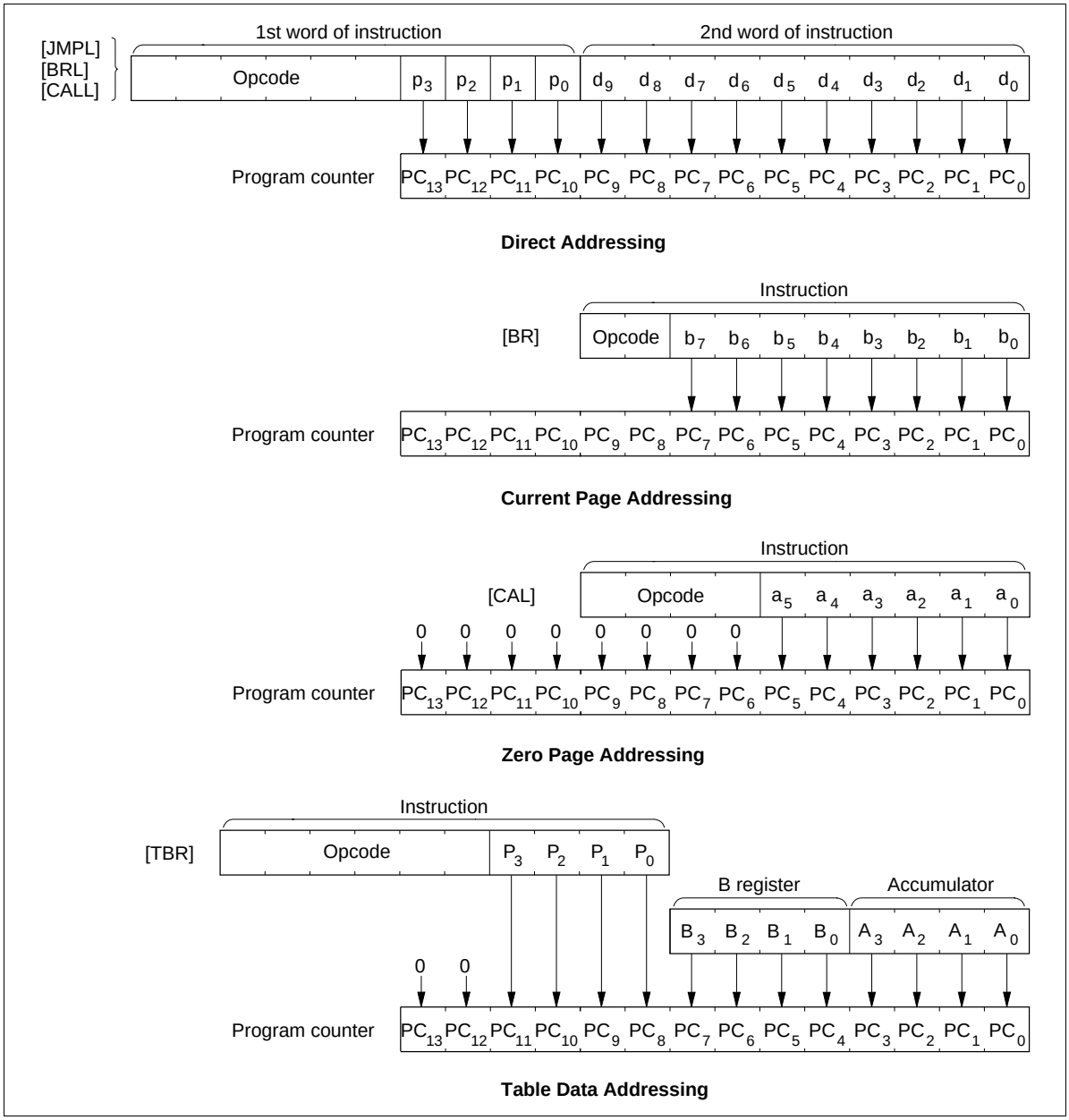


Figure 45 ROM Addressing Modes

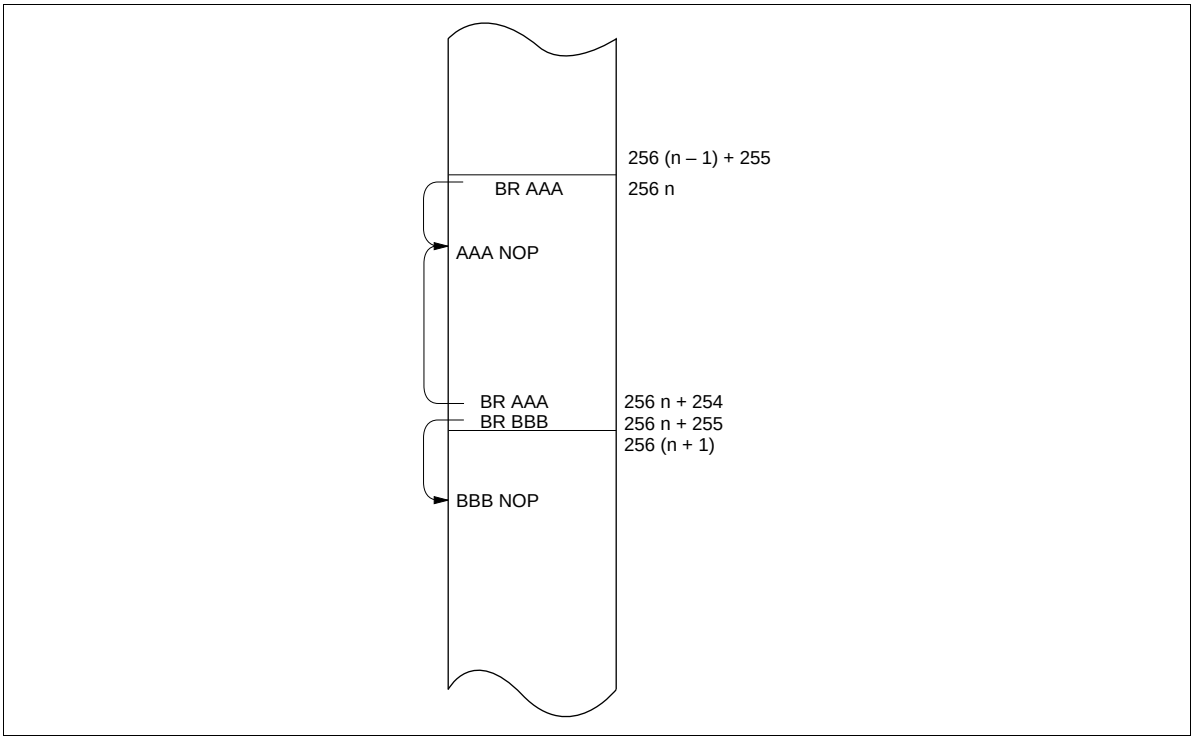


Figure 46 Page Boundary between BR Instruction and Branch Destination

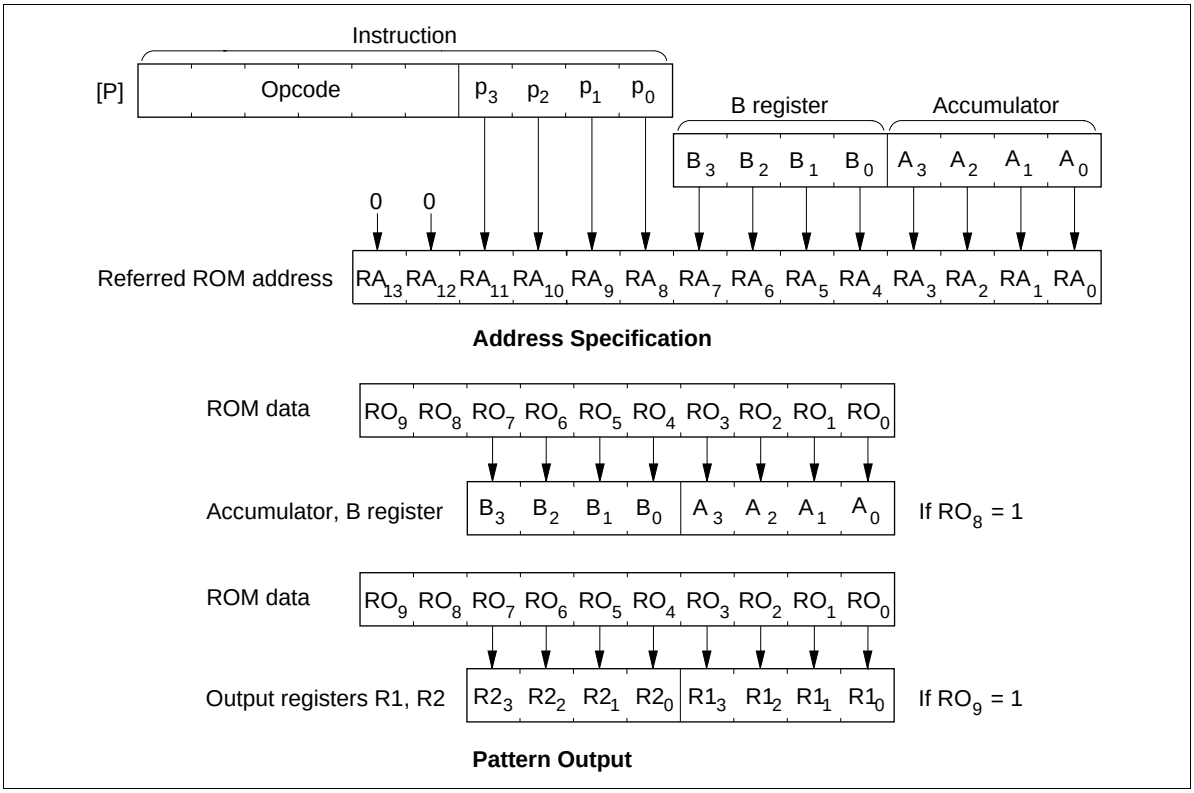


Figure 47 P Instruction

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +7.0	V	
Programming voltage	V_{PP}	–0.3 to +14.0	V	1
Pin voltage	V_T	–0.3 to (V_{CC} + 0.3)	V	
Total permissible input current	$\sum I_O$	100	mA	2
Total permissible output current	$-\sum I_O$	50	mA	3
Maximum input current	I_O	4	mA	4, 5
		30	mA	4, 6
Maximum output current	$-I_O$	4	mA	7, 8
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	

Notes: Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation must be under the conditions stated in the electrical characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.

1. D_{10} (V_{PP}) of the HD4074618.
2. Total permissible input current is the total of input currents simultaneously flowing in from all the I/O pins to GND.
3. Total permissible output current is the total of output currents simultaneously flowing out from V_{CC} to all I/O pins.
4. The maximum input current is the maximum current flowing from any I/O pin to ground.
5. Applies to R0–R3
6. Applies to D_0–D_9
7. The maximum output current is the maximum current flowing from V_{CC} to any I/O pin.
8. Applies to D_0–D_9, R0–R3

Electrical Characteristics (Please inquire about the characteristics of HD404612, HD404614, HD404616, and HD404618 at V_{CC} = 2.2 V)

DC Characteristics (HD404612, HD404614, HD404616, HD404618: V_{CC} = 2.7 V to 6.0 V; HD4074618: V_{CC} = 3.0 V to 5.5 V, GND = 0.0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	RESET, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$	$0.9V_{CC}$		V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.3		V_{CC} + 0.3	V	External clock operation	
		SI	$0.9V_{CC}$		V_{CC} + 0.3	V		
Input low voltage	V_{IL}	RESET, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$	–0.3		$0.1V_{CC}$	V		
		OSC_1	–0.3		0.3	V	External clock operation	
		SI	–0.3		$0.1V_{CC}$	V		
Output high voltage	V_{OH}	$\overline{SCK}$, TIMO, SO	V_{CC} – 1.0			V	$–I_{OH}$ = 0.5 mA	
Output low voltage	V_{OL}	$\overline{SCK}$, TIMO, SO			0.4	V	I_{OL} = 0.4 mA	
I/O leakage current	$\|I_{IL}\|$	RESET, $\overline{SCK}$, $\overline{INT_0}$, $\overline{INT_1}$, SI, SO, TIMO, OSC_1			1	µA	V_{in} = 0 to V_{CC}	1
Stop mode retaining voltage	V_{STOP}	V_{CC}	2			V	No 32-kHz oscillator	7
Current dissipation in active mode	I_{CC1}	V_{CC}		400	1000	µA	V_{CC} = 3 V f_{OSC} = 400 kHz	2
	I_{CC2}	V_{CC}		500	1500	µA	V_{CC} = 3 V DTMF: active f_{OSC} = 400 kHz	3
	I_{CC3}	V_{CC}		1	2	mA	V_{CC} = 3 V f_{OSC} = 400 kHz D_{12}, D_{13} analog input mode	4
Current dissipation in standby mode	I_{SBY}	V_{CC}		200	500	µA	V_{CC} = 3 V LCD on f_{OSC} = 400 kHz	5
Current dissipation in stop mode	I_{STOP}	V_{CC}		1	10	µA	V_{CC} = 3 V No 32-kHz oscillator	

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Current dissipation in subactive mode	I_{SUB}	V_{CC}		50	100	µA	V_{CC} = 3 V LCD on	
				35	70	µA		6
Current dissipation in watch mode (1)	I_{WTC1}	V_{CC}		5	15	µA	V_{CC} = 3 V LCD off	
Current dissipation in watch mode (2)	I_{WTC2}	V_{CC}		15	35	µA	V_{CC} = 3 V LCD on	
Comparator input reference voltage scope	VC_{ref}	VC_{ref}	0	—	V_{CC} – 1.2	V		

Notes: 1. Output buffer current is excluded.

2. I_{CC} is the source current when no I/O current is flowing while the MCU is in reset state.
   Test conditions: MCU: Reset
   Pins: RESET, $\overline{TEST}$ at V_{CC}
3. I_{SBY} is the source current when no I/O current is flowing while the MCU timer is in operation.
   Test conditions: D_{12}, D_{13} in digital input mode
   DTMF in operation (excludes current flowing from VT_{ref} to GND)
4. Pins D_{12} and D_{13} are in analog input mode and I/O current is not flowing.
   Test conditions: VC_{ref}/D_{11}, COMP0/D_{12}, COMP1/D_{13} at GND
   DTMF stopped
5. Timer is in operation and I/O current is not flowing.
   Test conditions: MCU: I/O in reset state
   Serial interface stopped
   D_{12}, D_{13} in digital input mode
   DTMF stopped
   Stanby mode
   Pins : RESET at GND
   $\overline{TEST}$ at V_{CC}
6. Applies only to HD404612, HD404614, HD404616, and HD404618.
7. RAM data retention.

I/O Characteristics for Standard Pins (HD404612, HD404614, HD404616, HD404618: V_{CC} = 2.7 V to 6.0 V; HD4074618: V_{CC} = 3.0 V to 5.5 V, GND = 0.0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Test Conditions	Unit	Notes
Input high voltage	V_{IH}	D_{10}–D_{13}, R0– R3	$0.7V_{CC}$	—	V_{CC} + 0.3		V	
Input low voltage	V_{IL}	D_{10}–D_{13}, R0–R3	–0.3	—	$0.3V_{CC}$		V	
Output high voltage	V_{OH}	R0–R3	V_{CC} – 1.0	—	—	$–I_{OH}$ = 0.5 mA	V	
Pull-up MOS current	$–I_{PU}$	R0–R3	5	40	90	V_{CC} = 3 V, V_{in} = 0 V	µA	
Output low voltage	V_{OL}	R0–R3	—	—	0.4	I_{OL} = 0.4 mA	V	
I/O leakage current	$\|I_{IL}\|$	D_{11} to D_{13}, R0 to R3	—	—	1	HD404612, HD404614 HD404616, HD404618: V_{in} = 0 V to V_{CC}	µA	1
		D_{10}	—	—	20	HD4074618: V_{in} = 0 V to V_{CC}	µA	2
Input high voltage	V_{IHA}	D_{12}, D_{13} (analog compare mode)	VC_{ref}+ 0.1	—	—		V	
Input low voltage	V_{ILA}	D_{12}, D_{13} (analog compare mode)	—	—	VC_{ref} – 0.1		V	

Note: 1. Output buffer current is excluded.
2. The Max value for the HD404618, HD404616, HD404614, and HD404612 is 1µA.

I/O Characteristics for High-Current Pins (HD404612, HD404614, HD404616, HD404618: V_{CC} = 2.7 V to 6.0 V; HD4074618: V_{CC} = 3.0 V to 5.5 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Test Conditions	Unit	Notes
Input high voltage	V_{IH}	D_0–D_9	0.7V_{CC}	—	V_{CC} + 0.3		V	
Input low voltage	V_{IL}	D_0–D_9	–0.3	—	0.3V_{CC}		V	
Output high voltage	V_{OH}	D_0–D_9	V_{CC} – 1.0	—		$-I_{OH}$ = 0.5 mA	V	
Pull-up MOS current	$-I_{PU}$	D_0–D_9	5	40	90	V_{CC} = 3 V, V_{in} = 0 V	µA	
Output low voltage	V_{OL}	D_0–D_9	—	—	2.0	I_{OL} = 15 mA V_{CC} = 4.5 V to 6 V	V	
			—	—	0.4	I_{OL} = 0.4 mA	V	
I/O leakage current	$\|I_{IL}\|$	D_0–D_9	—	—	1	V_{in} = 0 to V_{CC}	µA	1

Note: 1. Output buffer current is excluded.

LCD Circuit Characteristics (HD404612, HD404614, HD404616, HD404618: V_{CC} = 2.7 V to 6.0 V; HD4074618: V_{CC} = 3.0 V to 5.5 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Test Condition	Unit	Notes
Segment driver voltage drop	V_{ds}	SEG1–SEG32	—	—	0.6	I_d = 3 µA	V	1
Common driver voltage drop	V_{dc}	COM1–COM4	—	—	0.3	I_d = 3 µA	V	1
LCD power supply division resistor	R_{Well}		100	300	900	Between V_1 and GND	kΩ	
LCD voltage	V_{LCD}	V_1	2.7	—	V_{CC}	HD404612, HD404614, HD404616, HD404618	V	2
			3.0	—	V_{CC}	HD4074618	V	2

Notes: 1. V_{DS} and V_{DC} are the voltage drops from power supply pins V_1, V_2, and V_3, and GND to each segment pin and each common pin.

2. When V_{LCD} is supplied from an external source, the following relations must be retained:
$V_{CC} \geq V_1 \geq V_2 \geq V_3 \geq$ GND

DTMF Characteristics (HD404612, HD404614, HD404616, HD404618: V_{CC} = 2.7 V to 6.0 V; HD4074618: V_{CC} = 3.0 V to 5.5 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Test Conditions	Unit	Notes
Tone output voltage (1)	V_{OR}	TONER	500	660	—	VT_{ref} – GND = 2.0 V, R_L = 100 kΩ	mV_{rms}	1
Tone output voltage (2)	V_{OC}	TONEC	520	690	—	VT_{ref} – GND = 2.0 V, R_L = 100 kΩ	mV_{rms}	1
Tone output distortion	%DIS		—	3	7	Short circuit between TONER and TONEC, R_L = 100 kΩ	%	2
Tone output ratio	dB_{CR}		—	2.5	—	Short circuit between TONER and TONEC, R_L = 100 kΩ	dB	2

Notes: 1. See figure 48.
2. See figure 49.

AC Characteristics (HD404612, HD404614, HD404616, HD404618: V_{CC} = 2.7 V to 6.0 V; HD4074618: V_{CC} = 3.0 V to 5.5 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Test Condition	Unit	Notes
Clock oscillation frequency	f_{OSC}	OSC_1, OSC_2	—	400	—	1/4 division	kHz	
			—	800	—		kHz	
		X1, X2	—	32.768	—		kHz	
Instruction cycle time	t_{cyc}		—	10	—	f_{OSC} / f_{CP} = 400 kHz	µs	
			—	5	—	f_{OSC} / f_{CP} = 800 kHz	µs	
Oscillator stabilization time	t_{RC}	OSC_1, OSC_2	—	—	7.5	f_{OSC} = 400 kHz	ms	1
			—	—	7.5	f_{OSC} = 800 kHz	ms	1
		X1, X2	—	—	3	T_a = –10 to +60°C	s	2
External clock frequency	f_{CP}	OSC_1	—	400	—		kHz	
			—	800	—		kHz	
External clock high width	t_{CPH}	OSC_1	1100	—	—	f_{CP} = 400 kHz	ns	3
			550	—	—	f_{CP} = 800 kHz	ns	3
External clock low width	t_{CPL}	OSC_1	1100	—	—	f_{CP} = 400 kHz	ns	3
			550	—	—	f_{CP} = 800 kHz	ns	3
External clock rise time	t_{CPr}	OSC_1	—	—	150	f_{CP} = 400 kHz	ns	3
			—	—	75	f_{CP} = 800 kHz	ns	3
External clock fall time	t_{CPf}	OSC_1	—	—	150	f_{CP} = 400 kHz	ns	3
			—	—	75	f_{CP} = 800 kHz	ns	3
$\overline{INT_0}$ high width	t_{IH}	$\overline{INT_0}$	2	—	—		t_{cyc}/ t_{subcyc}	4, 6
$\overline{INT_0}$ low width	t_{IL}	$\overline{INT_0}$	2	—	—		t_{cyc}/ t_{subcyc}	4, 6
$\overline{INT_1}$ high width	t_{IH}	$\overline{INT_1}$	2	—	—		t_{cyc}	4

Item	Symbol	Pin(s)	Min	Typ	Max	Test Condition	Unit	Notes
$\overline{INT_1}$ low width	t_{IL}	$\overline{INT_1}$	2	—	—		t_{cyc}	4
RESET high width	t_{RSTH}	RESET	2	—	—		t_{cyc}	5
Input capacitance	C_{in}	D_{10}	—	—	90	HD4074618: f = 1 MHz, V_{in} = 0 V	pF	8
		All pins except D_{10}	—	—	15	f = 1 MHz, V_{in} = 0 V	pF	
RESET fall time	t_{RSTf}		—	—	20		ms	5
Analog comparator stabilization time	t_{CSTB}	D_{12}, D_{13} (analog input mode)	—	—	2		t_{cyc}	7

Notes:
1. The oscillation stabilization time is the period required for the oscillator to stabilize after V_{CC} reaches 2.7 V (3.0 V for HD4074618) at power-on or after RESET input goes high after stop mode is cancelled. At power-on or when stop mode is cancelled, RESET must remain high for at least t_{RC} to ensure the oscillation stabilization time. Since t_{RC} depends on the ceramic oscillator's circuit constant and stray capacitance, contact the manufacturer when designing a reset circuit.
2. The oscillation stabilization time is the period required for the oscillator to stabilize after V_{CC} reaches 2.7 V (3.0 V for HD4074618) at power-on. The oscillation stabilization time (t_{RC}) must be ensured. If using a crystal oscillator, contact the manufacturer to determine what oscillation stabilization time is required, since it depends on the circuit constants and stray capacitances.
3. See figure 50.
4. See figure 51. The unit t_{cyc} applies when the MCU is in standby mode or active mode.
5. See figure 52.
6. The unit t_{subcyc} applies when the MCU is in watch mode or subactive mode.
   t_{subcyc} = 244.14 μs (32.768-kHz crystal oscillator)
7. The analog comparator stabilization time is the period required for the oscillator to stabilize and for correct data to be read after D_{12}/D_{13} is input to enter analog input mode.
8. The Max value for the HD404618, HD404616, HD404614, and HD404612 is 15pF.

Serial Interface Timing Characteristics (HD404612, HD404614, HD404616, HD404618: V_{CC} = 2.7 V to 6.0 V; HD4074618: V_{CC} = 3.0 V to 5.5 V, GND = 0 V, T_a = –20 to +75°C, unless otherwise specified)

During Transmit Clock Output

Item	Symbol	Pin(s)	Min	Typ	Max	Test Condition	Unit	Notes
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—	Load shown in figure 54	t_{cyc}/t_{subcyc}	1, 3
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.5	—	—	Load shown in figure 54	t_{Scyc}	1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.5	—	—	Load shown in figure 54	t_{Scyc}	1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	200	Load shown in figure 54	ns	1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	200	Load shown in figure 54	ns	1
Serial output data delay time	t_{DSO}	SO	—	—	500	Load shown in figure 54	ns	1
Serial input data setup time	t_{SSI}	SI	300	—	—		ns	1
Serial input data hold time	t_{HSI}	SI	300	—	—		ns	1

During Transmit Clock Input

Item	Symbol	Pin(s)	Min	Typ	Max	Test Condition	Unit	Notes
Transmit clock cycle time	t_{Scyc}	$\overline{SCK}$	1	—	—		t_{cyc}/t_{subcyc}	1, 3
Transmit clock high width	t_{SCKH}	$\overline{SCK}$	0.5	—	—		t_{Scyc}	1
Transmit clock low width	t_{SCKL}	$\overline{SCK}$	0.5	—	—		t_{Scyc}	1
Transmit clock rise time	t_{SCKr}	$\overline{SCK}$	—	—	200		ns	1
Transmit clock fall time	t_{SCKf}	$\overline{SCK}$	—	—	200		ns	1
Serial output data delay time	t_{DSO}	SO	—	—	500	Load shown in figure 54	ns	1
Serial input data setup time	t_{SSI}	SI	300	—	—		ns	1
Serial input data hold time	t_{HSI}	SI	300	—	—		ns	1
Transmit clock completion detect time	t_{SCKHD}	$\overline{SCK}$	1	—	—		t_{cyc}/t_{subcyc}	1, 2, 3

Notes: 1. See figure 53.

2. The transmit clock completion detect time is the high level period after eight transmit clock pulses have been input. The serial interrupt request flag is not set if the next transmit clock is input before the transmit clock completion detect time has passed.
3. The unit t_{subcyc} applies when the MCU is in subactive mode.
   t_{subcyc} = 244.14 µs (32.768-kHz crystal oscillator)

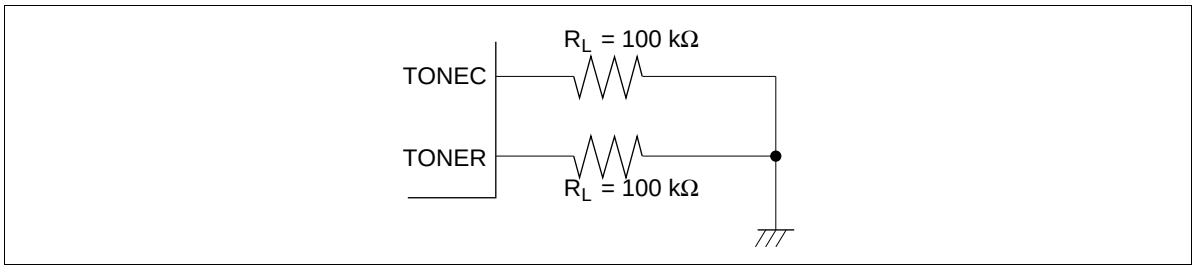


Figure 48 Tone Output Load Circuit

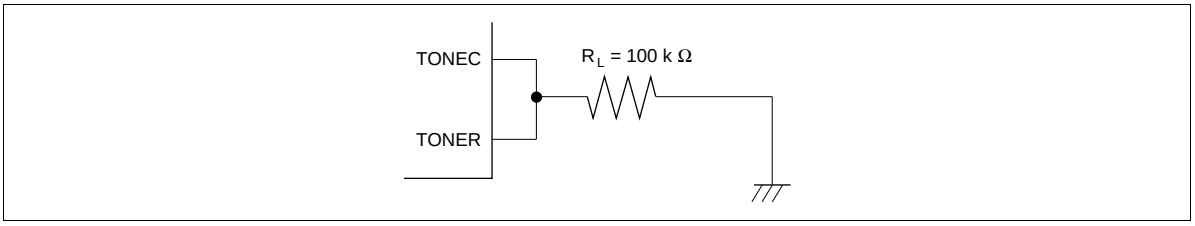


Figure 49 Distortion and dB_{CR} Load Circuit

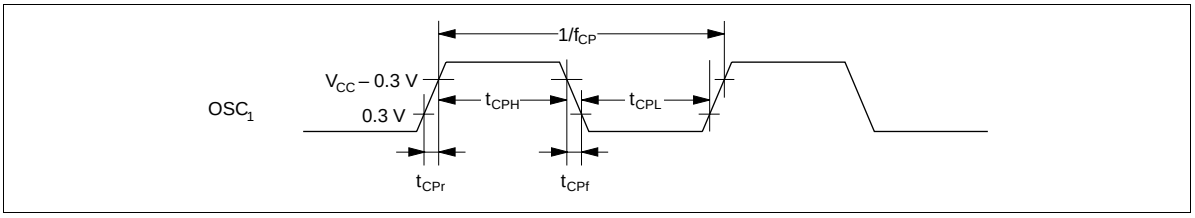


Figure 50 Oscillator Timing

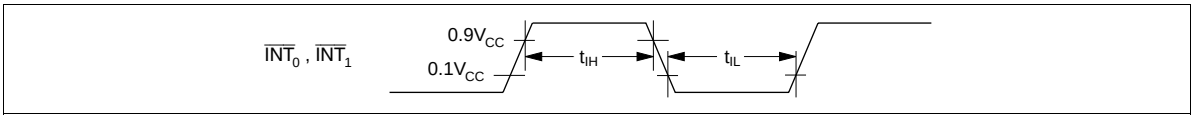


Figure 51 Interrupt Timing

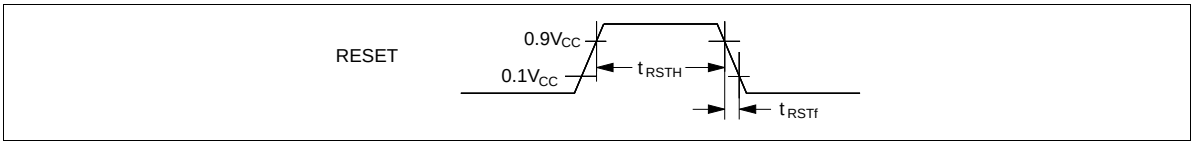
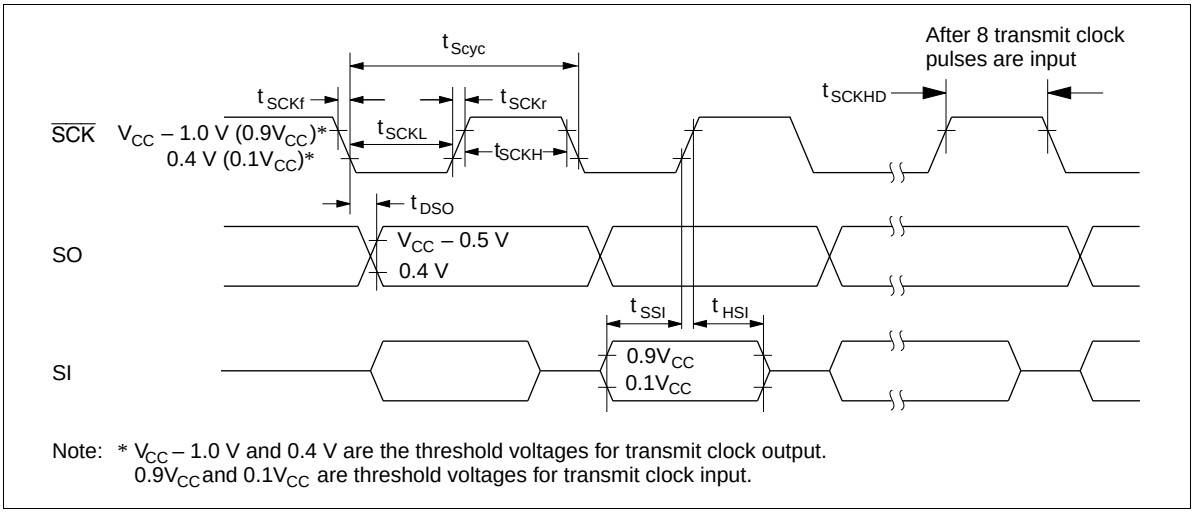


Figure 52 Reset Timing



Note: * V_{CC} – 1.0 V and 0.4 V are the threshold voltages for transmit clock output.
$0.9V_{CC}$ and $0.1V_{CC}$ are threshold voltages for transmit clock input.

Figure 53 Serial Interface Timing

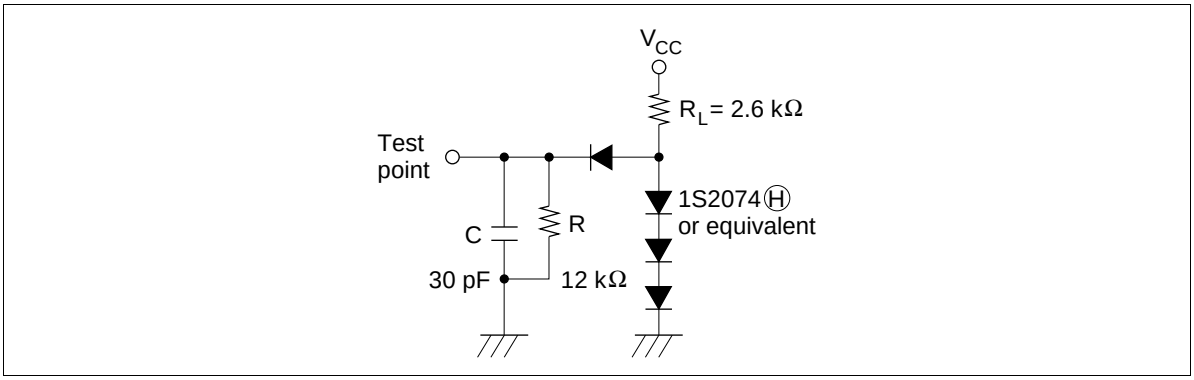


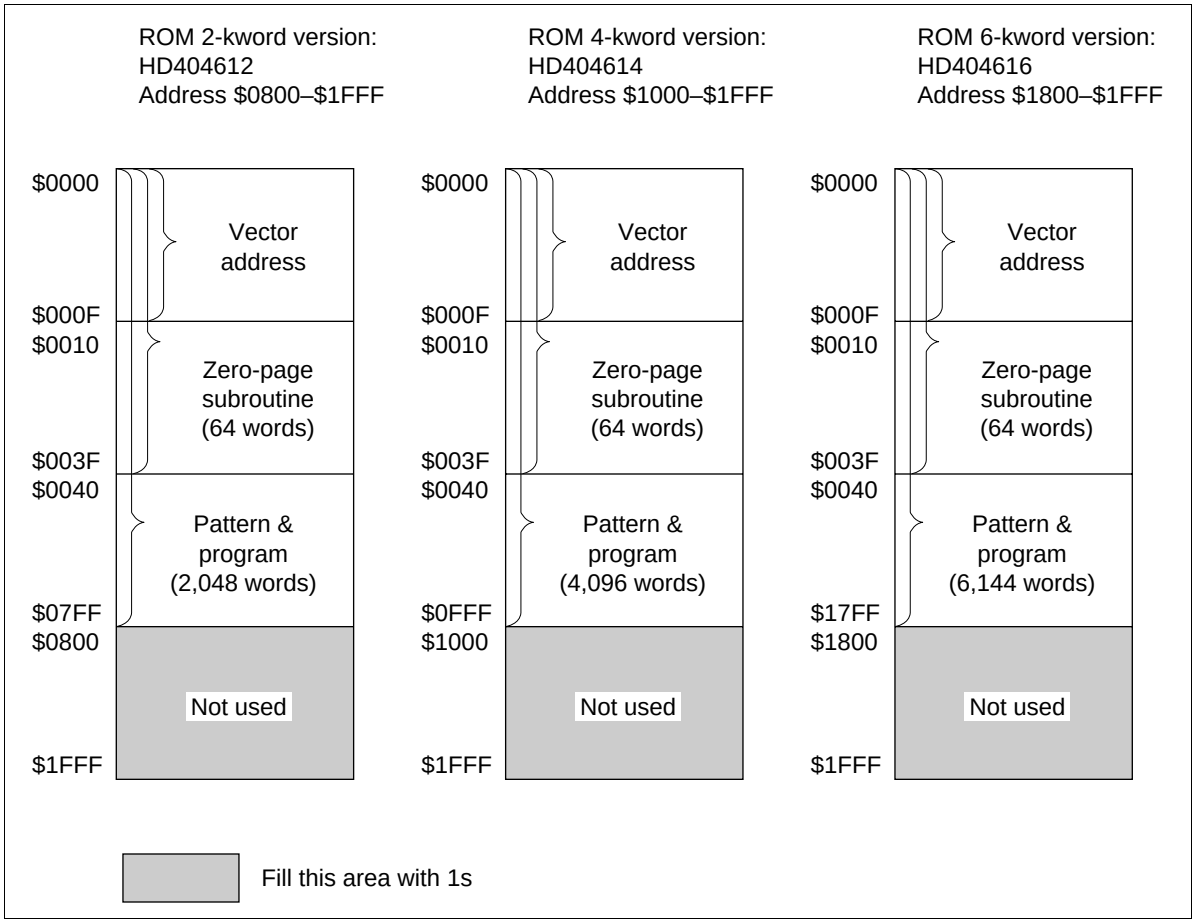
Figure 54 Timing Load Circuit

Notes on ROM Out

Please pay attention to the following items regarding ROM out.

On ROM out, fill the ROM area indicated below with 1s to create the same data size as a 8-kword version (HD404618). An 8-kword data size is required to change ROM data to mask manufac turing data since the program used is for a 8-kword version.

This limitation applies when using an EPROM or a data base.



HD404612, HD404614, HD404616, HD404618 Option List

Please check off the appropriate applications and enter the necessary information.

Date of order	/ /
Customer	
Department	
ROM code name	
LSI number (to be filled in by HITACHI)	

1. ROM Size

☐	HD404612	2-kword
☐	HD404614	4-kword
☐	HD404616	6-kword
☐	HD404618	8-kword

2. Optional Functions

*	☐	With 32-kHz CPU operation, with time-base for clock
*	☐	Without 32-kHz CPU operation, with time-base for clock
	☐	Without 32-kHz CPU operation, without time-base

Note: * Options marked with an asterisk require a subsystem crystal oscillator

5. ROM Code Media

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

☐	EPROM: The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...).
☐	EPROM: The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMS.

6. System oscillator (OSC1 and OSC2)

☐	Ceramic oscillator	f = MHz
☐	External clock	f = MHz

7. Stop Mode

☐	Used
☐	Not used

8. Package

☐	FP-80A
☐	FP-80B
☐	TFP-80

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