REALTEK/AVANCE LOGIC, INC.
TWO CHANNEL AC'97 AUDIO CODEC
ALC202 / ALC202A

1. Features

- Single chip audio CODEC with high S/N ratio (>90 dB)
- Compliant with AC'97 2.2 & WHQL specifications
- Support of S/PDIF out is compliant with AC'97 rev2.2 specifications
- Meets performance requirements for audio on PC2001 systems
- Meets Microsoft PC99 & WLP 2.0 audio requirements
- 18-bit Stereo full-duplex CODEC with independent and variable sampling rate
- 18-bit ADC and 20-bit DAC resolution
- Four analog line-level stereo inputs with 5-bit volume control: LINE_IN, CD, VIDEO, AUX
- High quality differential CD input
- Two analog line-level mono input: PC_BEEP,PHONE_IN
- Supports double sampling rate (96KHz) of DVD audio playback
- Two software selectable MIC inputs
- +30dB boost preamplifier for MIC input
- Stereo output with 6-bit volume control
- Mono output with 5-bit volume control
- Headphone output with 50mW/8Ω driving capability (ALC202)
- Line output with 50mW/8Ω driving capability (ALC202A)
- Headphone jack-detect function to mute LINE/MONO/HP output, and to control S/PDIF output
- 3D Stereo Enhancement
- Multiple CODEC extension capability
- External Amplifier Power Down (EAPD) capability
- High performance converter technology
- Power management and enhanced power saving features
- 2 GPIO pins
- No external crystal/clock required
- 14.318MHz→24.576MHz PLL saves crystal
- DC Voltage volume control
- Auxiliary power (VAUX) to support Power Off CD function
- Power support: Digital: 3.3V; Analog: 3.3V/5V
- Standard 48-Pin LQFP Package

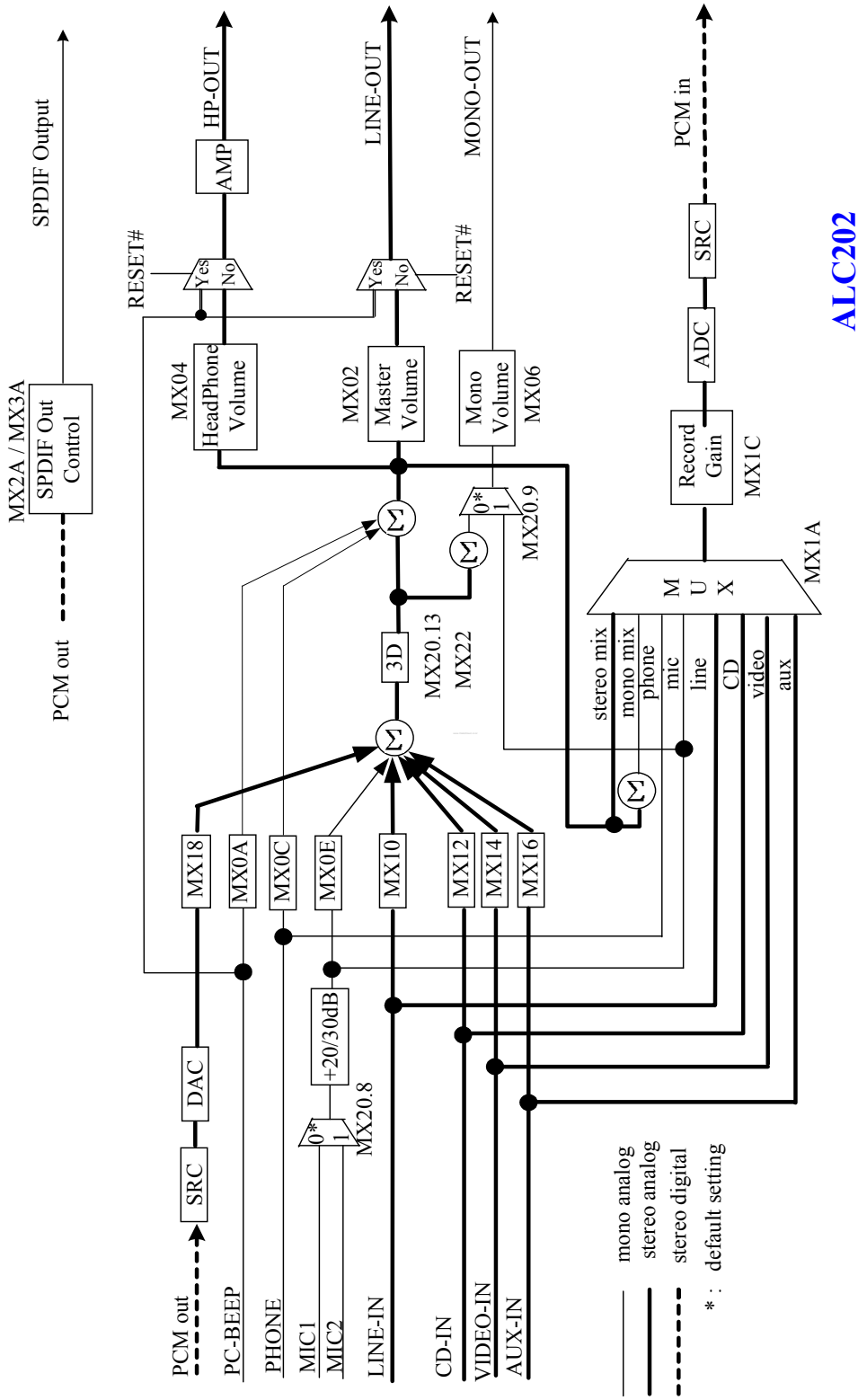
2. General Description

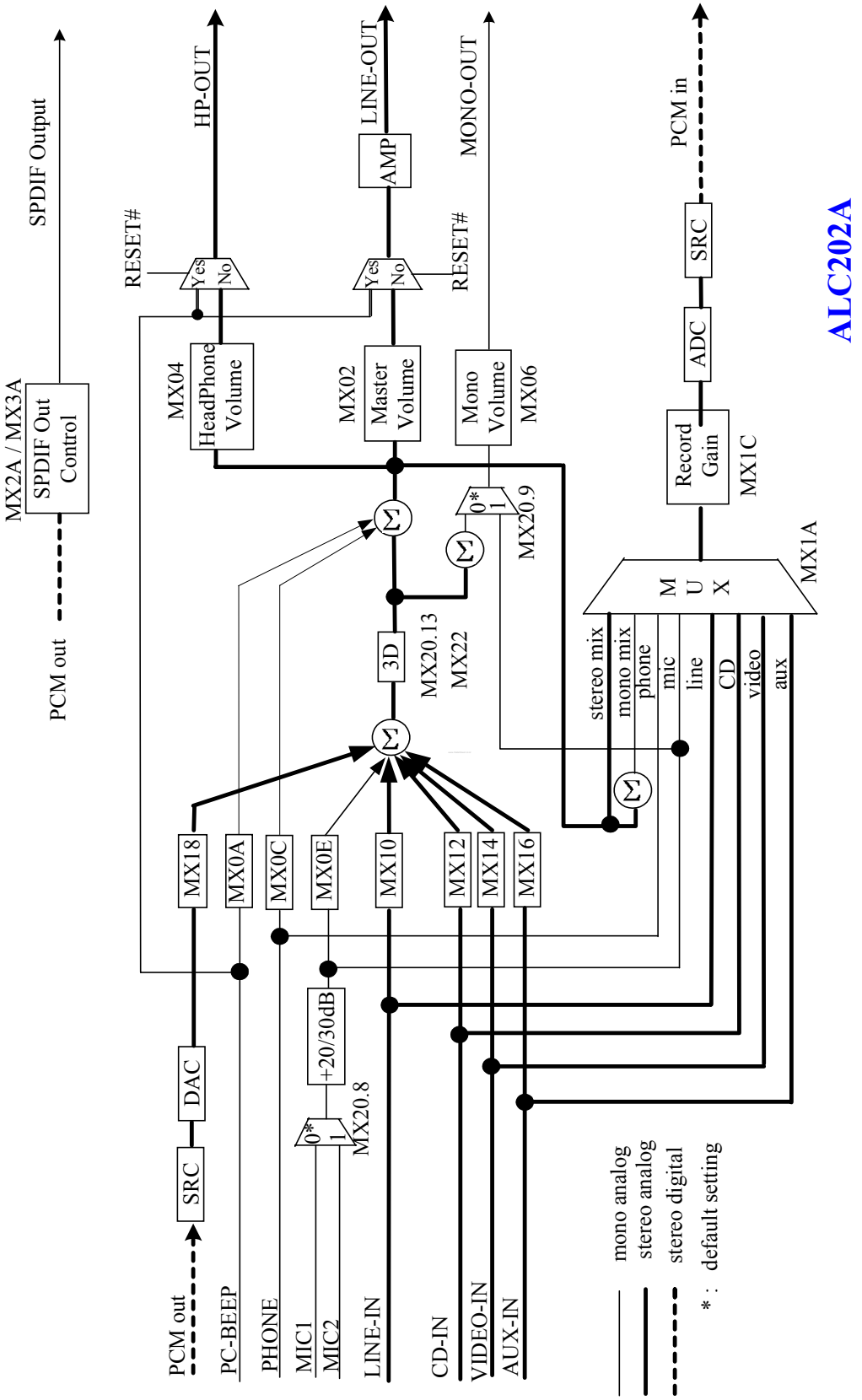
The ALC202/ALC202A is an 18-bit, full duplex AC'97 2.2 compatible stereo audio CODEC designed for PC multimedia systems, including host/soft audio and AMR/CNR based designs. The ALC202 incorporates proprietary converter technology to achieve a high SNR, greater than 90 dB. The ALC202 AC'97 CODEC supports multiple CODEC extensions with independent variable sampling rates and built-in 3D effects. The ALC202 CODEC provides two pairs of stereo outputs with independent volume controls, a mono output, and multiple stereo and mono inputs, along with flexible mixing, gain and mute functions to provide a complete integrated audio solution for PCs. The digital interface circuitry of the ALC202 CODEC operates from a 5V/3.3V power supply with EAPD (External Amplifier Power Down) control for use in notebook and PC applications. The ALC202 integrates a 50mW/8Ω headset audio amplifier into the CODEC, saving BOM costs. The ALC202 also supports the SPDIF out function, which is compliant to AC'97 2.2, which can offer easy connection of PCs to consumer electronic products, such as AC3 decoder/speaker and mini disk devices. The ALC202 CODEC supports host/soft audio from Intel 810/815/820/845 chipsets as well as audio controller based VIA/SIS/ALI chipsets. Bundled Windows series drivers (Win95/98/ME/2000/XP/NT) and sound effect utilities (supporting Karaoke, 26-kind of environment sound emulation, 10-band equalizer) provide an excellent entertainment package for PC users. Finally, internal PLL circuits generate required timing signals, eliminating the need for external clocking devices.

There are two differences between the ALC202 and the ALC202A. First, the ALC202 includes outputs for headphones with an op-amp, and in the ALC202A, those outputs are for True Line output and have no op-amp. Second, the Line Out channels on the ALC202 has no op-amp (1.0Vrms), where the ALC202A includes an op-amp (1.0Vrms).

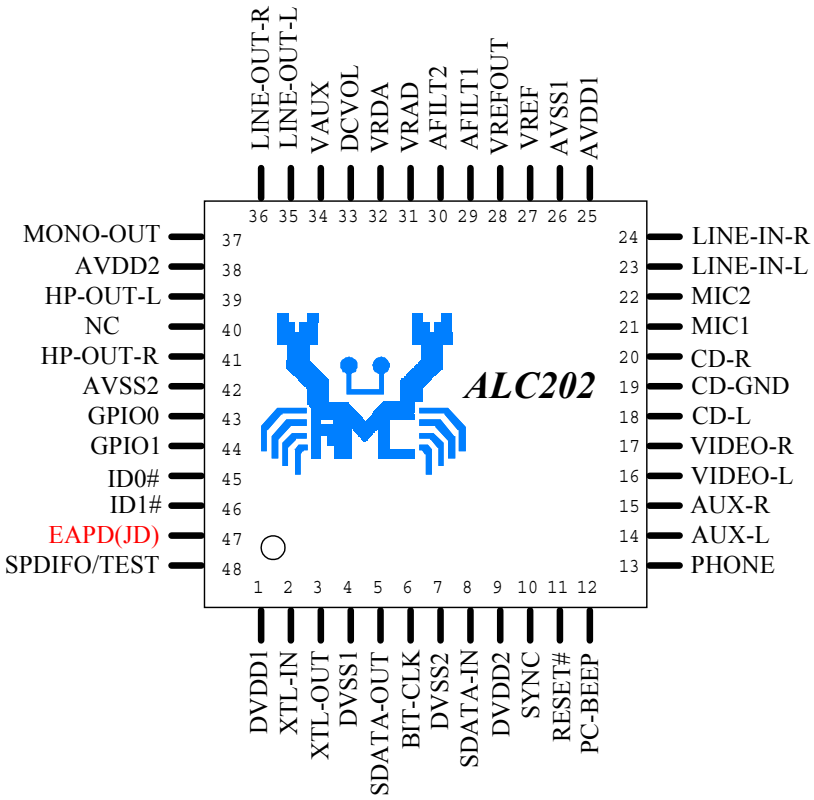
	ALC202	ALC202A
Line-Out Channel	No op-amp (1.0Vrms)	With op-amp (1.0Vrms)
Pins 39 & 41	Headphone output with op-amp	True-Line out without op-amp

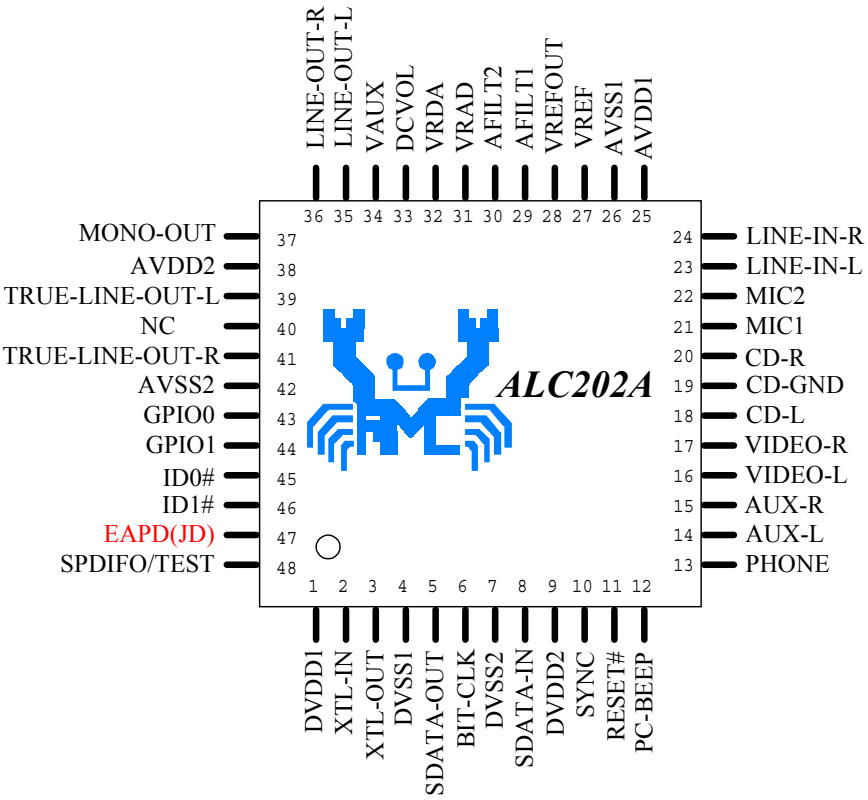
3. Block Diagram




ALC202A
SPDIF Output
HP-OUT
LINE-OUT
MONO-OUT
PCM in
RESET#
RESET#
Yes
No
Yes
No
AMP
SRC
ADC
Record Gain
MX1C
MX2A / MX3A
SPDIF Out Control
MX04 HeadPhone Volume
MX02 Master Volume
Mono Volume MX06
0*
1
MX20.9
MX1A
M U X
stereo mix
mono mix
phone
mic
line
CD
video
aux
3D
MX20.13
MX22
MX18
MX0A
MX0C
MX0E
MX10
MX12
MX14
MX16
DAC
SRC
+20/30dB
0*
1
MX20.8
PCM out
PC-BEEP
PHONE
MIC1
MIC2
LINE-IN
CD-IN
VIDEO-IN
AUX-IN
PCM out
mono analog
stereo analog
stereo digital
* : default setting

4. Pin Assignments





5. Pin Description

In order to reduce pin count, and therefore size and cost, some pins have multiple functions. In those cases, the functions are separated with a "/" symbol. Refer to the Pin Assignment diagram for a graphical representation.

5.1 Digital I/O Pins

Name	Type	Pin No	Description	Characteristic Definition
RESET#	I	11	AC'97 H/W reset	Schmitt trigger input
XTL-IN	I	2	Crystal input pad	Crystal: 24.576M/14.318M crystal input External: 24.576M/14.318M external clock input
XTL-OUT	O	3	Crystal output pad	Crystal: 24.576M/14.318M crystal output External: 24.576M/14.318M clock output
SYNC	I	10	Sample Sync (48KHz)	Schmitt trigger input
BIT-CLK	IO	6	Bit clock output (12.288Mhz)	CMOS input/output Vt=0.35Vdd
SDATA-OUT	I	5	Serial TDM AC97 output	Schmitt trigger input
SDATA-IN	O	8	Serial TDM AC97 input	CMOS output
GPIO0	I/O	43	I: General purpose input pin-0. (Can be software volume up) O: General purpose output pin-0.	Internally pulled high by a 50K resistor
GPIO1	I/O	44	I: General purpose input pin-1. (Can be software volume down) O: General purpose output pin-1	Internally pulled high by a 50K resistor
ID0#	I	45	ID strap 0 and PLL Control	CMOS input Vt=0.35Vdd, internally pulled high by a 50K resistor
ID1#	I	46	ID strap 1 and PLL Control	CMOS input Vt=0.35Vdd, internally pulled high by a 50K resistor
EAPD/JD	O	47	External Amplifier power down control / Jack –Detect sense a low to high edge.	CMOS output / input, JD should be internally pulled high by a 50K resistor
SPDIFO/ TEST	O	48	S/PDIF output / TEST output.	Digital output has 12 mA@75Ω driving capability
				Total: 13 Pins

5.2 Analog I/O Pins

Name	Type	Pin No	Description	Characteristic Definition
PC-BEEP	I	12	PC speaker input	Analog input (1Vrms)
PHONE	I	13	Speakerphone input	Analog input (1Vrms)
AUX-L	I	14	AUX Left channel	Analog input (1Vrms)
AUX-R	I	15	AUX Right channel	Analog input (1Vrms)
VIDEO-L	I	16	Video audio Left channel	Analog input (1Vrms)
VIDEO-R	I	17	Video audio Right channel	Analog input (1Vrms)
CD-L	I	18	CD audio Left channel	Analog input (1Vrms)
CD-GND	I	19	CD audio analog GND	Analog input (1Vrms)
CD-R	I	20	CD audio Right channel	Analog input (1Vrms)
MIC1	I	21	First MIC input	Analog input (1Vrms)
MIC2	I	22	Second MIC input	Analog input (1Vrms)
LINE-L	I	23	Line input Left channel	Analog input (1Vrms)
LINE-R	I	24	Line input Right channel	Analog input (1Vrms)
LINE-OUT-L	O	35	Line-Out Left channel	ALC202: Analog output without op-amp (1.0Vrms) ALC202A: Analog output with op-amp (1.0Vrms)
LINE-OUT-R	O	36	Line-Out Right channel	ALC202: Analog output without op-amp (1.0Vrms) ALC202A: Analog output with op-amp (1.0Vrms)
HP-OUT-L	O	39	ALC202: Headphone Out – Left ALC202A: True-LINE-Out – Left	ALC202: Analog output with op-amp ALC202A: Analog output without op-amp
HP-OUT-R	O	41	ALC202: Headphone Out – Left ALC202A: True-LINE-Out – Left	ALC202: Analog output with op-amp ALC202A: Analog output without op-amp
MONO-OUT	O	37	Speaker Phone output	Analog output (1Vrms)
				Total: 18 Pins

5.3 Filter/Reference

Name	Type	Pin No	Description	Characteristic Definition
VREF	-	27	Reference voltage	1uf capacitor to analog ground
VREFOUT	O	28	Ref. voltage out with 8mA drive	Analog output (2.25V – 2.75V)
AFILT1	-	29	ADC anti-aliasing filter capacitor	1000pf capacitor to analog ground.
AFILT2	-	30	ADC anti-aliasing filter capacitor	1000pf capacitor to analog ground.
VRAD	-	31	ADC reference voltage capacitor	1uf capacitor to analog ground
VRDA	-	32	DAC reference voltage capacitor	1uf capacitor to analog ground
DC VOL	I	33	DC Voltage Volume Control	Analog Input (AGND~AVDD)
VAUX	I	34	Auxiliary Power to keep CD and amplifier turned on.	+5V analog stand-by power
				Total: 8 Pins

5.4 Power/Ground

Name	Type	Pin No	Description	Characteristic Definition
AVDD1	I	25	Analog VDD (5.0V or 3.3V)	
AVDD2	I	38	Analog VDD (5.0V or 3.3V)	
AVSS1	I	26	Analog GND	
AVSS2	I	42	Analog GND	
DVDD1	I	1	Digital VDD (3.3V)	
DVDD2	I	9	Digital VDD (3.3V)	
DVSS1	I	4	Digital GND	
DVSS2	I	7	Digital GND	
				Total: 8 Pins

5.5 Others

Name	Type	Pin No	Description	Characteristic Definition
TEST	O	48	Output DAC clock and ADC clock	Digital pin shared with SPDIFO
NC	-	40,34	No Connection.	
				Total: 3 Pins

6. Registers

6.1 Mixer Registers

Access to registers with an odd number will return a 0. Reading unimplemented registers will also return a 0. X=Reserved bit.

REG.	NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	5990h
02h	Master Volume	Mute	X	ML5	ML4	ML3	ML2	ML1	ML0	X	X	MR5	MR4	MR3	MR2	MR1	MR0	8000h/ 0000h
04h	Headphone volume	Mute	X	HPL5	HPL4	HPL3	HPL2	HPL1	HPL0	X	X	HPR5	HPR4	HPR3	HPR2	HPR1	HPR0	8000h/ 0000h
06h	Mono-Out Volume	Mute	X	X	X	X	X	X	X	X	X	X	MM4	MM3	MM2	MM1	MM0	8000h/ 0000h
0Ah	PC_BEEP Volume	Mute	X	X	X	X	X	X	X	X	X	X	PB3	PB2	PB1	PB0	X	8000h
0Ch	PHONE Volume	Mute	X	X	X	X	X	X	X	X	X	X	PH4	PH3	PH2	PH1	PH0	8008h
0Eh	MIC Volume	Mute	X	X	X	X	X	BGO1	BGO0	X	BC	X	MI4	MI3	MI2	MI1	MI0	8008h
10h	Line-In Volume	Mute	X	X	NL4	NL3	NL2	NL1	NL0	X	X	X	NR4	NR3	NR2	NR1	NR0	8808h
12h	CD Volume	Mute	X	X	CL4	CL3	CL2	CL1	CL0	X	X	X	CR4	CR3	CR2	CR1	CR0	8808h
14h	Video Volume	Mute	X	X	VL4	VL3	VL2	VL1	VL0	X	X	X	VR4	VR3	VR2	VR1	VR0	8808h
16h	Aux Volume	Mute	X	X	AL4	AL3	AL2	AL1	AL0	X	X	X	AR4	AR3	AR2	AR1	AR0	8808h
18h	PCM Out Volume	Mute	X	X	PL4	PL3	PL2	PL1	PL0	X	X	X	PR4	PR3	PR2	PR1	PR0	8808h/ 0808h
1Ah	Record Select	X	X	X	X	X	LRS2	LRS1	LRS0	X	X	X	X	X	RRS2	RRS1	RRS0	0000h
1Ch	Record Gain	Mute	X	X	X	LRG3	LRG2	LRG1	LRG0	X	X	X	X	RRG3	RRG2	RRG1	RRG0	8000h
20h	General Purpose	POP	X	3D	X	X	X	MIX	MS	LBK	X	X	X	X	X	X	X	0000h
22h	3D Control	X	X	X	X	X	X	X	X	X	X	X	X	X	DP2	DP1	DP0	0000h
26h	Power Down Ctrl/Status	EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	000Fh
28h	Extended Audio ID	ID1	ID0	X	X	REV1	REV0	AMAP	X	X	X	X	X	X	SPDIF	X	VRA	0605h
2Ah	Extended Audio Status	X	X	X	X	X	SPCV	X	X	X	X	SPSA1	SPSA0	X	SPDIF	X	VRA	0000h
2Ch	PCM front Out Sample Rate	FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR9	FSR8	FSR7	FSR6	FSR5	FSR4	FSR3	FSR2	FSR1	FSR0	BB80h
32h	PCM Input Sample Rate	ISR15	ISR14	ISR13	ISR12	ISR11	ISR10	ISR9	ISR8	ISR7	ISR6	ISR5	ISR4	ISR3	ISR2	ISR1	ISR0	BB80h
3Ah	S/PDIF Ctl	V	0	SPSR1	SPSR0	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	PRE	COPY	/AUDIO	PRO	2000h
76h	GPIO Setup	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
78h	GPIO Status	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
7Ch	Vendor ID1	0	1	0	0	0	0	0	1	0	1	0	0	1	1	0	0	414Ch
7Eh	Vendor ID2	0	1	0	0	0	1	1	1	0	0	0	1	V3	V2	V1	V0	4740h

6.1.1 MX00 Reset
Default: 5990h

Writing any value to this register will start a register reset, and causes all of the registers to revert to their default values, then the written data is ignored. Reading this register returns the ID code of the specific part.

Bit	Type	Function
15		**Reserved**
14:10	R	Return 10110b
9	R	Read as 0 (No support for 20-bit ADC)
8	R	Read as 1 (Support for 18-bit ADC)
7	R	Read as 1 (Support for 20-bit DAC)
6	R	Read as 0 (No support for 18-bit DAC)
5	R	Read as 0 (No support for Loudness)
4	R	Read as 1 (Headphone output support)
3	R	Read as 0 (No simulated stereo; for analog 3D block use)
2	R	Read as 0 (No Bass & Treble Control)
1	R	**Reserved,** Read as 0
0	R	Read as 0 (No dedicated MIC PCM input)

6.1.2 MX02 Master Volume
Default: 8000h / 0000h

These registers control the overall volume level of the output functions. Each step on the left and right channels correspond to 1.5dB in increase/decrease in volume.

Bit	Type	Function
15	R/W	**Mute Control:** 1: Mute (-∞ dB) 0: Normal
14		**Reserved**
13:8	R/W	**Master Left Volume:** (MLV[5:0]) in 1.5 dB steps
7:6		**Reserved**
5:0	R/W	**Master Right Volume:** (MRV[5:0]) in 1.5 dB steps

❶ For MRV/MLV: 00h 0 dB attenuation
3Fh 94.5 dB attenuation

❷ When ID=01, the default value is 0000h.

6.1.3 MX04 Headphone/True Line Output Volume
Default: 8000h / 0000h

Register 04h controls the headphone (ALC202)/True Line (ALC202A) output volume. Each step in bits 5:0 and 13:8 correspond to 1.5dB in increase/decrease in volume, allowing 63 levels of volume, from 000000 to 111111.

Bit	Type	Function
15	R/W	**Mute Control:** 1: Mute (-∞ dB) 0: Normal
14		**Reserved**
13:8	R/W	**Headphone/True Line Output Left Volume:** (HPL[5:0]) in 1.5 dB steps
7:6		**Reserved**
5:0	R/W	**Headphone/True Line Output Right Volume:** (HPR[5:0]) in 1.5 dB steps

❶ For HPR/HPL: 00h 0 dB attenuation
3Fh 94.5 dB attenuation

❷ When ID=01, the default value is 0000h.

6.1.4 MX06 MONO_OUT Volume
Default: 8000h / 0000h

Register 06h controls the mono volume output. Mono output is the same data sent on all output channels. Each step in bits 4:0 correspond to 1.5dB in increase/decrease in volume, allowing 32 levels of volume from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control:** 1: Mute (-∞ dB) 0: Normal
14:5		**Reserved**
4:0	R/W	**Mono Master Volume:** (MMV[4:0]) in 1.5 dB steps

❶ For MMV: 00h 0 dB attenuation
1Fh 46.5 dB attenuation

❷ Implement 5-bit volume control only. Writing 1xxxxx will be interpreted as x11111 and respond when read with x11111 as well.

❸ When ID=01, the default value is 0000h.

6.1.5 MX0A PC BEEP Volume
Default: 8000h

This register controls the input volume for the PC beep signal. Each step in bits 4:1 correspond to a 3dB increase/decrease in volume. 16 levels of volume are available, from 0000 to 1111.

The purpose of this register is to allow the PC Beep signals to pass through the ALC202, eliminating the need for an external system speaker/buzzer. The PC BEEP pin is directly routed (internally hardwired) to the LINE-OUTL & R pins. If the PC speaker/buzzer is eliminated, it is recommended to connect the external speakers at all times so the POST codes can be heard during reset.

Bit	Type	Function
15	R/W	**Mute Control:** 1: Mute (-∞ dB) 0: Normal
14:5		**Reserved**
4:1	R/W	**PC Beep Volume:** (PBV[3:0]) in 3 dB steps
0		**Reserved**

❶ For PBV: 00h 0 dB attenuation
0Fh 45 dB attenuation

6.1.6 MX0C PHONE Volume
Default: 8008h

Register 0Ch controls the telephone input volume for software modem applications. Because software modem applications may not have a speaker, the CODEC can offer a speaker-out service. Each step in bits 4:0 correspond to 1.5dB in increase/decrease in volume, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control:** 1: Mute (-∞ dB) 0: Normal
14:5		**Reserved**
4:0	R/W	**Phone Volume:** (PV[4:0]) in 1.5 dB steps

❶ For PV: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.1.7 MX0E MIC Volume
Default: 8008h

Register 0Eh controls the microphone input volume. Each step in bits 4:0 correspond to 1.5dB in increase/decrease in volume, allowing 32 levels of volume, from 00000 to 11111. Bit 6 enables/disables a boost in volume to a magnification based on bits 9:8.

Bit	Type	Function
15	R/W	**Mute Control:** 1: Mute (-∞ dB) 0: Normal
14:10		**Reserved**
9:8	R/W	**Boost Gain Option:** (BGO) 00: 20 dB 01: 6 dB 10: 12 dB 11: 29.5 dB (V=30*Vmic-in)
7		**Reserved**
6	R/W	**Boost Control:** (BC) 0: Disable 1: Enable Boost
5		**Reserved**
4:0	R/W	**Mic Volume:** (MV[4:0]) in 1.5 dB steps

❶ For MV: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

❷ If 29.5dB boost gain is selected, input resistor can be reduced to save area of feedback resistor.

6.1.8 MX10 LINE_IN Volume
Default: 8808h

Register 10h controls the LINE_IN input volume. Each step in bits 4:0 correspond to 1.5dB in increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 12:8 correspond to 1.5dB in increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control:** 1: Mute (-∞ dB) 0: Normal
14:13		**Reserved**
12:8	R/W	**Line-In Left Volume:** (NLV[4:0]) in 1.5 dB steps
7:5		**Reserved**
4:0	R/W	**Line-In Right Volume:** (NRV[4:0]) in 1.5 dB steps

❶ For NLV/NRV: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.1.9 MX12 CD Volume
Default: 8808h

Register 12h controls the CD input volume. Each step in bits 4:0 correspond to 1.5dB in increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 12:8 correspond to 1.5dB in increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control:** 1: Mute (-∞ dB) 0: Normal
14:13		**Reserved**
12:8	R/W	**CD Left Volume:** (CLV[4:0]) in 1.5 dB steps
7:5		**Reserved**
4:0	R/W	**CD Right Volume:** (CRV[4:0]) in 1.5 dB steps

❶ For CLV/CRV: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.1.10 MX14 VIDEO Volume
Default: 8808h

Register 14h controls the video input volume. Each step in bits 4:0 correspond to 1.5dB in increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 12:8 correspond to 1.5dB in increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control:** 1: Mute (-∞ dB) 0: Normal
14:13		**Reserved**
12:8	R/W	**Video Left Volume:** (VLV[4:0]) in 1.5 dB steps
7:5		**Reserved**
4:0	R/W	**Video Right Volume:** (VRV[4:0]) in 1.5 dB steps

❶ For VLV/VRV: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.1.11 MX16 AUX Volume
Default: 8808h

Register 16h controls the auxiliary input volume. Each step in bits 4:0 correspond to 1.5dB in increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 12:8 correspond to 1.5dB in increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control:** 1: Mute (-∞ dB) 0: Normal
14:13		**Reserved**
12:8	R/W	**AUX Left Volume:** (ALV[4:0]) in 1.5 dB steps
7:5		**Reserved**
4:0	R/W	**AUX Right Volume:** (ARV[4:0]) in 1.5 dB steps

❶ For ALV/ARV: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

6.1.12 MX18 PCM_OUT Volume
Default: 8808h / 0808h

Register 18h controls the PCM_OUT output volume. Each step in bits 4:0 correspond to 1.5dB in increase/decrease in volume for the right channel, allowing 32 levels of volume, from 00000 to 11111. Each step in bits 12:8 correspond to 1.5dB in increase/decrease in volume for the left channel, allowing 32 levels of volume, from 00000 to 11111.

Bit	Type	Function
15	R/W	**Mute Control:** 1: Mute (-∞ dB) 0: Normal
14:13		**Reserved**
12:8	R/W	**PCM Volume:** (PLV[4:0]) in 1.5 dB steps
7:5		**Reserved**
4:0	R/W	**PCM Right Volume:** (PRV[4:0]) in 1.5 dB steps

❶ For PLV/PRV: 00h +12 dB Gain
08h 0dB gain
1Fh -34.5dB Gain

❷ When ID=01, the default value is 0808h.

6.1.13 MX1A Record Select
Default: 0000h

Register 1Ah controls the record input volume. Each step in bits 2:0 correspond to 1.5dB in increase/decrease in volume for the right channel, allowing 7 levels of volume, from 000 to 111. Each step in bits 10:8 correspond to 1.5dB in increase/decrease in volume for the left channel, allowing 7 levels of volume, from 000 to 111.

Bit	Type	Function
15:11		**Reserved**
10:8	R/W	**Left Record Source Select** (LRS[2:0])
7:3		**Reserved**
2:0	R/W	**Right Record Source Select** (RRS[2:0])

❶ For LRS

0	MIC
0	CD LEFT
0	VIDEO LEFT
0	AUX LEFT
0	LINE LEFT
0	STEREO MIXER OUTPUT LEFT
0	MONO MIXER OUTPUT
7	PHONE

❷ For RRS

0	MIC
0	CD RIGHT
0	VIDEO RIGHT
0	AUX RIGHT
0	LINE RIGHT
0	STEREO MIXER OUTPUT RIGHT
0	MONO MIXER OUTPUT
0	PHONE

6.1.14 MX1C Record Gain
Default: 8000h

Register 1Ch controls the record gain. Each step in bits 3:0 correspond to 1.5dB in increase/decrease in gain for the right channel, allowing 16 levels of gain, from 0000 to 1111. Each step in bits 11:8 correspond to 1.5dB in increase/decrease in gain for the left channel, allowing 16 levels of gain, from 0000 to 1111.

Bit	Type	Function
15	R/W	**Mute Control:** 1: Mute (-∞ dB) 0: Normal
14:12		**Reserved**
11:8	R/W	**Left Record Gain Select:** (LRG[3:0]) in 1.5 dB steps
7:4		**Reserved**
3:0	R/W	**Right Record Gain Select:** (RRG[3:0]) in 1.5 dB steps

❶For LRG/RRG: 0Fh +22.5dB
00h 0 dB (No Gain)

6.1.15 MX20 General Purpose Register
Default: 0000h

This register is used to control several functions. Bit 13 enables or disables 3D control. Bit 9 allows selection of mono output. Bit 8 controls the MIC selector. Bit 7 enables loopback of the AD output to the DA input without involving the AC-Link, allowing for full system performance measurements.

Bit	Type	Function
15:14		**Reserved**, Read as 0
13	R/W	**3D Control:** 1: On 0: Off
12:10		**Reserved**, Read as 0
9	R/W	**Mono Output Select:** 1: MIC 0: MIX
8	R/W	**MIC Select:** 1: MIC 2 0: MIC 1
7	R/W	**AD to DA Loop-back Control:** 1: Enable 0: Disable
6:0		**Reserved**

6.1.16 MX22 3D Control
Default: 0000h

This register is used to control the 3D stereo enhancement function built into the AC'97 component. The register bits, DP2-DP0 are used to control the separation ratios in the 3D control for both LINE_OUT and DAC_OUT.

The 3D stereo enhancement function provides for a deeper and wider sound experience with a potential 6-speaker arrangement. Note that the 3D bit in the general purpose register (bit 13) must be set to 1 to enable this function.

Bit	Type	Function
15:3		**Reserved**, Read as 0
2:0	R/W	**Depth Control** (DP[2:0])

❶3D effect control

DP[2:0]	Function	DP[2:0]	Function
000	0% (off*)	100	50%
001	12.5%	101	67.5%
010	25%	110	75%
011	37.5	111	100%

* Default

6.1.17 MX26 Powerdown Control/Status
Default: 000Fh

This read/write register is used to program powerdown states and monitor subsystem readiness. The lower half of this register is read only status; a "1" indicating that the subsection is "ready." Ready is defined as the subsection's ability to perform in its nominal state. When this register is written, the bit values that come in on AC-Link will have no effect on read only bits 0-7 and bit 15.

When the AC-Link "CODEC Ready" indicator bit (SDATA_IN slot 0, bit 15) is a 1, it indicates that the AC-Link and AC'97 control and status registers are in a fully operational state. The AC'97 controller must further probe this powerdown control /status register to determine exactly which subsections, if any are ready.

Bit	Type	Function
15	R/W	**PR7 External Amplifier Power Down** (EAPD): 1: Power down 0: Normal
14	R/W	**PR6**: 1: Power down Headphone Out (HP-OUT, pin-39/41) 0: Normal
13	R/W	**PR5:** 1: Disable internal clock 0: Normal
12	R/W	**PR4:** 1: Power down AC-Link 0: Normal
11	R/W	**PR3:** 1: Power down Mixer (Vref off) 0: Normal
10	R/W	**PR2:** 1: Power down Mixer (Vref still on) 0: Normal
9	R/W	**PR1:** 1: Power down PCM DAC 0: Normal
8	R/W	**PR0:** 1: Power down PCM ADC and input MUX 0: Normal
7:4		**Reserved**, Read as 0
3	R	**Vref Status:** 1: Vref is up to normal level 0: Not yet ready
2	R	**Analog Mixer Status:** 1: Ready 0: Not yet ready
1	R	**DAC Status:** 1: Ready 0: Not yet ready
0	R	**ADC Status:** 1: Ready 0: Not yet ready

❶True table for power down mode :

	ADC	DAC	Mixer	Verf	ACLINK	Int CLK	HP-OUT	EAPD
PR0=1	PD							
PR1=1		PD						
PR2=1			PD				PD	
PR3=1	PD	PD	PD	PD			PD	
PR4=1	PD	PD			PD			
PR5=1	PD	PD				PD		
PR6=1							PD	
PR7=1								PD

PD: Power down Blank: Don't care

❷If Mixer is power down (PR2=1 or PR3=1), the LINE-OUT (pin-35/36) is shut down and its output is floated.
❸If Headphone-Out is power down (PR6=1), the HP-OUT (pin-39/41) is shut down and its output is floated.

6.1.18 MX28 Extended Audio ID
Default: 0605h

The Extended Audio ID register is a read only register used to communicate information to the digital controller on two functions. ID1 and ID0 echo the configuration of the CODEC as defined by the programming of pins 45 and 46 externally. "00" returned defines the CODEC as the primary CODEC, while any other code identifies the CODEC as one of three secondary CODEC possibilities.

Bit	Type	Function
15	R	**ID1**
14	R	**ID0**
13:12		**Reserved**, Read as 0
11:10	R	REV[1:0]=01 to indicate that the ALC202 is AC'97 rev2.2 compliant
9	R	**AMAP** read as 1 (DAC mapping based on ID)
8:6		**Reserved**, Read as 0
5:4	R/W	**DAC Slot Assignment** DSA[1:0] (Default value depends on ID[1:0]) DSA[1:0] Controls the DAC slot assignment, as described in AC'97 rev2.2.
3		**Reserved**, Read as 0
2	R	**SPDIF** Read as 1 (S/PDIF is supported)
1	R	**DRA** Read as 1
0	R	**VRA** Read as 1 (Variable Rate Audio is supported)

❶ ID[1:0] depend on the states of pins 46, 45, 44, and 43 when power-on reset or AC97_RESET# is active. Refer to section 9.1 for detailed information on configuration of ID[1:0].

❷ The ALC202 maps DAC slot according to the following table: (default maps to AC'97 spec. rev2.2)

DSA[1:0]	Left DAC slot #	Right DAC slot #	Comment
0,0	3	4	Default when ID[1:0]=00
0,1	7	8	Default when ID[1:0]=01,10
1,0	6	9	Default when ID[1:0]=11
1,1	10	11	-

6.1.19 MX2A Extended Audio Status and Control
Default: 0000h

This register contains two active bits for powerdown and status of the surrounding DACs. Bits 0, 1 & 2 are read/write bits which are used to enable or disable VRA, DRA and SPDIF respectively. Bits 4 & 5 are read/write bits used to determine the AC-LINK slot assignment of the S/PDIF. Bit 10 is a read only bit which tells the controller if the S/PDIF configuration is valid.

Bit	Type	Function
15	R/W	**Validity Configuration of S/PDIF Output:** (VCFG) Combines with MX3A.15 to decide validity control in S/PDIF output signal.
14:11	NA	**Reserved**
10	R	**S/PDIF Configuration Valid:** (SPCV) 1: Current S/PDIF configuration {SPSA,SPSR,DAC/slot rate} is valid 0: Current S/PDIF configuration {SPSA,SPSR,DAC/slot rate} is not valid
9:6		**Reserved**
5:4	R/W	**S/PDIF Slot Assignment:** (SPSA[1:0]) 00: S/PDIF source data assigned to AC-LINK slot3/4 01: S/PDIF source data assigned to AC-LINK slot7/8 (Default when ID=00) 10: S/PDIF source data assigned to AC-LINK slot6/9 (Default when ID=01,10) 11: S/PDIF source data assigned to AC-LINK slot10/11 (Default when ID=11)
3		**Reserved**
2	R/W	**SPDIF:** 1: Enable 0: Disable (SPDIFO is in high impedance)
1	R/W	**DRA:** 1: Enable 0: Disable
0	R/W	**VRA:** 1: Enable 0: Disable

❶ If VRA = 0, ALC202 ADC/DAC operate at fixed 48KHz sampling rate. Otherwise, it operates with variable sampling rate defined in MX2C and MX32. VRA also control write operation of MX2Cand MX32.

❷ DRA can be written when (ID=00)&(DSA=00), otherwise it is always 0.
If DRA = 1, DAC operates at a fixed 96KHz sampling rate. The PCM(n) and PCM(n+1) data is captured in the same frame. In this mode, MX2C is fixed at BB80h, MX32 and ADC is still controlled by VRA.

6.1.20 MX2C PCM DAC Rate
Default: BB80h

The ALC202 allows adjustment of the front center output sample rate. This register is used to adjust the sample rate. By changing the values, sampling rates from 8000 to 48000 can be chosen.

Bit	Type	Function
15:0	R/W	**Output Sampling Rate:** FOSR[15:0]

❶ The ALC202 supports the following sampling rates, as required in the PC99/PC2001 design guide.

Sampling rate	FOSR[15:0]
8000	1F40h
11025	2B11h
12000	2EE0
16000	3E80h
22050	5622h
24000	5DC0
32000	7D00h
44100	AC44h
48000	BB80h

Note that If the value written is not support, the closest value is returned.
When MX2A.0=0 (VRA is disable), this register will return BB80h when read.

6.1.21 MX32 PCM ADC Rate
Default: BB80h

The ALC202 allows adjustment of the surround output sample rate. This register is used to adjust the sample rate. By changing the values, sampling rates from 8000 to 48000 can be chosen.

Bit	Type	Function
15:0	R/W	**Output Sampling Rate:** FISR[15:0]

❶ The ALC202 supports the following sampling rates, as required in the PC99/PC2001 design guide.

Sampling rate	FISR[15:0]
8000	1F40h
11025	2B11h
12000	2EE0
16000	3E80h
22050	5622h
24000	5DC0
32000	7D00h
44100	AC44h
48000	BB80h

Note that If the value written is not support, the closest value is returned.
When MX2A.0=0 (VRA is disable), this register will return BB80h when read.

6.1.22 MX3A S/PDIF Channel Status and Control
Default: 2000h

Bit	Type	Function
15	R/W	**Validity Control:** Control V bit in Sub-Frame. 1: The V bit in sub-frame is always send as 1 to indicate the invalid data is not suitable for receiver. 0: The V bit (valid flag) in sub-frame depends on whether the S/PDIF data is under-run or over-run.
14	R	**Double Rate S/PDIF:** (DRS) The ALC202 does not support double rate S/PDIF. This bit is always 0.
13:12	R/W	**S/PDIF Sample Rate:** SPSR[1:0] 00: Sample rate set to 44.1KHz, Fs[**0:3**]=0000 01: Reserved 10: Sample rate set to 48.0KHz, Fs[**0:3**]=0100 (default) 11: Sample rate set to 32.0KHz, Fs[**0:3**]=1100
11	R/W	**Generation Level** (LEVEL)
10:4	R/W	**Category Code** (CC[6:0])
3	R/W	**Preemphasis:** (PRE) 1: Filter preemphasis is 50/15 µsec 0: None
2	R/W	**Copyright:** (COPY) 1: Asserted 0: Not asserted
1	R/W	**Non-Audio Data Type:** (/AUDIO) 1: AC3 or other digital non-audio data 0: PCM data
0	R	**Professional or Consumer Format:** (PRO) 1: Professional format 0: Consumer format The ALC202 supports consumer channel status format, so this bit is always 0.

❶The consumer channel status block (bit0~bit31):

0	1	2	3	4	5	6	7
PRO=0	/AUDIO	COPY	PRE	0	0	0	0
8	9	10	11	12	13	14	15
CC0	CC1	CC2	CC3	CC4	CC5	CC6	LEVEL
16	17	18	19	20	21	22	23
0	0	0	0	0	0	0	0
24	25	26	27	28	29	30	31
Fs0	Fs1	Fs2	Fs3	0	0	0	0

❷ The “V” bit in the sub-frame is determined by Validity control (MX3A.15) and VCFG (MX2A.15):

Validity	VCFG	Operation
0	0	If S/PDIF FIFO is under-run, the “V” bit in the sub-frame is set to indicate that the S/PDIF data is invalid.
0	1	If S/PDIF FIFO is under-run, the “V” bit in the sub-frame is always 0, and pads the data with “0”s.
1	0	The “V” bit is always 1, and data bits (bit 8 ~ bit 27) should be forced to 0.
1	1	Reserved

6.2 Vendor Defined Registers

The ALC202 supports only one vendor defined register. This register, not defined in the AC’97 specifications, is available to Realtek and Realtek customers for specialized functions.

6.2.1 MX6A Miscellaneous Control

Default: 0000h

The default source of S/PDIF output is data sent by controller. When bit 12 is set, S/PDIF data comes from the ADC of the ALC202. To keep data concurrence, software must guarantee that the sample rates in MX32 and MX3A[13:12] are the same. SPCV is no longer a validity for S/PDIF configuration. If software does not keep the same sample rates, the S/PDIF output will be auto forbidden by hardware, and undefined consequences may occur.

Bit	Type	Function
15:14		**Reserved**
13	R/W	DAC PCM(n+1) Slot# Select (When DRA=1) 1: PCM(n+1) captured from Slot-7/8 0: PCM(n+1) captured from Slot-10/11. (Default in AC’97 rev2.2)
12	R/W	**S/PDIF Source:** 1: S/PDIF data is from ADC 0: S/PDIF data is from controller (default)
11:4		**Reserved**
3	R/W	**SPDIF Out Volume Control – Mute Bit:** 1: Clamp SPDIF output data to 0. (Mute) 0: Normal
2:0	R/W	**SPDIF Out Volume Control – In 6 dB Step Attenuation:** 000: 0dB 001: -6dB 010: -12dB … 111: -42dB

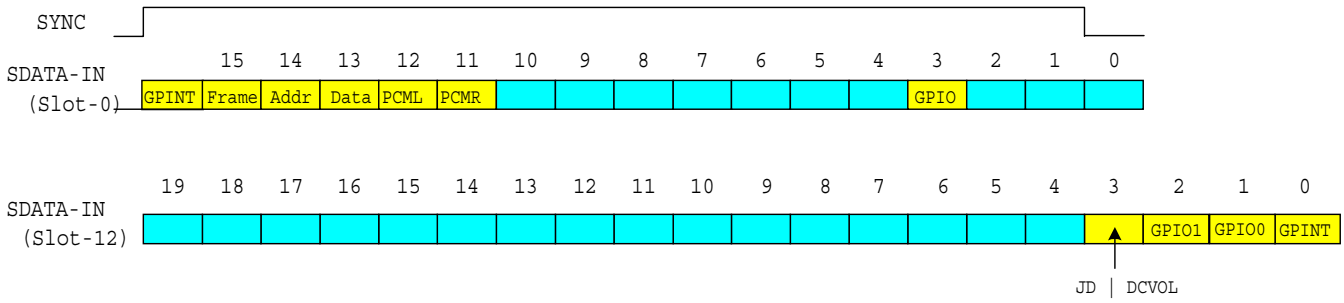
6.3 Extension Registers

6.3.1 MX76 GPIO Setup

Default: 0000h

Bit	Type	Function
15	R/W	**GPIO Status Indication in SDATA_IN:** 1: The status of GPIO0/GPIO1/JD and its valid tag are indicated in SDATA_IN 0: The status of GPIO0/GPIO1/JD and its valid tag are not indicated in SDATA_IN.
14:8		Reserved
7	R/W	**DCVOL (DC Volume Control) Interrupt Enable:** 1: Enable 0: Disable When the 5-bot volume code in the ramp counter ADC is changed (MX74.[4:0] is different from its previous value), it will trigger the DCVOL interrupt in bit0 of SDATA_IN's slot-12.
6	R/W	**JD (Jack-Detect) Interrupt Enable:** (when pin-47 is used as Jack-Detect) 1: Enabled 0: Disabled A low to high transaction will trigger the JD interrupt in bit0 of SDATA_IN's slot-12.
5	R/W	**GPIO1 Interrupt Enable:** (when GPIO1 is used as input) 1: Enabled 0: Disabled A low to high transaction will trigger the GPIO interrupt in bit0 of SDATA_IN's slot-12.
4	R/W	**GPIO0 Interrupt Enable:** (when GPIO0 is used as input) 1: Enabled 0: Disabled A low to high transaction will trigger the GPIO interrupt in bit0 of SDATA_IN's slot-12.
3:2		**Reserved**
1	R/W	**GPIO1Primitiveness Control:** 1: Set GPIO1 as output pin 0: Set GPIO1 as input pin
0	R/W	**GPIO0 Primitiveness Control:** 1: Set GPIO0 as output pin 0: Set GPIO0 as input pin

❶ Software can be designed to enable the JD interrupt when a "Jack Detection" event occurs.
❷ The Bit-Allocation of GPIO/JD/DCVOL status in AC-LINK:



***GPINT = (MX78.7 | MX78.6 | MX78.5 | MX78.4)**

6.3.2 MX78 GPIO Status
Default: 0000h

Bit	Type	Function
15:10		**Reserved**
9	R/W	**GPIO1 Output Control:** 1: Drive GPIO1 high 0: Drive GPIO1 low
8	R/W	**GPIO0 Output Control:** 1: Drive GPIO0 as high 0: Drive GPIO0 as low
7	R/W	**DCVOL Interrupt Status:** (DCVOL_IS) 1: DCVOL interrupt 0: No DCVOL interrupt DCVOL_IS= (MX76.7=1)&(MX74.[4:0] is changed). Write 1 to clear this status bit.
6	R/W	**JD Interrupt Status:** (JD_IS) 1: JD interrupt 0: No JD interrupt JD_IS= (MX78.2=1)&(MX76.6=1) & (JD low-to-high transition). Write 1 to clear this status bit.
5	R/W	**GPIO1 Interrupt Status:** (GPIO1_IS). (When GPIO1 is used as input) 1: GPIO1 interrupt 0: No GPIO1 interrupt GPIO1_IS= (MX76.1=0)&(MX76.5=1) & (GPIO1 low-to-high transition). Write 1 to clear this status bit.
4	R/W	**GPIO0 Interrupt Status:** (GPIO0_IS). (When GPIO0 is used as input) 1: GPIO0 interrupt 0: No GPIO0 interrupt GPIO0_IS= (MX76.0=0)&(MX76.4=1) & (GPIO0 low-to-high transition) Write 1 to clear this status bit.
3	NA	**Reserved**
2	R	**Jack-Detect Event:** (JDEVT) 1: Jack-Detect event has occurred 0: No Jack-Detect event has occurred JDEVT = MX7A.1
1	R	**GPIO1 Input Status:** 1: GPIO1 is driven high by external device (input) 0: GPIO1 is driven low by external device (input)
0	R	**GPIO0 Input Status:** 1: GPIO0 is driven high by external device (input) 0: GPIO0 is driven low by external device (input)

❶ GPIO interrupt (GPINT) in bit0 of SDATA_IN's slot-12 = (MX78.4 | MX78.5 | MX78.6 | MX78.7).

❷ When GPIO1/0 is used as input pin, its status will be also reflected in bit2/1 of SDIN's slot-12. Once GPIO1/0 is used as output pin, the bit2/1 of SDATA_IN's slot-12 is always 0.

❸ The GPIOx is internally pulled high by a weak resistor.

6.3.3 MX7A Various Controls
Default: 57C0h

This register is used for several types of information.

Bit	Type	Function
15	R	**Clock Source Selection:** (XTLSEL) 1: 14.318MHz crystal is used. 14.318M→24.576M digital PLL is enabled. (XTLSEL is pulled low) 0: 24.576MHz crystal is used. DPLL is bypassed. (XTLSEL is floating or open)
14	R/W	**Buffer Under-run Policy:** (BUP) 1: Hold a zero PCM sample when FIFO is under-run 0: Hold the last PCM sample when FIFO is under-run
13	R/W	**Digital High-pass Filter to Eliminate Variation in DC Offset:** (ENHPF) 1: Enabled (default) 0: Disabled
12	R/W	**Enable DC Voltage Volume Control:** 1: Enable. Master volume and headphone volume are determined by the sum of the 5-bit volume code and MX02/MX04/MX06. 0: Disable. Reset 5-bit volume code to 0.
11:8	NA	**Reserved**
7	R/W	**Pin-48 Function Selection:** 1: TEST 0: S/PDIF output (default)
6	R/W	**Output value of TEST:** (when bit-7 is set) 1: DAC CLK 0: ADC CLK
5	R/W	**Pin-47 Function Selection:** 1: Jack-Detect input 0: EAPD output (default)
4	R/W	**HP-OUT Control:** 1: HP-OUT is auto muted by H/W when JDS=1 0: Normal
3	R/W	**MONO-OUT Control:** 1: MONO-OUT is auto muted by H/W when JDS=1 0: Normal
2	R/W	**SPDIF Output Gating:** 1: SPDIF output is gated with JDS 0: SPDIF output is not gated with JDS
1	R	**Jack-Detect Status:** (JDS) 1: JD is floating or pulled high 0: JD is pulled low This bit always indicates the JD pin status after power on.
0	R/W	**LINE-OUT Control:** 1: LINE-OUT is auto muted by H/W when JDS=1 0: Normal

6.3.4 MX7C VENDOR ID1
Default: 414Ch

The two registers (MX7C Vendor ID1 and MX7E Vendor ID2) contain four 8-bit ID codes. The first three codes have been assigned by Microsoft for Plug and Play definitions. The fourth code is a Realtek assigned code identifying the ALC202. The MX7C Vendor ID1 register contains the value 414Ch, which is the first and second characters of the Microsoft ID code. The MX7C Vendor ID2 register contains the value 4740h, which is the third of the Microsoft ID code.

Bit	Type	Function
15:0	R	**Vendor ID** "AL"

6.3.5 MX7E VENDOR ID2
Default: 4740h

Bit	Type	Function
15:8	R	**Vendor ID** "G"
7:4	R	**Chip ID** 0100 (ALC202)
3:0	R	**Version Number:** 00: Version A. Due to WHQL issues, the version number is always 0.

7. Electrical Characteristics

7.1 DC Characteristics

7.1.1 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power Supplies					
Digital	DVDD	3.0	3.3	3.6	V
Analog	AVDD	3.0	5.0	5.5	V
Operating Ambient Temperature	Ta	0	-	+70	^oC
Storage Temperature	Ts			+125	^oC
ESD (Electrostatic Discharge)					
	Susceptibility Voltage				
Pin-38	Over 4000V (Pass 4000V)				
Pin-2, 6, 10, 11	Over 4500V (Pass 4500V)				
Others	Over 5000V (Pass 5000V)				

7.1.2 Threshold Hold Voltage

Dvdd= 3.3V±5%, $T_{ambient}$=25^{0}C, with 50pF external load.

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input voltage range	V_{in}	-0.30	-	Dvdd+0.30	V
Low level input voltage (SYNC,SDATA_OUT,RESET#)	V_{IL}	-	0.7	0.35Dvdd	V
Low level input voltage (XTAL_IN,BIT_CLK)	V_{IL}	-	1.0	0.35Dvdd	V
Low level input voltage (Other digital pins)	V_{IL}	-	1.2	0.35Dvdd	V
High level input voltage (SYNC,SDATA_OUT,RESET#)	V_{IH}	0.4DVdd	1.7	-	V
High level input voltage (XTAL_IN,BIT_CLK)	V_{IH}	0.4DVdd	2.2	-	V
High level input voltage (Other digital pins)	V_{IH}	0.4DVdd	1.7	-	V
High level output voltage	V_{OH}	0.9DVdd		-	V
Low level output voltage	V_{OL}	-	-	0.1DVdd	V
Input leakage current	-	-10	-	10	µA
Output leakage current (Hi-Z)	-	-10	-	10	µA
Output buffer drive current	-	-	5	-	mA
Internal pull up resistance	-	50k	100k	200k	Ω

7.1.3 Digital Filter Characteristics

Filter	Symbol	Minimum	Typical	Maximum	Units
ADC Lowpass Filter	Passband	0	-	19.2	KHz
	Stopband	28.8			KHz
	Stopband Rejection		-76.0		dB
	Passband Frequency Response		+- 0.15		dB
DAC Lowpass Filter	Passband	0	-	19.2	KHz
	Stopband	28.8			KHz
	Stopband Rejection		-78.5		dB
	Passband Frequency Response		+- 0.15		dB

7.1.4 S/PDIF output Characteristics

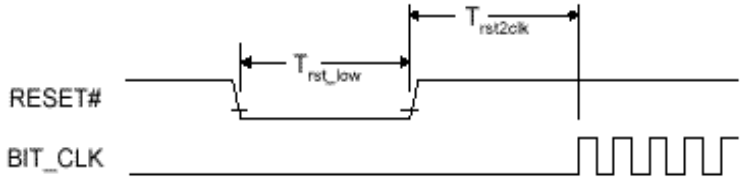
Dvdd= 3.3V, $T_{ambient}=25^0C$, with 75Ω external load.

Parameter	Symbol	Minimum	Typical	Maximum	Units
High level output voltage	V_{OH}	3.0	3.3		V
Low level output voltage	V_{OL}	-	0	0.5	V

7.2 AC Timing Characteristics

7.2.1 Cold Reset

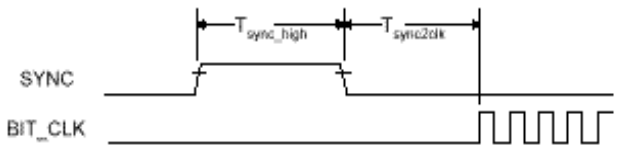
Parameter	Symbol	Minimum	Typical	Maximum	Units
RESET# active low pulse width	T_{rst_low}	1.0	-	-	µs
RESET# inactive to BIT_CLK Startup delay	$T_{rst2clk}$	162.8	-	-	ns



Cold reset timing diagram

7.2.2 Warm Reset

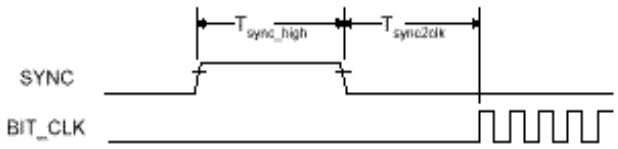
Parameter	Symbol	Minimum	Typical	Maximum	Units
SYNC active high pulse width	T_{sync_high}	1.0	-	-	µs
SYNC inactive to BIT_CLK Startup delay	$T_{sync2clk}$	162.8	-	-	ns



Warm reset timing diagram

7.2.3 AC-Link Clocks

Parameter	Symbol	Minimum	Typical	Maximum	Units
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	T_{clk_period}	-	81.4	-	ns
BIT_CLK output jitter		-	-	750	ps
BIT_CLK high pulse width (note 2)	T_{clk_high}	36	40.7	45	ns
BIT_CLK low pulse width (note 2)	T_{clk_low}	36	40.7	45	ns
SYNC frequency		-	48.0	-	KHz
SYNC period	T_{sync_period}	-	20.8	-	µs
SYNC high pulse width	T_{sync_high}	-	1.3	-	µs
SYNC low pulse width	T_{sync_low}	-	19.5	-	µs
Note 1: Worse case duty cycle restricted to 45/55.					



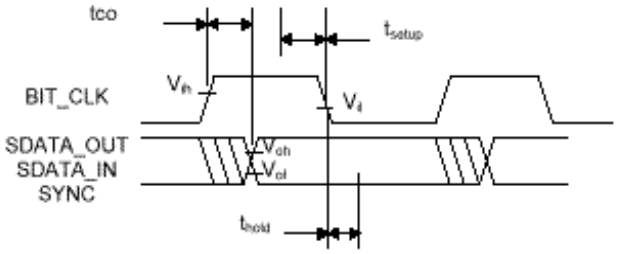
BIT_CLK and SYNC timing diagram

7.2.4 Data Output and Input Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
Output Valid Delay from rising edge of BIT_CLK	t_{co}	-	-	15	ns
Note 1: Timing is for SDATA and SYNC outputs with respect to BIT_CLK at the device driving the output. Note 2: 50pF external load					

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input Setup to falling edge of BIT_CLK	t_{setup}	10	-	-	ns
Input Hold from falling edge of BIT_CLK	t_{hold}	10	-	-	ns
Note: Timing is for SDATA and SYNC outputs with respect to BIT_CLK at the device driving the output.					

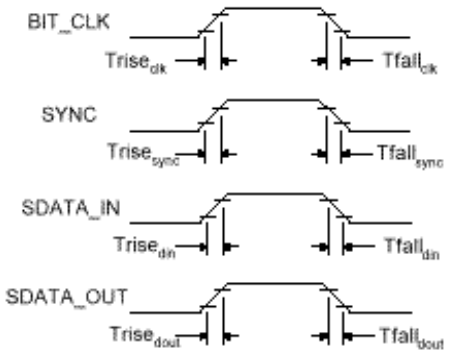
Parameter	Symbol	Minimum	Typical	Maximum	Units
BIT_CLK combined rise or fall plus flight time		-	-	7	ns
SDATA combined rise or fall plus flight time		-	-	7	ns
Note: Combined rise or fall plus flight times are provided for worst case scenario modeling purposes.					



Data Output and Input timing diagram

7.2.5 Signal Rise and Fall Timing

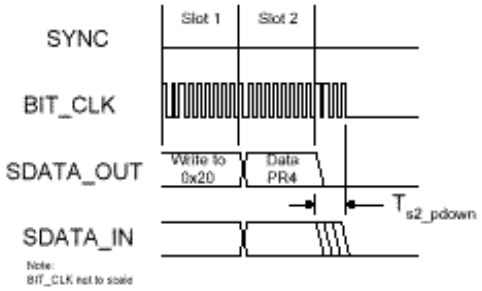
Parameter	Symbol	Minimum	Typical	Maximum	Units
BIT_CLK rise time	$Trise_{clk}$	-	-	6	ns
BIT_CLK fall time	$Tfall_{clk}$	-	-	6	ns
SYNC rise time	$Trise_{sync}$	-	-	6	ns
SYNC fall time	$Tfall_{sync}$	-	-	6	ns
SDATA_IN rise time	$Trise_{din}$	-	-	6	ns
SDATA_IN fall time	$Tfall_{din}$	-	-	6	ns
SDATA_OUT rise time	$Trise_{dout}$	-	-	6	ns
SDATA_OUT fall time	$Tfall_{dout}$	-	-	6	ns
Note 1: 75pF external load (50 pF in AC'97 rev2.1) Note 2: rise is from 10% to 90% of Vdd (V_{ol} to V_{oh}) Note 3: fall is from 90% to 10% of Vdd (V_{oh} to V_{ol})					



Signal Rise and Fall timing diagram

7.2.6 AC-Link Low Power Mode Timing

Parameter	Symbol	Minimum	Typical	Maximum	Units
End of slot 2 to BIT_CLK, SDATA_IN low	T_{s2_pdown}	-	-	1.0	µs

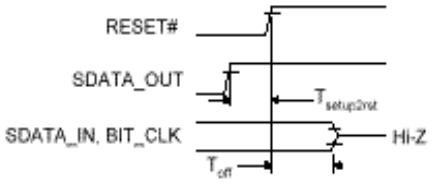


AC-Link low power mode timing diagram

7.2.7 ATE Test Mode

To meet AC'97 rev2.2 specifications, EAPD, SPDIFO, BIT_CLK and SDATA_IN should be floating in test mode.

Parameter	Symbol	Minimum	Typical	Maximum	Units
Setup to trailing edge of RESET# (also applies to SYNC)	$T_{setup2rst}$	15.0	-	-	ns
Rising edge of RESET# to Hi-Z delay	T_{off}	-	-	25.0	ns



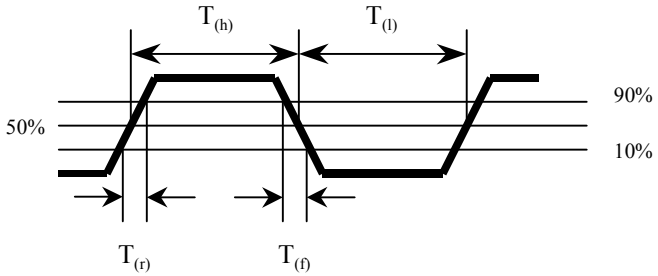
ATE test mode timing diagram

7.2.8 AC-Link IO Pin Capacitance and Loading

Output Pin	1 CODEC	2 CODEC	3 CODEC	4 CODEC
BIT_CLK (must support ≥ 2 CODECs)	55pF	62.5pF	75pF	85pF
SDATA_IN	47.5pF	55pF	60pF	62.5pF

7.2.9 SPDIF Output

SPDIF_OUT	Minimum	Typical	Maximum	Units
Rise time/fall time	0		10	%
Duty cycle	45		55	%



Notes: Rise time = 100 * $T_{(r)}$/ ($T_{(l)}$+ $T_{(h)}$)%
Fall time = 100 * $T_{(f)}$/ ($T_{(l)}$+ $T_{(h)}$)%
Duty cycle = 100 * $T_{(h)}$/ ($T_{(l)}$+ $T_{(h)}$)%

7.2.10 BIT-CLK and SDATA-IN State

When RESET# is active, BIT-CLK and SDATA-IN must be floating. The ac-link signals are driven by another AC'97 on a CNR board. This requirement is not mentioned in the AC'97 specifications Rev 2.1. Please refer to CNR (Communication Network Riser) specifications Rev.1.0 pages 23~25 or AC'97 Rev.2.2 for detailed information.

8. Analog Performance Characteristics

Standard test conditions: $T_{ambient}=25^0C$, Dvdd=3.3V ±5%,Avdd=5.0V±5%
1KHz input sine wave; Sampling frequency=48KHz; 0dB=1Vrms
10KΩ/50pF load; Test bench Characterization BW: 10Hz~22KHz
0dB attenuation; tone and 3D disabled

Parameter	Minimum	Typical	Maximum	Units
Full scale input voltage: Line inputs (Mixers)	-	1.6	-	
Line inputs (A/D)	-	1.2	-	Vrms
Mic input (0 dB)	-	1.6	-	
Mic input (20 dB boost)	-	0.16	-	
Full scale output voltage				
LINE-OUT (ALC202 / ALC202A)	-	1.1 / 1.5	-	Vrms
HP-OUT (ALC202 / ALC202A)	-	1.5 / 1.1	-	Vrms
Analog to Analog S/N: CD to LINE-OUT	-	95	-	dB
Other to LINE-OUT	-	95	-	
Analog frequency response	16	-	22,000	Hz
S/N (A-weighted): D/A	-	90	-	dB
A/D	-	85	-	
Total Harmonic Distortion (A-weighted): D/A	-	-80	-	dB
A/D	-	-78	-	
D/A & A/D frequency response	20	-	19,200	Hz
Transition Band	19,200	-	28,800	Hz
Stop Band	28,800	-	∞	Hz
Stop Band Rejection	-75	-	-	dB
Out-of-Band Rejection	-	-65	-	dB
Group delay	-	-	1	ms
Power Supply Rejection	-	-65	-	dB
MIC Amplifier 20dB Gain	18	20	22	dB
Master Volume (LINE- / HP-OUT): 64 step				
Step Size	-	1.5	-	dB
Attenuation Control Range	0	-	-94.5	dB
Master Volume (MONO-OUT): 32 step				
Step Size	-	1.5	-	dB
Attenuation Control Range	0	-	-46.5	dB
PC Beep Volume 16 steps:				
Step Size	-	3.0	-	dB
Attenuation Control Range	0	-	-45	dB
Analog Mixer Volume 32 steps:				
Step Size	-	1.5	-	dB
Gain Control Range	-34.5	-	+12	dB
Record Gain 16 steps:				
Step Size	-	1.5	-	dB
Gain Control Range	0	-	+22.5	dB
DC Volume Control: 32 step				
Gain Control Range	0		-43	dB
0 dB DC voltage			0.1	V
Mute DC voltage	4.7			V
Input impedance (gain = 0dB, mixer = off)				
LINE-IN, CD-IN, AUX-IN, VIDEO-IN		64		KΩ
MIC1 / MIC2		64 / 16		KΩ
PCBEEP, PHONE		16		KΩ

cont…

Output Impedance LINE-OUT (ALC202 / ALC202A) HP-OUT (ALC202 / ALC202A) MONO-OUT (ALC202 / ALC202A)		 280 / 1 1 / 280 500		 Ω Ω Ω
Amplifier Maximum Output Power @20Ω load @8Ω load			 80 60	 mW mW
Power Supply Current VA=5.0V (Powered Speaker / 20Ω / 4Ω) VA=3.3V (Powered Speaker / 20Ω / 4Ω) VD=3.3V			- 40 / 88 / 150 40 / 88 / 150 20	 mA mA
Power Down Current VA=5.0V / 3.3V VD=3.3V		 - -	 2 / 1 3	 mA mA
Vrefout	-	2.50	-	V
Vrefout Drive Current		8	12	mA

9. Design Suggestions

9.1 Clocking

The clock source and ID[1:0] are determined by status latched from pin-46/45/44/43 on the **power-on reset and AC97_RESET# trailing edge**. Different clock source configurations are listed below.

Configuration		Operation & ID[1:0]		
Pin-46 / 45 (ID1# / ID0#)	**Pin-44 / 43 (GPIO1 / 0)**	**ID[1:0]**	**BIT-CLK**	**Clock source**
NC / NC	X	00 (Primary)	Output	Crystal or external 24.576MHz source input from XTAL-IN.
Low / X	X	00 (Primary)	Output	External 14.318MHz clock source input from XTAL-IN.
NC / Low	NC / NC	01 (Secondary)	Input	12.288MHz clock input from BIT-CLK.
NC / Low	NC / LOW	01 (Secondary)	Input	12.288MHz clock input from BIT-CLK.
NC / Low	Low/NC	10 (Secondary)	Input	12.288MHz clock input from BIT-CLK.
NC / Low	Low / Low	11 (Secondary)	Input	12.288MHz clock input from BIT-CLK.

*Low: Pulled low by a 0Ω resistor. NC: Not connected or pulled high X: Don't care
*Pin-46/45/44/43 are all internally pulled high by weak resistors.

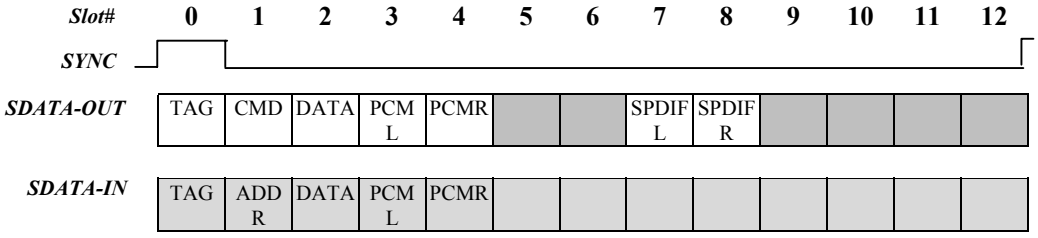
❶ Standard primary mode (ID=00), use external or crystal 24.576MHz as clock source.
❷ External 14.318M is used as clock source, digital PLL transmit 14.318M clock into 24.576MHz.
❸ Standard secondary mode (ID=01), ALC202 receive external 12.288MHz clock from BIT-CLK pin.
❹ Extended secondary mode (ID=01,10,11), pin-44/43 are used to configure ID, ALC202 receive external 12.288MHz clock from BIT-CLK pin.

9.2 AC-Link

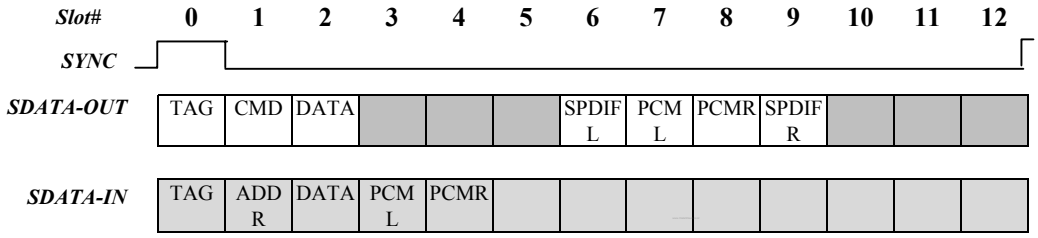
When the ALC202 receives serial data from the AC97 controller, it samples SDATA_OUT on the falling edge of BIT_CLK. When the ALC202 sends serial data to the AC97 controller, it starts to drive SDATA_IN on the rising edge of BIT_CLK.

The ALC202 will return any uninstalled bits or registers with 0 for read operations. The ALC202 also stuffs the unimplemented slot or bit with 0 in SDATA_IN. Note that AC-LINK is MSB-justified.

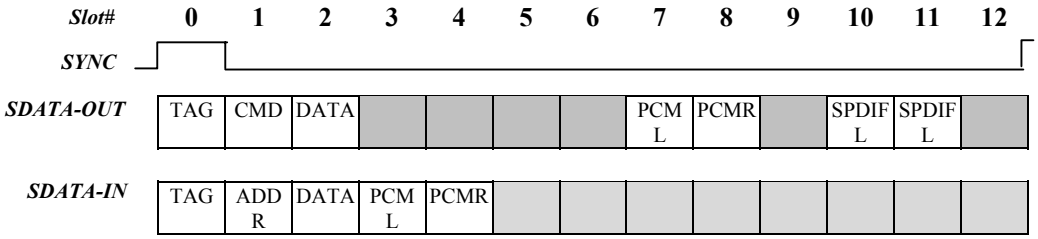
Refer to "Audio CODEC '97 Component Specification Revision 2.1/2.2" for details.



Default ALC202 Slot Arrangement – CODEC ID = 00



Default ALC202 Slot Arrangement – CODEC ID = 01,10



Default ALC202 slot arrangement – CODEC ID = 11

9.3 Reset

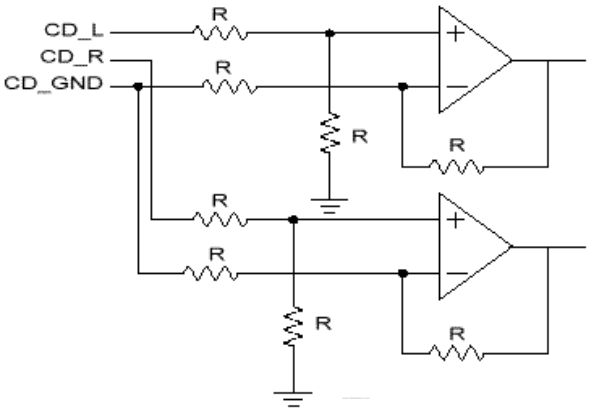
There are 3 types of reset operations: Cold, Warm and Register.

Reset Type	Trigger condition	CODEC response
Cold	Assert RESET# for a specified period	Reset all hardware logic and all registers to its default value.
Register	Write register indexed 00h	Reset all registers to its default value.
Warm	Driven SYNC high for specified period without BIT_CLK	Reactivates AC-LINK, no change to register values.

The AC97 controller should drive SYNC and SDATA_OUT low during the period of RESET# assertion to guarantee that the ALC202 has reset successfully.

9.4 CD Input

It is important to pay attention to differential CD input. Below is an example of differential CD input.



Example of differential CD input

9.5 Odd Addressed Register Access

The ALC202 will return “0000h” when odd-addressed and unimplemented registers are read.

9.6 Power-down Mode

It is important to pay special attention to the power down control register (index 26h), especially PR4 (powerdown AC-link).

9.7 Test Mode

To provide compatibility with AC’97 rev2.2, the ALC202 will float its digital output pins in both ATE and Vendor-Specific test modes. Please refer to AC’97 rev2.2 section 9.2 for a detailed description of the test modes.

9.7.1 ATE In Circuit Test Mode

SDATA_OUT is sampled high at the trailing edge of RESET#. In this mode, the ALC202 will drive BIT_CLK, SDATA_IN, EAPD and SPDIFO to high impedance.

9.7.2 Vendor Specific Test Mode

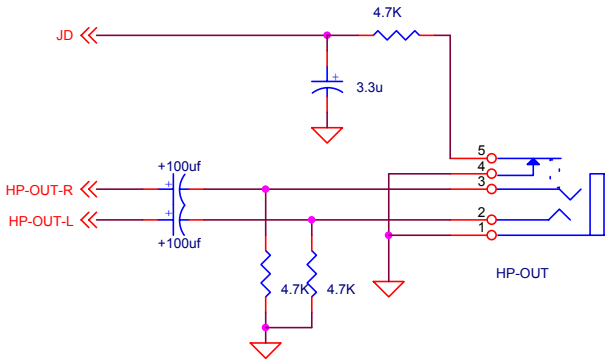
The Vendor Specific Test mode is no longer supported.

9.8 Jack-Detect Function

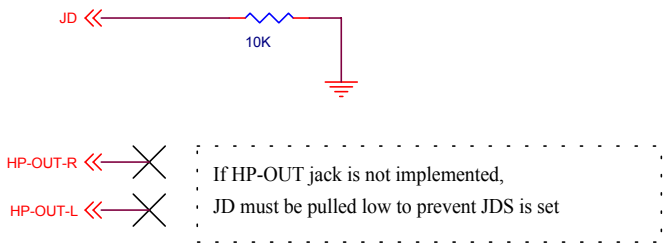
JD (Jack-Detect) is an internal, pulled high input pin used to decide if LINE_OUT should be auto muted. If JDE (Jack Detect Enable) is set and ALC202 detects the JD is floating or pull high (JDS=1), the ALC202 will disable the analog output of LINE_OUT even when the MX02 is not muted.

The first figure below shows an example of jack detect which can implement this function. If no audio plug is inserted in HP_OUT jack, JD is detected as low, and LINE output is normal. If an audio plug is inserted, the ALC202 disables the LINE output, (MX7A.0=1), SPDIF output (MX7A.2=1), MONO_OUT (MX7A.3=1), HP_OUT (MX7A.4=1). This is useful for some PC applications, such as notebook and home based computers.

If a headphone output jack is not implemented and HP_OUT kept as floating, once JDE is enabled, LINE_OUT will be muted (depending if MX7A.4=0) unless JD is pull low by a 10KΩ resistor (See second figure). To conquer this disadvantage, the Jack-Detect mute LINE_OUT function is disabled after power up (default JDE is 0). This makes the ALC202 compatible with other AC'97 devices. Therefore, it is the responsibility of the software to enable this function if headphone jack detection is implemented.



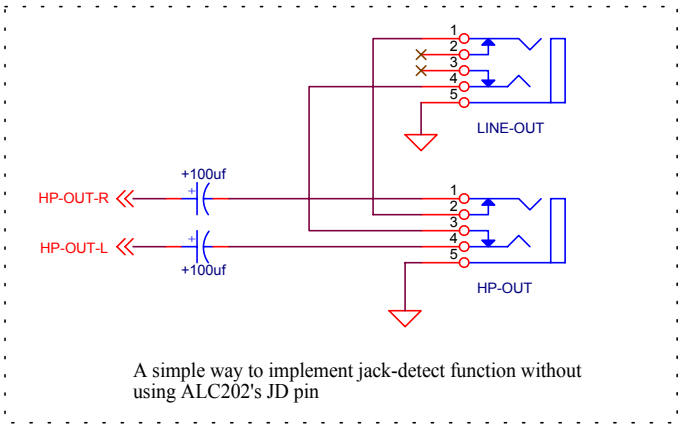
Example of a Jack Detect Circuit



JD is Pulled Low by a 10KΩ Resistor

The figure below shows another simple way to implement the jack detect function without using the JD pin of the ALC202. It is a good circuit for motherboard makers, as it is only a layout issue and no extra components are needed.

Once the HP_OUT jack is plugged in, output signals to LINE_OUT will be isolated, and no signals will be output to the LINE_OUT jack. The only drawback to this plan is that software will not sense that the HP_OUT jack is plugged in. It may be not convenient for software to pay attention to this special application.



Implementing the Jack-Detect Function Without Using the JD Pin

9.9 DC Voltage Volume Control

The ALC202 has a 32-step internal volume control that is controlled by the DC voltage applied the 'DC Vol' pin (pin-33). The volume control input range is from GND to AVDD. A low speed of counter ramp ADC transmits the DC voltage into a 5-bit volume code to attenuate the master volume (real MX02), headphone volume (real MX04) and mono-out volume (real MX06). A higher DC voltage means more attenuation related to output volume. The table below shows the relation between input DC voltage and the 5-bit volume code.

Input DC Voltage	Volume Code	Note	Input DC Voltage	Volume Code	Note
95%=< DC	1F	**DCMute=1**	47%< DC <= 50%	F	
92%< DC <= 95%	1E	DCMute=0	44%< DC <= 47%	E	
89%< DC <= 92%	1D		41%< DC <= 44%	D	
86%< DC <= 89%	1C		38%< DC <= 41%	C	
83%< DC <= 86%	1B		35%< DC <= 38%	B	
80%< DC <= 83%	1A		32%< DC <= 35%	A	
77%< DC <= 80%	19		29%< DC <= 32%	9	
74%< DC <= 77%	18		26%< DC <= 29%	8	
71%< DC <= 74%	17		23%< DC <= 26%	7	
68%< DC <= 71%	16		20%< DC <= 23%	6	
65%< DC <= 68%	15		17%< DC <= 20%	5	
62%< DC <= 65%	14		14%< DC <= 17%	4	
59%< DC <= 62%	13		11%< DC <= 14%	3	
56%< DC <= 59%	12		8%< DC <= 11%	2	
53%< DC <= 56%	11		5%< DC <= 8%	1	
50%< DC <= 53%	10		DC <= 5%	0	DCMute=0

Input DC Voltage is ratio of AVDD (+5VA).

❷This 5-bit volume code adds extra attenuation for master volume and headphone volume, the absolute maximum volume is determined by MX02, MX04 and MX06.
Once the sum of MX value and volume code exceeds 3Fh, the real MX value is 3Fh.

Example 1: (Normal case)
MX02=0002h, MX04=0300h, MX06=0001h, Volume Code=2h,
then Master Volume=0204h, Headphone Volume=0502h, Mono-Out=0003h

Example 2: (The sum exceeds 3Fh for MX02/MX04, 1Fh for MX06)
MX02=2F2Fh, MX04=2E2Eh, MX06=0002h, Volume Code=1Eh,
then Master Volume=3F3Fh, real Headphone Volume=3D3Dh, Mono-Out=001Fh

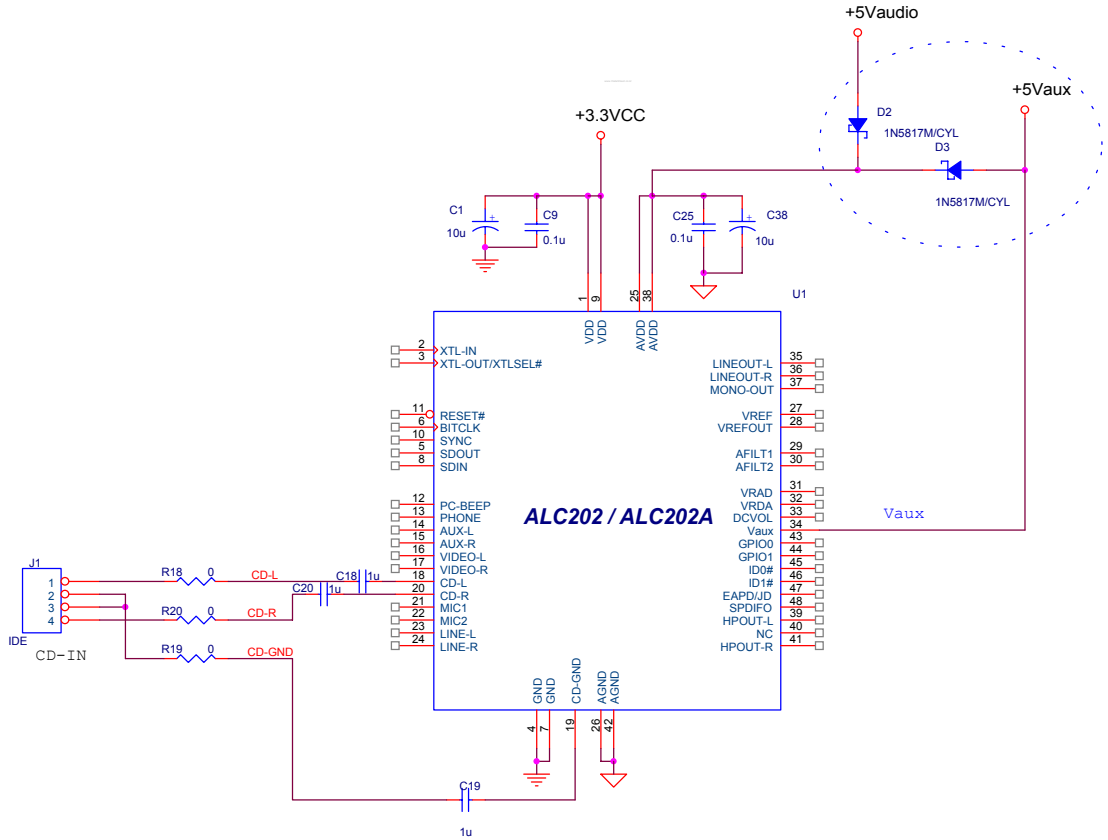
Example 3: (Volume code is 1Fh, DCMute=1, real MXs should be muted)
MX02=0000h, MX04=2020h, MX06=0010h, Volume Code=1Fh,
then Master Volume=9F1Fh, Headphone Volume=BF3Fh, Mono-Out=801Fh

9.10 POWER OFF CD Function

The 'POWER OFF CD' function describes a state which, after the system has been shut down and a +5V analog power is supplied at VAUX, the ALC202 will turn on the CD-IN op and output amplifier. It is possible to design a system which will save op-amp circuitry and bypass CD output directly to the speaker.

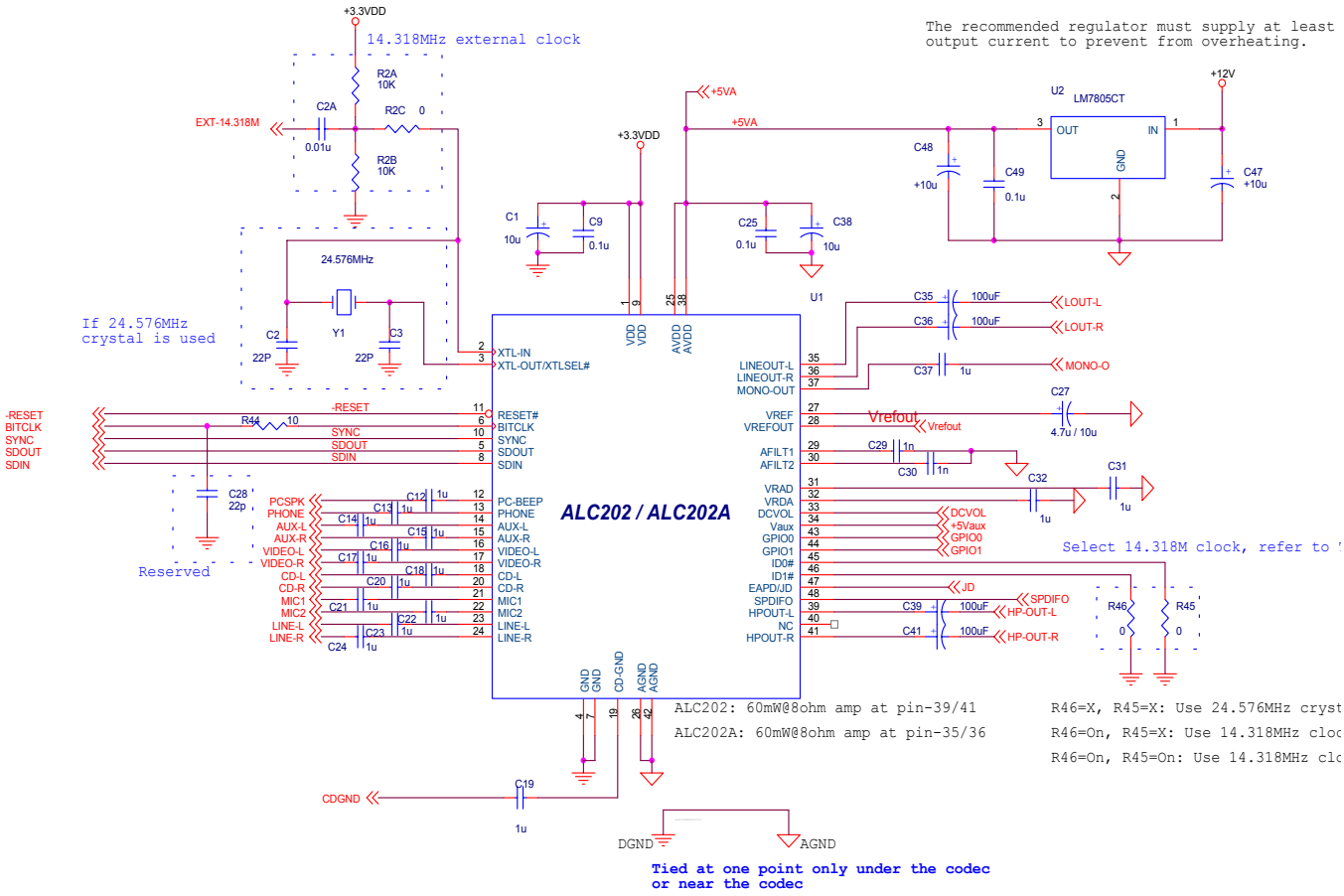
The figure below indicates the system application circuitry to support the 'POWER OFF CD' function. The operation mode is defined by +3.3VCC and +5Vaux.

+3.3VCC	+5Vaux	Operation Mode
No (0)	No (0)	Shut Down
No (0)	Yes (1)	Power Off CD
Yes (1)	No (0)	Normal (+5Vaudio must be on)
Yes (1)	Yes (1)	Normal (+5Vaudio must be on)



POWER OFF CD Circuitry

10. Application Circuit



Filter Connection Schematic

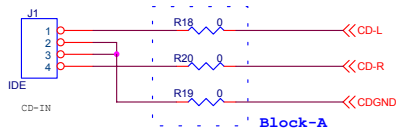
Table-1. Clock Source

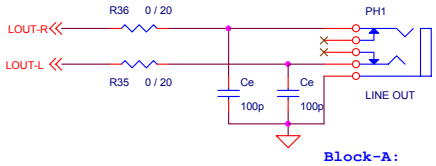
	Y1	C2	C3	R2A	R2B	R2C	C2A	R46	R45
Crystal	24.576M	22pF	22pF	X	X	X	X	X	X
ID=00									
(Primary) Ext. 14.318M	X	X	X	10K	10K	0	0.01uF	0	X
Ext. 14.318M	X	X	X	X	X	0	0	0	X

R2A,R2B and C2A can bias external clock to acceptible level if external clock is weak.

Filter Connection Table

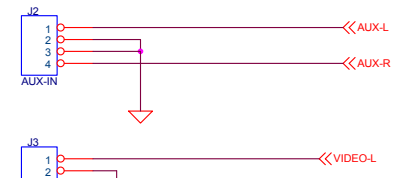
*If system designer use +5VA regulator has less then 200mA output current capability, please modify R35 and R36 as 20 ohm to limit amplifier current. (ALC202A)

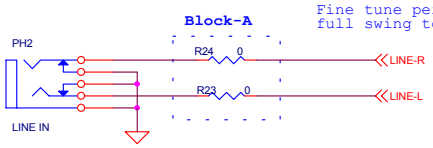


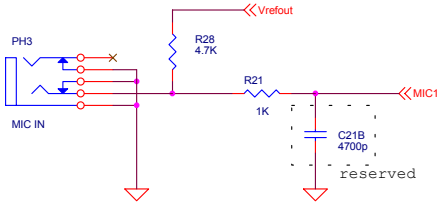


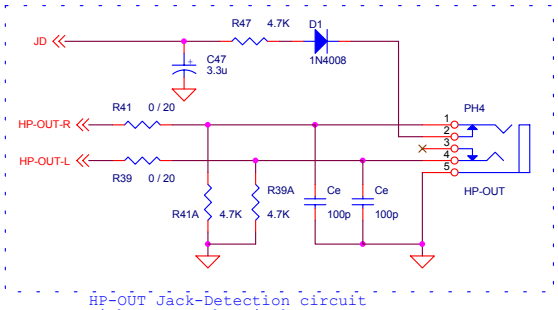
Block-A:

Fine tune performace or adjust input full swing to meet PC99

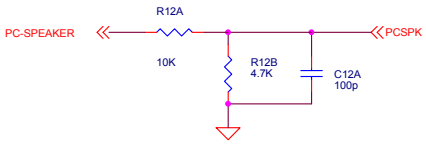




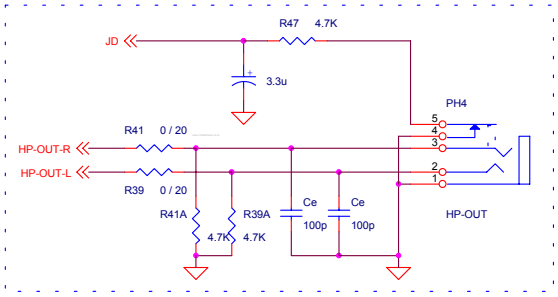


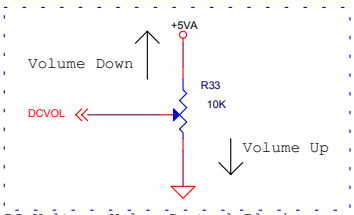


HP-OUT Jack-Detection circuit with stereo phonejack



*If system designer use +5VA regulator has less then 200mA output current capability, please modify R39 and R41 as 20 ohm to limit amplifier current. (ALC202)



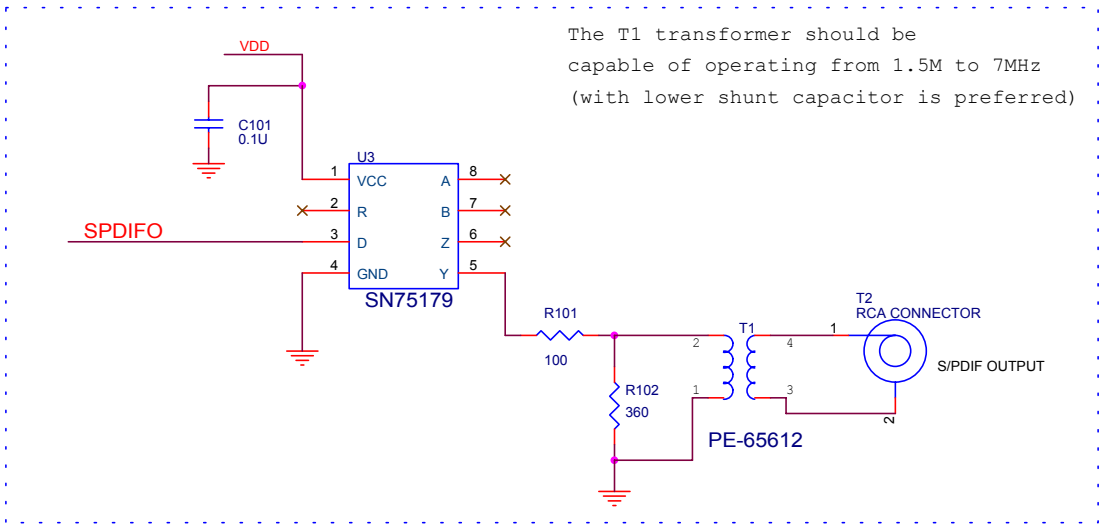


DC Voltage Volue Control Block

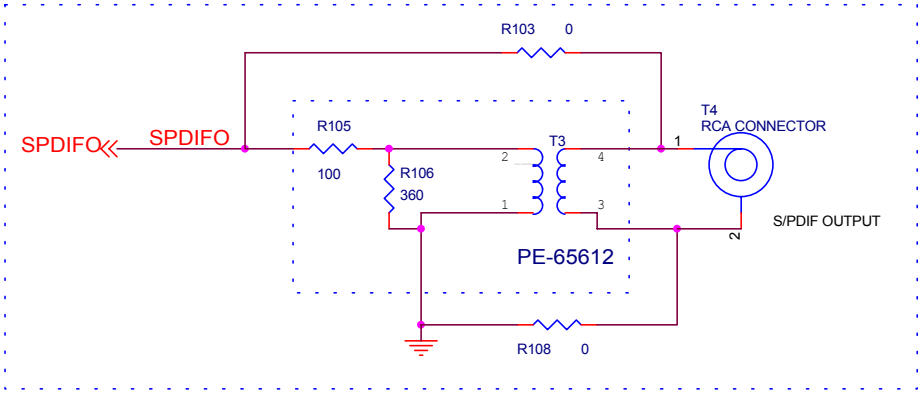
HP-OUT Jack-Detection circuit with isolated phonejack

IO Connection

Option (I): S/PDIF signal use RCA connector
+ Line Driver/ Receiver (is suitable for long transmission line)

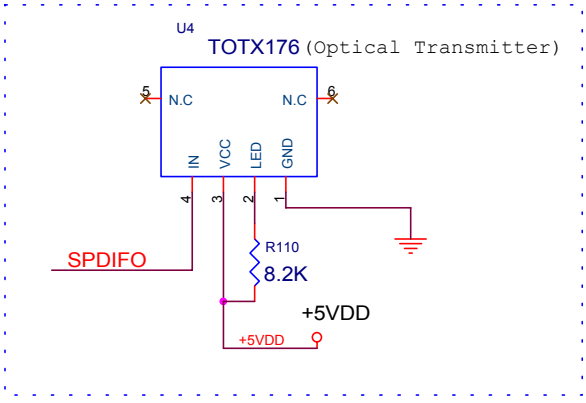


Option (III): Without Line Driver/ Receiver
Use R103 and R108: Guaranteed transmission distance <= 7 feet
Use T3,R105,R106: At least 10 feet of transmission distance

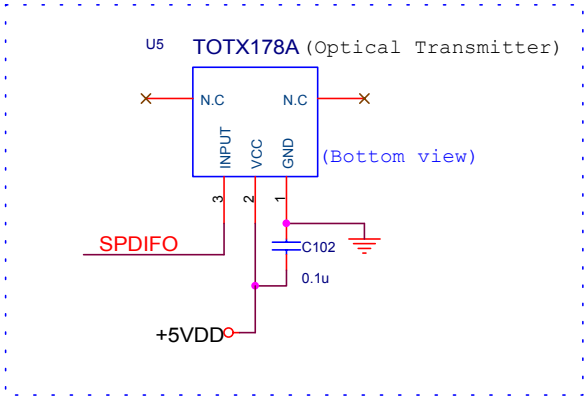


Option (II): S/PDIF signal use fiber optic transmitter

TOTX176 - maximum 10m transmission distance

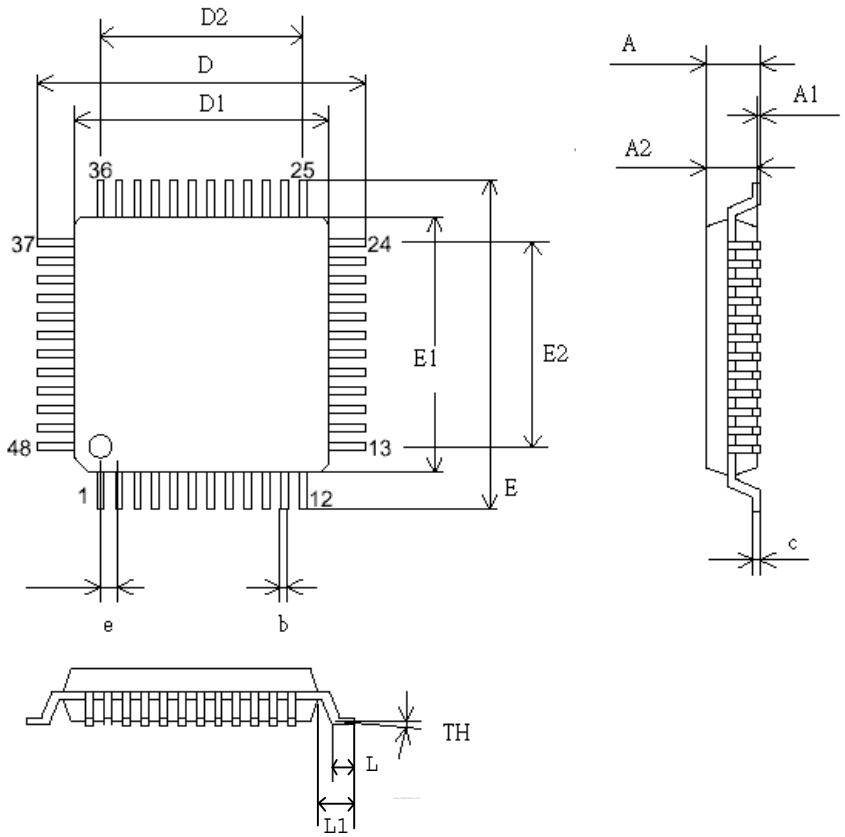


TOTX178 - maximum 5m transmission distance



S/PDIF Output Connection (I, II, III are optional)

11. Mechanical Dimensions



SYMBOL	MILLIMETER			INCH		
	MIN.	TYPICAL	MAX.	MIN.	TYPICAL	MAX
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
c	0.09		0.20	0.004		0.008
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
D2	5.50			0.217		
E	9.00 BSC			0.354 BSC		
E1	7.00BSC			0.276 BSC		
E2	5.50			0.217		
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC			0.016 BSC		
TH	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.0236	0.030
L1		1.00			0.0393	

TITLE: LQFP-48 (7.0x7.0x1.6mm) PACKAGE OUTLINE DRAWING, FOOTPRINT 2.0mm		
LEADFRAME MATERIAL		
APPROVE	DOC. NO.	
	VERSION	02
CHECK	DWG NO.	PKGC-065
	DATE	
REALTEK SEMICONDUCTOR CORP.		

12. Revision History

Version 1.27:
(1) 14.318MHz →24.576MHz PLL is enabled when pin-46 is pulled low. 48MHz→24.576MHz PLL is no longer supported.

Version 1.28:
(1) Fix typing error in filter connection schematic.

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