

TVGA8900D SUPER VGA CONTROLLER

Overview

- Single-chip solution for IBM PC/AT and compatible, PS/2 and compatible
- Built-in data bus transceiver and feature connector support
- Only one 32Kb EPROM required to achieve 16-bit BIOS operation speed
- Fully hardware compatible with VGA, EGA, CGA, MDA, and Hercules at the register level
- Programmable DRAM timing
- Supports 256Kx4, 256Kx8, 256Kx16, 512Kx4 and 512Kx8 DRAM chips
- Requires only two 256Kx4 DRAM chips for VGA solution
- Supports up to 1 MB of DRAM
- Supports 640x400, 640x480, 800x600, 1024x768 (interlaced or non-interlaced) in 256 colors
- Supports 800x600, 1024x768, and 768x1024 (interlaced or non-interlaced) in 16 colors
- Supports 640x400, 640x480, and 800x600 in 32K/64K colors (Trident's TKD8001 or other 15/16-bit DAC required)
- Supports 640x480 16M color mode (Trident's TKD8001 or other 24-bit DAC required)
- Supports 1024x768x256 72Hz non-interlaced
- Supports 70Hz refresh at 800x600 and 1024x768
- Supports Edsun CEG™ DAC
- Zero-wait state ISA bus performance
- Supports linear addressing
- Supports 80/132-column text in 25, 30, 43, or 60 rows
- High-resolution drivers available
- 0.8 µm low power CMOS technology
- 160 pin PFP package

General Description

The TVGA8900D is the successor to the popular TVGA8900CL and TVGA8900C. The TVGA8900D is a highly integrated and cost effective solution for high performance VGA (Video Graphics Array) systems. The built-in data bus transceiver and feature connector support mean a minimum motherboard solution can be achieved with only three support chips: the TKD8001 Truecolor DAC/clock chip, and two pieces 256Kx4 DRAM. Programmable DRAM timing allows the designer to choose either slower speed DRAM for a cost saving solution or faster speed DRAM for high speed performance. Display support for Super VGA, VGA, EGA, CGA, and MDA monitors assures TVGA8900D solutions can be matched up with virtually any monitor on the market.

The TVGA8900D also provides improved speed over the TVGA8900CL and TVGA8900C. This is achieved by zero-wait state direct memory write ISA bus performance, faster base DRAM clock (48MHz), and 1 MB linear addressing. The linear addressing eliminates memory bank switching and increases the speed for software that accesses more than 256K of memory.



TVGA8900D DATA SHEET

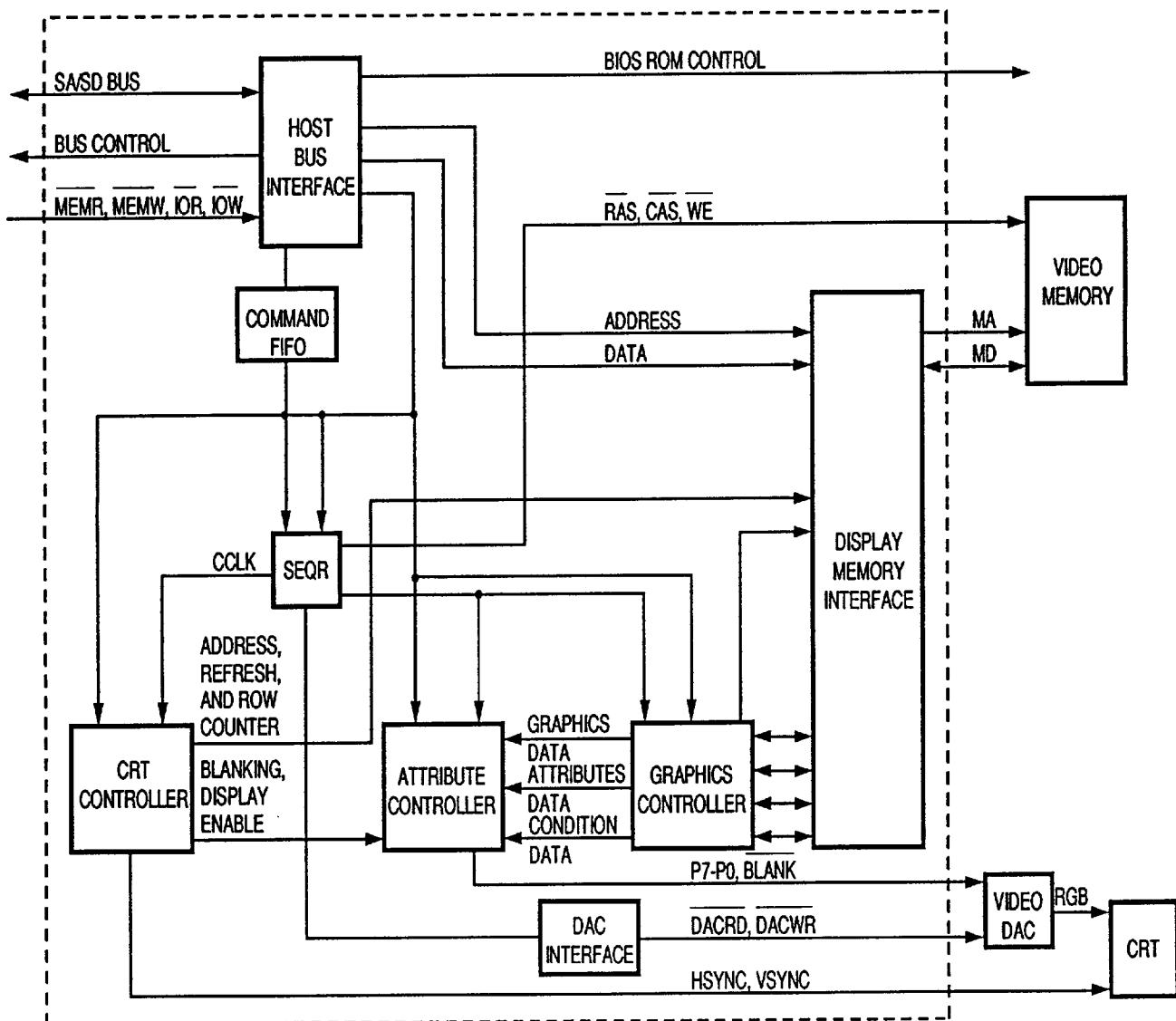


Figure 1. TVGA8900D Functional Block Diagram



Compatibility

The TVGA8900D is fully compatible with all standard IBM VGA modes and EGA, CGA, MDA, and Hercules modes, and allows:

- Use of application software that uses any of the above modes
- Emulation of EGA, CGA, MDA, and Hercules modes on a VGA monitor

Extended Graphics and Text Modes

Extended graphics modes supported include:

- 640x400, 640x480, and 800x600 in 32K or 64K colors
- 640x480 in 16M colors
- 640x400, 640x480, 800x600, and 1024x768 (interlaced or non-interlaced) in 256 colors from a palette of 256K colors (with 6-bit DAC) or 16M colors (with 8-bit DAC)
- 800x600, 768x1024, and 1024x768 (interlaced or non-interlaced) and 1280x1024 (interlaced) in 16 colors out of 256K/16M
- 1024x768 in 4 colors out of 256K/16M
- Extended text modes offer 80-column text with 30, 43, and 60 rows; and 132-column text with 25, 30, 43, and 60 rows

Hardware Features

The TVGA8900D supports PC/AT bus and PS/2 Micro Channel bus and offers speed improvement and flexible memory type selections over the TVGA8900CL.

The support of pseudo 16-bit ROM operation in TVGA8900D means high performance can be achieved using a single ROM chip. A single ROM solution helps minimize the number of chips required for VGA implementation.

The chip allows programmable DRAM timing and

supports 256Kx4, 256Kx8, 256Kx16, 512Kx4 and 512Kx8 DRAM. Table 1 outlines the amount and speed of Fast Page Mode 256Kx4 DRAM required to implement the 16-, 256-, 32K-, and 16M-color modes. For other types of DRAM, typically 80ns speed is required.

Table 1. 16, 256, 32K, and 16M-Color DRAM Requirements

Resolution	16	Colors				DRAM Count			Speed ns	
		256	32K ^a	16M	2	4	8	100	80	
Standard VGA	•				•					•
640x480		•				•				•
640x480			•			•				•
640x480				•						•
800x600	•				•					•
800x600		•				•				•
800x600			•			•				•
800x600				•						•
1024x768 (Interlaced)	•					•				•
1024x768 (Non-interlaced)	•					•				•
1024x768 (Interlaced)	•					•				•
1024x768 (Non-interlaced)	•					•				•
1280x1024 (Interlaced)	•					•				•

^aSame DRAM requirement for 64K color

A CPU command FIFO allows zero-wait state performance on the PC/AT and MCA bus. On the display side, base DRAM clock speed has improved and linear addressing eliminates bank switching overhead for all display resolutions.

Software Drivers Supported

The TVGA8900D is compatible with all drivers currently available for the TVGA8900CL. The following applications are supported:

- AutoCAD
- Autoshade
- CADKEY
- Framework
- GEM
- Lotus
- MS Windows
- MS Word
- P-CAD
- Symphony
- Ventura
- VersaCAD
- WordPerfect
- Wordstar
- OS/2
- SCO X-Windows (contact SCO)
- Edsun CEG™ (Windows, Lotus, ACAD)

Contact Trident for the latest high-resolution driver releases.



TVGA8900D Applications

The TVGA8900D works with your hardware allowing you to develop a high-end or low-end system. You can use Trident's DAC/clock chip, the TKD8001, to select up to 16 different clock frequencies. Such frequency selection ability allows you to implement specific applications such as support for high-resolution analog VGA monitors, fixed-frequency VGA monitors, and EGA, CGA, MDA, and Hercules monitors. The TVGA8900D allows you to divide clock input frequencies by one and one half, two, or four. Four chips signals (SC1, SC2, SC3, and SC4) can be programmed to select specific clock inputs for the TVGA8900D.

A minimum configuration requires a TVGA8900D, TKD8001 DAC/clock chip, two 256Kx4 DRAM chips, 32KB EPROM, 15-pin connector, 14.318MHz crystal, jumpers, and miscellaneous ferrite beads, capacitors, resistors.

TVGA8900D Components

The TVGA8900D consists of eight major components: Sequencer, CRT Controller, Graphics Controller, Attribute Controller, DAC Support Logic, Host Bus Interface, Display Memory Bus Interface and Command FIFO. These components are used to generate video output and timing for video memory and the monitor. See Figure 1 on page 2 for the TVGA8900D Functional Block Diagram.

Sequencer

The sequencer provides basic memory timing for DRAM interfacing, and a character clock for the CRTC and for controlling regenerative memory fetch. The sequencer uses a 32 byte video cache to let the CPU access display memory during active display intervals. Video data from the cache can be output to the video screen while the CPU accesses video memory. This greatly increases performance over standard implementations for CPU access.

CRT Controller

The CRT (Cathode Ray Tube) Controller provides complete control for horizontal and vertical synchronous timing, address interface between video memory and display screen, cursor and underline timing, and refresh addressing for dynamic RAMs.

Graphics Controller

During the active display interval, the Graphics Controller directs data from video memory to the Attribute Controller. In graphics modes, memory data is formatted into serialized form and sent to the Attribute Controller in 4-bit plane format. In text mode, the parallel attribute byte goes directly to the Attribute Controller without going through the Graphics Controller. During video memory read/write operations, the Graphics Controller acts as an interface to the CPU. The Graphics Controller can perform logic operations on memory data before it reaches the display memory or system data bus.

Attribute Controller

The Attribute Controller takes in data from video memory and formats it for output on the display monitor. In addition, the Attribute Controller takes care of blinking, underlining, cursor insertion, and PEL panning. In text mode, 16 bits of code are divided into 8 bits of character code and 8 bits of attribute code. The character code is used as a look-up into a font table. The attribute code is used to determine character color, blinking, bold, etc. In graphics mode, the Graphics Controller serializes memory bits. Each output color is translated through the internal color palettes and then sent to the Video DAC. Here it is used as an address to the 18/24-bit color look-up table. The value read from the color look-up table is converted into three analog signals (R, G, B) for driving an analog display.



DAC Support Logic

To simplify the chip hardware design, the TVGA8900D provides a pixel clock and DAC write, DAC read, and blank signals to an off-chip color look-up table/DAC. See Figure 7-A and 7-B for diagrams of standard applications (page 14 and 15). 15/16-bit color and true color DACs are supported.

Host Bus Interface

The TVGA8900D supports the PC/AT bus and the Micro Channel bus by setting or resetting configuration bits MD4 during the system reset time. When the TVGA8900D is part of a Micro Channel board solution, several host bus interface pins are defined or designated differently from a PC/AT solution. Reference Table 10 for details.

The TVGA8900D video ROM is located at C0000-C7FFF. The PROM data width can be configured as 16-bit or 8-bit at system reset time by pulling MD7 high or low, respectively. If the 16-bit mode is turned on, the TVGA8900D will return MCS16 when the PROM is addressed. If the on-board BIOS is not used, the ROM chip(s) can be disabled by pulling MD6 low at system reset time.

The TVGA8900D can address up to 1MB of video memory depending on the mode (text or graphics). After system reset the TVGA8900D is configured for an 8-bit data width for video memory access. The 16-bit-wide data bus can be activated automatically by ROM. The TVGA8900D will drive MCS16 when the 16-bit mode is set and video memory is accessed.

In order to comply with the Micro Channel specifications, the TVGA8900D supports channel ID (I/O address 100 and 101) as well as the card-enable control bit (bit 0 of I/O port 102). When the video memory or on-board I/O registers are accessed, the TVGA8900D responds with CD SFDBK. CD SFDBK is generated by decoding the following address groups with a read/write command:

I/O Read/Write:

- 3BX - excluding 3B6, 3B7, 3BC, 3BD, and 3BX. For monochrome mode only.
- 3DX - excluding 3D6, 3D7, 3DE, and 3DF. For color mode only.
- 3CX - excluding 3CA, 3CB, and 3CD.

Memory Read/Write:

- ROMCS - on-board BIOS EPROM address from C0000 to C7FFF.
- MEMR/W - default display memory address space.

Since there is only the decoding delay for generation of CD SFDBK, the signal will look very much like that of a system read/write command.

Display Memory Bus Interface

The TVGA8900D provides a bus interface for the video display DRAM. The interface provides address multiplexing, data multiplexing, refresh, and RAS, CAS, and write-enable signals. Nineteen address pins (MA9, MAA8-MAA0 and MAB8-MAB0 for Bank A and B) and 32 data pins (MD31-MD0) are available for display memory.

Command FIFO

The FIFO enhances the memory write performance. CPU write data is stored in the FIFO without being written into memory so the CPU does not have to wait when the video interface is busy. When the memory bus is available, data is written into memory from the FIFO.



MD & RMD Definitions at System Reset

Tables 2 through 4 list values and definitions for MD29-MD16, MD7-MD0 and RMD7-RMD0 at system reset.

Table 2. MD29-MD16 Definitions

MD	Logic Value ¹	Definition
MD29	-	Default logic value 1
MD28	0	Pins WE3-WE0 defined as CASA3-CASA0. Pin CASA defined as WE
	1	Default
MD27-MD24	NA	Sets base address of the linear address window
MD23	0	Enables true color mode
	1	Disables true color mode
MD22	NA	Reserved
MD21	0	Reserved
	1	ISA/MCA bus
MD20	NA	Reserved
MD19-MD18	00	Supports 256Kx16 DRAM. Pin 158 is not used
	01	Supports 512Kx8 DRAM. Pin 158 is used as MA9
	10	Reserved
	11	Supports 256Kx4 or 256Kx8 DRAM up to 1MB. Pin 158 is used as NMI.
MD17	0	Selects LA23-20
	1	Selects SA19-17, HAD
MD16	0	8-bit ISA bus
	1	16-bit ISA bus
MD15	NA	Reserved

¹No pull-up resistor required to set a Logical 1 value. Set a Logical 0 value by pulling-down to GND through a 4.7K-10K resistor.

Table 3. MD7-MD0 Definitions

MD	Logic Value ¹	Definition
MD7	0	8-bit BIOS
	1	16-bit BIOS
MD6	0	ROM disabled
	1	ROM enabled
MD5	0	I/O port at 2xx
	1	I/O port at 3xx
MD4	0	MCA bus
	1	ISA bus
MD3-MD0		DIP switch settings ²

¹No pull-up resistor required to set a Logical 1 value. Set a Logical 0 value by pulling-down to GND through a 4.7K-10K resistor.

²Data read into a 4-bit register. The data values can be used by the BIOS or application software.

**Table 4. RMD7-RMD0 Definitions**

RMD	Logic Value ¹	Definition
RMD7	0	8-bit video memory
	1	16-bit video memory
RMD6-RMD5	00	Reserved
	01	8-bit DRAM data bus
	10	16-bit DRAM data bus
	11	32-bit DRAM data bus
RMD4	0	Selects 46E8 for port control
	1	Selects 3C3 for port control
RMD3	0	24K BIOS
	1	32K BIOS
RMD2	1	Reserved
RMD1	0	Standard BIOS wait states
	1	Extended BIOS wait states
RMD0	0	Slow mode address detect
	1	Fast mode address detect

Chip Specifications

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typ.	Maximum	Units
Power Supply Voltage	V _{DD}	4.75	5.0	5.25	V
Input Voltage	V _{IN}	GND		V _{DD}	V
Operating Temperature	T _{OP}	0		70	°C
Storage Temperature	T _{STO}	-40		100	°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

Table 6. DC Specifications

Parameter	Symbol	Minimum	Maximum	Units	Conditions
Input Low Voltage	V _{IL}	GND	0.8	V	V _{DD} =5V
Input High Voltage	V _{IH}	2.0	V _{DD}	V	V _{DD} =5V
Input Low Current	I _{IL}	-	-0.5	μA	V _{IN} =0.0V
Input High Current	I _{IH}	-	20	μA	V _{IN} =V _{DD}
Output Low Voltage	V _{OL}	-	0.4	V	see Note 1
Output High Voltage	V _{OH}	2.4	-	V	see Note 1
High Impedance Leakage	I _{OZ}	-	10.0	μA	V _{SS} <V _{OUT} <V _{DD}
Supply Current	I _{OC}	-	100.0	mA	V _{DD} =5.25V (V _{DD} MAX.)

Note 1: I_{OL}/I_{OZ} = 4/-4 mA for SC4-SC1, ROMCS, EXTCLK, EXENPD, DACRD, DACWR, ESYNC, RS2-RS0. I_{OL}/I_{OZ} = 6/-6 mA for MAA8-MAA0, MAB8-MAB0. I_{OL}/I_{OZ} = 8/-8 mA MD31-MD0, SD15-SD0, IREQ, P7-P0, VSYNC, HSYNC, BLANK, WE3-WE0/CAS3-CAS0, PCLK. I_{OL}/I_{OZ} = 16/-16 mA for RAS, IOCHRDY, NMI, MCS16, ZWS

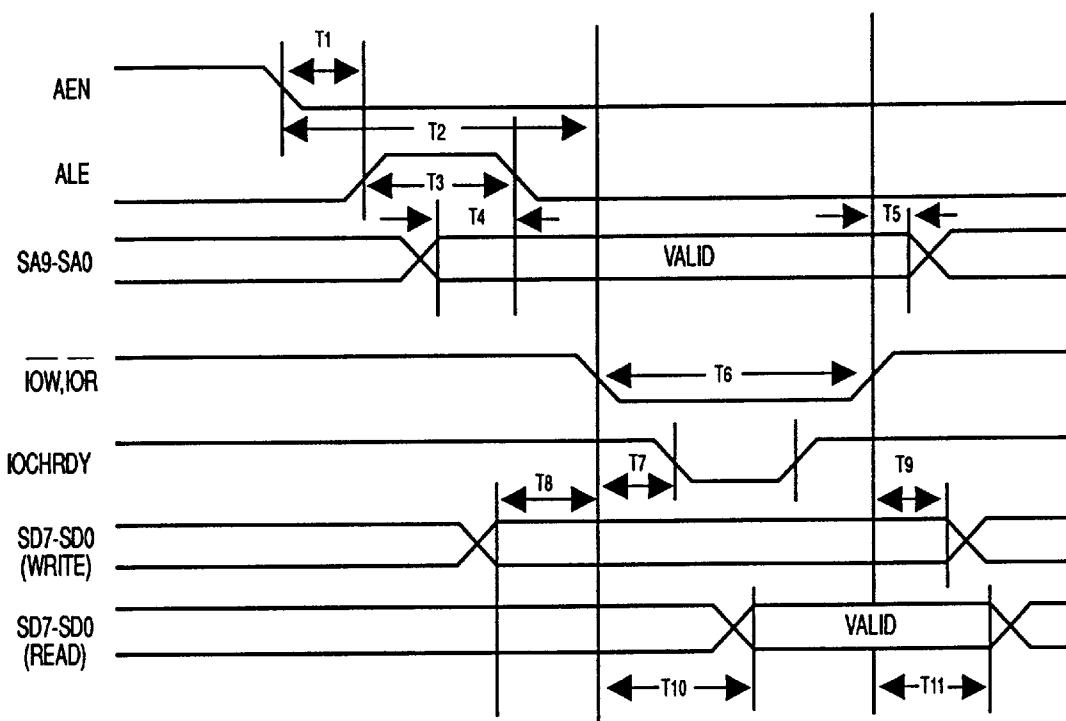


Figure 2. PC/AT ISA Bus I/O Read/Write Timing

Table 7. AC Specifications for ISA Bus I/O Read/Write In Nanoseconds

SYM	Description	Min	Typ	Max
T1	AEN Valid to Rising Edge of ALE	100		
T2	AEN Valid to I/O Command Active	5		
T3	ALE Active to Inactive	15.5		
T4	SA9-SA0 & SBHE Valid to Falling Edge of ALE	29.5		
T5	SA9-SA0 & SBHE Valid Hold From Command Inactive	18		
T6	I/O Command Active		60	
T7	IOCHRDY Inactive From Active Command	10	15	
T8	Valid Write Data Setup to I/O Command Active	4.5	80	
T9	Write Data Valid Hold From I/O Command Inactive	30		
T10	Read Data Valid From Read Command Active		60	
T11	Read Command Inactive to SD7-SD0 Invalid		20	

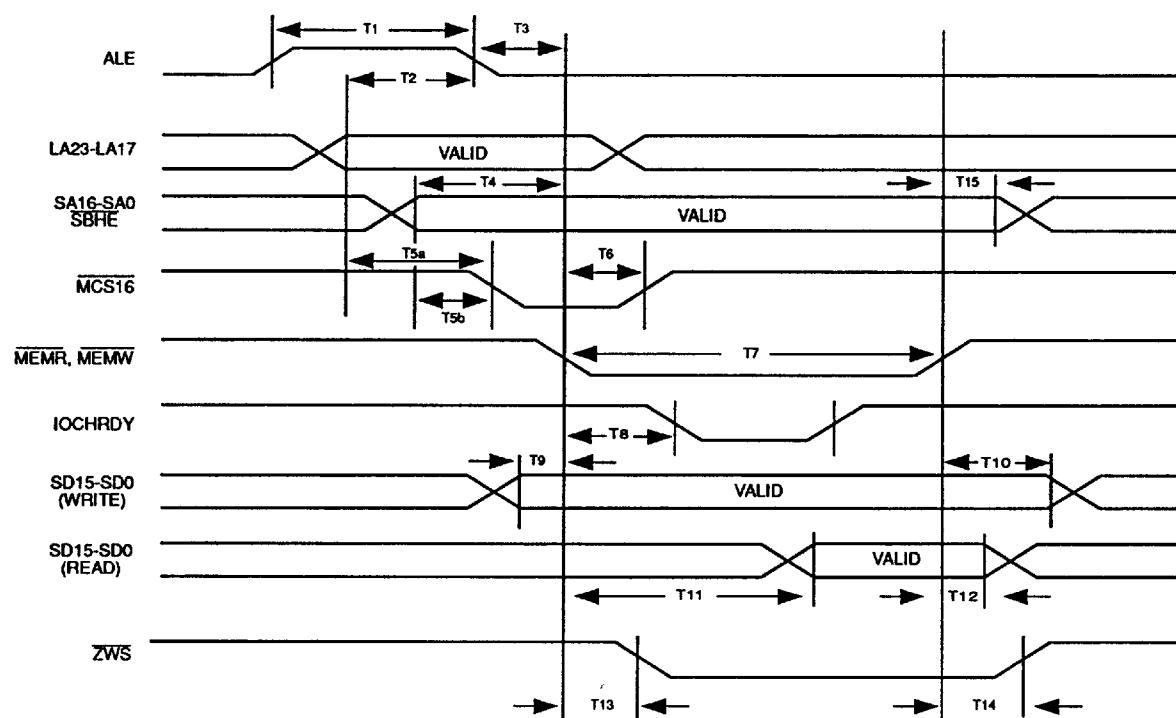


Figure 3. PC/AT ISA Bus Memory Read/Write Timing

Table 8. AC Specifications for ISA Bus Memory Read/Write In Nanoseconds

SYM	Description	Min	Typ	Max
T1	ALE Active to Inactive	15		
T2	LA23-LA17 Valid Setup to Falling Edge of ALE	20		
T3	ALE Inactive to Command Active	20		
T4	SA16-SA0 & SBHE Valid to Memory Command Active	5		
T5a	MCS16 Active From Unlatched Address			20
T5b	MCS16 Active From Latched Address			14
T6	MCS16 Valid Hold From Invalid LA23-LA17			25
T7	Memory Command Active to Inactive	80		
T8	IOCHRDY Inactive From Memory Command Active	10		20
T9	Valid Write Data Setup to Memory Command Active	0		
T10	Write Data Valid Hold From Memory Command Inactive	10		
T11	Valid Read Data From Memory Command Active	0		
T12	Read Command Inactive to SD15-SD0 Invalid			20
T13	ZWS Active From Command Active	8		15
T14	ZWS Inactive From Command Inactive	10		15
T15	Latched Address Hold Time After Command	0		



T V G A 8 9 0 0 D D A T A S H E E T

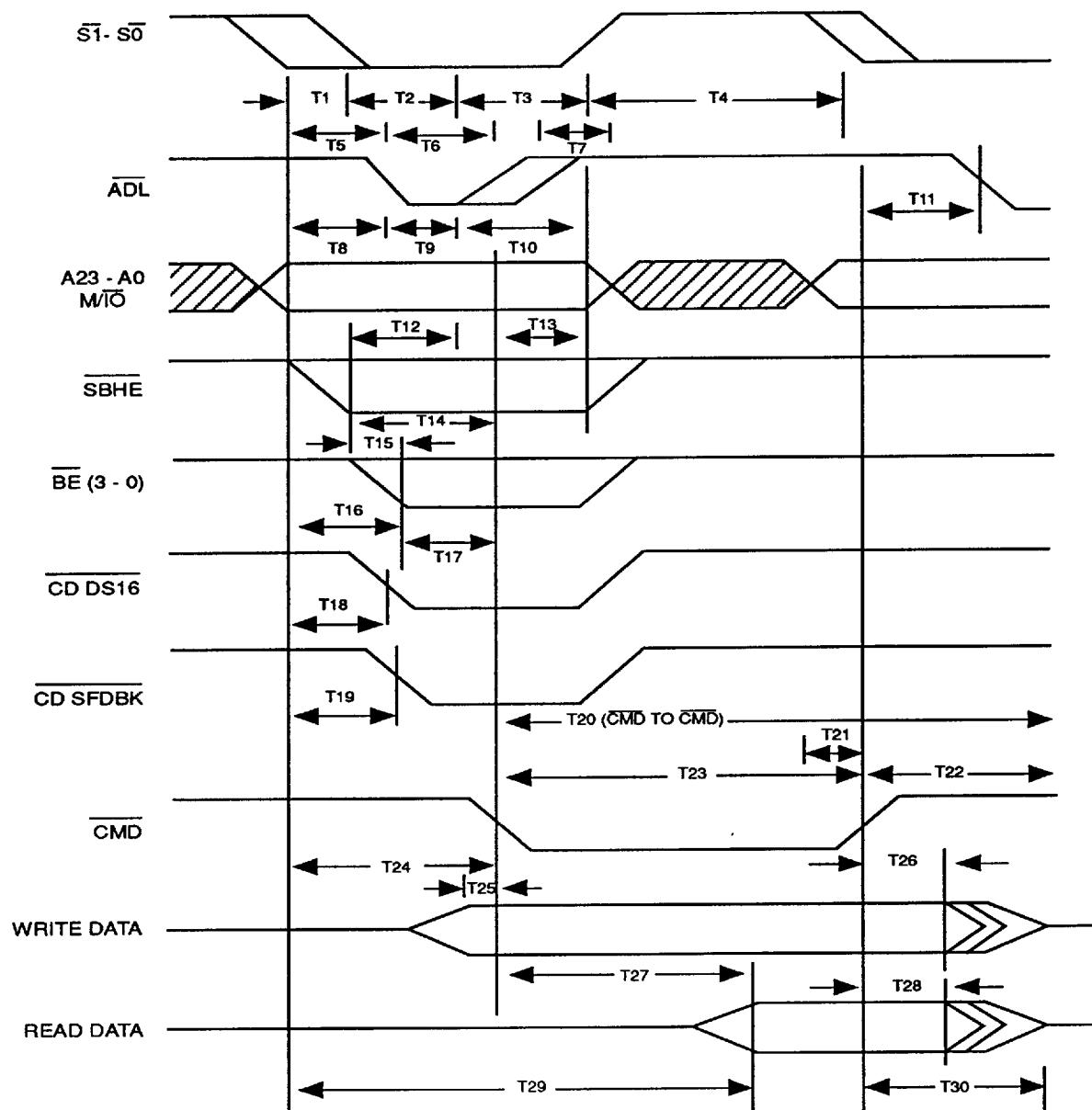


Figure 4. Micro Channel Bus Timing

Table 9. AC Specifications for MCA Bus in Nanoseconds

SYM	Description	Min	Typ	Max
T1	Status Active From ADDRESS, M/I/O, REFRESH	10		
T2	CMD Active From Status Active	55		
T3	Status Hold From CMD Active	30		
T4	Next Status Active From Status Inactive	30		
T5	ADL Active From ADDRESS, M/I/O, REFRESH	45		
T6	ADL Active to CMD Active	40		
T7	ADDRESS, M/I/O, REFRESH, SBHE hold from ADL Inactive	25		
T8	ADL Active from Status Active	12		
T9	ADL Active to Inactive	40		
T10	Status Hold From ADL Inactive	25		
T11	CMD Inactive to next ADL Active	40		
T12	SBHE Setup to ADL Inactive	40		
T13	ADDRESS, M/I/O, REFRESH, SBHE Hold From CMD Active	30		
T14	SBHE Setup to CMD Active	40		
T15	BE3-BE0 Active From SBHE, A0, A1 Active			30
T17	BE3-BE0 Active to CMD Active	10		
T18	CD DS 16 Active (n) From ADDRESS, M/I/O, REFRESH Valid			55
T19	CD SFDBK Active From ADDRESS, M/I/O, REFRESH Valid		60	
T20	CMD Active to Next CMD Active	190		
T21	Next Status Active to CMD Inactive		20	
T22	CMD Inactive to Next CMD Active	80		
T23	CMD Active to Inactive	90		
T24	CMD Active From Address Valid	85		
T25	Write Data Setup to CMD Active	0		
T26	Write Data Hold From CMD Inactive	30		
T27	Read Data Valid From CMD Active		60	
T28	Read Data Hold From CMD Inactive		0	
T29	Status to Read Data Valid			125
T30	Read Data Bus Tri-state From CMD Inactive			40



TVGA 8900D DATA SHEET

Table 10. Vertical and Horizontal Timing

Mode	CLK		Display	Max Colors	VERTICAL				CLK		MAX						
	(MHz)	Type			T1	T2	T3	T4	T5	Polarity	T6	T7	T8	T9	T10	T11	Polarity
0.1	25.2	A/N	40x25	16	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
2,3	25.2	A/N	80x25	16	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
0*,1*	25.2	A/N	40x25	16	3.146	11.122	1.208	14.268	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	+
2*,3*	25.2	A/N	80x25	16	3.146	11.122	1.208	14.268	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	+
0+,1+	28.3	A/N	40x25	16	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
2+,3+	28.3	A/N	80x25	16	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
4,5	25.2	APA	320x200	4	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
6	25.2	APA	640x200	2	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
7	28.3	A/N	80x25	Mono	3.146	11.122	1.208	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	+
7+	28.3	A/N	80x25	Mono	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	+
D	25.2	APA	320x200	16	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
E	25.2	APA	640x200	16	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
F	25.2	APA	640x350	Mono	3.146	11.122	1.208	14.268	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	+
10	25.2	APA	640x350	16	3.146	11.122	1.208	14.268	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	+
11	25.2	APA	640x480	2	1.430	15.253	0.350	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
12	25.2	APA	640x480	16	1.430	15.253	0.350	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
13	25.2	APA	320x200	256	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.477	2.066	3.813	31.778	-
50	25.2	A/N	80x30	16	1.430	15.253	0.350	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
51	25.2	A/N	80x43	16	1.652	15.031	0.540	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
52	25.2	A/N	80x60	16	1.430	15.253	0.350	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
53	40.0	A/N	132x25	16	3.168	11.200	1.248	14.368	0.064	-	5.600	26.400	0.000	1.800	3.800	32.000	+
54	40.0	A/N	132x30	16	1.376	15.360	0.352	16.736	0.064	-	5.600	26.400	0.000	1.800	3.800	32.000	-
55	40.0	A/N	132x43	16	1.600	15.136	0.576	16.736	0.064	-	5.600	26.400	0.000	1.800	3.800	32.000	-
56	40.0	A/N	132x60	16	1.376	15.360	0.352	16.736	0.064	-	5.600	26.400	0.000	1.800	3.800	32.000	-
57	44.9	A/N	132x25	16	3.079	11.225	1.219	14.304	0.064	-	5.612	26.459	-0.200	1.804	4.009	32.071	+
58	44.9	A/N	132x30	16	1.315	15.394	0.321	16.709	0.064	-	5.612	26.459	-0.200	1.804	4.009	32.071	-
59	44.9	A/N	132x43	16	1.539	15.170	0.417	16.709	0.064	-	5.612	26.459	-0.200	1.804	4.009	32.071	-
5A	44.9	A/N	132x60	16	1.315	15.394	0.321	16.709	0.064	-	5.612	26.459	-0.200	1.804	4.009	32.071	-
5B	36.0	APA	800x600	16	0.711	17.067	0.028	17.715	0.057	-	6.222	22.222	0.667	3.500	2.028	28.660	-
5B	50.35	APA	800x600	16	1.395	12.489	0.479	13.883	0.125	+	4.926	15.889	0.794	2.066	2.066	20.814	+
SC	50.35	APA	640x400	256	1.557	12.711	0.413	14.268	0.064	+	6.356	25.422	0.556	1.668	4.131	31.778	-
5C	25.2	APA	640x400	256	1.577	12.711	0.413	14.268	0.064	+	6.356	25.422	0.636	1.907	3.813	31.778	-
SD	50.35	APA	640x480	256	1.430	15.253	0.350	16.683	0.064	-	6.356	25.422	0.556	1.668	4.131	31.778	-
SD ¹	25.2	APA	640x480	256	1.430	12.253	0.350	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
SE	72.0	APA	800x600 (I)	256	0.711	17.067	0.028	17.778	0.057	-	6.222	22.222	0.667	3.500	2.028	28.660	-
SE ¹	36.0	APA	800x600 (NI)	256	0.711	17.067	0.028	17.778	0.057	-	6.222	22.222	0.667	3.500	2.028	28.660	-
SE ²	50.3	APA	800x600 (NI)	256	1.395	12.489	0.479	13.883	0.125	+	4.926	15.889	0.794	2.066	2.066	20.814	+
SF ¹	44.9	APA	1024x768 (I)	16	0.873	10.810	0.155	11.683	0.056	+	5.345	22.806	0.204	1.260	3.956	28.151	+
SF	65.0	APA	1024x768 (NI)	16	0.945	15.785	0.329	16.731	0.041	+	4.800	15.754	0.615	1.108	3.077	20.554	+
SF ²	75.0	APA	1024x768	16	0.673	13.599	0.053	14.272	0.106	+	4.053	13.653	0.320	1.920	1.813	17.707	+
60	44.9	APA	1024x768 (I)	4	0.873	10.810	0.155	11.683	0.056	+	5.345	22.806	1.069	1.782	2.494	28.151	+
61	44.9	APA	768x1024 (I)	16	0.791	13.501	0.119	14.292	0.040	+	9.265	17.105	-1.782	4.633	4.811	26.370	+
62	44.9	APA	1024x768 (I)	256	0.873	10.810	0.155	11.683	0.056	+	5.345	22.806	-1.78	2.851	2.316	28.151	+
62	65.0	APA	1024x768 (NI)	256	0.945	15.785	0.329	16.731	0.041	+	4.800	15.754	0.615	1.108	3.077	20.554	+
62 ²	75.0	APA	1024x768	256	0.673	13.599	0.053	14.272	0.106	+	4.053	13.653	0.320	1.920	1.813	17.707	+
63	75.0	APA	1280x1024	16	1.120	10.705	0.379	11.835	0.084	+	3.765	17.035	0.255	0.205	3.400	21.000	+
6C	75.0	APA	640x480	16M	1.430	15.253	0.350	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
70/71	77.0	APA	512x480	32/64K	1.430	15.253	0.350	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
74/75	50.35	APA	640x480	32/64K	1.430	15.253	0.350	16.683	0.064	-	6.356	25.422	0.636	1.907	3.813	31.778	-
76/77	72.0	APA	800x600	32/64K	0.711	17.067	0.028	17.715	0.057	-	6.222	22.222	0.667	3.500	2.028	28.660	-

¹Same timing for 32K and 64K color modes²Based on VESA (Video Electronics Standards Association) standards VS900502 and VS910801

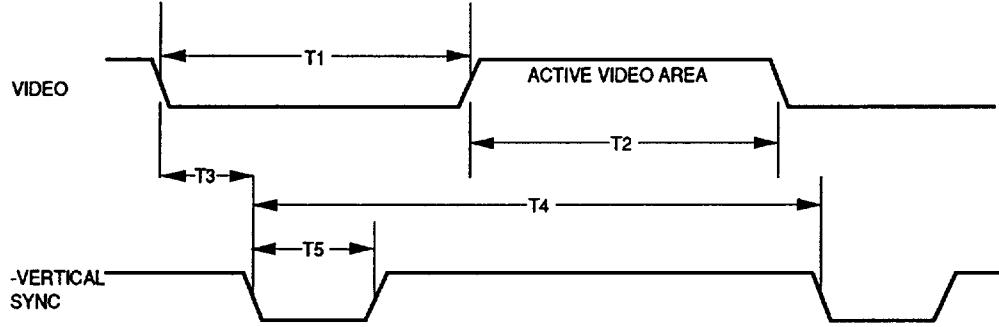
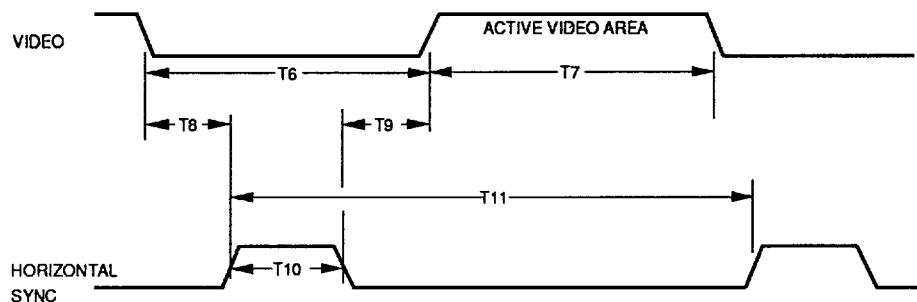
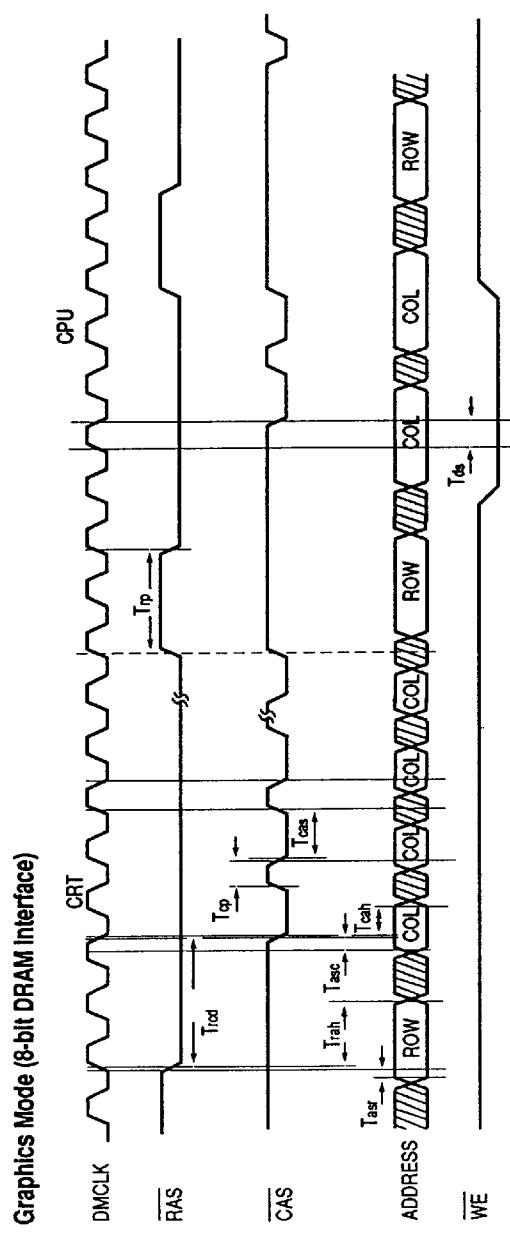


Figure 5-A. Vertical Timing (ms)

Figure 5-B. Horizontal Timing (μ s)



Graphics Mode (16/32-bit DRAM Interface)

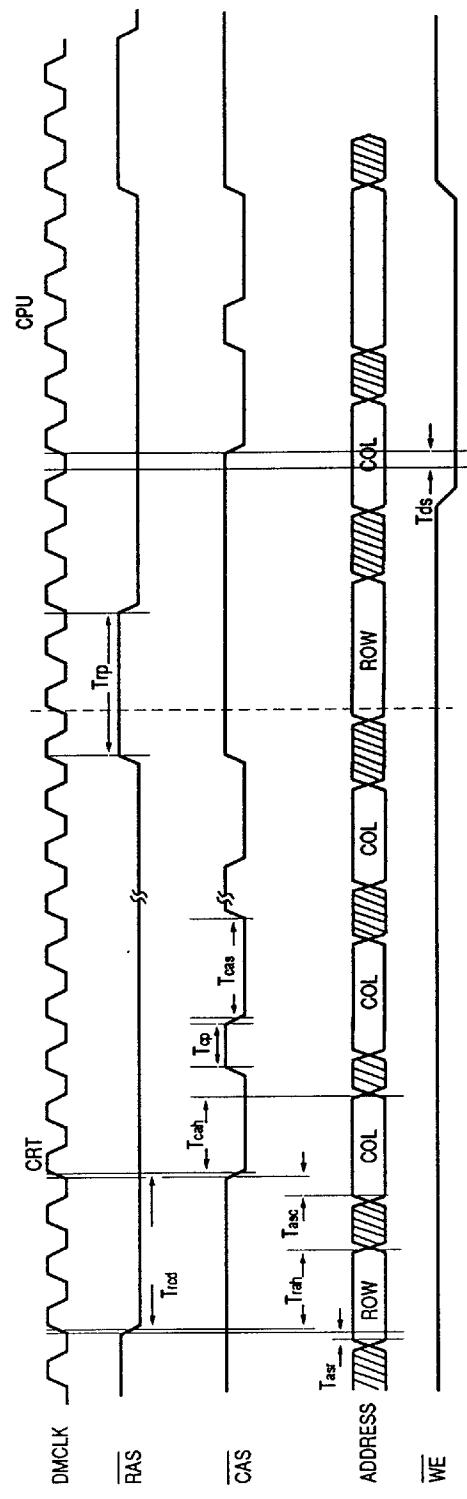


Figure 6-A. Trident TVGA8900D DRAM Timing (Graphics)

T V G A 8 9 0 0 D DATA SHEET

Trident

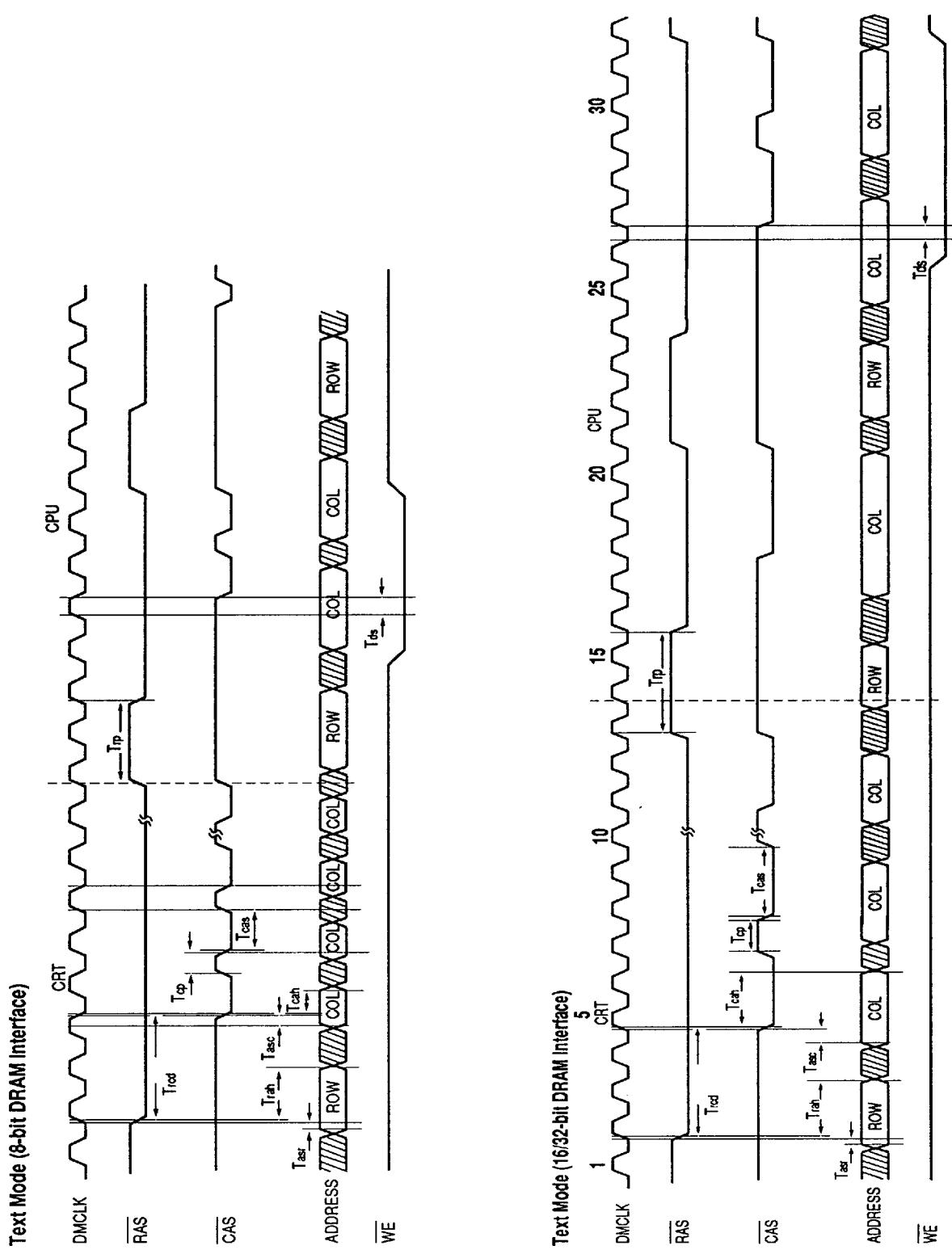


Figure 6-B. Trident TVGA8900D DRAM Timing (Text)

Table 11. Worst Case Memory Timing Parameters¹

Parameter	8 bit DRAM Interface	16 bit DRAM Interface	32 bit DRAM Interface
Trcd 1	$2.5t + 1.5ns$	$3t + 1.5ns$	$3t + 3ns$
Trah 2	$1.5t + 2ns$	$2t + 2ns$	$2t + 2ns$
Tasr 3	≥ 0	≥ 0	≥ 0
Tasc 4	$\geq 0.5t$	$\geq t$	$\geq t$
Tcah 5	t	$2t$	$2t$
Tcp 6	$0.5t - 2.5ns$	$t - 5ns$	$t - 6ns$
Tcas 7	$t - 4ns$	$2t - 6.5ns$	$2t - 10ns$
Tds 8	≥ 0	≥ 0	≥ 0
Trp 9	$2t - 1.5ns$	$3t - 4ns$	$3t - 6ns$
Test Load	25pf	50pf	85pf

*(t=1/DMCLK)

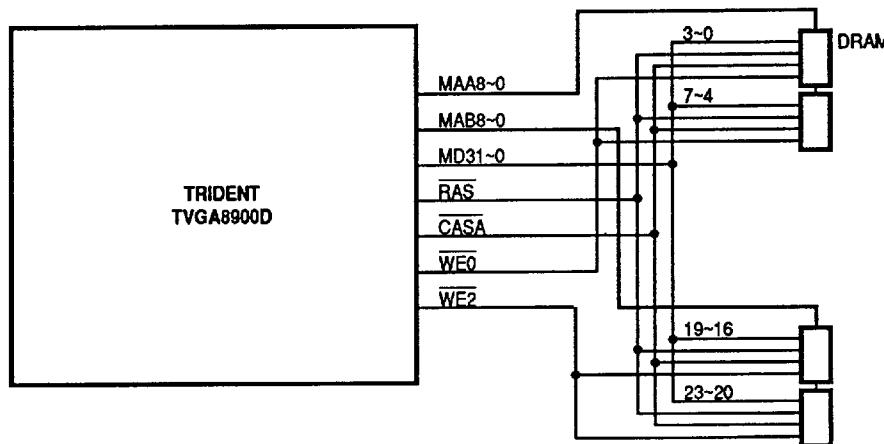


Figure 7-A. Application For Four 256Kx4 DRAM (ISA Bus)

T V G A 8 9 0 0 D D A T A S H E E T

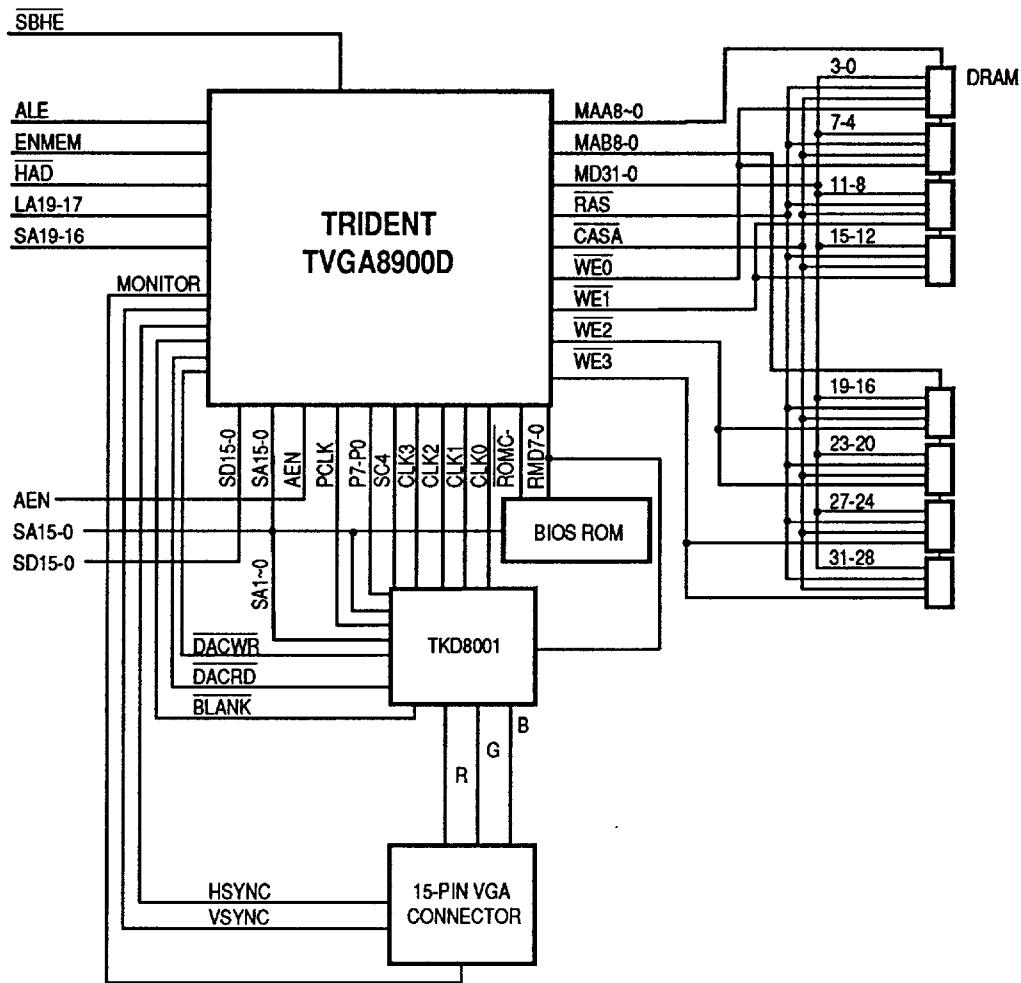
 Trident


Figure 7-B. Application For Eight 256Kx4 DRAM (ISA Bus)


Trident
T V G A 8 9 0 0 D D A T A S H E E T

VSS	121	VDD	119	SD8	118	SD9	117	SD10	116	SD11	115	SD12	114	SD13	113	SD14	112	SD15	111	VSS	110	DNCLK	109	CLK10	108	CLK1SC3	107	CLK2SC1	106	CLK3SC2	105	MD31	104	MD30	103	MD29	102	MD28	101	VSS	100	VDD	99	MD27	98	MD26	97	MD25	96	MD24	95	MD23	94	MD22	93	MD21	92	MD20	91	MD19	90	MD18	89	MD17	88	MD16	87	WE1CASA1	86	WE1CASA1	85	WE2CASA2	84	WE3CASA3	83	RAS	82	CAS/WAE	81	VDD	80	VSS	79	VSYNC	78	MAB8	77	MAB7	76	MAB6	75	MAB5	74	MAB4	73	MAB3	72	MAB2	71	MAB1	70	MAB0	69	MD15	68	MD14	67	MD13	66	MD12	65	VSS	64	MD11	63	MD10	62	MD9	61	MD8	60	MD7	59	MD6	58	MD5	57	MD4	56	MD3	55	MD2	54	MD1	53	MD0	52	VSS	51	MAA8	50	MAA7	49	MAA6	48	MAA5	47	MAA4	46	MAA3	45	MAA2	44	MAA1	43	MAA0	42	FSYNC	41	VSS																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																			
VDD	2	SD0	3	SD1	4	SD2	5	SD3	6	SD4	7	SD5	8	SD6	9	SD7	10	I/O	11	RONBAO	12	RONICS	13	VSS	14	P0	15	P1	16	P2	17	P3	18	P4	19	P5	20	P6	21	VSS	22	P7	23	P8	24	P9	25	P10	26	P11	27	P12	28	P13	29	P14	30	P15	31	P16	32	P17	33	P18	34	P19	35	P20	36	P21	37	P22	38	P23	39	P24	40	P25	41	P26	42	P27	43	P28	44	P29	45	P30	46	P31	47	P32	48	P33	49	P34	50	P35	51	P36	52	P37	53	P38	54	P39	55	P30	56	P31	57	P32	58	P33	59	P34	60	P35	61	P36	62	P37	63	P38	64	P39	65	P30	66	P31	67	P32	68	P33	69	P34	70	P35	71	P36	72	P37	73	P38	74	P39	75	P30	76	P31	77	P32	78	P33	79	P34	80	P35	81	P36	82	P37	83	P38	84	P39	85	P30	86	P31	87	P32	88	P33	89	P34	90	P35	91	P36	92	P37	93	P38	94	P39	95	P30	96	P31	97	P32	98	P33	99	P34	100	P35	101	P36	102	P37	103	P38	104	P39	105	P30	106	P31	107	P32	108	P33	109	P34	110	P35	111	P36	112	P37	113	P38	114	P39	115	P30	116	P31	117	P32	118	P33	119	P34	120	P35	121	P36	122	P37	123	P38	124	P39	125	P30	126	P31	127	P32	128	P33	129	P34	130	P35	131	P36	132	P37	133	P38	134	P39	135	P30	136	P31	137	P32	138	P33	139	P34	140	P35	141	P36	142	P37	143	P38	144	P39	145	P30	146	P31	147	P32	148	P33	149	P34	150	P35	151	P36	152	P37	153	P38	154	P39	155	P30	156	P31	157	P32	158	P33	159	P34	160	P35	161	P36	162	P37	163	P38	164	P39	165	P30	166	P31	167	P32	168	P33	169	P34	170	P35	171	P36	172	P37	173	P38	174	P39	175	P30	176	P31	177	P32	178	P33	179	P34	180	P35	181	P36	182	P37	183	P38	184	P39	185	P30	186	P31	187	P32	188	P33	189	P34	190	P35	191	P36	192	P37	193	P38	194	P39	195	P30	196	P31	197	P32	198	P33	199	P34	200	P35	201	P36	202	P37	203	P38	204	P39	205	P30	206	P31	207	P32	208	P33	209	P34	210	P35	211	P36	212	P37	213	P38	214	P39	215	P30	216	P31	217	P32	218	P33	219	P34	220	P35	221	P36	222	P37	223	P38	224	P39	225	P30	226	P31	227	P32	228	P33	229	P34	230	P35	231	P36	232	P37	233	P38	234	P39	235	P30	236	P31	237	P32	238	P33	239	P34	240	P35	241	P36	242	P37	243	P38	244	P39	245	P30	246	P31	247	P32	248	P33	249	P34	250	P35	251	P36	252	P37	253	P38	254	P39	255	P30	256	P31	257	P32	258	P33	259	P34	260	P35	261	P36	262	P37	263	P38	264	P39	265	P30	266	P31	267	P32	268	P33	269	P34	270	P35	271	P36	272	P37	273	P38	274	P39	275	P30	276	P31	277	P32	278	P33	279	P34	280	P35	281	P36	282	P37	283	P38	284	P39	285	P30	286	P31	287	P32	288	P33	289	P34	290	P35	291	P36	292	P37	293	P38	294	P39	295	P30	296	P31	297	P32	298	P33	299	P34	300	P35	301	P36	302	P37	303	P38	304	P39	305	P30	306	P31	307	P32	308	P33	309	P34	310	P35	311	P36	312	P37	313	P38	314	P39	315	P30	316	P31	317	P32	318	P33	319	P34	320	P35	321	P36	322	P37	323	P38	324	P39	325	P30	326	P31	327	P32	328	P33	329	P34	330	P35	331	P36	332	P37	333	P38	334	P39	335	P30	336	P31	337	P32	338	P33	339	P34	340	P35	341	P36	342	P37	343	P38	344	P39	345	P30	346	P31	347	P32	348	P33	349	P34	350	P35	351	P36	352	P37	353	P38	354	P39	355	P30	356	P31	357	P32	358	P33	359	P34	360	P35	361	P36	362	P37	363	P38	364	P39	365	P30	366	P31	367	P32	368	P33	369	P34	370	P35	371	P36	372	P37	373	P38	374	P39	375	P30	376	P31	377	P32	378	P33	379	P34	380	P35	381	P36	382	P37	383	P38	384	P39	385	P30	386	P31	387	P32	388	P33	389	P34	390	P35	391	P36	392	P37	393	P38	394	P39	395	P30	396	P31	397	P32	398	P33	399	P34	400	P35	401	P36	402	P37	403	P38	404	P39	405	P30	406	P31	407	P32	408	P33	409	P34	410	P35	411	P36	412	P37	413	P38	414	P39	415	P30	416	P31	417	P32	418	P33	419	P34	420	P35	421	P36	422	P37	423	P38	424	P39	425	P30	426	P31	427	P32	428	P33	429	P34	430	P35	431	P36	432	P37	433	P38	434	P39	435	P30	436	P31	437	P32	438	P33	439	P34	440	P35	441	P36	442	P37	443	P38	444	P39	445	P30	446	P31	447	P32	448	P33	449	P34	450	P35	451	P36	452	P37	453	P38	454	P39	455	P30	456	P31	457	P32	458	P33	459	P34	460	P35	461	P36	462	P37	463	P38	464	P39	465	P30	466	P31	467	P32	468	P33	469	P34	470	P35	471	P36	472	P37	473	P38	474	P39	475	P30	476	P31	477	P32	478	P33	479	P34	480	P35	481	P36	482	P37	483	P38	484	P39	485	P30	486	P31	487	P32	488	P33	489	P34	490	P35	491	P36	492	P37	493	P38	494	P39	495	P30	496	P31	497	P32	498	P33	499	P34	500	P35	501	P36	502	P37	503	P38	504	P39	505	P30	506	P31	507	P32	508	P33	509	P34	510	P35	511	P36	512	P37	513	P38	514	P39	515	P30	516	P31	517	P32	518	P33	519	P34	520	P35	521	P36	522	P37	523	P38	524	P39	525	P30	526	P31	527	P32	528	P33	529	P34	530	P35	531	P36	532	P37	533	P38	534	P39	535	P30	536	P31	537	P32	538	P33	539	P34	540	P35	541	P36	542	P37	543	P38	544	P39	545	P30	546	P31	547	P32	548	P33	549	P34	550	P35	551	P36	552	P37	553	P38	554	P39	555	P30	556	P31	557	P32	558	P33	559	P34	560	P35	561	P36	562	P37	563	P38	564	P39	565	P30	566	P31	567	P32	568	P33	569	P34	570	P35	571	P36	572	P37	573	P38	574	P39	575	P30	576	P31	577	P32	578	P33	579	P34	580	P35	581	P36	582	P37	583	P38	584	P39	585	P30	586	P31	587

TVGA8900D DATA SHEET

 Trident

VSS	121	120	VDD	D8	D9	D10	D11	D12	D13	D14	D15	VSS	DMCLK	CLKO	CLK1/SCA	CLK2/SC1	CLK3/SC2	MD31	MD30	MD29	MD28	VSS	YDD	MD27	MD26	MD25	MD24	MD23	MD22	MD21	MD20	MD19	MD18	MD17	MD16	WE0/CASA0	WE1/CASA1	WE2/CASA2	WE3/CASA3	RAS	CAS/W	VDD	80	VSS
SC4	122																																				79	VSYNC						
PCLK	123																																				78	MAB8						
SBHE	124																																				77	MAB7						
ADL	125																																				76	MAB6						
A17	126																																				75	MAB5						
A18	127																																				74	MAB4						
A19	128																																				73	MAB3						
A20	129																																				72	MAB2						
A21	130																																				71	MAB1						
A22	131																																				70	MAB0						
A23	132																																				69	MD15						
A0	133																																				68	MD14						
A1	134																																				67	MD13						
A2	135																																				66	MD12						
A3	136																																				65	VSS						
A4	137																																				64	MD11						
A5	138																																				63	MD10						
A6	139																																				62	MD9						
A7	140																																				61	MD8						
A8	141																																				60	MD7						
A9	142																																				59	MD6						
A10	143																																				58	MD5						
A11	144																																				57	MD4						
A12	145																																				56	MD3						
A13	146																																				55	MD2						
A14	147																																				54	MD1						
A15	148																																				53	MD0						
A16	149																																				52	VSS						
ENMEM	150																																				51	MAA8						
SI	151																																				50	MAA7						
CMD	152																																				49	MAA6						
MJO	153																																				48	MAA5						
S0	154																																				47	MAA4						
CD SETUP	155																																				46	MAA3						
CD CHRDY	156																																				45	MAA2						
RESET	157																																				44	MAA1						
NMI/MA9	158																																				43	MAA0						
CD DS16	159																																				42	ESYNC						
VSS	160																																				41	VSS						

Figure 8-B. TVGA8900D Pin-Out (MCA Bus)



Table 12. TVGA8900D Pin Description

Pin	Pin Type	Pin Number	Description
<i>Host Interface</i>			
<i>a. AT Bus Signals</i>			
<u>IOR</u>	I	151	I/O read strobe
<u>IOW</u>	I	152	I/O write strobe
<u>MEMR</u>	I	153	Memory read strobe
<u>MEMW</u>	I	154	Memory write strobe
<u>IOCHRDY</u>	O	156	I/O channel ready
<u>ALE</u>	I	125	System address latch enable
<u>AEN</u>	I	155	Enable on-board I/O
<u>LA19-LA17</u>	I	128-126	Unlatched address bus, bit 19 to bit 17
<u>SA19-SA17¹</u>	I	131-129	Address bus, bit 19 to bit 17 (Unlatched address bus, bit 22 to bit 20)
<u>(LA22-LA20)</u>			
<u>HAD(LA23)</u>	I	132	High address (Unlatched address bus bit 23)
<u>SA16-SA0</u>	I	149-133	Address Bus
<u>MCS16</u>	O	159	Enable 16-bit transfer, open drain output
<u>SD15-SD0</u>	I/O	112-119,9-2	Data bus, bit 15 to bit 0
<u>ZWS</u>	O	37	Zero wait state
<u>IRQ</u>	O	10	Interrupt request
<u>SBHE</u>	I	124	Bus high-byte enable
<u>ENMEM</u>	I	150	Enable display memory
<i>b. MCA Bus Signals</i>			
<u>S1-S0</u>	I	151,154	Status bit 1-0
<u>CMD</u>	I	152	Command
<u>M/I/O</u>	I	153	Bus memory or I/O cycle
<u>CD CHRDY</u>	O	156	Channel ready
<u>CD SETUP</u>	I	155	Card setup
<u>A23-A0</u>	I	132-126,149-133	System address bus, bit 23 to bit 0
<u>CD DS16</u>	O	159	Card data size 16-bit
<u>D15-D0</u>	I/O	112-119,9-2	System data bus, bit 15 to bit 0
<u>CD SFDBK</u>	O	37	Card select feedback
<u>IRQ</u>	O	10	Interrupt request
<u>SBHE</u>	I	124	Bus high-byte enable
<u>ENMEM</u>	I	150	Enable display memory
<u>ADL</u>	I	125	Address decode latch
<i>Common Bus Signals</i>			
<u>RESET</u>	I	157	System reset (active high); the falling edge latches configuration information into internal registers from memory data lines and AD7-AD0



Table 12. TVGA8900D Pin Description - Continued

Pin	Pin Type	Pin Number	Description
NMI/MA9	O	158	Non-maskable interrupt/additional address bus for 1MB of 512Kx8 or 256Kx16 DRAM chips
<i>Display Memory Interface</i>			
CASA/WE	O	82	Column address strobe for Bank A/memory write enable for DRAM requires multiple CAS and one memory write
WE3-WE0/ CASA3-CASA0	O	84-87	Write enable/column address strobe for Bank A when DRAM requires multiple CAS and one memory write
RAS	O	83	Row address strobe
MAA8-MAA0	O	51-43	Multiplexing address bus of display memory Bank A
MAB8-MAB0	O	78-70	Multiplexed address bus of display memory Bank B
MD31-MD0	I/O	105-102,99-88 69-66,64-53	Memory data bus (bit 31 to bit 0)
DMCLK	I	110	DRAM clock
<i>Video Interface</i>			
VSYNC	O	79	Vertical synchronization pulse, polarity programmable
Hsync	O	36	Horizontal synchronization pulse, polarity programmable
RMD7-RMD0	I/O	24-31	ROM/DAC data bus bit 7 to bit 0
P7-P0	O	23-22,19-14	Video DAC address, bit 7 to bit 0
PCLK	O	123	Pixel clock output
BLANK	O	32	Blank output
DACRD	O	33	DAC read strobe
DACWR	O	34	DAC write strobe
MONITOR	I	35	Monitor type detect (analog monitor)
EVIDEO/RS2	I/O	38	External pixel data enable (feature connector)/extra DAC address (for true color mode)
EDCLK/RS3	I/O	39	External clock enable (feature connector)/extra DAC address (for true color mode)
ESYNC	I/O	42	External sync enable (feature connector)
<i>Clock Synthesizer Interface</i>			
CLK1/SC3	I/O	108	Video clock input/Clock select output 3
CLK2/SC1	I/O	107	Video clock input/Clock select output 1
CLK3/SC2	I/O	106	Video clock input/Clock select output 2
CLK0	I	109	Video clock input
SC4	O	122	Clock select, output connect to pin 1 of TCK9004
<i>BIOS Interface</i>			
ROMCS	O	12	BIOS EPROM chip select



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Table 12. TVGA8900D Pin Description - Continued

Pin	Pin Type	Pin Number	Description
ROMBA0	O	11	BIOS EPROM address bit 0
<i>Other External Interfaces</i>			
MONITOR	I	35	Monitor type detect (analog monitors)
<i>Power Pins</i>			
VSS	GND	13,21,41,52,65,80 101,111,121,160	Ground
VDD	PWR	1,20,40,81,100,120	+5VDC

¹Pins definition in parentheses are for linear addressing

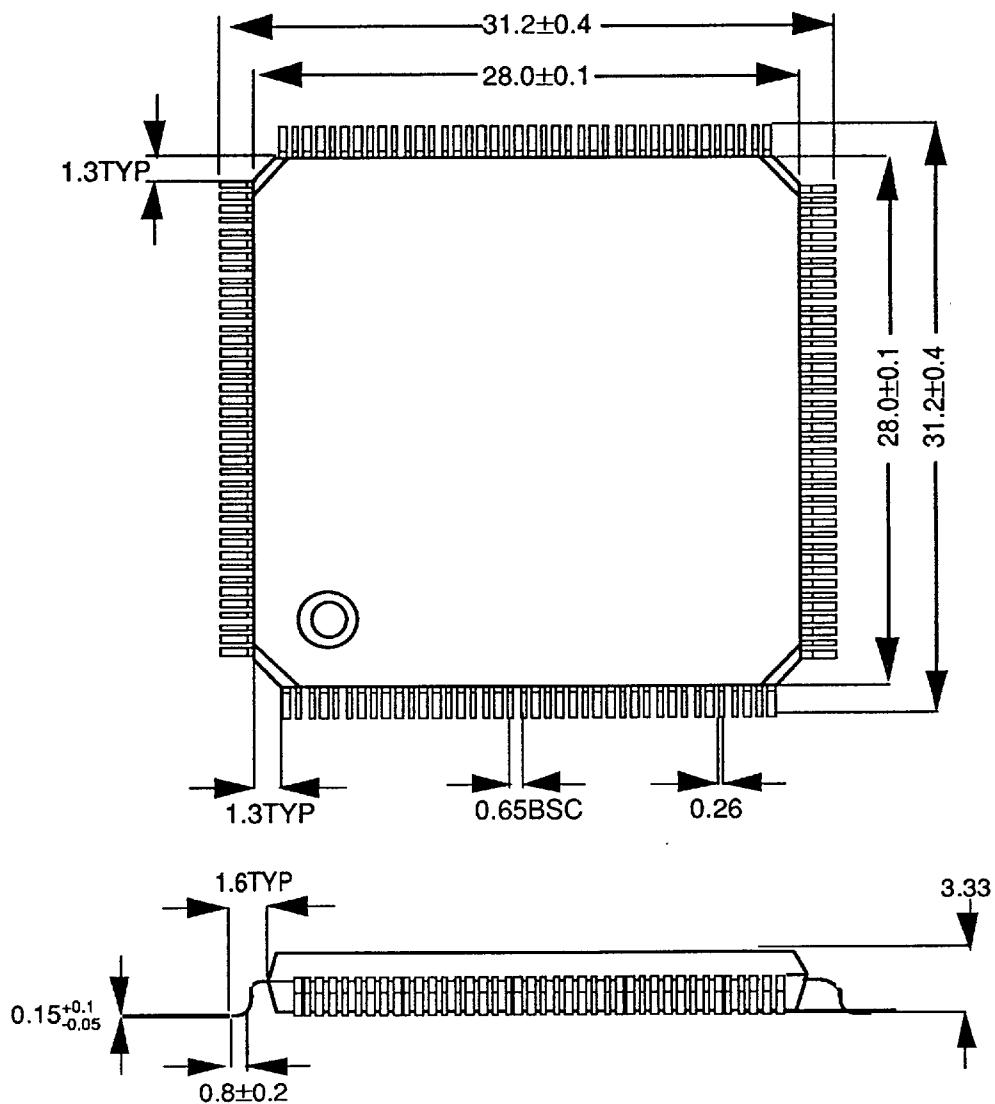


Figure 9. TVGA8900D Packaging PFP 160 Pins (dimensions in mm)