S75WS256Nxx Based MCPs

Stacked Multi-Chip Product (MCP)
256 Megabit (16M x 16-bit) CMOS 1.8 Volt-only Simultaneous Read/Write, Burst-mode Flash Memory with 128 Mb (8M x 16-Bit) CellularRAM and 512 Mb (32M x 16-bit) Data Storage

Data Sheet **PRELIMINARY**

Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See Notice On Data Sheet Designations for definitions.

Publication Number S75WS-N-00 **Revision** A **Amendment** 0 **Issue Date** February 17, 2005

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Data Sheet

PRELIMINARY

General Description

The S75WS-N Series is a product line of stacked Multi-Chip Product (MCP) packages and consists of the following items:

- One or more S29WSxxxN code Flash
- CellularRAM
- One or more S29RS-N data storage Flash

The products covered by this document are listed in the table below:

Device	Code Flash Density	RAM Density	Data Storage Flash Density
	256 Mb	128 Mb	512 Mb
S75WS256NDF	■	■	■

Distinctive Characteristics

MCP Features

- **Power supply voltage of 1.7 V to 1.95 V**
- **High Performance**
  - — 54 MHz, 66 MHz
- **Packages**
  - — 9 x 12 mm 84 ball FBGA
- Operating Temperature
  - — Wireless, –25°C to +85°C

Publication Number S75WS-N-00 **Revision** A **Amendment** 0 **Issue Date** February 17, 2005

Notice On Data Sheet Designations

Spansion LLC issues data sheets with Advance Information or Preliminary designations to advise readers of product information or intended specifications throughout the product life cycle, including development, qualification, initial production, and full production. In all cases, however, readers are encouraged to verify that they have the latest information before finalizing their design. The following descriptions of Spansion data sheet designations are presented here to highlight their presence and definitions.

Advance Information

The Advance Information designation indicates that Spansion LLC is developing one or more specific products, but has not committed any design to production. Information presented in a document with this designation is likely to change, and in some cases, development on the product may discontinue. Spansion LLC therefore places the following conditions upon Advance Information content:

> "This document contains information on one or more products under development at Spansion LLC. The information is intended to help you evaluate this product. Do not design in this product without contacting the factory. Spansion LLC reserves the right to change or discontinue work on this proposed product without notice."

Preliminary

The Preliminary designation indicates that the product development has progressed such that a commitment to production has taken place. This designation covers several aspects of the product life cycle, including product qualification, initial production, and the subsequent phases in the manufacturing process that occur before full production is achieved. Changes to the technical specifications presented in a Preliminary document should be expected while keeping these aspects of production under consideration. Spansion places the following conditions upon Preliminary content:

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Combination

Some data sheets will contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document will distinguish these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with the DC Characteristics table and the AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion LLC applies the following conditions to documents in this category:

> "This document states the current technical specifications regarding the Spansion product(s) described herein. Spansion LLC deems the products to have been in sufficient production volume such that subsequent versions of this document are not expected to change. However, typographical or specification corrections, or modifications to the valid combinations offered may occur."

Questions regarding these document designations may be directed to your local AMD or Fujitsu sales office.

Contents

Tables

Figures

1 Product Selector Guide

Device	Model Numbers	MCP Configuration: Code Flash	MCP Configuration: Code pSRAM (Mb)	MCP Configuration: Data Storage Flash	Code Flash Density (Mb)	RAM Density (Mb)	Data Storage Flash Density (Mb/Gb)	Flash Speed (MHz)	pSRAM Speed (MHz)	DYB Power-Up State (See Note)	pSRAM (Cellular RAM) Supplier	Package 84 ball FBGA (mm)
S75WS256NDF	MA	WS256N	128	RS512N	256	128	512 Mb	54	54	0	2	9x12
	PA									1		
	MB							66	66	0		
	PB									1		

Note: *0 (Protected), 1 (Unprotected [Default State])*

2 Ordering Information

The ordering part number is formed by a valid combination of the following:

S75WS 256 N D F BA W M A

RAM Supplier; Speed Combination
A = Cellular RAM2, 54 MHz
B = Cellular RAM2, 66 MHz

Package Dimensions and Ball Count; DYB Power Up; Flash Device Family (Data Storage)
M = 1.4 mm, 9 x 12, 84 ball; 0; RS
P = 1.4 mm, 9 x 12, 84 ball; 1; RS

Temperature Range
W = Wireless (–25°C to +85°C)

Package Type And Material
BA = Very Thin Fine-Pitch Ball Grid Array (BGA), Lead (Pb)-free Compliant Package
BF = Very Thin Fine-Pitch Ball Grid Array (BGA), Lead (Pb)-free Package

Data Storage Density
F = 512 Mb

Code Flash Density
D = 128 Mb

Process Technology
N = 110 nm, Mirror Bit Technology

Flash Density
256 = 256 Mb

Device Family
S75WS = Multi-chip Product (MCP)
1.8-volt Burst Mode Flash Memory, RAM, and NAND Data Storage

Table 2.1 MCP Configurations and Valid Combinations

Valid Combinations						
S75WS256N	D	F	BA, BF	W	M, P	A, B

Package Marking Note:

The BGA package marking omits the leading S75 and packing type designator from the ordering part number.

Valid Combinations

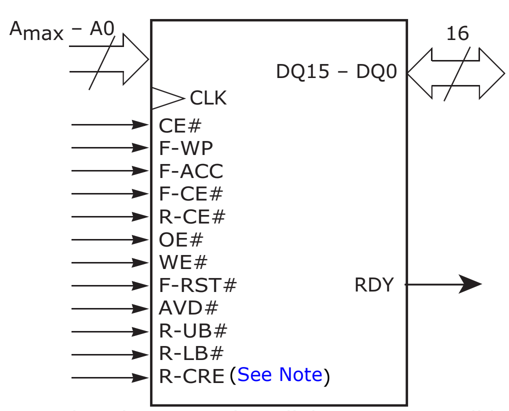
Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

3 Input/Output Descriptions and Logic Symbol

Table 3.1 identifies the input and output package connections provided on the device.

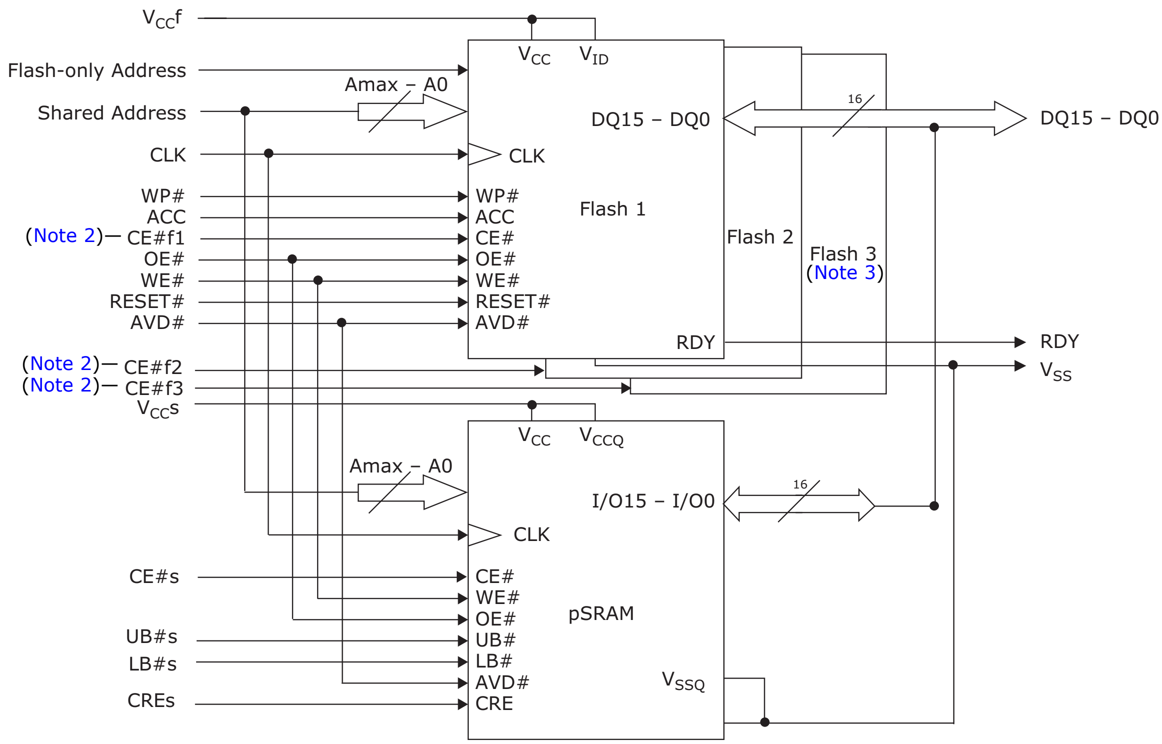
Table 3.1 Input/Output Descriptions

Symbol	Description	
A_{max} – A0	Address Inputs	
DQ15 - DQ0	Data Inputs/Outputs	
OE#	Output Enable input	(Common)
WE#	Write Enable input	
V_{SS}	Ground	
NC	No Connect; not connected internally.	
RDY	Ready output. Indicates the status of the Burst read.	(Flash)
CLK	Clock input. In burst mode, after the initial word is output, subsequent active edges of CLK increment the internal address counter. Should be at V_{IL} or V_{IH} while in asynchronous mode.	(Common)
AVD#	Address Valid input. Indicates to device that the valid address is present on the address inputs.	
F-RST#	Hardware reset input.	
F-WP#	Hardware write protect input. At V_{IL}, disables program and erase functions in the four outermost sectors. Should be at V_{IH} for all other conditions.	(Flash)
F-ACC	Accelerated input. At V_{HH}, accelerates programming; automatically places device in unlock bypass mode. At V_{IL}, disables all program and erase functions. Should be at V_{IH} for all other conditions.	
R-CE#	Chip-enable input for pSRAM	
F-CE#	Chip-enable input for Flash.	
F1-CE#	Chip-enable input for Flash 1.	Asynchronous relative to CLK for Burst Mode.
F2-CE#	Chip-enable input for Flash 2.	
F3-CE#	Chip-enable input for Flash 3.	
R-CRE	Control Register Enable .	(pSRAM – CellularRAM only)
F-V_{CC}	Flash 1.8 Volt-only single power supply.	
R-V_{CC}	pSRAM Power Supply.	
R-UB#	Upper Byte Control.	(pSRAM)
R-LB#	Lower Byte Control .	



Note: *R-CRE is only present in CellularRAM-compatible pSRAM.*

4 MCP Block Diagram



Notes:

1. *CREs is only present in CellularRAM-compatible pSRAM.*
2. *CE#f1, CE#f2, and CE#f3 are the chip enable pins for the first, second, and third Flash devices, respectively. CE#f3 may not be needed depending on the package.*
3. *If necessary.*

5 Connection Diagrams/Physical Dimensions

This section contains the I/O designations and package specifications for the S75WS.

5.1 Special Handling Instructions for FBGA Package

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

5.2 Connection Diagram – Cellular Ram-Based Pinout, 9 x 12 mm

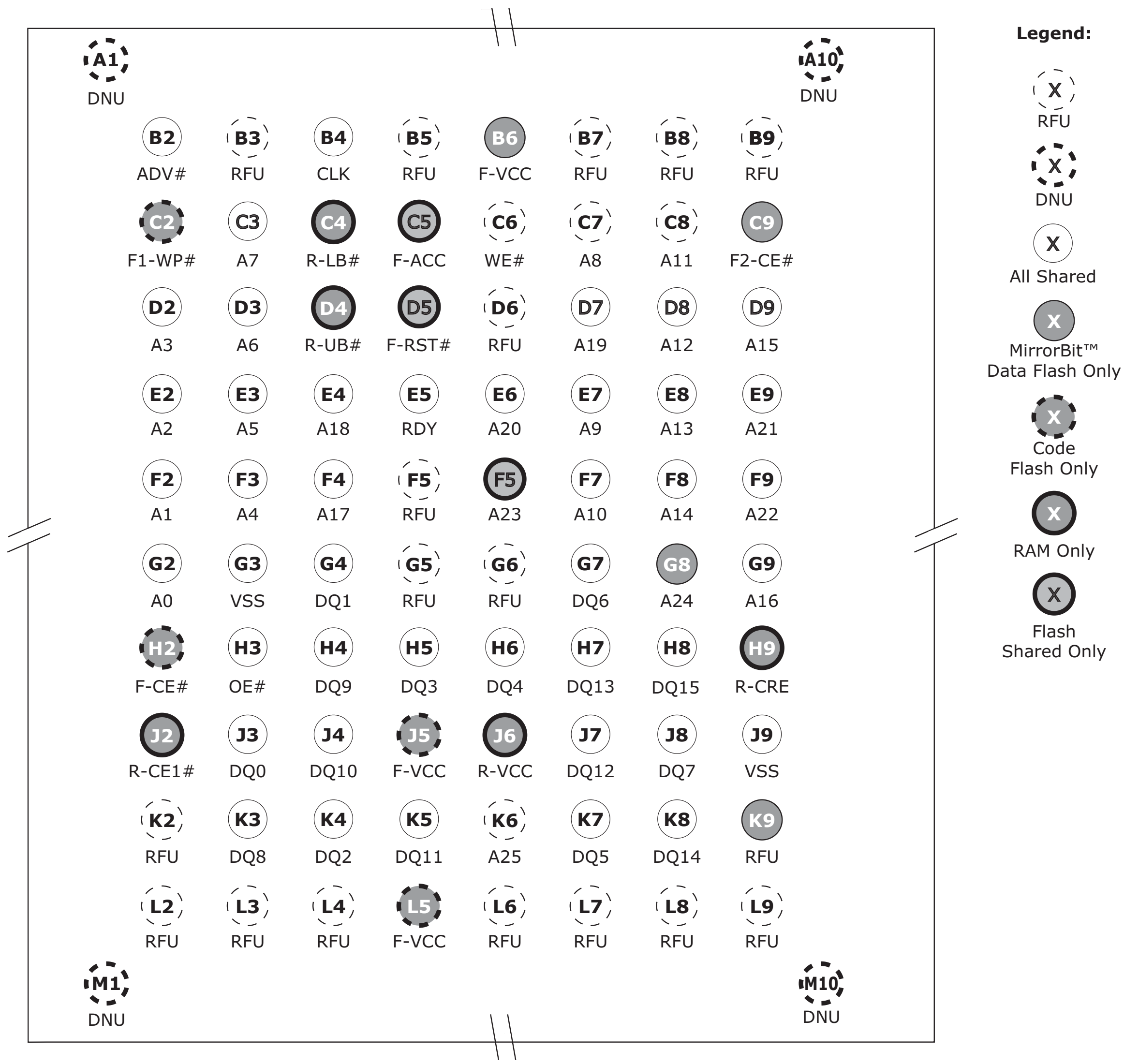


Figure 5.1 Connection Diagram – Cellular Ram-Based 84-ball Fine-Pitch Ball Grid Array

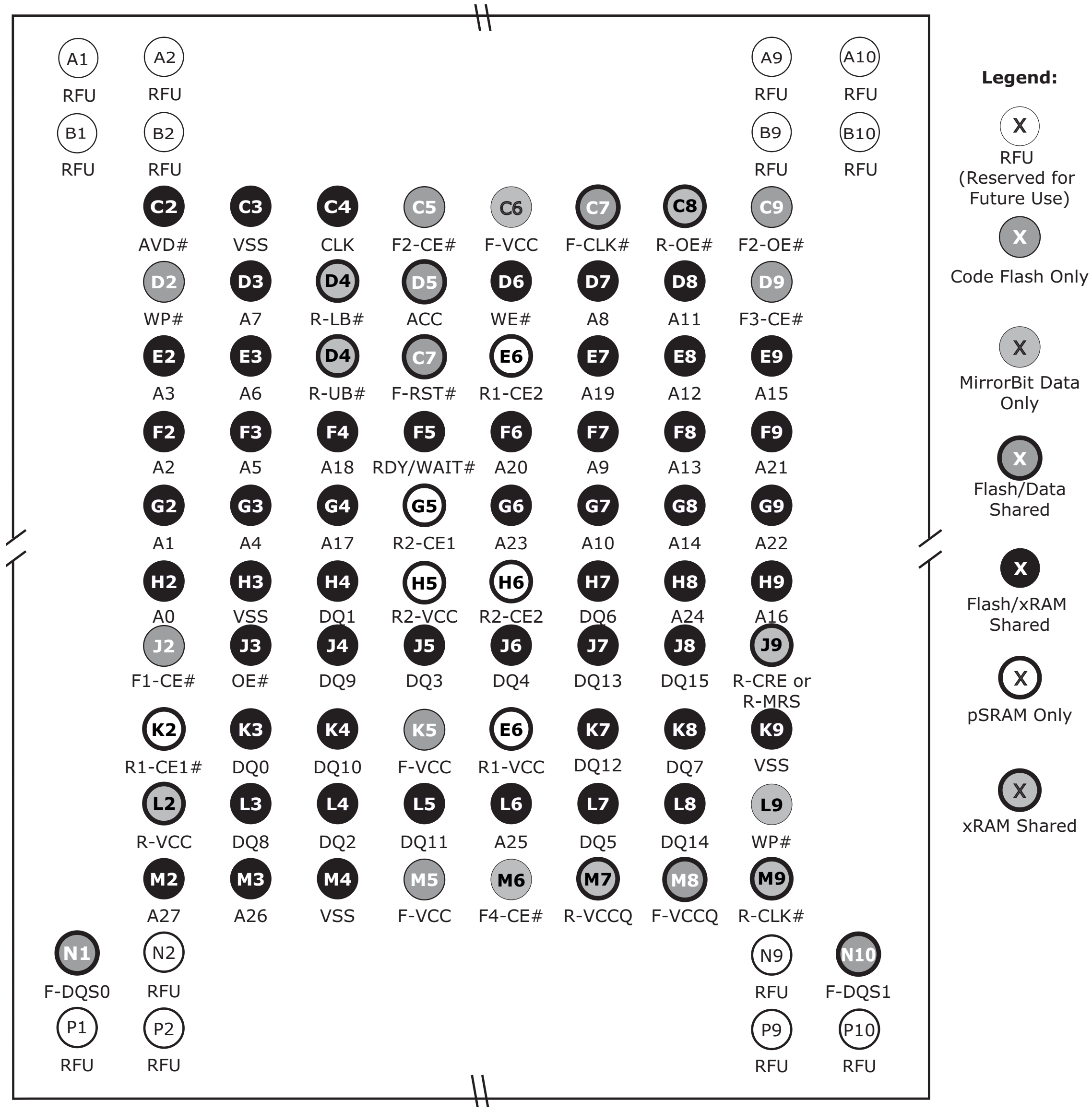
5.3 Physical Dimensions

5.3.1 Physical Dimensions – xxx084 – Fine Pitch Ball Grid Array 9 x 12 mm

TBD

5.4 Look-Ahead Connection Diagram

Look Ahead Pinout – 1.8 V only x 16NOR + x16pSRAM + x16MirrorBit Data



Notes:

1. *F1 and F2 denote XIP/Code Flash, while F3 and F4 denote Data/Companion Flash*
2. *In addition to being defined as F2-CE#, Ball C5 can also be assigned as F1-CE2# for code that has two chip enable signals.*

Figure 5.2 Look Ahead Pinout – 1.8 V only x 16NOR + x16pSRAM + x16MirrorBit Data

To provide customers with a migration path to higher densities, as well as the option to stack more die in a package, Spansion has prepared a standard pinout that supports:

- NOR Flash and SRAM densities up to 4 Gigabits
- NOR Flash and PSRAM densities up to 4 Gigabits
- NOR Flash and PSRAM and DATA STORAGE densities up to 4 Gigabits

The signal locations of the resultant MCP device are shown above. Note that for different densities, the actual package outline may vary. However, any pinout in any MCP will be a subset of the pinout above.

In some cases, there may be outrigger balls in locations outside the grid shown above. In such cases, the user is recommended to treat these as RFUs, and not connect them to any other signal.

In case of any further inquiries about the above look-ahead pinout, please refer to the application note on this subject, or contact your Spansion or Fujitsu sales office.

S75WS-N MirrorBit™ Flash Family

S29WS256N, S29WS128N, S29WS064N
256/128/64 Megabit (16/8/4 M x 16-Bit) CMOS 1.8 Volt-only Simultaneous Read/Write, Burst Mode Flash Memory

Data Sheet **PRELIMINARY**

General Description

The Spansion S29WS256/128/064N are Mirrorbit™ Flash products fabricated on 110 nm process technology. These burst mode Flash devices are capable of performing simultaneous read and write operations with zero latency on two separate banks using separate data and address pins. These products can operate up to 80 MHz and use a single V_{CC} of 1.7 V to 1.95 V that makes them ideal for today's demanding wireless applications requiring higher density, better performance and lowered power consumption.

Distinctive Characteristics

- **Single 1.8 V read / program / erase (1.70–1.95 V)**
- **110 nm MirrorBit™ Technology**
- **Simultaneous Read / Write operation with zero latency**
- **32-word Write Buffer**
- **Sixteen-bank architecture consisting of 16 / 8 / 4 Mwords for WS256N / 128N / 064N, respectively**
- **Four 16 Kword sectors at both top and bottom of memory array**
- **254 / 126 / 62 64 Kword sectors (WS256N / 128N / 064N)**
- **Programmable burst read modes**
  - Linear for 32, 16 or 8 words linear read with or without wrap-around
  - Continuous sequential read mode
- **Secured Silicon Sector region consisting of 128 words each for factory and customer**
- **20-year data retention (typical)**
- **Cycling Endurance: 100,000 cycles per sector (typical)**
- **RDY output indicates data available to system**
- **Command set compatible with JEDEC (42.4) standard**
- **Hardware (WP#) protection of top and bottom sectors**
- **Dual boot sector configuration (top and bottom)**
- **Offered Packages**
  - WS064N: 80-ball FBGA (7 mm x 9 mm)
  - WS256N/128N: 84-ball FBGA (8 mm x 11.6 mm)
- **Low V_{CC} write inhibit**
- **Persistent and Password methods of Advanced Sector Protection**
- **Write operation status bits indicate program and erase operation completion**
- **Suspend and Resume commands for Program and Erase operations**
- **Unlock Bypass program command to reduce programming time**
- **Synchronous or Asynchronous program operation, independent of burst control register settings**
- **ACC input pin to reduce factory programming time**
- **Support for Common Flash Interface (CFI)**
- **Industrial Temperature range (contact factory)**

Performance Characteristics

Read Access Times			
Speed Option (MHz)	**80**	**66**	**54**
Max. Synch. Latency, ns (t_{IACC})	80	80	80
Max. Synch. Burst Access, ns (t_{BACC})	9	11.2	13.5
Max. Asynch. Access Time, ns (t_{ACC})	80	80	80
Max CE# Access Time, ns (t_{CE})	80	80	80
Max OE# Access Time, ns (t_{OE})	13.5	13.5	13.5

Current Consumption (typical values)	
Continuous Burst Read @ 66 MHz	35 mA
Simultaneous Operation (asynchronous)	50 mA
Program (asynchronous)	19 mA
Erase (asynchronous)	19 mA
Standby Mode (asynchronous)	20 µA

Typical Program & Erase Times	
Single Word Programming	40 µs
Effective Write Buffer Programming (V_{CC}) Per Word	9.4 µs
Effective Write Buffer Programming (V_{ACC}) Per Word	6 µs
Sector Erase (16 Kword Sector)	150 ms
Sector Erase (64 Kword Sector)	600 ms

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6 Additional Resources

Visit www.amd.com and www.fujitsu.com to obtain the following related documents:

Application Notes

- Using the Operation Status Bits in AMD Devices
- Understanding Burst Mode Flash Memory Devices
- Simultaneous Read/Write vs. Erase Suspend/Resume
- MirrorBit™ Flash Memory Write Buffer Programming and Page Buffer Read
- Design-In Scalable Wireless Solutions with Spansion Products
- Common Flash Interface Version 1.4 Vendor Specific Extensions

Specification Bulletins

Contact your local sales office for details.

Drivers and Software Support

- Spansion low-level drivers
- Enhanced Flash drivers
- Flash file system

CAD Modeling Support

- VHDL and Verilog
- IBIS
- ORCAD

Technical Support

Contact your local sales office or contact Spansion LLC directly for additional technical support:

Email
US and Canada: HW.support@amd.com
Asia Pacific: asia.support@amd.com
Europe, Middle East, and Africa
Japan: http://edevice.fujitsu.com/jp/support/tech/#b7

Frequently Asked Questions (FAQ)
http://ask.amd.com/
http://edevice.fujitsu.com/jp/support/tech/#b7

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7 Product Overview

The S29WS-N family consists of 256, 128 and 64Mbit, 1.8 volts-only, simultaneous read/write burst mode Flash device optimized for today's wireless designs that demand a large storage array, rich functionality, and low power consumption.

These devices are organized in 16, 8 or 4 Mwords of 16 bits each and are capable of continuous, synchronous (burst) read or linear read (8-, 16-, or 32-word aligned group) with or without wrap around. These products also offer single word programming or a 32-word buffer for programming with program/erase and suspend functionality. Additional features include:

- Advanced Sector Protection methods for protecting sectors as required
- 256 words of Secured Silicon area for storing customer and factory secured information. The Secured Silicon Sector is One Time Programmable.

7.1 Memory Map

The S29WS256/128/064N Mbit devices consist of 16 banks organized as shown in Tables Table 7.1, Table 7.2, and Table 7.3.

Table 7.1 S29WS256N Sector & Memory Address Map

Bank Size	Sector Count	Sector Size (KB)	Bank	Sector/ Sector Range	Address Range	Notes
2 MB	4	32	0	SA000	000000h–003FFFh	Contains four smaller sectors at bottom of addressable memory.
				SA001	004000h–007FFFh	
				SA002	008000h–00BFFFh	
				SA003	00C000h–00FFFFh	
	15	128		SA004 to SA018	010000h–01FFFFh to 0F0000h–0FFFFFh	All 128 KB sectors. Pattern for sector address range is xx0000h–xxFFFFh. (see note)
2 MB	16	128	1	SA019 to SA034	100000h–10FFFFh to 1F0000h–1FFFFFh	
2 MB	16	128	2	SA035 to SA050	200000h–20FFFFh to 2F0000h–2FFFFFh	
2 MB	16	128	3	SA051 to SA066	300000h–30FFFFh to 3F0000h–3FFFFFh	
2 MB	16	128	4	SA067 to SA082	400000h–40FFFFh to 4F0000h–4FFFFFh	
2 MB	16	128	5	SA083 to SA098	500000h–50FFFFh to 5F0000h–5FFFFFh	
2 MB	16	128	6	SA099 to SA114	600000h–60FFFFh to 6F0000h–6FFFFFh	
2 MB	16	128	7	SA115 to SA130	700000h–70FFFFh to 7F0000h–7FFFFFh	
2 MB	16	128	8	SA131 to SA146	800000h–80FFFFh to 8F0000h–8FFFFFh	
2 MB	16	128	9	SA147 to SA162	900000h–90FFFFh to 9F0000h–9FFFFFh	
2 MB	16	128	10	SA163 to SA178	A00000h–A0FFFFh to AF0000h–AFFFFFh	
2 MB	16	128	11	SA179 to SA194	B00000h–B0FFFFh to BF0000h–BFFFFFh	
2 MB	16	128	12	SA195 to SA210	C00000h–C0FFFFh to CF0000h–CFFFFFh	
2 MB	16	128	13	SA211 to SA226	D00000h–D0FFFFh to DF0000h–DFFFFFh	
2 MB	16	128	14	SA227 to SA242	E00000h–E0FFFFh to EF0000h–EFFFFFh	
2 MB	15	128	15	SA243 to SA257	F00000h–F0FFFFh to FE0000h–FEFFFFh	
	4	32		SA258	FF0000h–FF3FFFh	Contains four smaller sectors at top of addressable memory.
				SA259	FF4000h–FF7FFFh	
				SA260	FF8000h–FFBFFFh	
				SA261	FFC000h–FFFFFFh	

Note: *This table has been condensed to show sector-related information for an entire device on a single page. Sectors and their address ranges that are not explicitly listed (such as SA005–SA017) have sector starting and ending addresses that form the same pattern as all other sectors of that size. For example, all 128 KB sectors have the pattern xx00000h–xxFFFFh.*

Table 7.2 S29WS128N Sector & Memory Address Map

Bank Size	Sector Count	Sector Size (KB)	Bank	Sector/ Sector Range	Address Range	Notes
1 MB	4	32	0	SA000	000000h–003FFFh	Contains four smaller sectors at bottom of addressable memory.
		32		SA001	004000h–007FFFh	
		32		SA002	008000h–00BFFFh	
		32		SA003	00C000h–00FFFFh	
	7	128		SA004 to SA010	010000h–01FFFFh to 070000h–07FFFFh	All 128 KB sectors. Pattern for sector address range is xx0000h–xxFFFFh. (See Note)
1 MB	8	128	1	SA011 to SA018	080000h–08FFFFh to 0F0000h–0FFFFFh	
1 MB	8	128	2	SA019 to SA026	100000h–10FFFFh to 170000h–17FFFFh	
1 MB	8	128	3	SA027 to SA034	180000h–18FFFFh to 1F0000h–1FFFFFh	
1 MB	8	128	4	SA035 to SA042	200000h–20FFFFh to 270000h–27FFFFh	
1 MB	8	128	5	SA043 to SA050	280000h–28FFFFh to 2F0000h–2FFFFFh	
1 MB	8	128	6	SA051 to SA058	300000h–30FFFFh to 370000h–37FFFFh	
1 MB	8	128	7	SA059 to SA066	380000h–38FFFFh to 3F0000h–3FFFFFh	
1 MB	8	128	8	SA067 to SA074	400000h–40FFFFh to 470000h–47FFFFh	
1 MB	8	128	9	SA075 to SA082	480000h–48FFFFh to 4F0000h–4FFFFFh	
1 MB	8	128	10	SA083 to SA090	500000h–50FFFFh to 570000h–57FFFFh	
1 MB	8	128	11	SA091 to SA098	580000h–58FFFFh to 5F0000h–5FFFFFh	
1 MB	8	128	12	SA099 to SA106	600000h–60FFFFh to 670000h–67FFFFh	
1 MB	8	128	13	SA107 to SA114	680000h–68FFFFh to 6F0000h–6FFFFFh	
1 MB	8	128	14	SA115 to SA122	700000h–70FFFFh to 770000h–77FFFFh	
1 MB	7	128	15	SA123 to SA129	780000h–78FFFFh to 7E0000h–7EFFFFh	
	4	32		SA130	7F0000h–7F3FFFh	Contains four smaller sectors at top of addressable memory.
		32		SA131	7F4000h–7F7FFFh	
		32		SA132	7F8000h–7FBFFFh	
		32		SA133	7FC000h–7FFFFFh	

Note: *This table has been condensed to show sector-related information for an entire device on a single page. Sectors and their address ranges that are not explicitly listed (such as SA005–SA009) have sector starting and ending addresses that form the same pattern as all other sectors of that size. For example, all 128 KB sectors have the pattern xx00000h–xxFFFFh.*

Table 7.3 S29WS064N Sector & Memory Address Map

Bank Size	Sector Count	Sector Size (KB)	Bank	Sector/ Sector Range	Address Range	Notes
0.5 MB	4	32	0	SA000	000000h–003FFFh	Contains four smaller sectors at bottom of addressable memory.
				SA001	004000h–007FFFh	
				SA002	008000h–00BFFFh	
				SA003	00C000h–00FFFFh	
	3	128		SA004	010000h–01FFFFh	All 128 KB sectors. Pattern for sector address range is xx0000h–xxFFFFh. (see note)
				SA005	020000h–02FFFFh	
				SA006	030000h–03FFFFh	
0.5 MB	4	128	1	SA007–SA010	040000h–04FFFFh to 070000h–07FFFFh	
0.5 MB	4	128	2	SA011–SA014	080000h–08FFFFh to 0B0000h–0BFFFFh	
0.5 MB	4	128	3	SA015–SA018	0C0000h–0CFFFFh to 0F0000h–0FFFFFh	
0.5 MB	4	128	4	SA019–SA022	100000h–10FFFFh to 130000h–13FFFFh	
0.5 MB	4	128	5	SA023–SA026	140000h–14FFFFh to 170000h–17FFFFh	
0.5 MB	4	128	6	SA027–SA030	180000h–18FFFFh to 1B0000h–1BFFFFh	
0.5 MB	4	128	7	SA031–SA034	1C0000h–1CFFFFh to 1F0000h–1FFFFFh	
0.5 MB	4	128	8	SA035–SA038	200000h–20FFFFh to 230000h–23FFFFh	
0.5 MB	4	128	9	SA039–SA042	240000h–24FFFFh to 270000h–27FFFFh	
0.5 MB	4	128	10	SA043–SA046	280000h–28FFFFh to 2B0000h–2BFFFFh	
0.5 MB	4	128	11	SA047–SA050	2C0000h–2CFFFFh to 2F0000h–2FFFFFh	
0.5 MB	4	128	12	SA051–SA054	300000h–30FFFFh to 330000h–33FFFFh	
0.5 MB	4	128	13	SA055–SA058	340000h–34FFFFh to 370000h–37FFFFh	
0.5 MB	4	128	14	SA059–SA062	380000h–38FFFFh to 3B0000h–3BFFFFh	
0.5 MB	3	128	15	SA063	3C0000h–3CFFFFh	
				SA064	3D0000h–3DFFFFh	
				SA065	3E0000h–3EFFFFh	
	4	32		SA066	3F0000h–3F3FFFh	Contains four smaller sectors a t top of addressable memory.
				SA067	3F4000h–3F7FFFh	
				SA068	3F8000h–3FBFFFh	
				SA069	3FC000h–3FFFFFh	

Note: *This table has been condensed to show sector-related information for an entire device on a single page. Sectors and their address ranges that are not explicitly listed (such as SA008–SA009) have sector starting and ending addresses that form the same pattern as all other sectors of that size. For example, all 128 KB sectors have the pattern xx00000h–xxFFFFh.*

8 Device Operations

This section describes the read, program, erase, simultaneous read/write operations, handshaking, and reset features of the Flash devices.

Operations are initiated by writing specific commands or a sequence with specific address and data patterns into the command registers (see Table 13.1 and Table 13.2). The command register itself does not occupy any addressable memory location; rather, it is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as input to the internal state machine and the state machine outputs dictate the function of the device. Writing incorrect address and data values or writing them in an improper sequence may place the device in an unknown state, in which case the system must write the reset command to return the device to the reading array data mode.

8.1 Device Operation Table

The device must be setup appropriately for each operation. Table 8.1 describes the required state of each control pin for any particular operation.

Table 8.1 Device Operations

Operation	CE#	OE#	WE#	Addresses	DQ15–0	RESET#	CLK	AVD#
Asynchronous Read - Addresses Latched	L	L	H	Addr In	Data Out	H	X	↑
Asynchronous Read - Addresses Steady State	L	L	H	Addr In	Data Out	H	X	L
Asynchronous Write	L	H	L	Addr In	I/O	H	X	L
Synchronous Write	L	H	L	Addr In	I/O	H	↑	↑
Standby (CE#)	H	X	X	X	HIGH Z	H	X	X
Hardware Reset	X	X	X	X	HIGH Z	L	X	X
Burst Read Operations (Synchronous)								
Load Starting Burst Address	L	X	H	Addr In	X	H	↑	↑
Advance Burst to next address with appropriate Data presented on the Data Bus	L	L	H	X	Burst Data Out	H	↑	H
Terminate current Burst read cycle	H	X	H	X	HIGH Z	H	↑	X
Terminate current Burst read cycle via RESET#	X	X	H	X	HIGH Z	L	X	X
Terminate current Burst read cycle and start new Burst read cycle	L	X	H	Addr In	I/O	H	↑	↑

Legend: *L = Logic 0, H = Logic 1, X = Don't Care, I/O = Input/Output.*

8.2 Asynchronous Read

All memories require access time to output array data. In an asynchronous read operation, data is read from one memory location at a time. Addresses are presented to the device in random order, and the propagation delay through the device causes the data on its outputs to arrive asynchronously with the address on its inputs.

The device defaults to reading array data asynchronously after device power-up or hardware reset. Asynchronous read requires that the CLK signal remain at V_{IL} during the entire memory read operation. To read data from the memory array, the system must first assert a valid address on A_{max}–A0, while driving AVD# and CE# to V_{IL}. WE# must remain at V_{IH}. The rising edge of AVD# latches the address. The OE# signal must be driven to V_{IL}, once AVD# has been driven to V_{IH}. Data is output on A/DQ15-A/DQ0 pins after the access time (t_{OE}) has elapsed from the falling edge of OE#.

8.3 Synchronous (Burst) Read Mode and Configuration Register

When a series of adjacent addresses needs to be read from the device (in order from lowest to highest address), the synchronous (or burst read) mode can be used to significantly reduce the overall time needed for the device to output array data. After an initial access time required for the data from the first address location, subsequent data is output synchronized to a clock input provided by the system.

The device offers both continuous and linear methods of burst read operation, which are discussed in sections 8.3.1, 8.3.2, and 8.3.3.

Since the device defaults to asynchronous read mode after power-up or a hardware reset, the configuration register must be set to enable the burst read mode. Other Configuration Register settings include the number of wait states to insert before the initial word (t_{IACC}) of each burst access, the burst mode in which to operate, and when RDY indicates data is ready to be read. Prior to entering the burst mode, the system should first determine the configuration register settings (and read the current register settings if desired via the Read Configuration Register command sequence), and then write the configuration register command sequence. See 8.3.4 and Table 13.1 for further details.

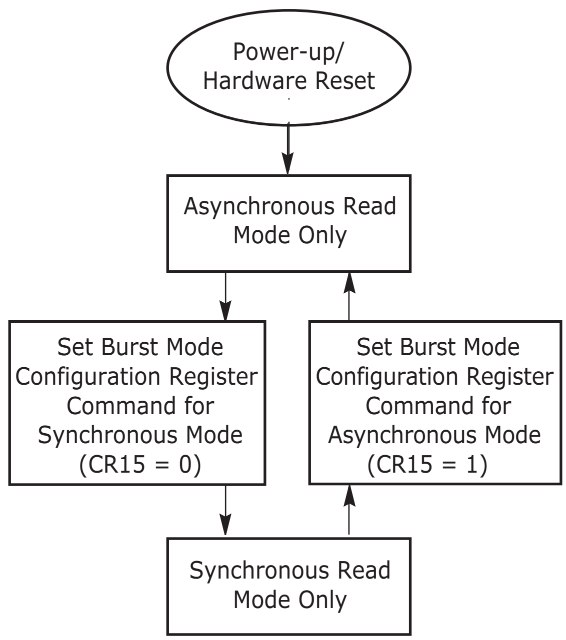


Figure 8.1 Synchronous/Asynchronous State Diagram

The device outputs the initial word subject to the following operational conditions:

- t_{IACC} specification: the time from the rising edge of the first clock cycle after addresses are latched to valid data on the device outputs.
- Configuration register setting CR13–CR11: the total number of clock cycles (wait states) that occur before valid data appears on the device outputs. The effect is that t_{IACC} is lengthened.

The device outputs subsequent words t_{BACC} after the active edge of each successive clock cycle, which also increments the internal address counter. The device outputs burst data at this rate subject to the following operational conditions:

- Starting address: whether the address is divisible by four (where A[1:0] is 00). A divisible-by-four address incurs the least number of additional wait states that occur after the initial word. The number of additional wait states required increases for burst operations in which the starting address is one, two, or three locations above the divisible-by-four address (i.e., where A[1:0] is 01, 10, or 11).
- Boundary crossing: There is a boundary at every 128 words due to the internal architecture of the device. One additional wait state must be inserted when crossing this boundary if the memory bus is operating at a high clock frequency. Please refer to the tables below.
- Clock frequency: the speed at which the device is expected to burst data. Higher speeds require additional wait states after the initial word for proper operation.

In all cases, with or without latency, the RDY output indicates when the next data is available to be read.

Tables 8.2 – 8.6 reflect wait states required for S29WS256/128/064N devices. Refer to the Configuration Register table (CR11 – CR14) and timing diagrams for more details.

Table 8.2 Address Latency (S29WS256N)

Word	Wait States	Cycle								
0	x ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1	x ws	D1	D2	D3	1 ws	D4	D5	D6	D7	D8
2	x ws	D2	D3	1 ws	1 ws	D4	D5	D6	D7	D8
3	x ws	D3	1 ws	1 ws	1 ws	D4	D5	D6	D7	D8

Table 8.3 Address Latency (S29WS128N/S29WS064N)

Word	Wait States	Cycle								
0	5, 6, 7 ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1	5, 6, 7 ws	D1	D2	D3	1 ws	D4	D5	D6	D7	D8
2	5, 6, 7 ws	D2	D3	1 ws	1 ws	D4	D5	D6	D7	D8
3	5, 6, 7 ws	D3	1 ws	1 ws	1 ws	D4	D5	D6	D7	D8

Table 8.4 Address/Boundary Crossing Latency (S29WS256N @ 80/66 MHz)

Word	Wait States	Cycle								
0	7, 6 ws	D0	D1	D2	D3	1 ws	D4	D5	D6	D7
1	7, 6 ws	D1	D2	D3	1 ws	1 ws	D4	D5	D6	D7
2	7, 6 ws	D2	D3	1 ws	1 ws	1 ws	D4	D5	D6	D7
3	7, 6 ws	D3	1 ws	1 ws	1 ws	1 ws	D4	D5	D6	D7

Table 8.5 Address/Boundary Crossing Latency (S29WS256N @ 54MHz)

Word	Wait States	Cycle								
0	5 ws	D0	D1	D2	D3	D4	D5	D6	D7	D8
1	5 ws	D1	D2	D3	1 ws	D4	D5	D6	D7	D8
2	5 ws	D2	D3	1 ws	1 ws	D4	D5	D6	D7	D8
3	5 ws	D3	1 ws	1 ws	1 ws	D4	D5	D6	D7	D8

Table 8.6 Address/Boundary Crossing Latency (S29WS128N/S29WS064N)

Word	Wait States	Cycle								
0	5, 6, 7 ws	D0	D1	D2	D3	1 ws	D4	D5	D6	D7
1	5, 6, 7 ws	D1	D2	D3	1 ws	1 ws	D4	D5	D6	D7
2	5, 6, 7 ws	D2	D3	1 ws	1 ws	1 ws	D4	D5	D6	D7
3	5, 6, 7 ws	D3	1 ws	1 ws	1 ws	1 ws	D4	D5	D6	D7

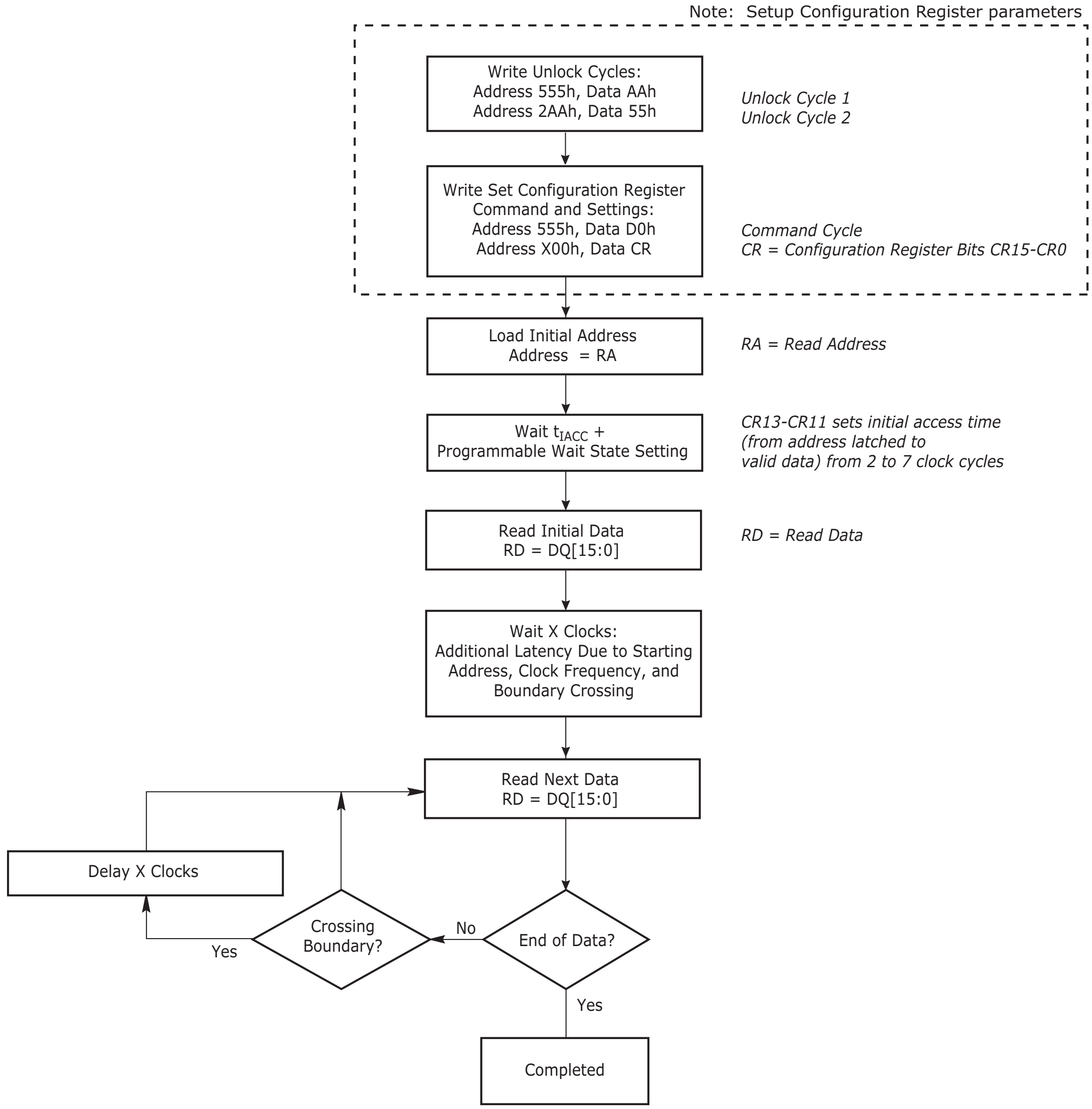


Figure 8.2 Synchronous Read

8.3.1 Continuous Burst Read Mode

In the continuous burst read mode, the device outputs sequential burst data from the starting address given and then wrap around to address 000000h when it reaches the highest addressable memory location. The burst read mode continues until the system drives CE# high, or RESET= V_{IL}. Continuous burst mode can also be aborted by asserting AVD# low and providing a new address to the device.

If the address being read crosses a 128-word line boundary (as mentioned above) and the subsequent word line is not being programmed or erased, additional latency cycles are required as reflected by the configuration register table (Table 8.8).

If the address crosses a bank boundary while the subsequent bank is programming or erasing, the device provides read status information and the clock is ignored. Upon completion of status read or program or erase operation, the host can restart a burst read operation using a new address and AVD# pulse.

8.3.2 8-, 16-, 32-Word Linear Burst Read with Wrap Around

In a linear burst read operation, a fixed number of words (8, 16, or 32 words) are read from consecutive addresses that are determined by the group within which the starting address falls. The groups are sized according to the number of words read in a single burst sequence for a given mode (see Table 8.7).

For example, if the starting address in the 8-word mode is 3Ch, the address range to be read would be 38-3Fh, and the burst sequence would be 3C-3D-3E-3F-38-39-3A-3Bh. Thus, the device outputs all words in that burst address group until all word are read, regardless of where the starting address occurs in the address group, and then terminates the burst read.

In a similar fashion, the 16-word and 32-word Linear Wrap modes begin their burst sequence on the starting address provided to the device, then wrap back to the first address in the selected address group.

Note that in this mode the address pointer does not cross the boundary that occurs every 128 words; thus, no additional wait states are inserted due to boundary crossing.

Table 8.7 Burst Address Groups

Mode	Group Size	Group Address Ranges
8-word	8 words	0-7h, 8-Fh, 10-17h,...
16-word	16 words	0-Fh, 10-1Fh, 20-2Fh,...
32-word	32 words	00-1Fh, 20-3Fh, 40-5Fh,...

8.3.3 8-, 16-, 32-Word Linear Burst without Wrap Around

If wrap around is not enabled for linear burst read operations, the 8-word, 16-word, or 32-word burst executes up to the maximum memory address of the selected number of words. The burst stops after 8, 16, or 32 addresses and does not wrap around to the first address of the selected group.

For example, if the starting address in the 8- word mode is 3Ch, the address range to be read would be 39-40h, and the burst sequence would be 3C-3D-3E-3F-40-41-42-43h if wrap around is not enabled. The next address to be read requires a new address and AVD# pulse. Note that in this burst read mode, the address pointer may cross the boundary that occurs every 128 words, which will incur the additional boundary crossing wait state.

8.3.4 Configuration Register

The configuration register sets various operational parameters associated with burst mode. Upon power-up or hardware reset, the device defaults to the asynchronous read mode, and the configuration register settings are in their default state. The host system should determine the proper settings for the entire configuration register, and then execute the Set Configuration Register command sequence, before attempting burst operations. The configuration register is not reset after deasserting CE#. The Configuration Register can also be read using a command sequence (see Table 13.1). The following list describes the register settings.

Table 8.8 Configuration Register

CR Bit	Function		54 MHz	66 Mhz	80 MHz	Settings (Binary)
CR15	Set Device Read Mode					0 = Synchronous Read (Burst Mode) Enabled 1 = Asynchronous Read Mode (default) Enabled
CR14	Boundary Crossing	S29WS064N S29WS128N	N/A	N/A	N/A	Default value is *0*
		S29WS256N	0	1	1	0 = No extra boundary crossing latency 1 = With extra boundary crossing latency (default) Must be set to *1* greater than 54 MHz.
CR13	Programmable Wait State	S29WS064N S29WS128N S29WS256N	0	1	1	011 = Data valid on 5th active CLK edge after addresses latched 100 = Data valid on 6th active CLK edge after addresses latched 101 = Data valid on 7th active CLK edge after addresses latched (default) 110 = Reserved 111 = Reserved Inserts wait states before initial data is available. Setting greater number of wait states before initial data reduces latency after initial data. (Notes 1, 2)
CR12		S29WS064N S29WS128N S29WS256N	1	0	0	
CR11		S29WS064N S29WS128N S29WS256N	1	0	1	
CR10	RDY Polarity					0 = RDY signal active low 1 = RDY signal active high (default)
CR9	Reserved					1 = default
CR8	RDY					0 = RDY active one clock cycle before data 1 = RDY active with data (default) When CR13-CR11 are set to 000, RDY is active with data regardless of CR8 setting.
CR7	Reserved					1 = default
CR6	Reserved					1 = default
CR5	Reserved					0 = default
CR4	Reserved					0 = default
CR3	Burst Wrap Around					0 = No Wrap Around Burst 1 = Wrap Around Burst (default)
CR2 CR1 CR0	Burst Length					000 = Continuous (default) 010 = 8-Word Linear Burst 011 = 16-Word Linear Burst 100 = 32-Word Linear Burst (All other bit settings are reserved)

Notes:

1. *Refer to Tables 8.2 - 8.6 for wait states requirements.*
2. *Refer to Synchronous Burst Read timing diagrams*
3. *Configuration Register is in the default state upon power-up or hardware reset.*

Reading the Configuration Table. The configuration register can be read with a four-cycle command sequence. See Table 13.1 for sequence details. Once the data has been read from the configuration register, a software reset command is required to set the device into the correct state.

8.4 Autoselect

The Autoselect is used for manufacturer ID, Device identification, and sector protection information. This mode is primarily intended for programming equipment to automatically match a device with its corresponding programming algorithm. The Autoselect codes can also be accessed in-system. When verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table 8.9). The remaining address bits are don't care. The most significant four bits of the address during the third write cycle selects the bank from which the Autoselect codes are read by the host. All other banks can be accessed normally for data read without exiting the Autoselect mode.

- To access the Autoselect codes, the host system must issue the Autoselect command.

- The Autoselect command sequence may be written to an address within a bank that is either in the read or erase-suspend-read mode.
- The Autoselect command may not be written while the device is actively programming or erasing. Autoselect does not support simultaneous operations or burst mode.
- The system must write the reset command to return to the read mode (or erase-suspend-read mode if the bank was previously in Erase Suspend).

See Table 13.1 for command sequence details.

Table 8.9 Autoselect Addresses

Description	Address	Read Data
Manufacturer ID	(BA) + 00h	0001h
Device ID, Word 1	(BA) + 01h	227Eh
Device ID, Word 2	(BA) + 0Eh	2230 (WS256N) 2231 (WS128N) 2232 (WS064N)
Device ID, Word 3	(BA) + 0Fh	2200
Indicator Bits (See Note)	(BA) + 03h	DQ15 - DQ8 = Reserved DQ7 (Factory Lock Bit): 1 = Locked, 0 = Not Locked DQ6 (Customer Lock Bit): 1 = Locked, 0 = Not Locked DQ5 (Handshake Bit): 1 = Reserved, 0 = Standard Handshake DQ4, DQ3 (WP# Protection Boot Code): 00 = WP# Protects both Top Boot and Bottom Boot Sectors. 01, 10, 11 = Reserved DQ2 = Reserved DQ1 (DYB Power up State [Lock Register DQ4]): 1 = Unlocked (user option), 0 = Locked (default) DQ0 (PPB Eraseability [Lock Register DQ3]): 1 = Erase allowed, 0 = Erase disabled
Sector Block Lock/ Unlock	(SA) + 02h	0001h = Locked, 0000h = Unlocked

Note: *For WS128N and WS064, DQ1 and DQ0 are reserved.*

Software Functions and Sample Code

Table 8.10 Autoselect Entry

(LLD Function = lld_AutoselectEntryCmd)

Cycle	Operation	Byte Address	Word Address	Data
Unlock Cycle 1	Write	BAxAAAh	BAx555h	0x00AAh
Unlock Cycle 2	Write	BAx555h	BAx2AAh	0x0055h
Autoselect Command	Write	BAxAAAh	BAx555h	0x0090h

Table 8.11 Autoselect Exit

(LLD Function = lld_AutoselectExitCmd)

Cycle	Operation	Byte Address	Word Address	Data
Unlock Cycle 1	Write	base + XXXh	base + XXXh	0x00F0h

Notes:

1. Any offset within the device works.

2. BA = Bank Address. The bank address is required.

3. base = base address.

The following is a C source code example of using the autoselect function to read the manufacturer ID. Refer to the *Spansion Low Level Driver User Guide* (available on www.amd.com and www.fujitsu.com) for general information on Spansion Flash memory software development guidelines.

```
/* Here is an example of Autoselect mode (getting manufacturer ID) */
/* Define UINT16 example: typedef unsigned short UINT16; */

UINT16 manuf_id;

/* Auto Select Entry */

*( (UINT16 *)bank_addr + 0x555 ) = 0x00AA; /* write unlock cycle 1 */
*( (UINT16 *)bank_addr + 0x2AA ) = 0x0055; /* write unlock cycle 2 */
*( (UINT16 *)bank_addr + 0x555 ) = 0x0090; /* write autoselect command */


/* multiple reads can be performed after entry */

manuf_id = *( (UINT16 *)bank_addr + 0x000 ); /* read manuf. id */

/*  Autoselect exit */

*( (UINT16 *)base_addr + 0x000 ) = 0x00F0; /* exit autoselect (write reset command) */
```

8.5 Program/Erase Operations

These devices are capable of several modes of programming and or erase operations which are described in detail in the following sections. However, prior to any programming and or erase operation, devices must be setup appropriately as outlined in the configuration register (Table 8.8).

For any program and or erase operations, including writing command sequences, the system must drive AVD# and CE# to V_{IL}, and OE# to V_{IH} when providing an address to the device, and drive WE# and CE# to V_{IL}, and OE# to V_{IH} when writing commands or programming data.

Addresses are latched on the last falling edge of WE# or CE#, while data is latched on the 1st rising edge of WE# or CE#.

Note the following:

- When the Embedded Program algorithm is complete, the device returns to the read mode.
- The system can determine the status of the program operation by using DQ7 or DQ6. Refer to the Write Operation Status section for information on these status bits.
- A *0* cannot be programmed back to a *1*. Attempting to do so causes the device to set DQ5 = 1 (halting any further operation and requiring a reset command). A succeeding read shows that the data is still *0.* Only erase operations can convert a *0* to a *1*.
- Any commands written to the device during the Embedded Program Algorithm are ignored except the Program Suspend command.
- Secured Silicon Sector, Autoselect, and CFI functions are unavailable when a program operation is in progress.
- A hardware reset immediately terminates the program operation and the program command sequence should be reinitiated once the device has returned to the read mode, to ensure data integrity.
- Programming is allowed in any sequence and across sector boundaries for single word programming operation.

8.5.1 Single Word Programming

Single word programming mode is the simplest method of programming. In this mode, four Flash command write cycles are used to program an individual Flash address. The data for this programming operation could be 8-, 16- or 32-bits wide. While this method is supported by all Spansion devices, in general it is not recommended for devices that support Write Buffer Programming. See Table 13.1 for the required bus cycles and Figure 8.3 for the flowchart.

When the Embedded Program algorithm is complete, the device then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7 or DQ6. Refer to the Write Operation Status section for information on these status bits.

- During programming, any command (except the Suspend Program command) is ignored.
- The Secured Silicon Sector, Autoselect, and CFI functions are unavailable when a program operation is in progress.
- A hardware reset immediately terminates the program operation. The program command sequence should be reinitiated once the device has returned to the read mode, to ensure data integrity.

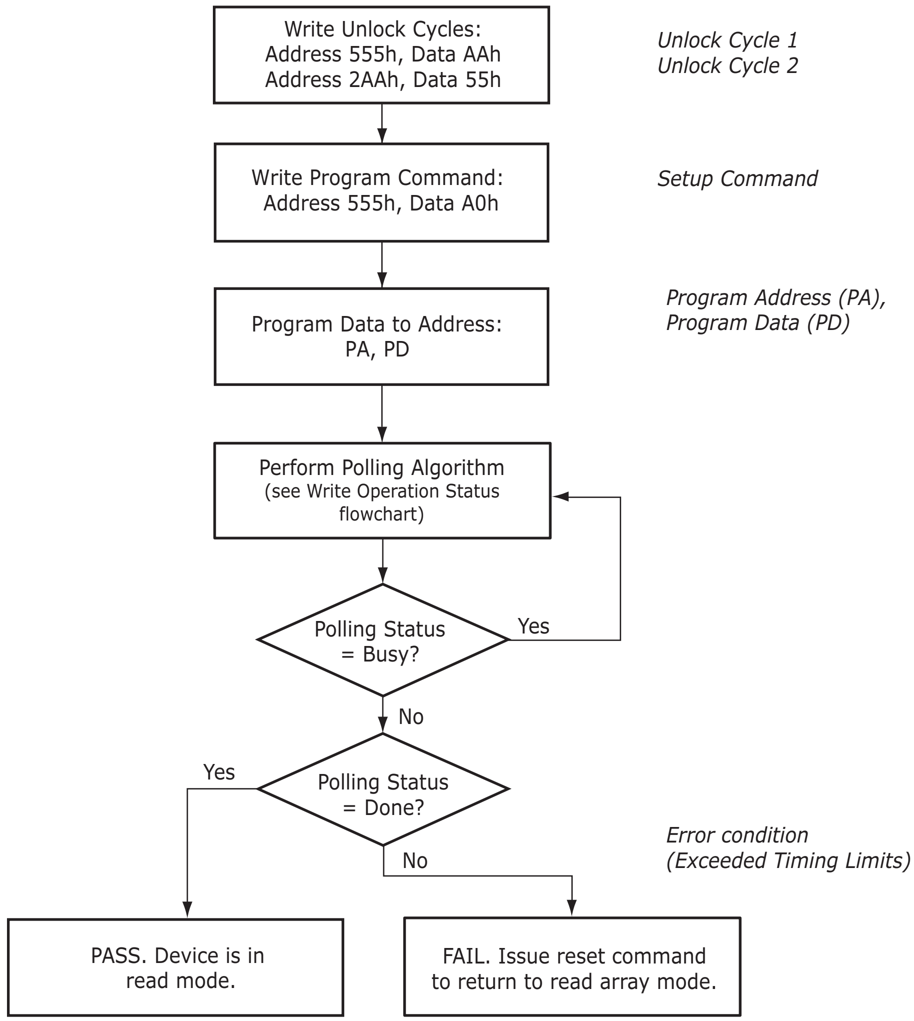


Figure 8.3 Single Word Program

Software Functions and Sample Code

Table 8.12 Single Word Program

(LLD Function = lld_ProgramCmd)

Cycle	Operation	Byte Address	Word Address	Data
Unlock Cycle 1	Write	Base + AAAh	Base + 555h	00AAh
Unlock Cycle 2	Write	Base + 554h	Base + 2AAh	0055h
Program Setup	Write	Base + AAAh	Base + 555h	00A0h
Program	Write	Word Address	Word Address	Data Word

Note: *Base = Base Address.*

The following is a C source code example of using the single word program function. Refer to the *Spansion Low Level Driver User's Guide* (available on www.amd.com and www.fujitsu.com) for general information on Spansion Flash memory software development guidelines.

```
/* Example: Program Command    */
  *( (UINT16 *)base_addr + 0x555 ) = 0x00AA;   /* write unlock cycle 1           */
  *( (UINT16 *)base_addr + 0x2AA ) = 0x0055;   /* write unlock cycle 2           */
  *( (UINT16 *)base_addr + 0x555 ) = 0x00A0;   /* write program setup command    */
  *( (UINT16 *)pa )                = data;     /* write data to be programmed    */
/* Poll for program completion */
```

8.5.2 Write Buffer Programming

Write Buffer Programming allows the system to write a maximum of 32 words in one programming operation. This results in a faster effective word programming time than the standard *word* programming algorithms. The Write Buffer Programming command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the Write Buffer Load command written at the Sector Address in which programming occurs. At this point, the system writes the number of *word locations minus 1* that are loaded into the page buffer at the Sector Address in which programming occurs. This tells the device how many write buffer addresses are loaded with data and therefore when to expect the *Program Buffer to Flash* confirm command. The number of locations to program cannot exceed the size of the write buffer or the operation aborts. (Number loaded = the number of locations to program minus *1*. For example, if the system programs 6 address locations, then 05h should be written to the device.)

The system then writes the starting address/data combination. This starting address is the first address/data pair to be programmed, and selects the *write-buffer-page* address. All subsequent address/data pairs must fall within the elected-write-buffer-page.

The *write-buffer-page* is selected by using the addresses A_{MAX} - A5.

The *write-buffer-page* addresses must be the same for all address/data pairs loaded into the write buffer. (This means Write Buffer Programming cannot be performed across multiple *write-buffer-pages*. This also means that Write Buffer Programming cannot be performed across multiple sectors. If the system attempts to load programming data outside of the selected *write-buffer-page*, the operation ABORTs.)

After writing the Starting Address/Data pair, the system then writes the remaining address/data pairs into the write buffer.

Note that if a Write Buffer address location is loaded multiple times, the *address/data pair* counter is decremented for every data load operation. Also, the last data loaded at a location before the *Program Buffer to Flash* confirm command is programmed into the device. It is the software's responsibility to comprehend ramifications of loading a write-buffer location more than once. The counter decrements for each data load operation, NOT for each unique write-buffer-address location. Once the specified number of write buffer locations have been loaded, the system must then write the *Program Buffer* to Flash command at the Sector Address. Any other address/data write combinations abort the Write Buffer Programming operation. The device goes *busy*. The Data Bar polling techniques should be used while monitoring the last address location loaded into the write buffer. This eliminates the need to store an address in memory because the system can load the last address location, issue the program confirm command at the last loaded address location, and then data bar poll at that same address. DQ7, DQ6, DQ5, DQ2, and DQ1 should be monitored to determine the device status during Write Buffer Programming.

The write-buffer *embedded* programming operation can be suspended using the standard suspend/resume commands. Upon successful completion of the Write Buffer Programming operation, the device returns to READ mode.

The Write Buffer Programming Sequence is ABORTED under any of the following conditions:

- Load a value that is greater than the page buffer size during the *Number of Locations to Program step*.
- Write to an address in a sector different than the one specified during the Write-Buffer-Load command.
- Write an Address/Data pair to a different write-buffer-page than the one selected by the *Starting Address* during the *write buffer data loading* stage of the operation.
- Write data other than the *Confirm Command* after the specified number of *data load* cycles.

The ABORT condition is indicated by DQ1 = 1, DQ7 = Data# (for the *last address location loaded*), DQ6 = TOGGLE, DQ5 = 0. This indicates that the Write Buffer Programming Operation was ABORTED. A *Write-to-Buffer-Abort reset* command sequence is required when using the write buffer Programming features in Unlock Bypass mode. Note that the Secured Silicon sector, autoselect, and CFI functions are unavailable when a program operation is in progress.

Write buffer programming is allowed in any sequence of memory (or address) locations. These flash devices are capable of handling multiple write buffer programming operations on the same write buffer address range without intervening erases.

Use of the write buffer is strongly recommended for programming when multiple words are to be programmed. Write buffer programming is approximately eight times faster than programming one word at a time.

Software Functions and Sample Code

Table 8.13 Write Buffer Program

(LLD Functions Used = lld_WriteToBufferCmd, lld_ProgramBufferToFlashCmd)

Cycle	Description	Operation	Byte Address	Word Address	Data
1	Unlock	Write	Base + AAAh	Base + 555h	00AAh
2	Unlock	Write	Base + 554h	Base + 2AAh	0055h
3	Write Buffer Load Command	Write	Program Address		0025h
4	Write Word Count	Write	Program Address		Word Count (N–1)h
Number of words (N) loaded into the write buffer can be from 1 to 32 words.					
5 to 36	Load Buffer Word N	Write	Program Address, Word N		Word N
Last	Write Buffer to Flash	Write	Sector Address		0029h

Notes:

1. *Base = Base Address.*
2. *Last = Last cycle of write buffer program operation; depending on number of words written, the total number of cycles may be from 6 to 37.*
3. *For maximum efficiency, it is recommended that the write buffer be loaded with the highest number of words (N words) possible.*

The following is a C source code example of using the write buffer program function. Refer to the *Spansion Low Level Driver User Guide* (available on www.amd.com and www.fujitsu.comm) for general information on Spansion Flash memory software development guidelines.

```
/* Example: Write Buffer Programming Command           */
/* NOTES: Write buffer programming limited to 16 words. */
/*        All addresses to be written to the flash in   */
/*        one operation must be within the same flash   */
/*        page. A flash page begins at addresses       */
/*        evenly divisible by 0x20.                     */
  UINT16 *src = source_of_data;               /* address of source data          */
  UINT16 *dst = destination_of_data;         /* flash destination address       */
  UINT16 wc   = words_to_program -1;          /* word count (minus 1)            */
  *( (UINT16 *)base_addr + 0x555 ) = 0x00AA;  /* write unlock cycle 1            */
  *( (UINT16 *)base_addr + 0x2AA ) = 0x0055;  /* write unlock cycle 2            */
  *( (UINT16 *)sector_address )    = 0x0025;  /* write write buffer load command */
  *( (UINT16 *)sector_address )    = wc;      /* write word count (minus 1)      */
loop:
  *dst = *src; /* ALL dst MUST BE SAME PAGE */ /* write source data to destination */
  dst++;                                      /* increment destination pointer    */
  src++;                                      /* increment source pointer         */
  if (wc == 0) goto confirm                   /* done when word count equals zero */
  wc--;                                       /* decrement word count             */
  goto loop;                                  /* do it again                      */
confirm:
  *( (UINT16 *)sector_address )    = 0x0029;  /* write confirm command           */
  /* poll for completion */


/* Example: Write Buffer Abort Reset */
  *( (UINT16 *)addr + 0x555 ) = 0x00AA;    /* write unlock cycle 1            */
  *( (UINT16 *)addr + 0x2AA ) = 0x0055;    /* write unlock cycle 2            */
  *( (UINT16 *)addr + 0x555 ) = 0x00F0;    /* write buffer abort reset        */
```

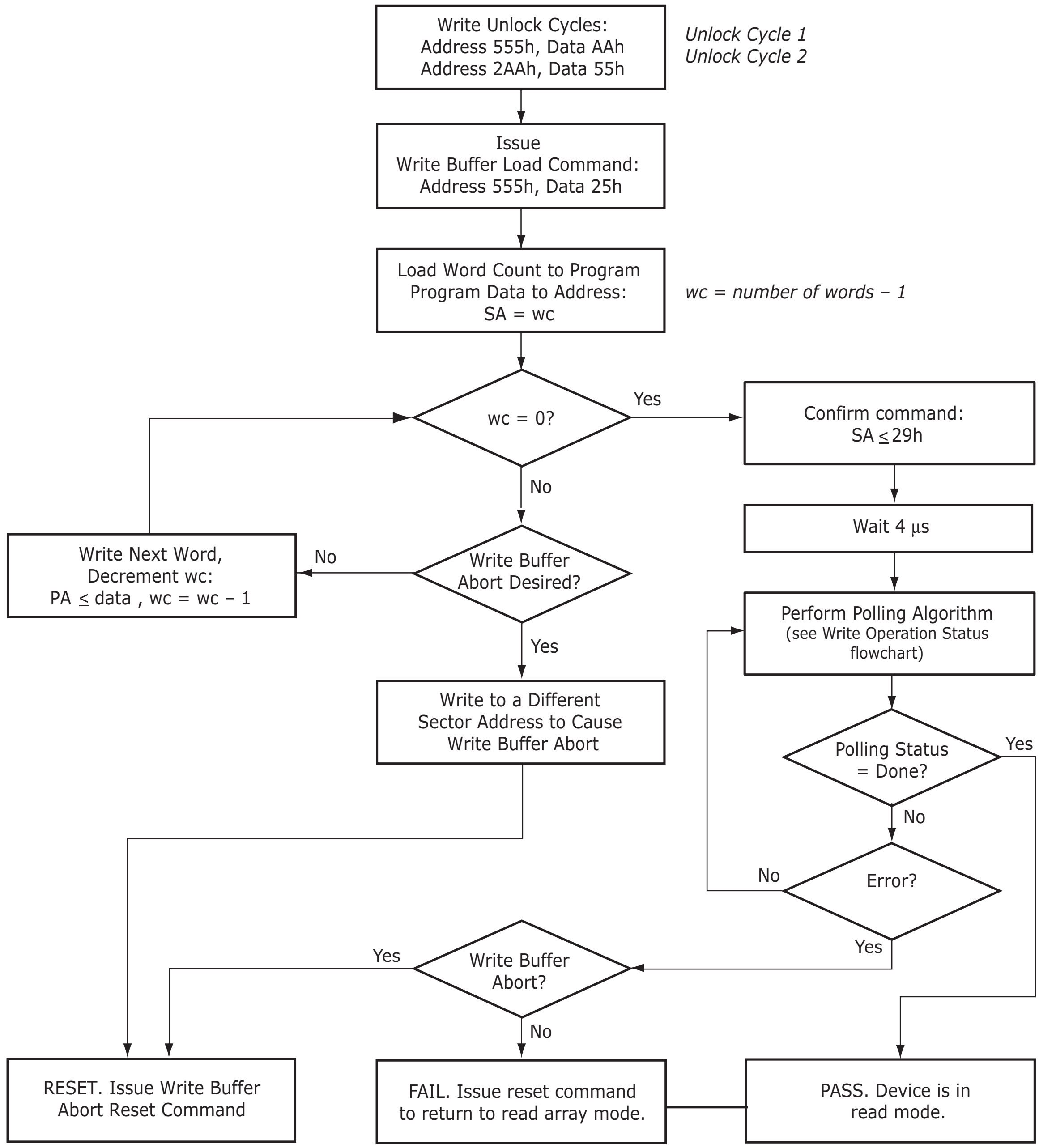


Figure 8.4 Write Buffer Programming Operation

8.5.3 Sector Erase

The sector erase function erases one or more sectors in the memory array. (See Table 13.1 and Figure 8.5) The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. After a successful sector erase, all locations within the erased sector contain FFFFh. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of no less than t_{SEA} occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than t_{SEA}.

Any sector erase address and command following the exceeded time-out (t_{SEA}) may or may not be accepted. Any command other than Sector Erase or Erase Suspend during the time-out period resets that bank to the read mode. The system can monitor DQ3 to determine if the sector erase timer has timed out (see DQ3: Sector Erase Timeout State Indicator). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the bank returns to reading array data and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can read data from the non-erasing banks. The system can determine the status of the erase operation by reading DQ7 or DQ6/DQ2 in the erasing bank. See Write Operation Status for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a hardware reset immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 8.5 illustrates the algorithm for the erase operation. See Erase/Program Timing for parameters and timing diagrams.

Software Functions and Sample Code

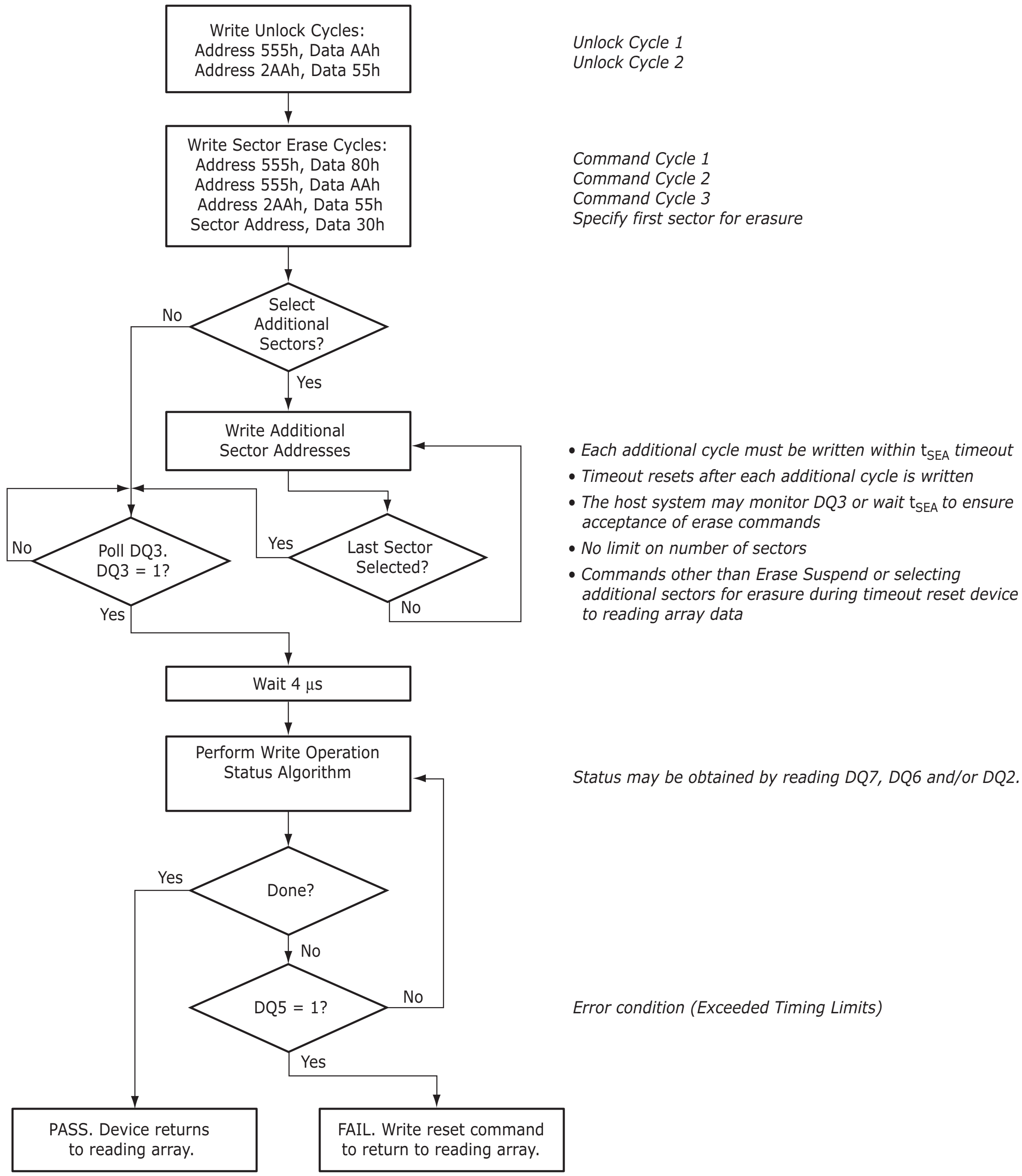
Table 8.14 Sector Erase

(LLD Function = lld_SectorEraseCmd)

Cycle	Description	Operation	Byte Address	Word Address	Data
1	Unlock	Write	Base + AAAh	Base + 555h	00AAh
2	Unlock	Write	Base + 554h	Base + 2AAh	0055h
3	Setup Command	Write	Base + AAAh	Base + 555h	0080h
4	Unlock	Write	Base + AAAh	Base + 555h	00AAh
5	Unlock	Write	Base + 554h	Base + 2AAh	0055h
6	Sector Erase Command	Write	Sector Address	Sector Address	0030h
Unlimited additional sectors may be selected for erase; command(s) must be written within t_{SEA}.					

The following is a C source code example of using the sector erase function. Refer to the *Spansion Low Level Driver User's Guide* (available on www.amd.com and www.fujitsu.com) for general information on Spansion Flash memory software development guidelines.

```
/* Example: Sector Erase Command */
  *( (UINT16 *)base_addr + 0x555 ) = 0x00AA;   /* write unlock cycle 1           */
  *( (UINT16 *)base_addr + 0x2AA ) = 0x0055;   /* write unlock cycle 2           */
  *( (UINT16 *)base_addr + 0x555 ) = 0x0080;   /* write setup command            */
  *( (UINT16 *)base_addr + 0x555 ) = 0x00AA;   /* write additional unlock cycle 1 */
  *( (UINT16 *)base_addr + 0x2AA ) = 0x0055;   /* write additional unlock cycle 2 */
  *( (UINT16 *)sector_address )    = 0x0030;   /* write sector erase command     */
```



Notes:

1. See Table 13.1 for erase command sequence.
2. See the section on DQ3 for information on the sector erase timeout.

Figure 8.5 Sector Erase Operation

8.5.4 Chip Erase Command Sequence

Chip erase is a six-bus cycle operation as indicated by Table 13.1. These commands invoke the Embedded Erase algorithm, which does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. After a successful chip erase, all locations of the chip contain FFFFh. The system is not required to provide any controls or timings during these operations. Table 13.1 and Table 13.2 in the appendix show the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, that bank returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7 or DQ6/DQ2. See Write Operation Status for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a hardware reset immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Software Functions and Sample Code

Table 8.15 Chip Erase

(LLD Function = lld_ChipEraseCmd)

Cycle	Description	Operation	Byte Address	Word Address	Data
1	Unlock	Write	Base + AAAh	Base + 555h	00AAh
2	Unlock	Write	Base + 554h	Base + 2AAh	0055h
3	Setup Command	Write	Base + AAAh	Base + 555h	0080h
4	Unlock	Write	Base + AAAh	Base + 555h	00AAh
5	Unlock	Write	Base + 554h	Base + 2AAh	0055h
6	Chip Erase Command	Write	Base + AAAh	Base + 555h	0010h

The following is a C source code example of using the chip erase function. Refer to the *Spansion Low Level Driver User's Guide* (available on www.amd.com and www.fujitsu.com) for general information on Spansion Flash memory software development guidelines.

```
/* Example: Chip Erase Command */
/* Note: Cannot be suspended   */
  *( (UINT16 *)base_addr + 0x555 ) = 0x00AA;   /* write unlock cycle 1            */
  *( (UINT16 *)base_addr + 0x2AA ) = 0x0055;   /* write unlock cycle 2            */
  *( (UINT16 *)base_addr + 0x555 ) = 0x0080;   /* write setup command             */
  *( (UINT16 *)base_addr + 0x555 ) = 0x00AA;   /* write additional unlock cycle 1 */
  *( (UINT16 *)base_addr + 0x2AA ) = 0x0055;   /* write additional unlock cycle 2 */
  *( (UINT16 *)base_addr + 0x000 ) = 0x0010;   /* write chip erase command        */
```

8.5.5 Erase Suspend/Erase Resume Commands

When the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation. The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. The bank address is required when writing this command. This command is valid only during the sector erase operation, including the minimum t_{SEA} time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation.

When the Erase Suspend command is written after the t_{SEA} time-out period has expired and during the sector erase operation, the device requires a maximum of t_{ESL} (erase suspend latency) to suspend the erase operation.

After the erase operation has been suspended, the bank enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device *erase suspends* all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7-DQ0. The system can use DQ7, or DQ6, and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to Table 8.23 for information on these status bits.

After an erase-suspended program operation is complete, the bank returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation.

In the erase-suspend-read mode, the system can also issue the Autoselect command sequence. See Write Buffer Programming and Autoselect for details.

To resume the sector erase operation, the system must write the Erase Resume command. The bank address of the erase-suspended bank is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Software Functions and Sample Code

Table 8.16 Erase Suspend

(LLD Function = lld_EraseSuspendCmd)

Cycle	Operation	Byte Address	Word Address	Data
1	Write	Bank Address	Bank Address	00B0h

The following is a C source code example of using the erase suspend function. Refer to the *Spansion Low Level Driver User's Guide* (available on www.amd.com and www.fujitsu.com) for general information on Spansion Flash memory software development guidelines.

```
/* Example: Erase suspend command */
  *( (UINT16 *)bank_addr + 0x000 ) = 0x00B0;   /* write suspend command           */
```

Table 8.17 Erase Resume

(LLD Function = lld_EraseResumeCmd)

Cycle	Operation	Byte Address	Word Address	Data
1	Write	Bank Address	Bank Address	0030h

The following is a C source code example of using the erase resume function. Refer to the *Spansion Low Level Driver User's Guide* (available on www.amd.com and www.fujitsu.com) for general information on Spansion Flash memory software development guidelines.

```
/* Example: Erase resume command */
  *( (UINT16 *)bank_addr + 0x000 ) = 0x0030;   /* write resume command            */
  /* The flash needs adequate time in the resume state */
```

8.5.6 Program Suspend / Program Resume Commands

The Program Suspend command allows the system to interrupt an embedded programming operation or a *Write to Buffer* programming operation so that data can read from any non-suspended sector. When the Program Suspend command is written during a programming process, the device halts the programming operation within t_{PSL} (program suspend latency) and updates the status bits. Addresses are *don't-cares* when writing the Program Suspend command.

After the programming operation has been suspended, the system can read array data from any non-suspended sector. The Program Suspend command may also be issued during a programming operation while an erase is suspended. In this case, data may be read from any addresses not in Erase Suspend or Program Suspend. If a read is needed from the Secured Silicon Sector area, then user must use the proper command sequences to enter and exit this region.

The system may also write the Autoselect command sequence when the device is in Program Suspend mode. The device allows reading Autoselect codes in the suspended sectors, since the codes are not stored in the memory array. When the device exits the Autoselect mode, the device reverts to Program Suspend mode, and is ready for another valid operation. See Autoselect for more information.

After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See Write Operation Status for more information.

The system must write the Program Resume command (address bits are *don't care*) to exit the Program Suspend mode and continue the programming operation. Further writes of the Program Resume command are ignored. Another Program Suspend command can be written after the device has resumed programming.

Software Functions and Sample Code

Table 8.18 Program Suspend

(LLD Function = lld_ProgramSuspendCmd)

Cycle	Operation	Byte Address	Word Address	Data
1	Write	Bank Address	Bank Address	00B0h

The following is a C source code example of using the program suspend function. Refer to the *Spansion Low Level Driver User's Guide* (available on www.amd.com and www.fujitsu.com) for general information on Spansion Flash memory software development guidelines.

```
/* Example: Program suspend command */
  *( (UINT16 *)base_addr + 0x000 ) = 0x00B0;   /* write suspend command           */
```

Table 8.19 Program Resume

(LLD Function = lld_ProgramResumeCmd)

Cycle	Operation	Byte Address	Word Address	Data
1	Write	Bank Address	Bank Address	0030h

The following is a C source code example of using the program resume function. Refer to the *Spansion Low Level Driver User's Guide* (available on www.amd.com and www.fujitsu.com) for general information on Spansion Flash memory software development guidelines.

```
/* Example: Program resume command */
  *( (UINT16 *)base_addr + 0x000 ) = 0x0030;   /* write resume command            */
```

8.5.7 Accelerated Program / Chip Erase

Accelerated single word programming, write buffer programming, sector erase, and chip erase operations are enabled through the ACC function. This method is faster than the standard chip program and erase command sequences.

The accelerated chip program and erase functions must not be used more than 10 times per sector. In addition, accelerated chip program and erase should be performed at room temperature (25°C ±10°C).

If the system asserts V_{HH} on this input, the device automatically enters the aforementioned Unlock Bypass mode and uses the higher voltage on the input to reduce the time required for program and erase operations. The system can then use the Write Buffer Load command sequence provided by the Unlock Bypass mode. Note that if a *Write-to-Buffer-Abort Reset* is required while in Unlock Bypass mode, the full 3-cycle RESET command sequence must be used to reset the device. Removing V_{HH} from the ACC input, upon completion of the embedded program or erase operation, returns the device to normal operation.

- Sectors must be unlocked prior to raising ACC to V_{HH}.
- The ACC pin must not be at V_{HH} for operations other than accelerated programming and accelerated chip erase, or device damage may result.
- The ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.
- ACC locks all sector if set to V_{IL}. ACC should be set to V_{IH} for all other conditions.

8.5.8 Unlock Bypass

The device features an Unlock Bypass mode to facilitate faster word programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program data, instead of the normal four cycles.

This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. See the Appendix for the requirements for the unlock bypass command sequences.

During the unlock bypass mode, only the Read, Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the bank address and the data 90h. The second cycle need only contain the data 00h. The bank then returns to the read mode.

Software Functions and Sample Code

The following are C source code examples of using the unlock bypass entry, program, and exit functions. Refer to the *Spansion Low Level Driver User's Guide* (available soon on www.amd.com and www.fujitsu.com) for general information on Spansion Flash "memory software development guidelines.

Table 8.20 Unlock Bypass Entry

(LLD Function = lld_UnlockBypassEntryCmd)

Cycle	Description	Operation	Byte Address	Word Address	Data
1	Unlock	Write	Base + AAAh	Base + 555h	00AAh
2	Unlock	Write	Base + 554h	Base + 2AAh	0055h
3	Entry Command	Write	Base + AAAh	Base + 555h	0020h

```
/* Example: Unlock Bypass Entry Command    */
  *( (UINT16 *)bank_addr + 0x555 ) = 0x00AA;   /* write unlock cycle 1          */
  *( (UINT16 *)bank_addr + 0x2AA ) = 0x0055;   /* write unlock cycle 2          */
  *( (UINT16 *)bank_addr + 0x555 ) = 0x0020;   /* write unlock bypass command   */
  /* At this point, programming only takes two write cycles.   */
  /* Once you enter Unlock Bypass Mode, do a series of like    */
  /* operations (programming or sector erase) and then exit    */
  /* Unlock Bypass Mode before beginning a different type of   */
  /* operations.                                               */
```

Table 8.21 Unlock Bypass Program

(LLD Function = lld_UnlockBypassProgramCmd)

Cycle	Description	Operation	Byte Address	Word Address	Data
1	Program Setup Command	Write	Base + xxxh	Base +xxxh	00A0h
2	Program Command	Write	Program Address	Program Address	Program Data

```
/* Example: Unlock Bypass Program Command  */
/* Do while in Unlock Bypass Entry Mode!   */
  *( (UINT16 *)bank_addr + 0x555 ) = 0x00A0;   /* write program setup command   */
  *( (UINT16 *)pa )                = data;     /* write data to be programmed   */
  /* Poll until done or error.    */
  /* If done and more to program, */
  /* do above two cycles again.   */
```

Table 8.22 Unlock Bypass Reset

(LLD Function = lld_UnlockBypassResetCmd)

Cycle	Description	Operation	Byte Address	Word Address	Data
1	Reset Cycle 1	Write	Base + xxxh	Base +xxxh	0090h
2	Reset Cycle 2	Write	Base + xxxh	Base +xxxh	0000h

```
/* Example: Unlock Bypass Exit Command */
  *( (UINT16 *)base_addr + 0x000 ) = 0x0090;
  *( (UINT16 *)base_addr + 0x000 ) = 0x0000;
```

8.5.9 Write Operation Status

The device provides several bits to determine the status of a program or erase operation. The following subsections describe the function of DQ1, DQ2, DQ3, DQ5, DQ6, and DQ7.

DQ7: Data# Polling. The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether a bank is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence. Note that the Data# Polling is valid only for the last word being programmed in the write-buffer-page during Write Buffer Programming. Reading Data# Polling status on any word other than the last word to be programmed in the write-buffer-page returns false status information.

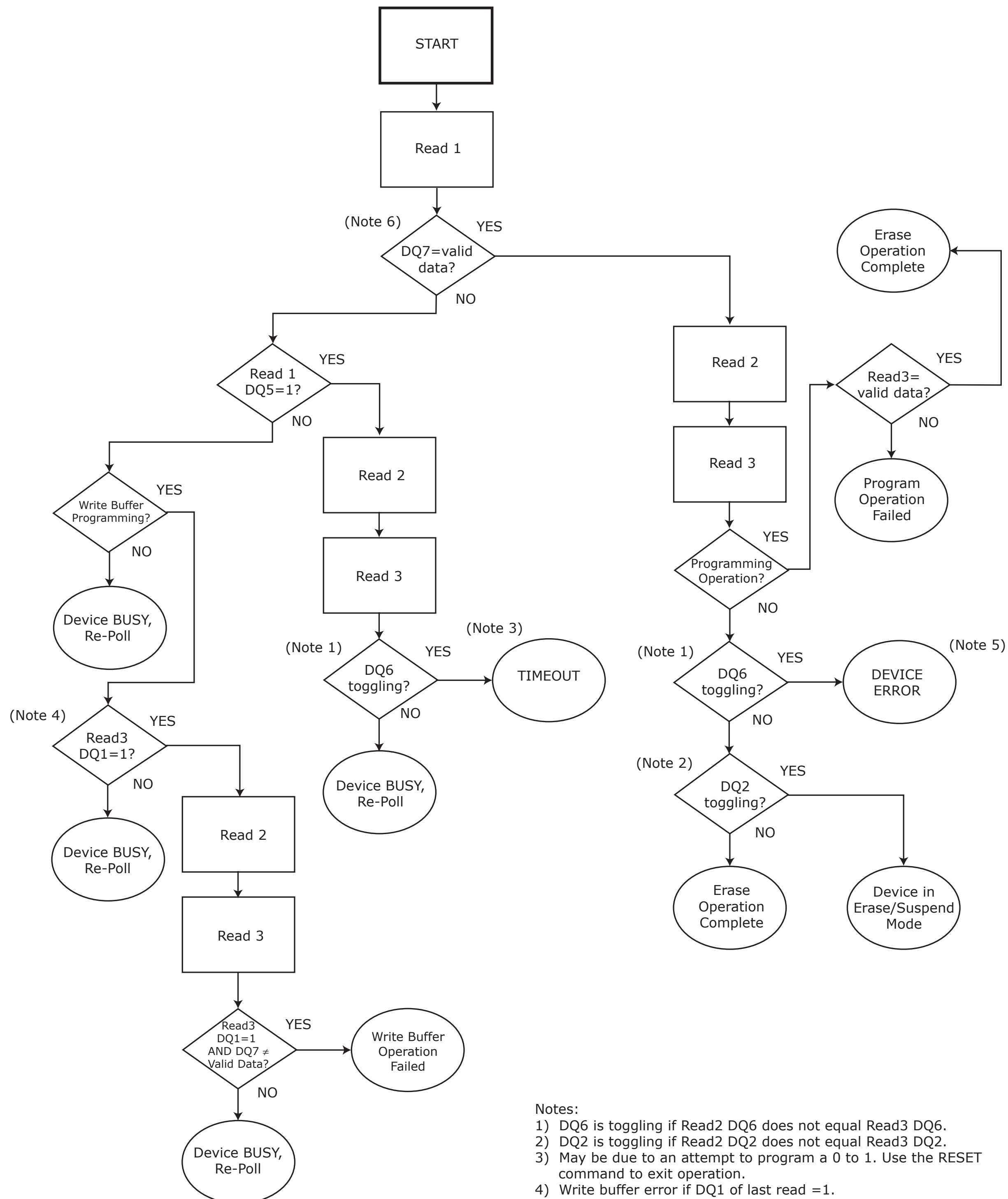
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# polling on DQ7 is active for approximately t_{PSP}, then that bank returns to the read mode.

During the Embedded Erase Algorithm, Data# polling produces a *0* on DQ7. When the Embedded Erase algorithm is complete, or if the bank enters the Erase Suspend mode, Data# Polling produces a *1* on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately t_{ASP}, then the bank returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ6-DQ0 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ6-DQ0 may be still invalid. Valid data on DQ7-D00 appears on successive read cycles.

See the following for more information: Table 8.23, Write Operation Status, shows the outputs for Data# Polling on DQ7. Figure 8.6, Write Operation Status Flowchart, shows the Data# Polling algorithm; and Figure 12.17, Data# Polling Timings (During Embedded Algorithm), shows the Data# Polling timing diagram.



Notes:
1) DQ6 is toggling if Read2 DQ6 does not equal Read3 DQ6.
2) DQ2 is toggling if Read2 DQ2 does not equal Read3 DQ2.
3) May be due to an attempt to program a 0 to 1. Use the RESET command to exit operation.
4) Write buffer error if DQ1 of last read =1.
5) Invalid state, use RESET command to exit operation.
6) Valid data is the data that is intended to be programmed or all 1's for an erase operation.
7) Data polling algorithm valid for all operations except advanced sector protection.

Figure 8.6 Write Operation Status Flowchart

DQ6: Toggle Bit I . Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address in the same bank, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately t_{ASP} [all sectors protected toggle time], then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately t_{PAP} after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program Algorithm is complete.

See the following for additional information: Figure 8.6, Write Operation Status Flowchart; Figure 12.18, Toggle Bit Timings (During Embedded Algorithm), and Table 8.23 and Table 8.24.

Toggle Bit I on DQ6 requires either OE# or CE# to be de-asserted and reasserted to show the change in state.

DQ2: Toggle Bit II . The *Toggle Bit II* on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence. DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 8.23 to compare outputs for DQ2 and DQ6. See the following for additional information: Figure 8.6, the DQ6: Toggle Bit I section, and Figures 12.17–12.20.

Reading Toggle Bits DQ6/DQ2. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erases operation. The system can read array data on DQ7–DQ0 on the following read cycle. However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erases operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data. The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation. Refer to Figure 8.6 for more details.

DQ5: Exceeded Timing Limits. DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a *1*, indicating that the program or erase cycle was not successfully completed. The device may output a *1* on DQ5 if the system tries to program a *1* to a location that was previously programmed to *0* Only an erase operation can change a *0* back to a *1.* Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a *1.* Under both these conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if a bank was previously in the erase-suspend-program mode).

DQ3: Sector Erase Timeout State Indicator. After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a *0* to a *1.* If the time between additional sector erase commands from the system can be assumed to be less than t_{SEA}, the system need not monitor DQ3. See Sector Erase Command Sequence for more details.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is *1*, the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is *0* the device accepts additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each sub-sequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. Table 8.23 shows the status of DQ3 relative to the other status bits.

DQ1: Write to Buffer Abort. DQ1 indicates whether a Write to Buffer operation was aborted. Under these conditions DQ1 produces a *1*. The system must issue the Write to Buffer Abort Reset command sequence to return the device to reading array data. See Write Buffer Programming Operation for more details.

Table 8.23 Write Operation Status

Program Suspend Mode (Note 3)	Reading within Program Suspended Sector	INVALID *(Not Allowed)*	INVALID *(Not Allowed)*	INVALID *(Not Allowed)*	INVALID *(Not Allowed)*	INVALID *(Not Allowed)*	INVALID *(Not Allowed)*
	Reading within Non-Program Suspended Sector	Data	Data	Data	Data	Data	Data
Write to Buffer (Note 5)	BUSY State	DQ7#	Toggle	0	N/A	N/A	0
	Exceeded Timing Limits	DQ7#	Toggle	1	N/A	N/A	0
	ABORT State	DQ7#	Toggle	0	N/A	N/A	1

Notes:

1. *DQ5 switches to* 1 *when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.*
2. *DQ7 a valid address when reading status information. Refer to the appropriate subsection for further details.*
3. *Data are invalid for addresses in a Program Suspended sector.*
4. *DQ1 indicates the Write to Buffer ABORT status during Write Buffer Programming operations.*
5. *The data-bar polling algorithm should be used for Write Buffer Programming operations. Note that DQ7# during Write Buffer Programming indicates the data-bar for DQ7 data for the* ***Last Loaded Write-buffer Address location****.*

8.6 Simultaneous Read/Write

The simultaneous read/write feature allows the host system to read data from one bank of memory while programming or erasing another bank of memory. An erase operation may also be suspended to read from or program another location within the same bank (except the sector being erased). Figure 12.24, Back-to-Back Read/Write Cycle Timings, shows how read and write cycles may be initiated for simultaneous operation with zero latency. Refer to the DC Characteristics table for read-while-program and read-while-erase current specification.

8.7 Writing Commands/Command Sequences

When the device is configured for Asynchronous read, only Asynchronous write operations are allowed, and CLK is ignored. When in the Synchronous read mode configuration, the device is able to perform both Asynchronous and Synchronous write operations. CLK and AVD# induced address latches are supported in the Synchronous programming mode. During a synchronous write operation, to write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive AVD# and CE# to V_{IL}, and OE# to V_{IH} when providing an address to the device, and drive WE# and CE# to V_{IL}, and OE# to V_{IH} when writing commands or data. During an asynchronous write operation, the system must drive CE# and WE# to V_{IL} and OE# to V_{IH} when providing an address, command, and data. Addresses are latched on the last falling edge of WE# or CE#, while data is latched on the 1st rising edge of WE# or CE#. An erase operation can erase one sector, multiple sectors, or the entire device. Tables 7.1–7.3 indicate the address space that each sector occupies. The device address space is divided into sixteen banks: Banks 1 through 14 contain only 64 Kword sectors, while Banks 0 and 15 contain both 16 Kword boot sectors in addition to 64 Kword sectors. A *bank address* is the set of address bits required to uniquely select a bank. Similarly, a *sector address* is the address bits required to uniquely select a sector. I_{CC2} in DC Characteristics represents the active current specification for the write mode. AC Characteristics—Synchronous and AC Characteristics—Asynchronous Read contain timing specification tables and timing diagrams for write operations.

8.8 Handshaking

The handshaking feature allows the host system to detect when data is ready to be read by simply monitoring the RDY (Ready) pin, which is a dedicated output and controlled by CE#.

When the device is configured to operate in synchronous mode, and OE# is low (active), the initial word of burst data becomes available after either the falling or rising edge of the RDY pin (depending on the setting for bit 10 in the Configuration Register). It is recommended that the host system set CR13–CR11 in the Configuration Register to the appropriate number of wait states to ensure optimal burst mode operation (see Table 8.8, Configuration Register).

Bit 8 in the Configuration Register allows the host to specify whether RDY is active at the same time that data is ready, or one cycle before data is ready.

8.9 Hardware Reset

The RESET# input provides a hardware method of resetting the device to reading array data. When RESET# is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all outputs, resets the configuration register, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data.

To ensure data integrity the operation that was interrupted should be reinitiated once the device is ready to accept another command sequence.

When RESET# is held at V_{SS}, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL}, but not at V_{SS}, the standby current is greater.

RESET# may be tied to the system reset circuitry which enables the system to read the boot-up firmware from the Flash memory upon a system reset.

See Figures 12.5 and 12.12 for timing diagrams.

8.10 Software Reset

Software reset is part of the command set (see Table 13.1) that also returns the device to array read mode and must be used for the following conditions:

1. to exit Autoselect mode
2. when DQ5 goes high during write status operation that indicates program or erase cycle was not successfully completed
3. exit sector lock/unlock operation.
4. to return to erase-suspend-read mode if the device was previously in Erase Suspend mode.
5. after any aborted operations

Software Functions and Sample Code

Table 8.24 Reset

(LLD Function = lld_ResetCmd)

Cycle	Operation	Byte Address	Word Address	Data
Reset Command	Write	Base + xxxh	Base + xxxh	00F0h

Note: *Base = Base Address.*

The following is a C source code example of using the reset function. Refer to the *Spansion Low Level Driver User's Guide* (available on www.amd.com and www.fujitsu.com) for general information on Spansion Flash memory software development guidelines.

```
/* Example: Reset (software reset of Flash state machine) */
  *( (UINT16 *)base_addr + 0x000 ) = 0x00F0;
```

The following are additional points to consider when using the reset command:

- This command resets the banks to the read and address bits are ignored.
- Reset commands are ignored once erasure has begun until the operation is complete.
- Once programming begins, the device ignores reset commands until the operation is complete
- The reset command may be written between the cycles in a program command sequence before programming begins (prior to the third cycle). This resets the bank to which the system was writing to the read mode.

- If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode.
- The reset command may be also written during an Autoselect command sequence.
- If a bank has entered the Autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode.
- If DQ1 goes high during a Write Buffer Programming operation, the system must write the *Write to Buffer Abort Reset* command sequence to RESET the device to reading array data. The standard RESET command does not work during this condition.
- To exit the unlock bypass mode, the system must issue a two-cycle unlock bypass reset command sequence [see command table for details].

9 Advanced Sector Protection/Unprotection

The Advanced Sector Protection/Unprotection feature disables or enables programming or erase operations in any or all sectors and can be implemented through software and/or hardware methods, which are independent of each other. This section describes the various methods of protecting data stored in the memory array. An overview of these methods in shown in Figure 9.1.

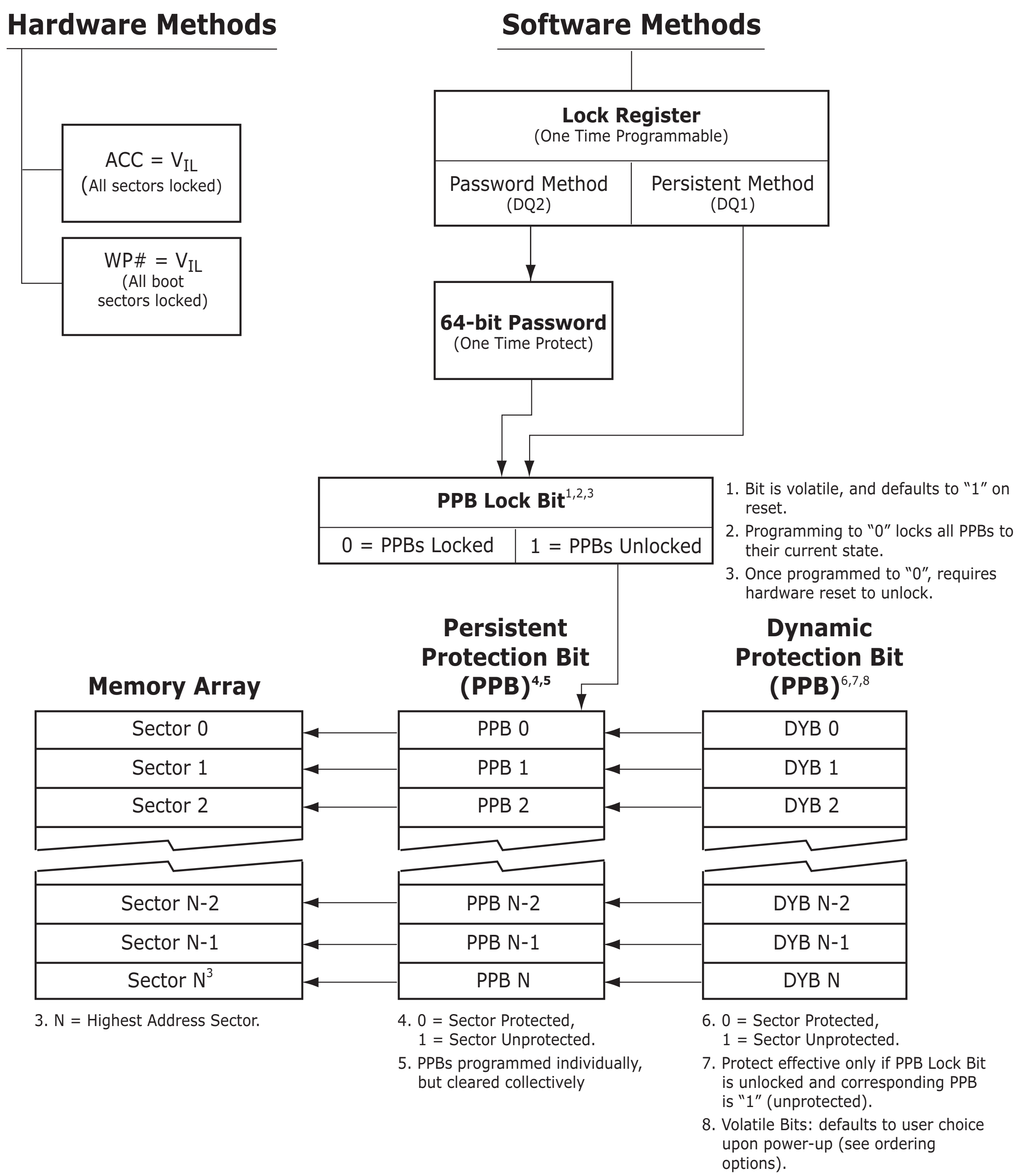


Figure 9.1 Advanced Sector Protection/Unprotection

9.1 Lock Register

As shipped from the factory, all devices default to the persistent mode when power is applied, and all sectors are unprotected, unless otherwise chosen through the DYB ordering option. The device programmer or host system must then choose which sector protection method to use. Programming (setting to *0*) any one of the following two one-time programmable, non-volatile bits locks the part permanently in that mode:

- Lock Register Persistent Protection Mode Lock Bit (DQ1)
- Lock Register Password Protection Mode Lock Bit (DQ2)

Table 9.1 Lock Register

Device	DQ15-05	DQ4	DQ3	DQ2	DQ1	DQ0
S29WS256N	1	1	1	Password Protection Mode Lock Bit	Persistent Protection Mode Lock Bit	Customer Secured Silicon Sector Protection Bit
S29WS128N/ S29WS064N	Undefined	DYB Lock Boot Bit 0 = sectors power up protected 1 = sectors power up unprotected	PPB One-Time Programmable Bit 0 = All PPB erase command disabled 1 = All PPB Erase command enabled	Password Protection Mode Lock Bit	Persistent Protection Mode Lock Bit	Secured Silicon Sector Protection Bit

For programming lock register bits refer to Table 13.2.

Notes

1. If the password mode is chosen, the password must be programmed before setting the corresponding lock register bit.
2. After the Lock Register Bits Command Set Entry command sequence is written, reads and writes for Bank 0 are disabled, while reads from other banks are allowed until exiting this mode.
3. If both lock bits are selected to be programmed (to zeros) at the same time, the operation aborts.
4. Once the Password Mode Lock Bit is programmed, the Persistent Mode Lock Bit is permanently disabled, and no changes to the protection scheme are allowed. Similarly, if the Persistent Mode Lock Bit is programmed, the Password Mode is permanently disabled.

After selecting a sector protection method, each sector can operate in any of the following three states:

1. *Constantly locked.* The selected sectors are protected and can not be reprogrammed unless PPB lock bit is cleared via a password, hardware reset, or power cycle.
2. *Dynamically locked.* The selected sectors are protected and can be altered via software commands.
3. *Unlocked.* The sectors are unprotected and can be erased and/or programmed.

These states are controlled by the bit types described in Sections 9.2–9.6.

9.2 Persistent Protection Bits

The Persistent Protection Bits are unique and nonvolatile for each sector and have the same endurances as the Flash memory. Preprogramming and verification prior to erasure are handled by the device, and therefore do not require system monitoring.

Notes

1. Each PPB is individually programmed and all are erased in parallel.
2. While programming PPB for a sector, array data can be read from any other bank, except Bank 0 (used for Data# Polling) and the bank in which sector PPB is being programmed.
3. Entry command disables reads and writes for the bank selected.
4. Reads within that bank return the PPB status for that sector.
5. Reads from other banks are allowed while writes are not allowed.
6. All Reads must be performed using the Asynchronous mode.
7. The specific sector address (A23-A14 WS256N, A22-A14 WS128N, A21-A14 WS064N) are written at the same time as the program command.
8. If the PPB Lock Bit is set, the PPB Program or erase command does not execute and times-out without programming or erasing the PPB.
9. There are no means for individually erasing a specific PPB and no specific sector address is required for this operation.
10. Exit command must be issued after the execution which resets the device to read mode and re-enables reads and writes for Bank 0
11. The programming state of the PPB for a given sector can be verified by writing a PPB Status Read Command to the device as described by the flow chart shown in Figure 9.2.

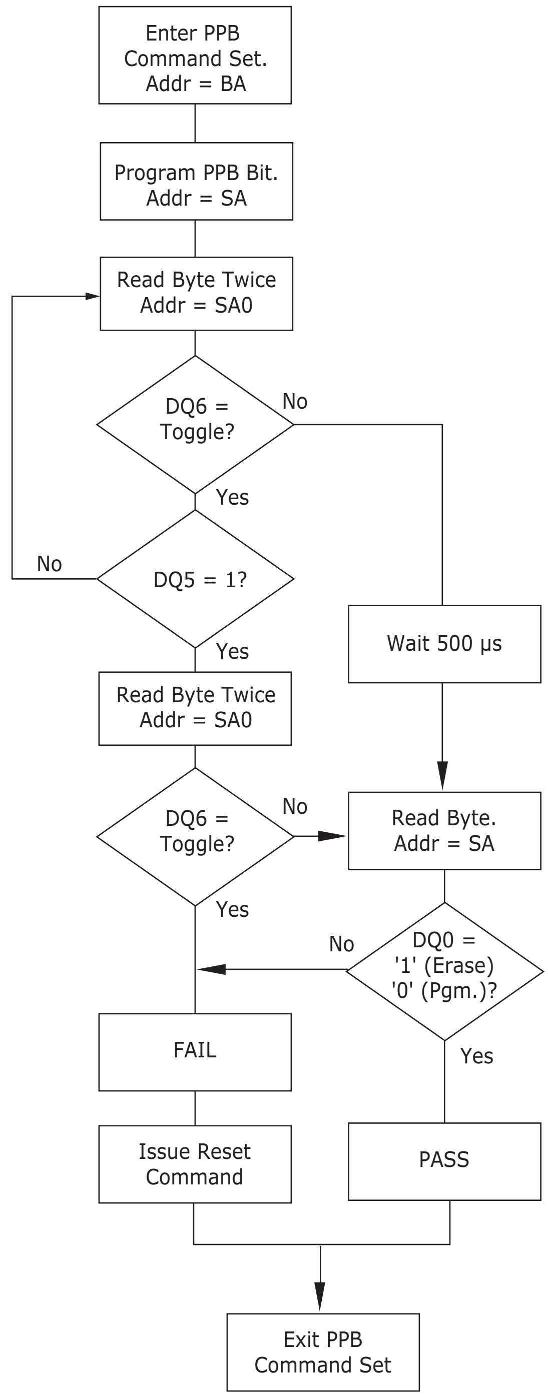


Figure 9.2 PPB Program/Erase Algorithm

9.3 Dynamic Protection Bits

Dynamic Protection Bits are volatile and unique for each sector and can be individually modified. DYBs only control the protection scheme for unprotected sectors that have their PPBs cleared (erased to *1*). By issuing the DYB Set or Clear command sequences, the DYBs are set (programmed to *0*) or cleared (erased to *1*), thus placing each sector in the protected or unprotected state respectively. This feature allows software to easily protect sectors against inadvertent changes yet does not prevent the easy removal of protection when changes are needed.

Notes

1. The DYBs can be set (programmed to *0*) or cleared (erased to *1*) as often as needed.

When the parts are first shipped, the PPBs are cleared (erased to *1*) and upon power up or reset, the DYBs can be set or cleared depending upon the ordering option chosen.

2. If the option to clear the DYBs after power up is chosen, (erased to *1*), then the sectorsmay be modified depending upon the PPB state of that sector (see Table 9.2).
3. The sectors would be in the protected state If the option to set the DYBs after power up is chosen (programmed to *0*).
4. It is possible to have sectors that are persistently locked with sectors that are left in the dynamic state.
5. The DYB Set or Clear commands for the dynamic sectors signify protected or unprotected state of the sectors respectively. However, if there is a need to change the status of the persistently locked sectors, a few more steps are required. First, the PPB Lock Bit must be cleared by either putting the device through a power-cycle, or hardware reset. The PPBs can then be changed to reflect the desired settings. Setting the PPB Lock Bit once again locks the PPBs, and the device operates normally again.
6. To achieve the best protection, it is recommended to execute the PPB Lock Bit Set command early in the boot code and protect the boot code by holding WP# = V_{IL}. Note that the PPB and DYB bits have the same function when ACC = V_{HH} as they do when ACC =V_{IH}.

9.4 Persistent Protection Bit Lock Bit

The Persistent Protection Bit Lock Bit is a global volatile bit for all sectors. When set (programmed to *0*), it locks all PPBs and when cleared (programmed to *1*), allows the PPBs to be changed. There is only one PPB Lock Bit per device.

Notes

1. No software command sequence unlocks this bit unless the device is in the password protection mode; only a hardware reset or a power-up clears this bit.
2. The PPB Lock Bit must be set (programmed to *0*) only after all PPBs are configured to the desired settings.

9.5 Password Protection Method

The Password Protection Method allows an even higher level of security than the Persistent Sector Protection Mode by requiring a 64 bit password for unlocking the device PPB Lock Bit. In addition to this password requirement, after power up and reset, the PPB Lock Bit is set *0* to maintain the password mode of operation. Successful execution of the Password Unlock command by entering the entire password clears the PPB Lock Bit, allowing for sector PPBs modifications.

Notes

1. There is no special addressing order required for programming the password. Once the Password is written and verified, the Password Mode Locking Bit must be set in order to prevent access.
2. The Password Program Command is only capable of programming *0*s. Programming a *1* after a cell is programmed as a *0* results in a time-out with the cell as a *0*.
3. The password is all *1*s when shipped from the factory.
4. All 64-bit password combinations are valid as a password.
5. There is no means to verify what the password is after it is set.
6. The Password Mode Lock Bit, once set, prevents reading the 64-bit password on the data bus and further password programming.
7. The Password Mode Lock Bit is not erasable.
8. The lower two address bits (A1–A0) are valid during the Password Read, Password Program, and Password Unlock.
9. The exact password must be entered in order for the unlocking function to occur.
10. The Password Unlock command cannot be issued any faster than 1 µs at a time to prevent a hacker from running through all the 64-bit combinations in an attempt to correctly match a password.
11. Approximately 1 µs is required for unlocking the device after the valid 64-bit password is given to the device.
12. Password verification is only allowed during the password programming operation.
13. All further commands to the password region are disabled and all operations are ignored.
14. If the password is lost after setting the Password Mode Lock Bit, there is no way to clear the PPB Lock Bit.
15. Entry command sequence must be issued prior to any of any operation and it disables reads and writes for Bank 0. Reads and writes for other banks excluding Bank 0 are allowed.
16. If the user attempts to program or erase a protected sector, the device ignores the command and returns to read mode.
17. A program or erase command to a protected sector enables status polling and returns to read mode without having modified the contents of the protected sector.
18. The programming of the DYB, PPB, and PPB Lock for a given sector can be verified by writing individual status read commands DYB Status, PPB Status, and PPB Lock Status to the device.

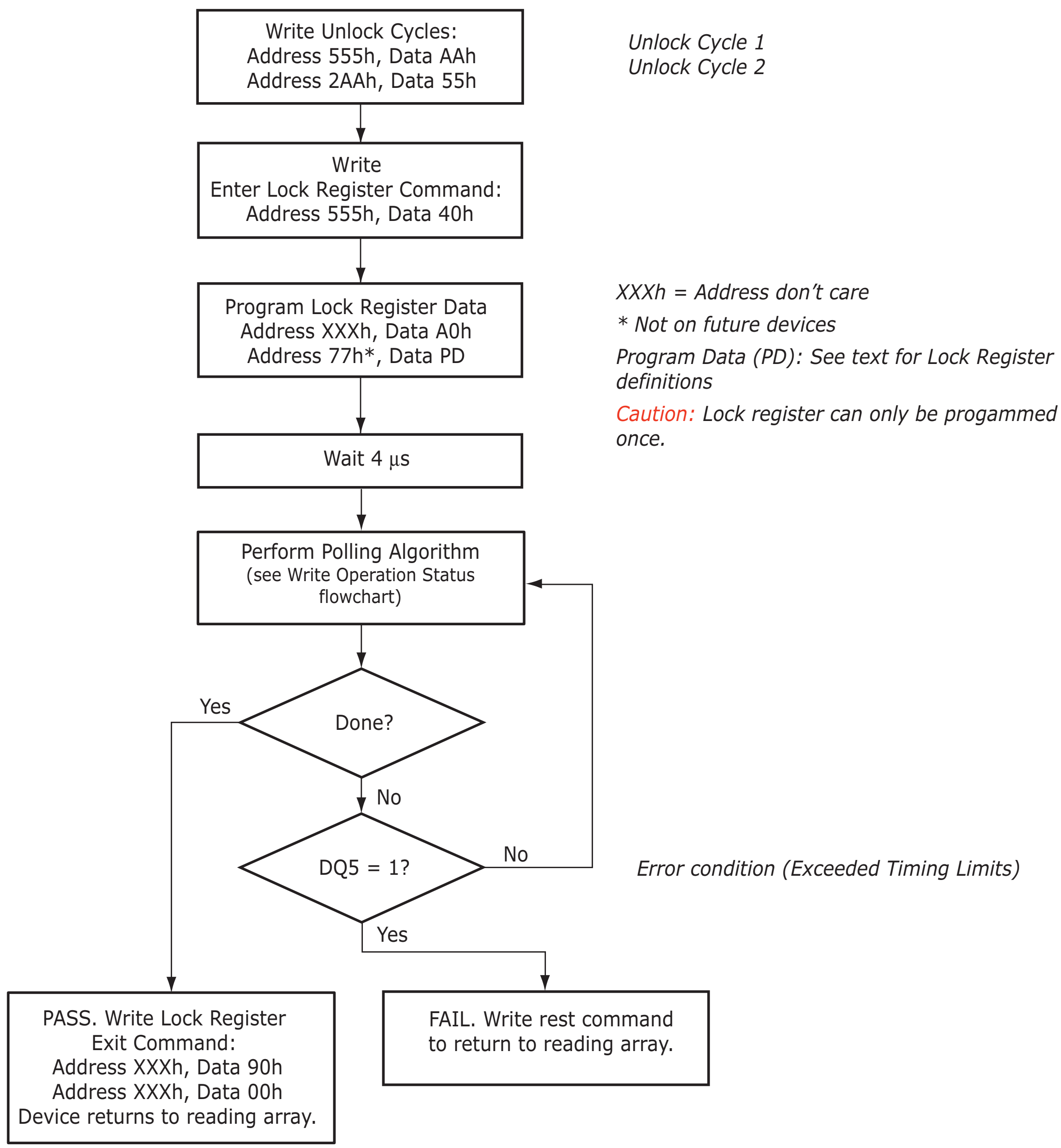


Figure 9.3 Lock Register Program Algorithm

9.6 Advanced Sector Protection Software Examples

Table 9.2

Unique Device PPB Lock Bit 0 = locked 1 = unlocked		**Sector PPB** 0 = protected 1 = unprotected	**Sector DYB** 0 = protected 1 = unprotected	**Sector Protection Status**
Any Sector	0	0	x	Protected through PPB
Any Sector	0	0	x	Protected through PPB
Any Sector	0	1	1	Unprotected
Any Sector	0	1	0	Protected through DYB
Any Sector	1	0	x	Protected through PPB
Any Sector	1	0	x	Protected through PPB
Any Sector	1	1	0	Protected through DYB
Any Sector	1	1	1	Unprotected

Table 9.2 contains all possible combinations of the DYB, PPB, and PPB Lock Bit relating to the status of the sector. In summary, if the PPB Lock Bit is locked (set to *0*), no changes to the PPBs are allowed. The PPB Lock Bit can only be unlocked (reset to *1*) through a hardware reset or power cycle. See also Figure 9.1 for an overview of the Advanced Sector Protection feature.

9.7 Hardware Data Protection Methods

The device offers two main types of data protection at the sector level via hardware control:

- When WP# is at V_{IL}, the four outermost sectors are locked (device specific).
- When ACC is at V_{IL}, all sectors are locked.

There are additional methods by which intended or accidental erasure of any sectors can be prevented via hardware means. The following subsections describes these methods:

9.7.1 WP# Method

The Write Protect feature provides a hardware method of protecting the four outermost sectors. This function is provided by the WP# pin and overrides the previously discussed Sector Protection/Unprotection method.

If the system asserts V_{IL} on the WP# pin, the device disables program and erase functions in the *outermost* boot sectors. The outermost boot sectors are the sectors containing both the lower and upper set of sectors in a dual-boot-configured device.

If the system asserts V_{IH} on the WP# pin, the device reverts to whether the boot sectors were last set to be protected or unprotected. That is, sector protection or unprotection for these sectors depends on whether they were last protected or unprotected.

Note that the WP# pin must not be left floating or unconnected as inconsistent behavior of the device may result.

The WP# pin must be held stable during a command sequence execution

9.7.2 ACC Method

This method is similar to above, except it protects all sectors. Once ACC input is set to V_{IL}, all program and erase functions are disabled and hence all sectors are protected.

9.7.3 Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down.

The command register and all internal program/erase circuits are disabled, and the device resets to reading array data. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control inputs to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

9.7.4 Write Pulse Glitch Protection

Noise pulses of less than 3 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

9.7.5 Power-Up Write Inhibit

If WE# = CE# = RESET# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

10 Power Conservation Modes

10.1 Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input. The device enters the CMOS standby mode when the CE# and RESET# inputs are both held at V_{CC} ± 0.2 V. The device requires standard access time (t_{CE}) for read access, before it is ready to read data. If the device is deselected during erasure or programming, the device draws active current until the operation is completed. I_{CC3} in DC Characteristics represents the standby current specification

10.2 Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption while in asynchronous mode. the device automatically enables this mode when addresses remain stable for t_{ACC} + 20 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. While in synchronous mode, the automatic sleep mode is disabled. Note that a new burst operation is required to provide new data. I_{CC6} in DC Characteristics represents the automatic sleep mode current specification.

10.3 Hardware RESET# Input Operation

The RESET# input provides a hardware method of resetting the device to reading array data. When RESET# is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all outputs, resets the configuration register, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence to ensure data integrity.

When RESET# is held at V_{SS} ± 0.2 V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within V_{SS} ± 0.2 V, the standby current is greater.

RESET# may be tied to the system reset circuitry and thus, a system reset would also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

10.4 Output Disable (OE#)

When the OE# input is at V_{IH}, output from the device is disabled. The outputs are placed in the high impedance state.

11 Secured Silicon Sector Flash Memory Region

The Secured Silicon Sector provides an extra Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The Secured Silicon Sector is 256 words in length that consists of 128 words for factory data and 128 words for customer-secured areas. All Secured Silicon reads outside of the 256-word address range returns invalid data. The Factory Indicator Bit, DQ7, (at Autoselect address 03h) is used to indicate whether or not the Factory Secured Silicon Sector is locked when shipped from the factory. The Customer Indicator Bit (DQ6) is used to indicate whether or not the Customer Secured Silicon Sector is locked when shipped from the factory.

Please note the following general conditions:

- While Secured Silicon Sector access is enabled, simultaneous operations are allowed except for Bank 0.
- On power-up, or following a hardware reset, the device reverts to sending commands to the normal address space.
- Reads can be performed in the Asynchronous or Synchronous mode.
- Burst mode reads within Secured Silicon Sector wrap from address FFh back to address 00h.
- Reads outside of sector 0 return memory array data.
- Continuous burst read past the maximum address is undefined.
- Sector 0 is remapped from memory array to Secured Silicon Sector array.
- Once the Secured Silicon Sector Entry Command is issued, the Secured Silicon Sector Exit command must be issued to exit Secured Silicon Sector Mode.
- The Secured Silicon Sector is not accessible when the device is executing an Embedded Program or Embedded Erase algorithm.

Table 11.1 Addresses

Sector	Sector Size	Address Range
Customer	128 words	000080h-0000FFh
Factory	128 words	000000h-00007Fh

11.1 Factory Secured SiliconSector

The Factory Secured Silicon Sector is always protected when shipped from the factory and has the Factory Indicator Bit (DQ7) permanently set to a *1*. This prevents cloning of a factory locked part and ensures the security of the ESN and customer code once the product is shipped to the field.

These devices are available pre programmed with one of the following:

- A random, 8 Word secure ESN only within the Factory Secured Silicon Sector
- Customer code within the Customer Secured Silicon Sector through the Spansion™ programming service.
- Both a random, secure ESN and customer code through the Spansion programming service.

Customers may opt to have their code programmed through the Spansion programming services. Spansion programs the customer's code, with or without the random ESN. The devices are then shipped from the Spansion factory with the Factory Secured Silicon Sector and Customer Secured Silicon Sector permanently locked. Contact your local representative for details on using Spansion programming services.

11.2 Customer Secured Silicon Sector

The Customer Secured Silicon Sector is typically shipped unprotected (DQ6 set to *0*), allowing customers to utilize that sector in any manner they choose. If the security feature is not required, the Customer Secured Silicon Sector can be treated as an additional Flash memory space.

Please note the following:

- Once the Customer Secured Silicon Sector area is protected, the Customer Indicator Bit is permanently set to *1.*
- The Customer Secured Silicon Sector can be read any number of times, but can be programmed and locked only once. The Customer Secured Silicon Sector lock must be used with caution as once locked, there is no procedure available for unlocking the Customer Secured Silicon Sector area and none of the bits in the Customer Secured Silicon Sector memory space can be modified in any way.
- The accelerated programming (ACC) and unlock bypass functions are not available when programming the Customer Secured Silicon Sector, but reading in Banks 1 through 15 is available.
- Once the Customer Secured Silicon Sector is locked and verified, the system must write the Exit Secured Silicon Sector Region command sequence which return the device to the memory array at sector 0.

11.3 Secured Silicon Sector Entry and Secured Silicon Sector Exit Command Sequences

The system can access the Secured Silicon Sector region by issuing the three-cycle Enter Secured Silicon Sector command sequence. The device continues to access the Secured Silicon Sector region until the system issues the four-cycle Exit Secured Silicon Sector command sequence.

See Command Definition Table [Secured Silicon Sector Command Table, Appendix Table 13.1 for address and data requirements for both command sequences.

The Secured Silicon Sector Entry Command allows the following commands to be executed

- Read customer and factory Secured Silicon areas
- Program the customer Secured Silicon Sector

After the system has written the Enter Secured Silicon Sector command sequence, it may read the Secured Silicon Sector by using the addresses normally occupied by sector SA0 within the memory array. This mode of operation continues until the system issues the Exit Secured Silicon Sector command sequence, or until power is removed from the device.

Software Functions and Sample Code

The following are C functions and source code examples of using the Secured Silicon Sector Entry, Program, and exit commands. Refer to the *Spansion Low Level Driver User's Guide* (available soon on www.amd.com and www.fujitsu.com) for general information on Spansion Flash memory software development guidelines.

Table 11.2 Secured Silicon Sector Entry

(LLD Function = lld_SecSiSectorEntryCmd)

Cycle	Operation	Byte Address	Word Address	Data
Unlock Cycle 1	Write	Base + AAAh	Base + 555h	00AAh
Unlock Cycle 2	Write	Base + 554h	Base + 2AAh	0055h
Entry Cycle	Write	Base + AAAh	Base + 555h	0088h

Note: *Base = Base Address.*

```
/* Example: SecSi Sector Entry Command */
  *( (UINT16 *)base_addr + 0x555 ) = 0x00AA;   /* write unlock cycle 1           */
  *( (UINT16 *)base_addr + 0x2AA ) = 0x0055;   /* write unlock cycle 2           */
  *( (UINT16 *)base_addr + 0x555 ) = 0x0088;   /* write Secsi Sector Entry Cmd   */
```

Table 11.3 Secured Silicon Sector Program

(LLD Function = lld_ProgramCmd)

Cycle	Operation	Byte Address	Word Address	Data
Unlock Cycle 1	Write	Base + AAAh	Base + 555h	00AAh
Unlock Cycle 2	Write	Base + 554h	Base + 2AAh	0055h
Program Setup	Write	Base + AAAh	Base + 555h	00A0h
Program	Write	Word Address	Word Address	Data Word

Note: *Base = Base Address.*

```
/* Once in the SecSi Sector mode, you program */
/* words using the programming algorithm.     */
```

Table 11.4 Secured Silicon Sector Exit

(LLD Function = lld_SecSiSectorExitCmd)

Cycle	Operation	Byte Address	Word Address	Data
Unlock Cycle 1	Write	Base + AAAh	Base + 555h	00AAh
Unlock Cycle 2	Write	Base + 554h	Base + 2AAh	0055h
Exit Cycle	Write	Base + AAAh	Base + 555h	0090h

Note: *Base = Base Address.*

```
/* Example: SecSi Sector Exit Command */
  *( (UINT16 *)base_addr + 0x555 ) = 0x00AA;   /* write unlock cycle 1           */
  *( (UINT16 *)base_addr + 0x2AA ) = 0x0055;   /* write unlock cycle 2           */
  *( (UINT16 *)base_addr + 0x555 ) = 0x0090;   /* write SecSi Sector Exit cycle 3 */
  *( (UINT16 *)base_addr + 0x000 ) = 0x0000;   /* write SecSi Sector Exit cycle 4 */
```

12 Electrical Specifications

12.1 Absolute Maximum Ratings

Storage Temperature
Plastic Packages . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . –65°C to +125°C

Voltage with Respect to Ground:
All Inputs and I/Os except
as noted below (Note 1) . . . . –0.5 V to V_{IO} + 0.5 V

V_{CC} (Note 1). . . . . –0.5 V to +2.5 V

V_{IO} . . . . –0.5 V to +2.5 V

ACC (Note 2) . . . . –0.5 V to +9.5 V

Output Short Circuit Current (Note 3) . . . . 100 mA

Notes:

1. *Minimum DC voltage on input or I/Os is –0.5 V. During voltage transitions, inputs or I/Os may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 12.1. Maximum DC voltage on input or I/Os is V_{CC} + 0.5 V. During voltage transitions outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See Figure 12.2.*
2. *Minimum DC input voltage on pin ACC is -0.5V. During voltage transitions, ACC may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 12.1. Maximum DC voltage on pin ACC is +9.5 V, which may overshoot to 10.5 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
4. *Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

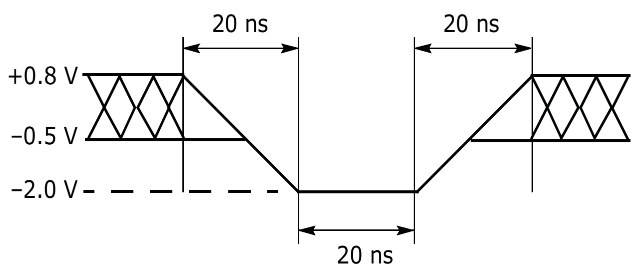


Figure 12.1 Maximum Negative Overshoot Waveform

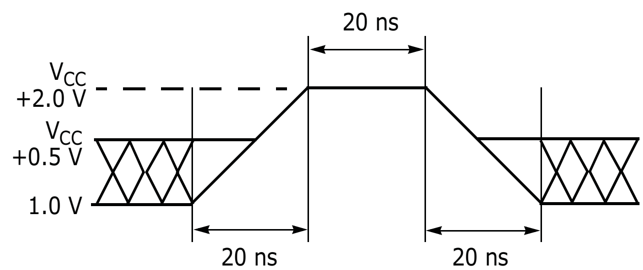


Figure 12.2 Maximum Positive Overshoot Waveform

Note: *The content in this document is Advance information for the S29WS064N and S29WS128N. Content in this document is Preliminary for the S29W256N.*

12.2 Operating Ranges

Wireless (W) Devices

Ambient Temperature (T_A) . . . . –25°C to +85°C

Industrial (I) Devices

Ambient Temperature (T_A) . . . . –40°C to +85°C

Supply Voltages

V_{CC} Supply Voltages . . . . +1.70 V to +1.95 V

V_{IO} Supply Voltages: . . . . +1.70 V to +1.95 V
(Contact local sales office for V_{IO} = 1.35 to +1.70 V.)

Note: *Operating ranges define those limits between which the device functionality is guaranteed.*

12.3 Test Conditions

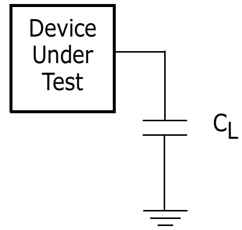


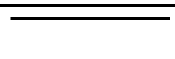
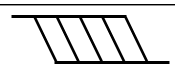
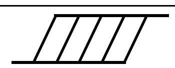
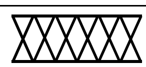
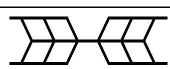
Figure 12.3 Test Setup

Table 12.1 Test Specifications

Test Condition	All Speed Options	Unit
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	3.0 @ 54, 66 MHz 2.5 @ 80 MHz	ns
Input Pulse Levels	0.0–V_{IO}	V
Input timing measurement reference levels	$V_{IO}/2$	V
Output timing measurement reference levels	$V_{IO}/2$	V

Note: *The content in this document is Advance information for the S29WS064N and S29WS128N. Content in this document is Preliminary for the S29W256N.*

12.4 Key to Switching Waveforms

Waveform	Inputs	Outputs
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

Note: *The content in this document is Advance information for the S29WS064N and S29WS128N. Content in this document is Preliminary for the S29W256N.*

12.5 Switching Waveforms

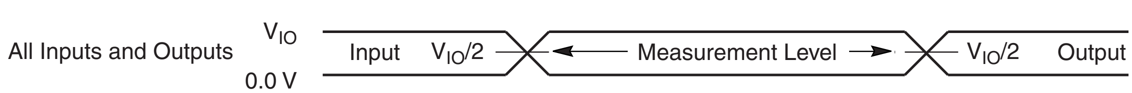


Figure 12.4 Input Waveforms and Measurement Levels

12.6 V_{CC} Power-up

Parameter	Description	Test Setup	Speed	Unit
t_{VCS}	V_{CC} Setup Time	Min	1	ms

Notes:

1. *V_{CC} >= V_{IO} - 100mV and V_{CC} ramp rate is > 1V / 100µs*
2. *V_{CC} ramp rate <1V / 100µs, a Hardware Reset is required.*
3. *The content in this document is Advance information for the S29WS064N and S29WS128N. Content in this document is Preliminary for the S29W256N.*

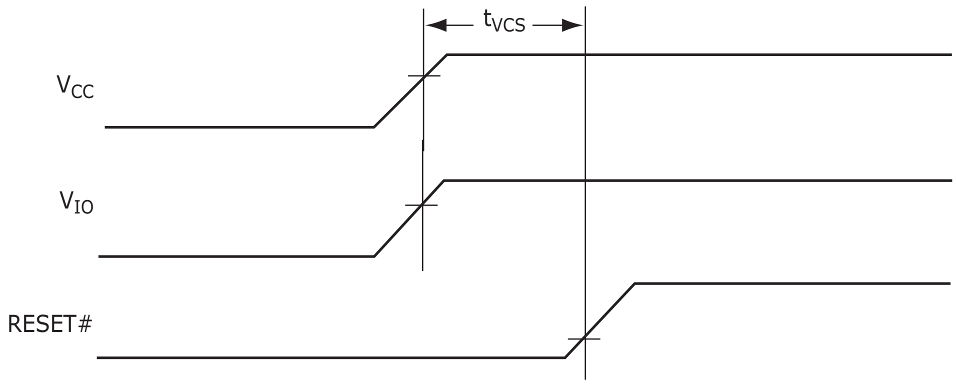


Figure 12.5 V_{CC} Power-up Diagram

12.7 DC Characteristics

(CMOS Compatible)

Parameter	Description (Notes)	Test Conditions (Notes 1, 2, 9)		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}max$				±1	µA
I_{LO}	Output Leakage Current (3)	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}max$				±1	µA
I_{CCB}	V_{CC} Active burst Read Current	CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}, burst length = 8	54 MHz		27	54	mA
			66 MHz		28	60	mA
			80 MHz		30	66	mA
		CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}, burst length = 16	54 MHz		28	48	mA
			66 MHz		30	54	mA
			80 MHz		32	60	mA
		CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}, burst length = 32	54 MHz		29	42	mA
			66 MHz		32	48	mA
			80 MHz		34	54	mA
		CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}, burst length = Continuous	54 MHz		32	36	mA
			66 MHz		35	42	mA
			80 MHz		38	48	mA
I_{IO1}	V_{IO} Non-active Output	OE# = V_{IH}			20	30	µA
I_{CC1}	V_{CC} Active Asynchronous Read Current (4)	CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}	10 MHz		27	36	mA
			5 MHz		13	18	mA
			1 MHz		3	4	mA
I_{CC2}	V_{CC} Active Write Current (5)	CE# = V_{IL}, OE# = V_{IH}, ACC = V_{IH}	V_{ACC}		1	5	µA
			V_{CC}		19	52.5	mA
I_{CC3}	V_{CC} Standby Current (6, 7)	CE# = RESET# = V_{CC} ± 0.2 V	V_{ACC}		1	5	µA
			V_{CC}		20	40	µA
I_{CC4}	V_{CC} Reset Current (7)	RESET# = V_{IL}, CLK = V_{IL}			70	150	µA
I_{CC5}	V_{CC} Active Current (Read While Write) (7)	CE# = V_{IL}, OE# = V_{IH}, ACC = V_{IH} @ 5 MHz			50	60	mA
I_{CC6}	V_{CC} Sleep Current (7)	CE# = V_{IL}, OE# = V_{IH}			2	40	µA
I_{ACC}	Accelerated Program Current (8)	CE# = V_{IL}, OE# = V_{IH}, V_{ACC} = 9.5 V	V_{ACC}		6	20	mA
			V_{CC}		14	20	mA
V_{IL}	Input Low Voltage	V_{IO} = 1.8 V		–0.5		0.4	V
V_{IH}	Input High Voltage	V_{IO} = 1.8 V		V_{IO} – 0.4		V_{IO} + 0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100 µA, $V_{CC} = V_{CC\ min} = V_{IO}$				0.1	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA, $V_{CC} = V_{CC\ min} = V_{IO}$		V_{IO} – 0.1			V
V_{HH}	Voltage for Accelerated Program			8.5		9.5	V
V_{LKO}	Low V_{CC} Lock-out Voltage			1.0		1.4	V

Notes:

1. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}max$.*
2. *$V_{CC} = V_{IO}$.*
3. *CE# must be set high when measuring the RDY pin.*
4. *The I_{CC} current listed is typically less than 3 mA/MHz, with OE# at V_{IH}.*
5. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
6. *Device enters automatic sleep mode when addresses are stable for t_{ACC} + 20 ns. Typical sleep mode current is equal to I_{CC3}.*
7. *$V_{IH} = V_{CC} \pm 0.2$ V and $V_{IL} > -0.1$ V.*
8. *Total current during accelerated programming is the sum of V_{ACC} and V_{CC} currents.*
9. *$V_{ACC} = V_{HH}$ on ACC input.*
10. *The content in this document is Advance information for the S29WS064N and S29WS128N. Content in this document is Preliminary for the S29W256N.*

12.8 AC Characteristics

12.8.1 CLK Characterization

Parameter	Description		54 MHz	66 MHz	80 MHz	Unit
f_{CLK}	CLK Frequency	Max	54	66	80	MHz
t_{CLK}	CLK Period	Min	18.5	15.1	12.5	ns
t_{CH}	CLK High Time	Min	7.4	6.1	5.0	ns
t_{CL}	CLK Low Time					
t_{CR}	CLK Rise Time	Max	3	3	2.5	ns
t_{CF}	CLK Fall Time					

Note: *The content in this document is Advance information for the S29WS064N and S29WS128N. Content in this document is Preliminary for the S29W256N.*

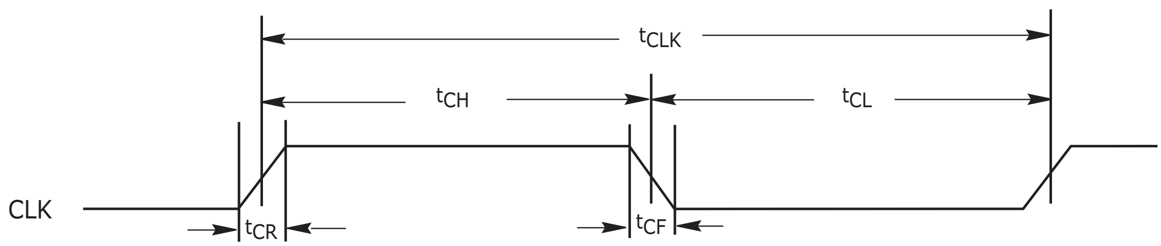


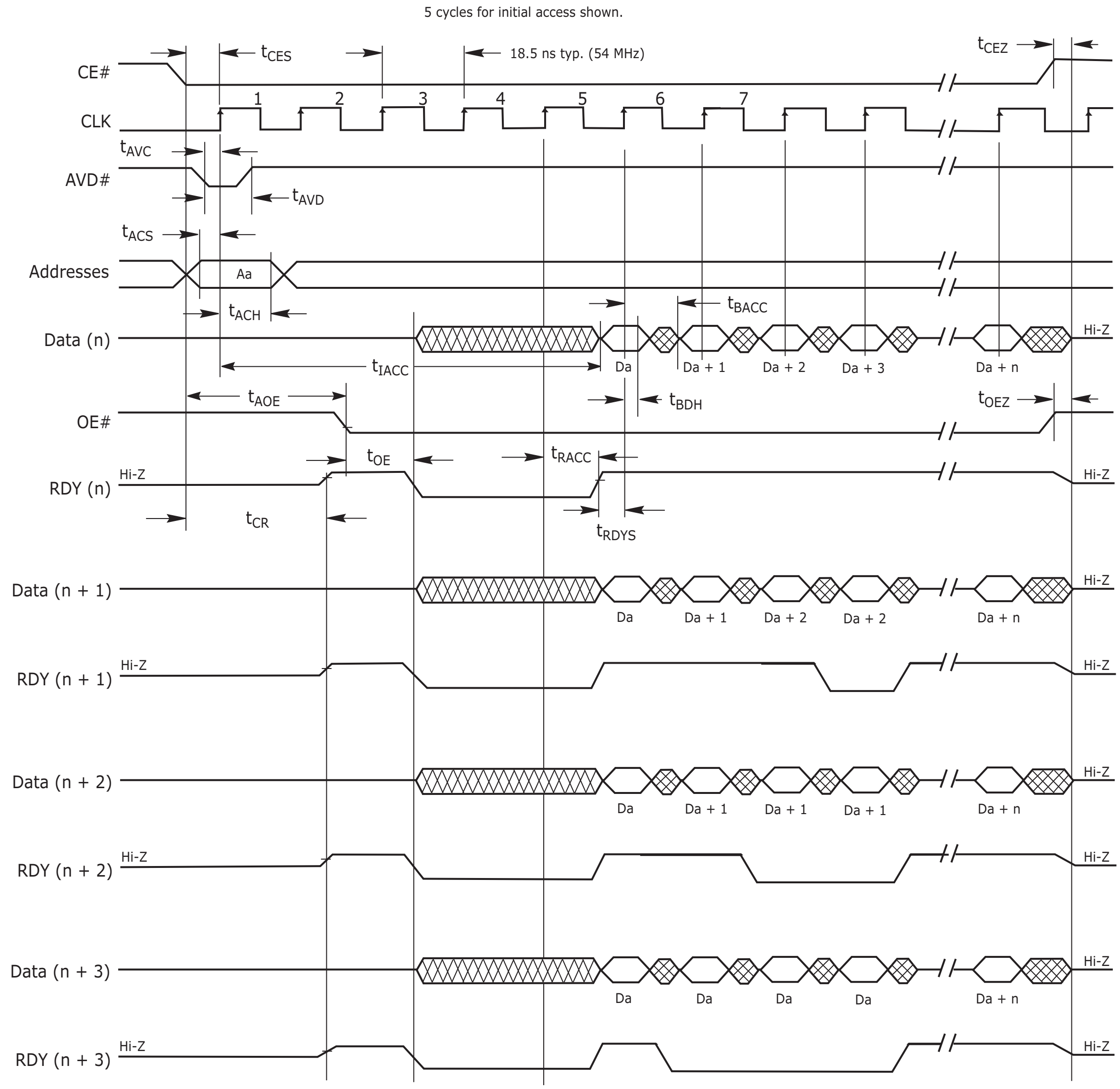
Figure 12.6 CLK Characterization

12.8.2 Synchronous/Burst Read

Parameter JEDEC	Parameter Standard	Description		54 MHz	66 MHz	80 MHz	Unit
	t_{IACC}	Latency	Max	80			ns
	t_{BACC}	Burst Access Time Valid Clock to Output Delay	Max	13.5	11.2	9	ns
	t_{ACS}	Address Setup Time to CLK (Note 1)	Min	5	4		ns
	t_{ACH}	Address Hold Time from CLK (Note 1)	Min	7	6		ns
	t_{BDH}	Data Hold Time from Next Clock Cycle	Min	4	3		ns
	t_{CR}	Chip Enable to RDY Valid	Max	13.5	11.2	9	ns
	t_{OE}	Output Enable to Output Valid	Max	13.5	11.2		ns
	t_{CEZ}	Chip Enable to High Z (Note 2)	Max	10			ns
	t_{OEZ}	Output Enable to High Z (Note 2)	Max	10			ns
	t_{CES}	CE# Setup Time to CLK	Min	4			ns
	t_{RDYS}	RDY Setup Time to CLK	Min	5	4	3.5	ns
	t_{RACC}	Ready Access Time from CLK	Max	13.5	11.2	9	ns
	t_{CAS}	CE# Setup Time to AVD#	Min	0			ns
	t_{AVC}	AVD# Low to CLK	Min	4			ns
	t_{AVD}	AVD# Pulse	Min	8			ns
	t_{AOE}	AVD Low to OE# Low	Max	38.4			ns

Notes:
1. *Addresses are latched on the first rising edge of CLK.*
2. *Not 100% tested.*
3. *The content in this document is Advance information for the S29WS064N and S29WS128N. Content in this document is Preliminary for the S29W256N.*

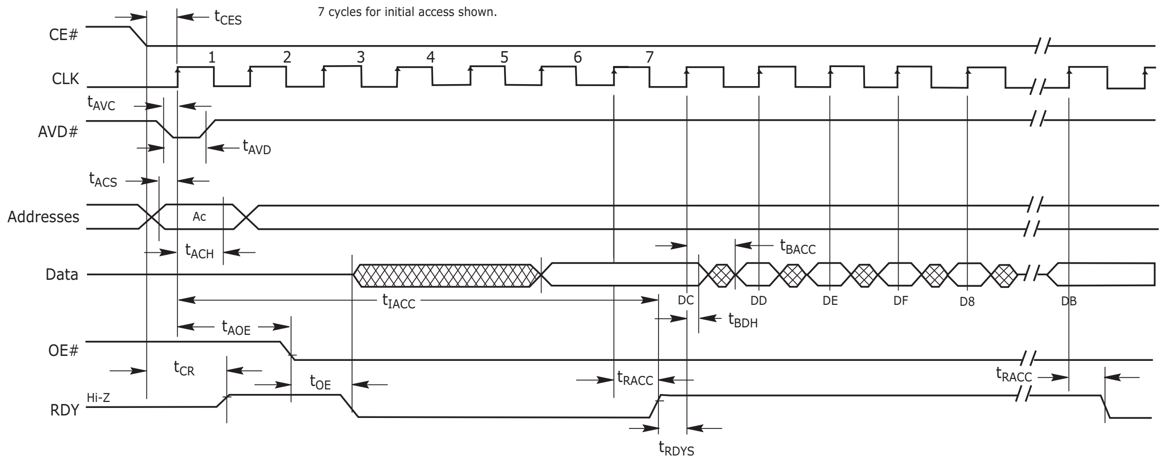
12.8.3 Timing Diagrams



Notes:

1. *Figure shows total number of wait states set to five cycles. The total number of wait states can be programmed from two cycles to seven cycles.*
2. *If any burst address occurs at* address + 1 , address + 2, *or* address + 3, *additional clock delay cycles are inserted, and are indicated by RDY.*
3. *The device is in synchronous mode.*

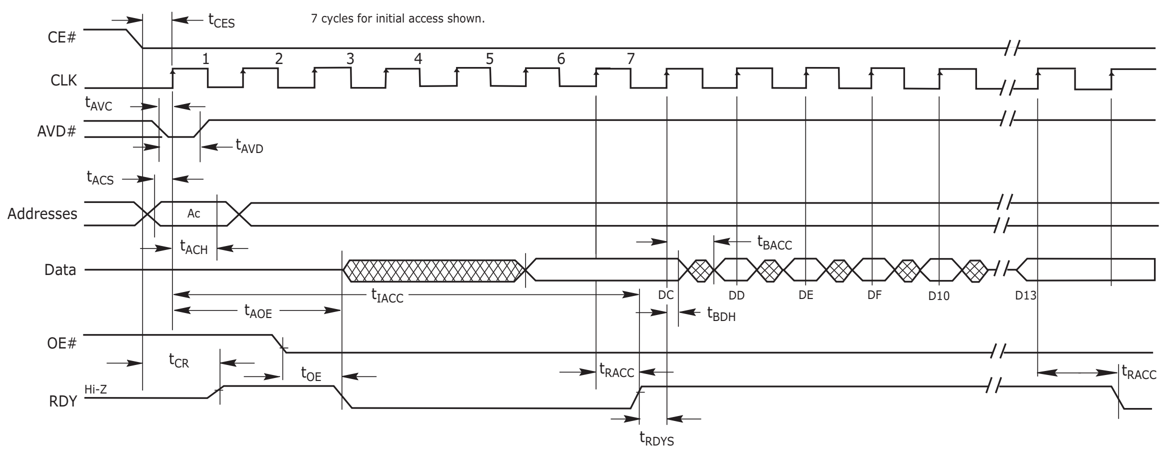
Figure 12.7 CLK Synchronous Burst Mode Read



Notes:

1. *Figure shows total number of wait states set to seven cycles. The total number of wait states can be programmed from two cycles to seven cycles.*
2. *If any burst address occurs at* address + 1 , address + 2, *or* address + 3, *additional clock delay cycles are inserted, and are indicated by RDY.*
3. *The device is in synchronous mode with wrap around.*
4. *D8–DF in data waveform indicate the order of data within a given 8-word address range, from lowest to highest. Starting address in figure is the 4th address in range (0-F).*

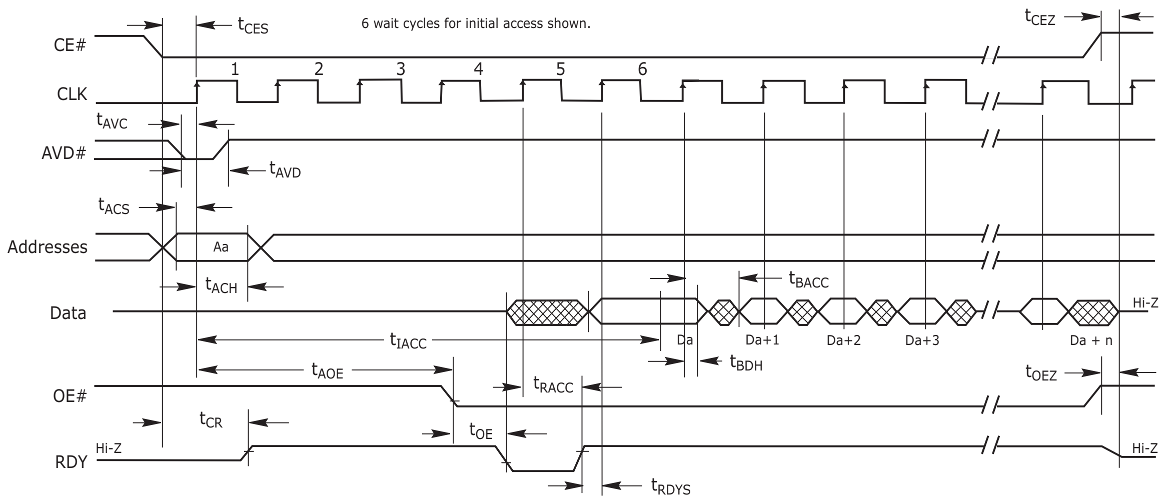
Figure 12.8 8-word Linear Burst with Wrap Around



Notes:

1. *Figure shows total number of wait states set to seven cycles. The total number of wait states can be programmed from two cycles to seven cycles. Clock is set for active rising edge.*
2. *If any burst address occurs at* address + 1 , address + 2, *or* address + 3, *additional clock delay cycles are inserted, and are indicated by RDY.*
3. *The device is in asynchronous mode with out wrap around.*
4. *DC–D13 in data waveform indicate the order of data within a given 8-word address range, from lowest to highest. Starting address in figure is the 1st address in range (c-13).*

Figure 12.9 8-word Linear Burst without Wrap Around



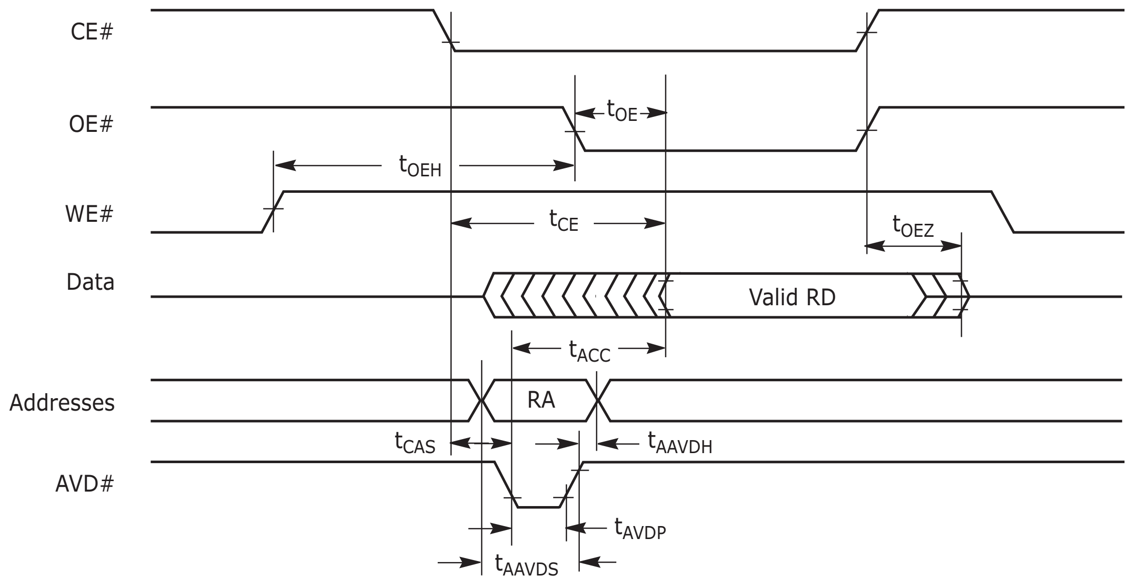
Notes:
1. *Figure assumes 6 wait states for initial access and synchronous read.*
2. *The Set Configuration Register command sequence has been written with CR8=0; device outputs RDY one cycle before valid data.*

Figure 12.10 Linear Burst with RDY Set One Cycle Before Data

12.8.4 AC Characteristics—Asynchronous Read

Parameter: JEDEC	Parameter: Standard	Description			54 MHz	66 MHz	80 MHz	Unit
	t_{CE}	Access Time from CE# Low		Max	80			ns
	t_{ACC}	Asynchronous Access Time		Max	80			ns
	t_{AVDP}	AVD# Low Time		Min	8			ns
	t_{AAVDS}	Address Setup Time to Rising Edge of AVD#		Min	4			ns
	t_{AAVDH}	Address Hold Time from Rising Edge of AVD#		Min	7	6		ns
	t_{OE}	Output Enable to Output Valid		Max	13.5			ns
	t_{OEH}	Output Enable Hold Time	Read	Min	0			ns
			Data# Polling	Min	10			ns
	t_{OEZ}	Output Enable to High Z (see Note)		Max	10			ns
	t_{CAS}	CE# Setup Time to AVD#		Min	0			ns

Notes:
1. *Not 100% tested.*
2. *The content in this document is Advance information for the S29WS064N and S29WS128N. Content in this document is Preliminary for the S29W256N.*



Note: *RA = Read Address, RD = Read Data.*

Figure 12.11 Asynchronous Mode Read

12.8.5 Hardware Reset (RESET#)

Parameter		Description		All Speed Options	Unit
JEDEC	Std.				
	t_{RP}	RESET# Pulse Width	Min	30	µs
	t_{RH}	Reset High Time Before Read (See Note)	Min	200	ns

Notes:

1. *Not 100% tested.*
2. *The content in this document is Advance information for the S29WS064N and S29WS128N. Content in this document is Preliminary for the S29W256N.*

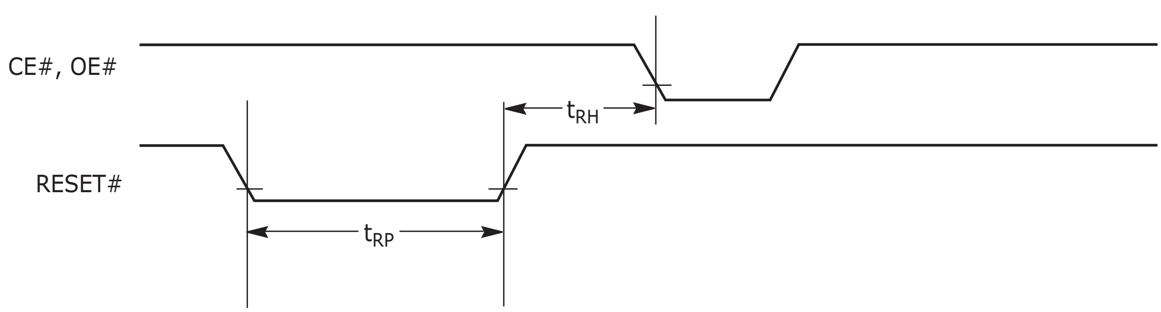


Figure 12.12 Reset Timings

12.8.6 Erase / Program Timing

Parameter JEDEC	Parameter Standard	Description			54 MHz	66 MHz	80 MHz	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	80			ns
t_{AVWL}	t_{AS}	Address Setup Time (Notes 2, 3)	Synchronous	Min	5			ns
			Asynchronous		0			ns
t_{WLAX}	t_{AH}	Address Hold Time (Notes 2, 3)	Synchronous	Min	9			ns
			Asynchronous		20			
	t_{AVDP}	AVD# Low Time		Min	8			ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	45	20		ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0			ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write		Min	0			ns
	t_{CAS}	CE# Setup Time to AVD#		Min	0			ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0			ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	30			ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min	20			ns
	$t_{SR/W}$	Latency Between Read and Write Operations		Min	0			ns
	t_{VID}	V_{ACC} Rise and Fall Time		Min	500			ns
	t_{VIDS}	V_{ACC} Setup Time (During Accelerated Programming)		Min	1			µs
	t_{VCS}	V_{CC} Setup Time		Min	50			µs
t_{ELWL}	t_{CS}	CE# Setup Time to WE#		Min	5			ns
	t_{AVSW}	AVD# Setup Time to WE#		Min	5			ns
	t_{AVHW}	AVD# Hold Time to WE#		Min	5			ns
	t_{AVSC}	AVD# Setup Time to CLK		Min	5			ns
	t_{AVHC}	AVD# Hold Time to CLK		Min	5			ns
	t_{CSW}	Clock Setup Time to WE#		Min	5			ns
	t_{WEP}	Noise Pulse Margin on WE#		Max	3			ns
	t_{SEA}	Sector Erase Accept Time-out		Max	50			µs
	t_{ESL}	Erase Suspend Latency		Max	20			µs
	t_{PSL}	Program Suspend Latency		Max	20			µs
	t_{ASP}	Toggle Time During Sector Protection		Typ	100			µs
	t_{PSP}	Toggle Time During Programming Within a Protected Sector		Typ	1			µs

Notes:

1. *Not 100% tested.*
2. *Asynchronous read mode allows Asynchronous program operation only. Synchronous read mode allows both Asynchronous and Synchronous program operation.*
3. *In asynchronous program operation timing, addresses are latched on the falling edge of WE#. In synchronous program operation timing, addresses are latched on the rising edge of CLK.*
4. *See the Erase and Programming Performance section for more information.*
5. *Does not include the preprogramming time.*
6. *The content in this document is Advance information for the S29WS064N and S29WS128N. Content in this document is Preliminary for the S29W256N.*

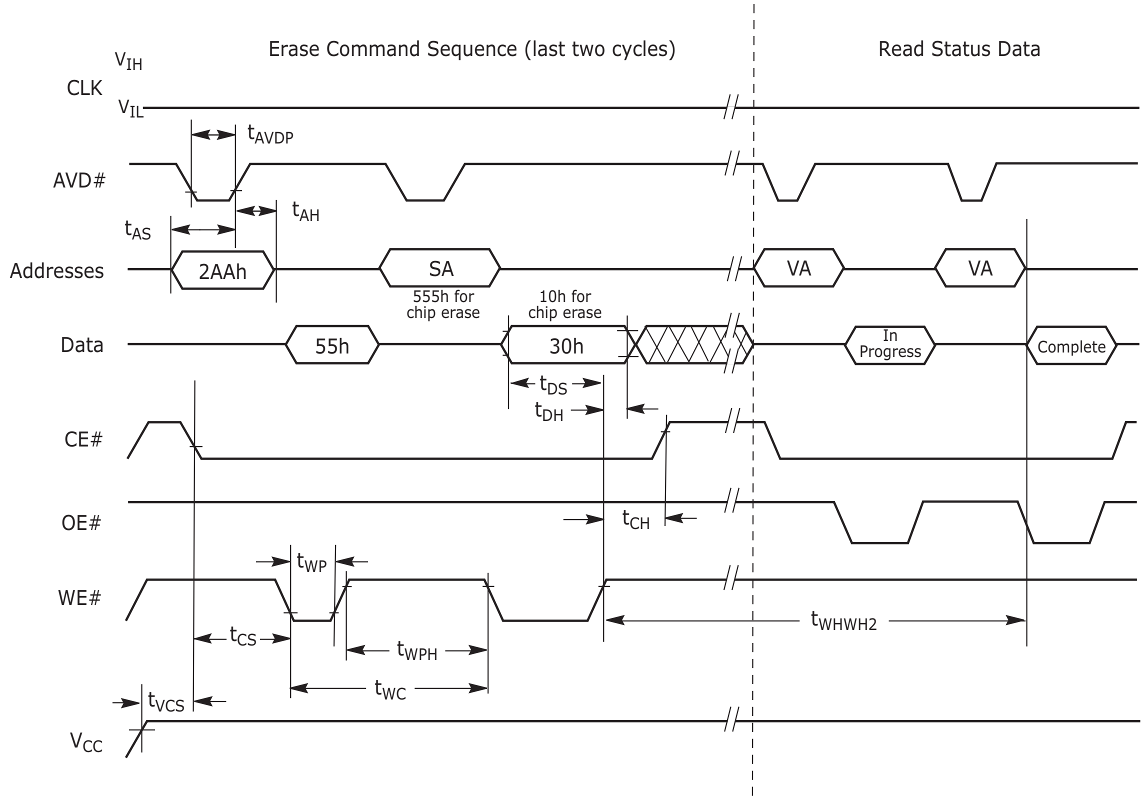
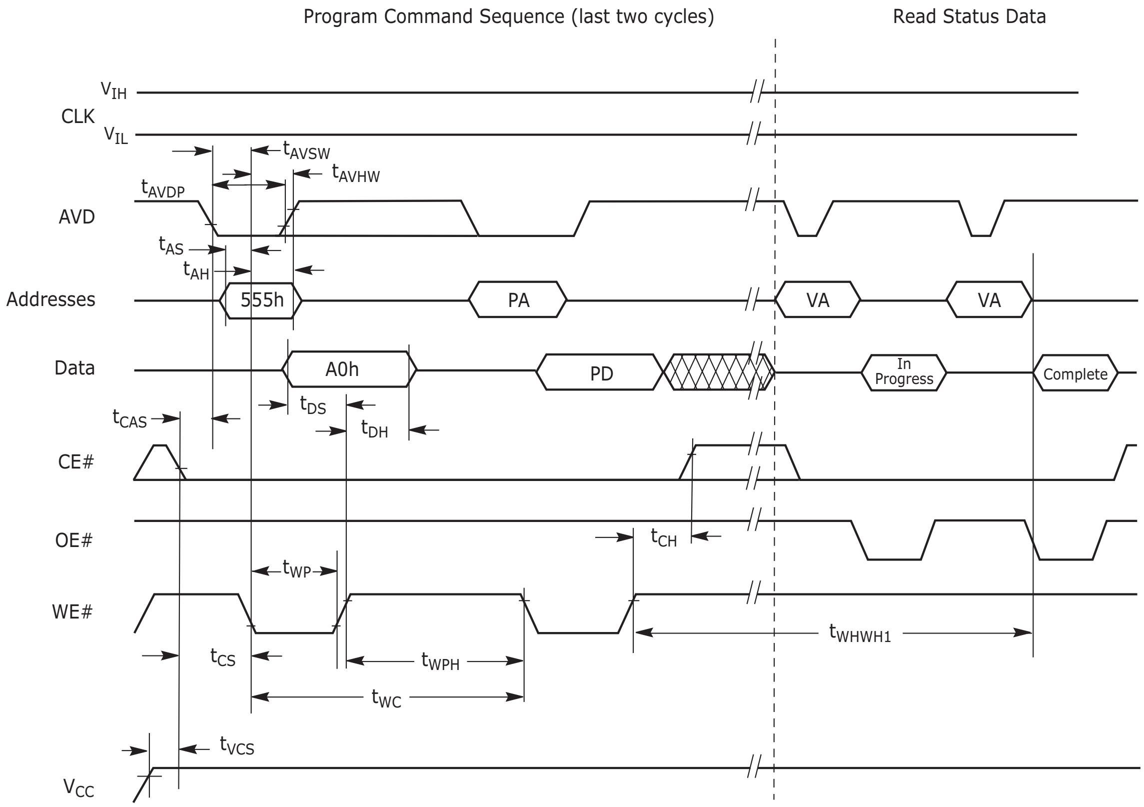


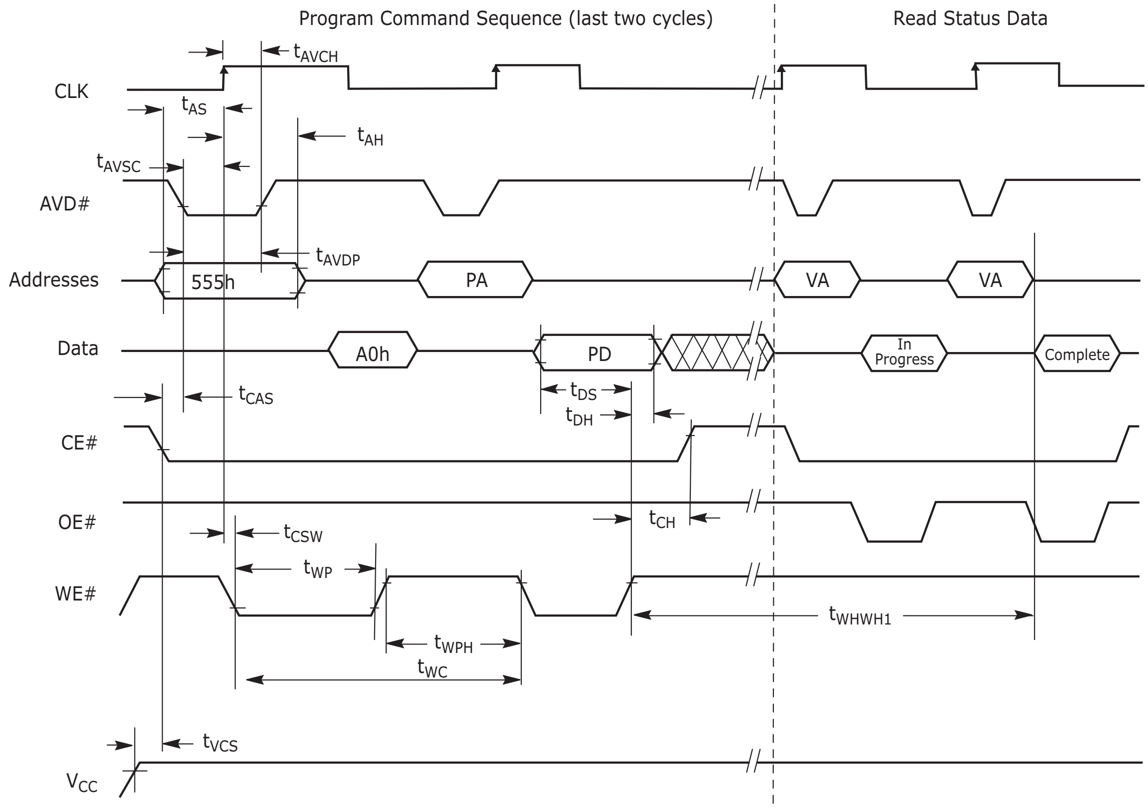
Figure 12.13 Chip/Sector Erase Operation Timings



Notes:

1. *PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.*
2. In progress *and* complete *refer to status of program operation.*
3. *A23–A14 for the WS256N (A22–A14 for the WS128N, A21–A14 for the WS064N) are don't care during command sequence unlock cycles.*
4. *CLK can be either V_{IL} or V_{IH}.*
5. *The Asynchronous programming operation is independent of the Set Device Read Mode bit in the Configuration Register.*

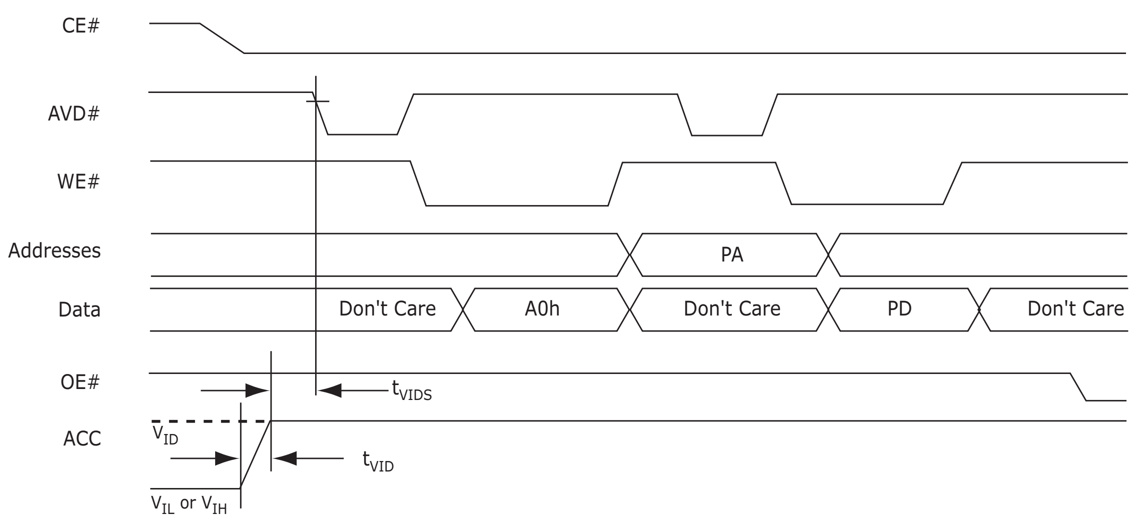
Figure 12.14 Asynchronous Program Operation Timings



Notes:

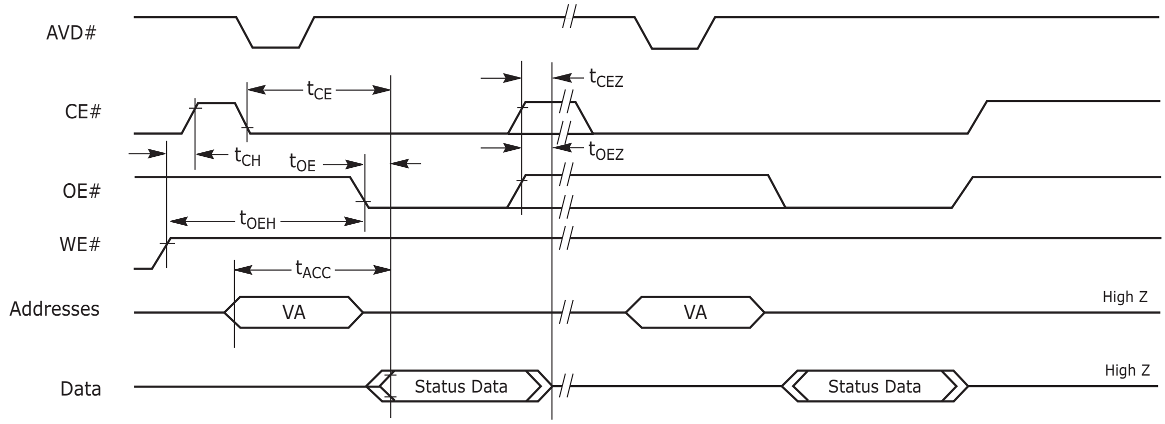
1. *PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.*
2. In progress *and* complete *refer to status of program operation.*
3. *A23–A14 for the WS256N (A22–A14 for the WS128N, A21–A14 for the WS064N) are don't care during command sequence unlock cycles.*
4. *Addresses are latched on the first rising edge of CLK.*
5. *Either CE# or AVD# is required to go from low to high in between programming command sequences.*
6. *The Synchronous programming operation is dependent of the Set Device Read Mode bit in the Configuration Register. The Configuration Register must be set to the Synchronous Read Mode.*

Figure 12.15 Synchronous Program Operation Timings



Note: *Use setup and hold times from conventional program operation.*

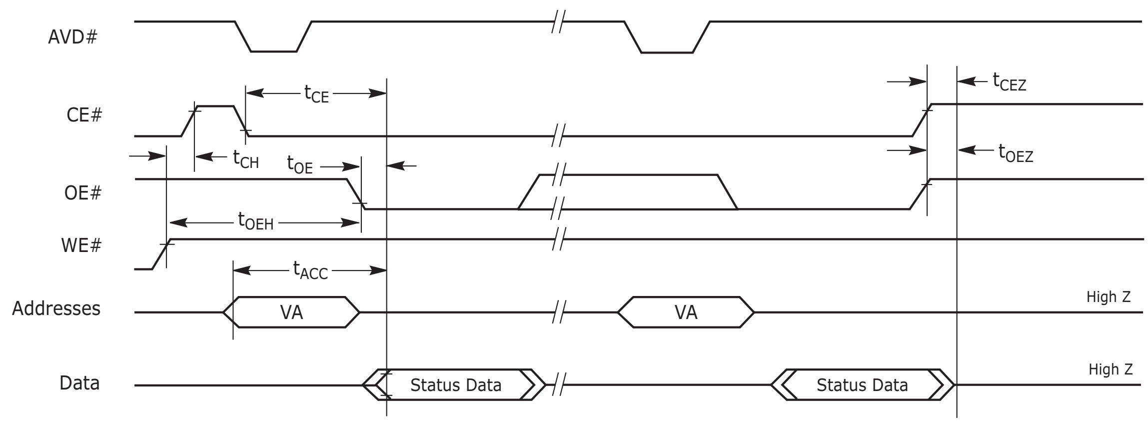
Figure 12.16 Accelerated Unlock Bypass Programming Timing



Notes:

1. *Status reads in figure are shown as asynchronous.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is completeData# Polling outputs true data.*

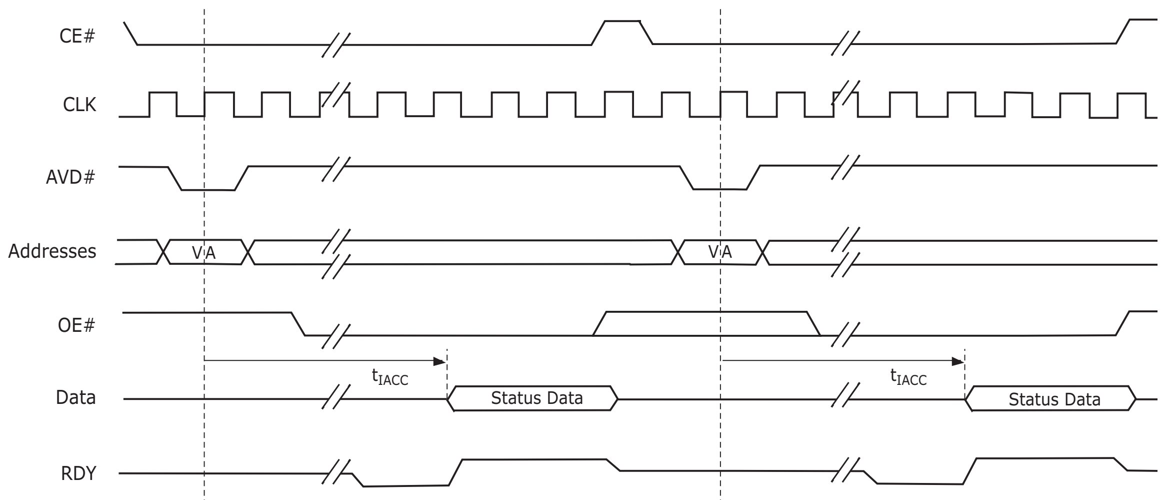
Figure 12.17 Data# Polling Timings (During Embedded Algorithm)



Notes:

1. *Status reads in figure are shown as asynchronous.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, .*

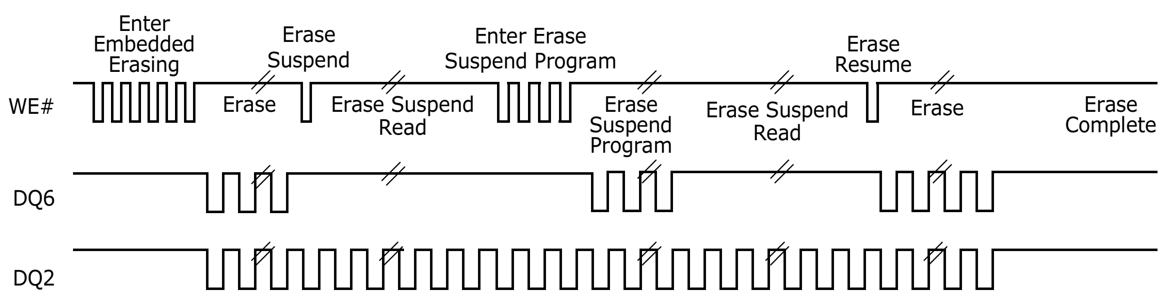
Figure 12.18 Toggle Bit Timings (During Embedded Algorithm)



Notes:

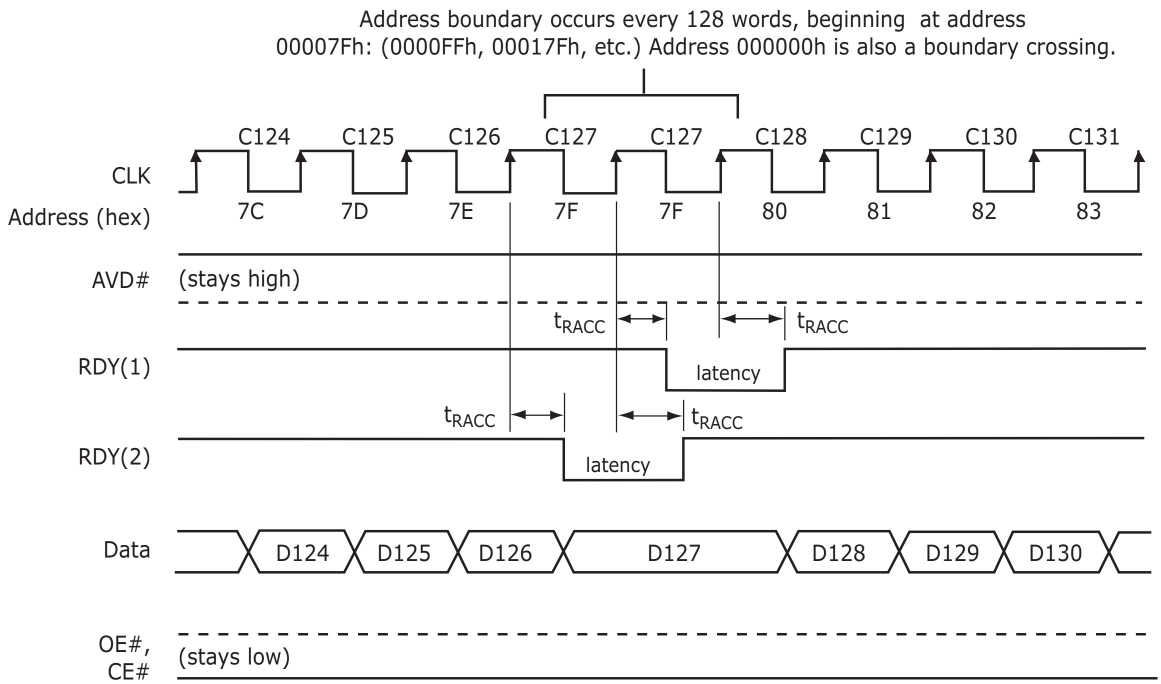
1. *The timings are similar to synchronous read timings.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, .*
3. *RDY is active with data (D8 = 1 in the Configuration Register). When D8 = 0 in the Configuration Register, RDY is active one clock cycle before data.*

Figure 12.19 Synchronous Data Polling Timings/Toggle Bit Timings



Note: *DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6*

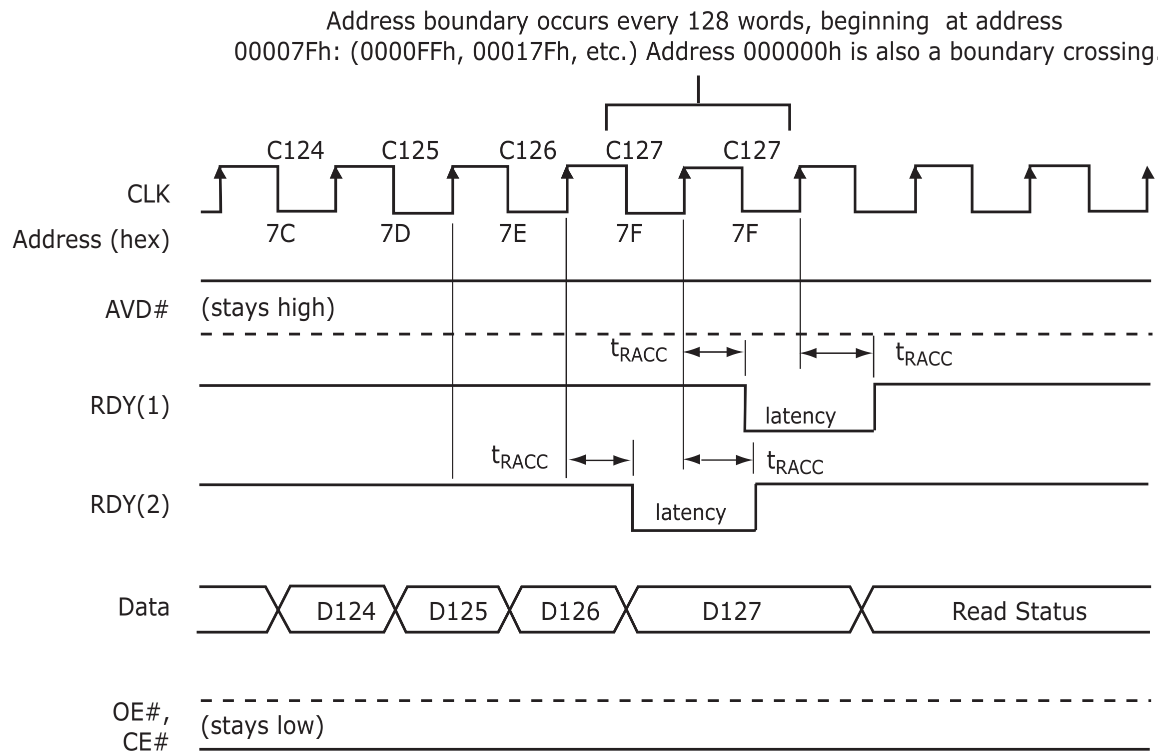
Figure 12.20 DQ2 vs. DQ6



Notes:

1. *RDY(1) active with data (D8 = 1 in the Configuration Register).*
2. *RDY(2) active one clock cycle before data (D8 = 0 in the Configuration Register).*
3. *Cxx indicates the clock that triggers Dxx on the outputs; for example, C60 triggers D60.*
4. *Figure shows the device not crossing a bank in the process of performing an erase or program.*
5. *RDY does not go low and no additional wait states are required if the Burst frequency is <=66 MHz and the Boundary Crossing bit (D14) in the Configuration Register is set to 0*

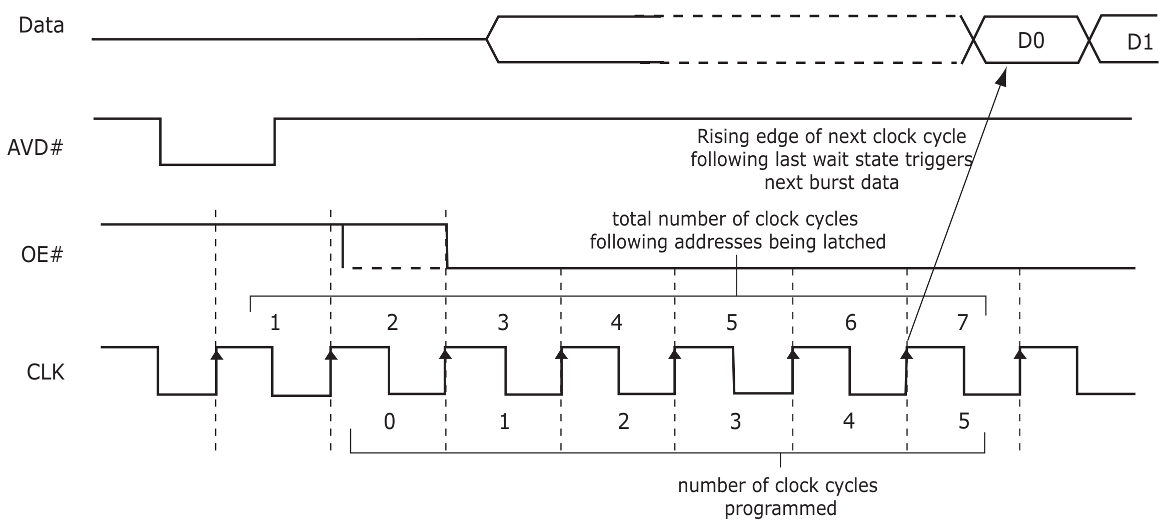
Figure 12.21 Latency with Boundary Crossing when Frequency > 66 MHz



Notes:

1. *RDY(1) active with data (D8 = 1 in the Configuration Register).*
2. *RDY(2) active one clock cycle before data (D8 = 0 in the Configuration Register).*
3. *Cxx indicates the clock that triggers Dxx on the outputs; for example, C60 triggers D60.*
4. *Figure shows the device crossing a bank in the process of performing an erase or program.*
5. *RDY does not go low and no additional wait states are required if the Burst frequency is ≤ 66 MHz and the Boundary Crossing bit (D14) in the Configuration Register is set to 0.*

Figure 12.22 Latency with Boundary Crossing into Program/Erase Bank

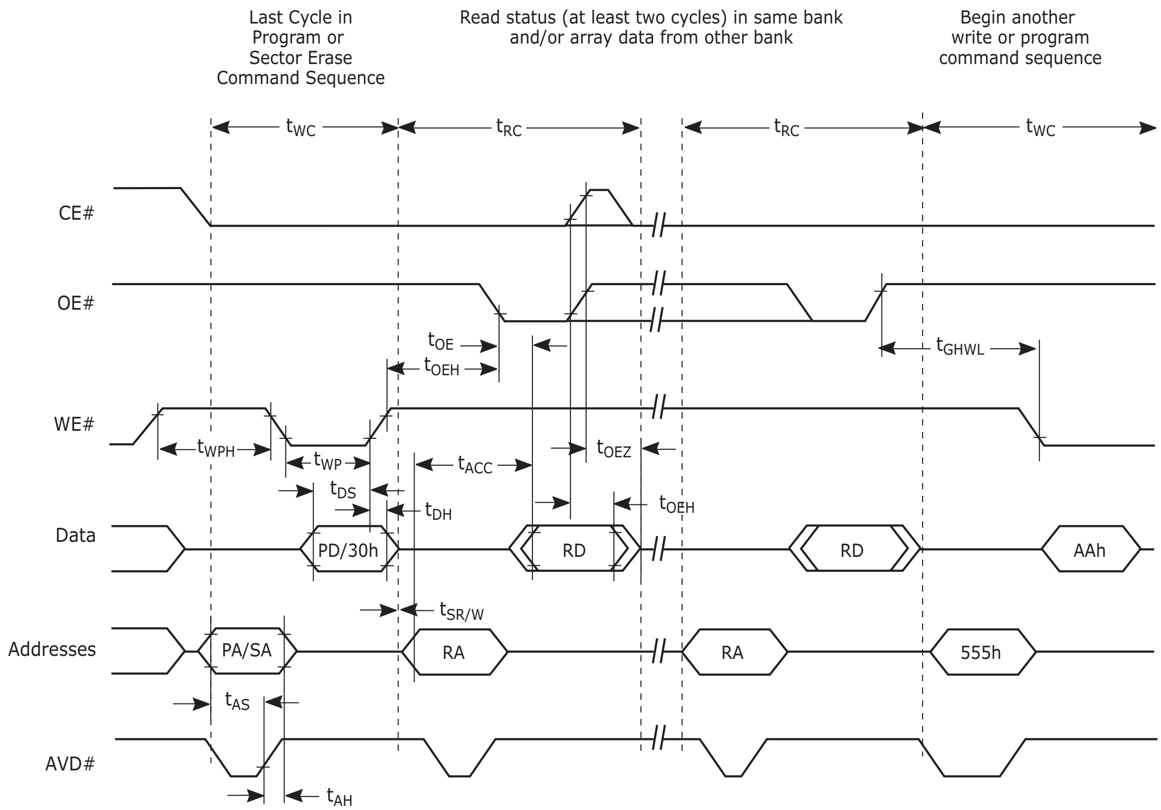


Wait State Configuration Register Setup:

D13, D12, D11 = 111 ⇒ *Reserved*
D13, D12, D11 = 110 ⇒ *Reserved*
D13, D12, D11 = 101 ⇒ *5 programmed, 7 total*
D13, D12, D11 = 100 ⇒ *4 programmed, 6 total*
D13, D12, D11 = 011 ⇒ *3 programmed, 5 total*
D13, D12, D11 = 010 ⇒ *2 programmed, 4 total*
D13, D12, D11 = 001 ⇒ *1 programmed, 3 total*
D13, D12, D11 = 000 ⇒ *0 programmed, 2 total*

Note: *6.Figure assumes address D0 is not at an address boundary, and wait state is set to* 101

Figure 12.23 Example of Wait State Insertion



Note: *Breakpoints in waveforms indicate that system may alternately read array data from the* non-busy *bank while checking the status of the program or erase operation in the* busy *bank. The system should read status twice to ensure valid information.*

Figure 12.24 Back-to-Back Read/Write Cycle Timings

12.8.7 Erase and Programming Performance

<table>
<tr><th colspan="3">Parameter</th><th>Typ (Note 1)</th><th>Max (Note 2)</th><th>Unit</th><th>Comments</th></tr>
<tr><td rowspan="2">Sector Erase Time</td><td>64 Kword</td><td>V_{CC}</td><td>0.6</td><td>3.5</td><td rowspan="2">s</td><td rowspan="4">Excludes 00h programming prior to erasure (Note 4)</td></tr>
<tr><td>16 Kword</td><td>V_{CC}</td><td><0.15</td><td>2</td></tr>
<tr><td colspan="2" rowspan="2">Chip Erase Time</td><td>V_{CC}</td><td>153.6 (WS256N)
77.4 (WS128N)
39.3 (WS064N)</td><td>308 (WS256N)
154 (WS128N)
78 (WS064N)</td><td rowspan="2">s</td></tr>
<tr><td>ACC</td><td>130.6 (WS256N)
65.8 (WS128N)
33.4 (WS064N)</td><td>262 (WS256N)
132 (WS128N)
66 (WS064N)</td></tr>
<tr><td colspan="2" rowspan="2">Single Word Programming Time (Note 8)</td><td>V_{CC}</td><td>40</td><td>400</td><td rowspan="2">µs</td><td rowspan="2"></td></tr>
<tr><td>ACC</td><td>24</td><td>240</td></tr>
<tr><td colspan="2" rowspan="2">Effective Word Programming Time utilizing Program Write Buffer</td><td>V_{CC}</td><td>9.4</td><td>94</td><td rowspan="2">µs</td><td rowspan="2"></td></tr>
<tr><td>ACC</td><td>6</td><td>60</td></tr>
<tr><td colspan="2" rowspan="2">Total 32-Word Buffer Programming Time</td><td>V_{CC}</td><td>300</td><td>3000</td><td rowspan="2">µs</td><td rowspan="2"></td></tr>
<tr><td>ACC</td><td>192</td><td>1920</td></tr>
<tr><td colspan="2" rowspan="2">Chip Programming Time (Note 3)</td><td>V_{CC}</td><td>157.3 (WS256N)
78.6 (WS128N)
39.3 (WS064N)</td><td>314.6 (WS256N)
157.3 (WS128N)
78.6 (WS064N)</td><td rowspan="2">s</td><td rowspan="2">Excludes system level overhead (Note 5)</td></tr>
<tr><td>ACC</td><td>100.7 (WS256N)
50.3 (WS128N)
25.2 (WS064N)</td><td>201.3 (WS256N)
100.7 (WS128N)
50.3 (WS064N)</td></tr>
</table>

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 1.8 V V_{CC}, 10,000 cycles; checkerboard data pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 1.70 V, 100,000 cycles.*
3. *Typical chip programming time is considerably less than the maximum chip programming time listed, and is based on utilizing the Write Buffer.*
4. *In the pre-programming step of the Embedded Erase algorithm, all words are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See the Appendix for further information about command definitions.*
6. *Contact the local sales office for minimum cycling endurance values in specific applications and operating conditions.*
7. *Refer to Application Note Erase Suspend/Resume Timing for more details.*
8. *Word programming specification is based upon a single word programming operation not utilizing the write buffer.*
9. *The content in this document is Advance information for the S29WS064N and S29WS128N. Content in this document is Preliminary for the S29W256N.*

12.8.8 BGA Ball Capacitance

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	5.3	6.3	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	5.8	6.8	pF
C_{IN2}	Control Pin Capacitance	$V_{IN} = 0$	6.3	7.3	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions $T_A = 25^{\circ}C$; f = 1.0 MHz.*
3. *The content in this document is Advance information for the S29WS064N and S29WS128N. Content in this document is Preliminary for the S29W256N.*

13 Appendix

This section contains information relating to software control or interfacing with the Flash device. For additional information and assistance regarding software, see the Additional Resources on page 19, or explore the Web at www.amd.com and www.fujitsu.com.

Table 13.1 Memory Array Commands

Command Sequence (Notes)		Cycles	Bus Cycles (Notes 1–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Asynchronous Read (6)		1	RA	RD										
Reset (7)		1	XXX	F0										
Autoselect (8)	Manufacturer ID	4	555	AA	2AA	55	[BA]555	90	[BA]X00	0001				
	Device ID (9)	6	555	AA	2AA	55	[BA]555	90	[BA]X01	227E	BA+X0E	Data	BA+X0F	2200
	Indicator Bits (10)	4	555	AA	2AA	55	[BA]555	90	[BA]X03	Data				
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Write to Buffer (11)		6	555	AA	2AA	55	PA	25	PA	WC	PA	PD	WBL	PD
Program Buffer to Flash		1	SA	29										
Write to Buffer Abort Reset (12)		3	555	AA	2AA	55	555	F0						
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase/Program Suspend (13)		1	BA	B0										
Erase/Program Resume (14)		1	BA	30										
Set Configuration Register (18)		4	555	AA	2AA	55	555	D0	X00	CR				
Read Configuration Register		4	555	AA	2AA	55	555	C6	X00	CR				
CFI Query (15)		1	[BA]555	98										
Unlock Bypass Mode	Entry	3	555	AA	2AA	55	555	20						
	Program (16)	2	XXX	A0	PA	PD								
	CFI (16)	1	XXX	98										
	Reset	2	XXX	90	XXX	00								
Secured Silicon Sector	Entry	3	555	AA	2AA	55	555	88						
	Program (17)	4	555	AA	2AA	55	555	A0	PA	PD				
	Read (17)	1	00	Data										
	Exit (17)	4	555	AA	2AA	55	555	90	XXX	00				

Legend:

X = Don't care.

RA = Read Address.

RD = Read Data.

PA = Program Address. Addresses latch on the rising edge of the AVD# pulse or active edge of CLK, whichever occurs first.

PD = Program Data. Data latches on the rising edge of WE# or CE# pulse, whichever occurs first.

SA = Sector Address. WS256N = A23–A14; WS128N = A22–A14; WS064N = A21–A14.

BA = Bank Address. WS256N = A23–A20; WS128N = A22–A20; WS064N = A21–A18.

CR = Configuration Register data bits D15–D0.

WBL = Write Buffer Location. Address must be within the same write buffer page as PA.

WC = Word Count. Number of write buffer locations to load minus 1.

Notes:

1. *See Table 8.1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Shaded cells indicate read cycles.*
4. *Address and data bits not specified in table, legend, or notes are don't cares (each hex digit implies 4 bits of data).*
5. *Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. The system must write the reset command to return the device to reading array data.*
6. *No unlock or command cycles required when bank is reading array data.*
7. *Reset command is required to return to reading array data (or to the erase-suspend-read mode if previously in Erase Suspend) when a bank is in the autoselect mode, or if DQ5 goes high (while the bank is providing status information) or performing sector lock/unlock.*
8. *The system must provide the bank address. See Autoselect section for more information.*
9. *Data in cycle 5 is 2230 (WS256N), 2232 (WS064N), or 2231 (WS128N).*
10. *See Table 8.9 for indicator bit values.*
11. *Total number of cycles in the command sequence is determined by the number of words written to the write buffer.*
12. *Command sequence resets device for next command after write-to-buffer operation.*
13. *System may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation, and requires the bank address.*
14. *Erase Resume command is valid only during the Erase Suspend mode, and requires the bank address.*
15. *Command is valid when device is ready to read array data or when device is in autoselect mode. Address equals 55h on all future devices, but 555h for WS256N/128N/064N.*
16. *Requires Entry command sequence prior to execution. Unlock Bypass Reset command is required to return to reading array data.*
17. *Requires Entry command sequence prior to execution. Secured Silicon Sector Exit Reset command is required to exit this mode; device may otherwise be placed in an unknown state.*
18. *Requires reset command to configure the Configuration Register.*

Table 13.2 Sector Protection Commands

Command Sequence (Notes)		Cycles	Bus Cycles (Notes 1–4)													
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Lock Register Bits	Command Set Entry (5)	3	555	AA	2AA	55	555	40								
	Program (6, 12)	2	XX	A0	77/00	data										
	Read (6)	1	77	data												
	Command Set Exit (7)	2	XX	90	XX	00										
Password Protection	Command Set Entry (5)	3	555	AA	2AA	55	555	60								
	Program [0-3] (8)	2	XX	A0	00	PWD[0-3]										
	Read (9)	4	0...00	PWD0	0...01	PWD1	0...02	PWD2	0...03	PWD3						
	Unlock	7	00	25	00	03	00	PWD0	01	PWD1	02	PWD2	03	PWD3	00	29
	Command Set Exit (7)	2	XX	90	XX	00										
Non-Volatile Sector Protection (PPB)	Command Set Entry (5)	3	555	AA	2AA	55	[BA]555	C0								
	PPB Program (10)	2	XX	A0	SA	00										
	All PPB Erase (10, 11)	2	XX	80	00	30										
	PPB Status Read	1	SA	RD(0)												
	Command Set Exit (7)	2	XX	90	XX	00										
Global Volatile Sector Protection Freeze (PPB Lock)	Command Set Entry (5)	3	555	AA	2AA	55	[BA]555	50								
	PPB Lock Bit Set	2	XX	A0	XX	00										
	PPB Lock Bit Status Read	1	BA	RD(0)												
	Command Set Exit (7)	2	XX	90	XX	00										
Volatile Sector Protection (DYB)	Command Set Entry (5)	3	555	AA	2AA	55	[BA]555	E0								
	DYB Set	2	XX	A0	SA	00										
	DYB Clear	2	XX	A0	SA	01										
	DYB Status Read	1	SA	RD(0)												
	Command Set Exit (7)	2	XX	90	XX	00										

Legend:

X = Don't care.

RA = Address of the memory location to be read.

PD(0) = Secured Silicon Sector Lock Bit. PD(0), or bit[0].

PD(1) = Persistent Protection Mode Lock Bit. PD(1), or bit[1], must be set to '0' for protection while PD(2), bit[2] must be left as '1'.

PD(2) = Password Protection Mode Lock Bit. PD(2), or bit[2], must be set to '0' for protection while PD(1), bit[1] must be left as '1'.

PD(3) = Protection Mode OTP Bit. PD(3) or bit[3].

SA = Sector Address. WS256N = A23–A14; WS128N = A22–A14; WS064N = A21–A14.

BA = Bank Address. WS256N = A23–A20; WS128N = A22–A20; WS064N = A21–A18.

PWD3–PWD0 = Password Data. PD3–PD0 present four 16 bit combinations that represent the 64-bit Password

PWA = Password Address. Address bits A1 and A0 are used to select each 16-bit portion of the 64-bit entity.

PWD = Password Data.

RD(0), RD(1), RD(2) = DQ0, DQ1, or DQ2 protection indicator bit. If protected, DQ0, DQ1, or DQ2 = 0. If unprotected, DQ0, DQ1, DQ2 = 1.

Notes:

1. *All values are in hexadecimal.*
2. *Shaded cells indicate read cycles.*
3. *Address and data bits not specified in table, legend, or notes are don't cares (each hex digit implies 4 bits of data).*
4. *Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. The system must write the reset command to return the device to reading array data.*
5. *Entry commands are required to enter a specific mode to enable instructions only available within that mode.*
6. *If both the Persistent Protection Mode Locking Bit and the Password Protection Mode Locking Bit are set at the same time, the command operation aborts and returns the device to the default Persistent Sector Protection Mode during 2nd bus cycle. Note that on all future devices, addresses equal 00h, but is currently 77h for the WS256N only. See Table 9.1 and Table 9.2 for explanation of lock bits.*
7. *Exit command must be issued to reset the device into read mode; device may otherwise be placed in an unknown state.*
8. *Entire two bus-cycle sequence must be entered for each portion of the password.*
9. *Full address range is required for reading password.*
10. *See Figure 9.2 for details.*
11. *The* All PPB Erase *command pre-programs all PPBs before erasure to prevent over-erasure.*
12. *The second cycle address for the lock register program operation is 77 for S29Ws256N; however, for WS128N and Ws064N this address is 00.*

13.1 Common Flash Memory Interface

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified soft-ware algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and back-ward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address (BA)555h any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 13.3–13.6) within that bank. All reads outside of the CFI address range, within the bank, returns non-valid data. Reads from other banks are allowed, writes are not. To terminate reading CFI data, the system must write the reset command.

The following is a C source code example of using the CFI Entry and Exit functions. Refer to the *Spansion Low Level Driver User's Guide* (available on www.amd.com and www.fujitsu.com) for general information on Spansion Flash memory software development guidelines.

```
/* Example: CFI Entry command */
  *( (UINT16 *)bank_addr + 0x555 ) = 0x0098;   /* write CFI entry command         */

/* Example: CFI Exit command  */
  *( (UINT16 *)bank_addr + 0x000 ) = 0x00F0;   /* write cfi exit command          */
```

For further information, please refer to the CFI Specification (see JEDEC publications JEP137-A and JESD68.01and CFI Publication 100). Please contact your sales office for copies of these documents.

Table 13.3 CFI Query Identification String

Addresses	Data	Description
10h 11h 12h	0051h 0052h 0059h	Query Unique ASCII string *QRY*
13h 14h	0002h 0000h	Primary OEM Command Set
15h 16h	0040h 0000h	Address for Primary Extended Table
17h 18h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 13.4 System Interface String

Addresses	Data	Description
1Bh	0017h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	0019h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	0006h	Typical timeout per single byte/word write 2^N µs
20h	0009h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	000Ah	Typical timeout per individual block erase 2^N ms
22h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	0004h	Max. timeout for byte/word write 2^N times typical
24h	0004h	Max. timeout for buffer write 2^N times typical
25h	0003h	Max. timeout per individual block erase 2^N times typical
26h	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 13.5 Device Geometry Definition

Addresses	Data	Description
27h	0019h (WS256N) 0018h (WS128N) 0017h (WS064N)	Device Size = 2^N byte
28h 29h	0001h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	0006h 0000h	Max. number of bytes in multi-byte write = 2^N (00h = not supported)
2Ch	0003h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	0003h 0000h 0080h 0000h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h	00FDh (WS256N) 007Dh (WS128N) 003Dh (WS064N)	Erase Block Region 2 Information
32h 33h 34h	0000h 0000h 0002h	
35h 36h 37h 38h	0003h 0000h 0080h 0000h	Erase Block Region 3 Information
39h 3Ah 3Bh 3Ch	0000h 0000h 0000h 0000h	Erase Block Region 4 Information

Table 13.6 Primary Vendor-Specific Extended Query

Addresses	Data	Description
40h 41h 42h	0050h 0052h 0049h	Query-unique ASCII string *PRI*
43h	0031h	Major version number, ASCII
44h	0034h	Minor version number, ASCII
45h	0100h	Address Sensitive Unlock (Bits 1-0), 0 = Required, 1 = Not Required Silicon Technology (Bits 5-2) 0100 = 0.11 µm
46h	0002h	Erase Suspend, 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	0001h	Sector Protect, 0 = Not Supported, X = Number of sectors in per group
48h	0000h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	0008h	Sector Protect/Unprotect scheme 08 = Advanced Sector Protection
4Ah	00F3h (WS256N) 007Bh (WS128N) 003Fh (WS064N)	Simultaneous Operation Number of Sectors in all banks except boot bank
4Bh	0001h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	0000h	Page Mode Type, 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page, 04 = 16 Word Page
4Dh	0085h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	0095h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	0001h	Top/Bottom Boot Sector Flag 0001h = Dual Boot Device
50h	0001h	Program Suspend. 00h = not supported

Table 13.6 Primary Vendor-Specific Extended Query (Continued)

Addresses	Data	Description
51h	0001h	Unlock Bypass, 00 = Not Supported, 01=Supported
52h	0007h	Secured Silicon Sector (Customer OTP Area) Size 2^N bytes
53h	0014h	Hardware Reset Low Time-out during an embedded algorithm to read mode Maximum 2^N ns
54h	0014h	Hardware Reset Low Time-out not during an embedded algorithm to read mode Maximum 2^N ns
55h	0005h	Erase Suspend Time-out Maximum 2^N ns
56h	0005h	Program Suspend Time-out Maximum 2^N ns
57h	0010h	Bank Organization: X = Number of banks
58h	0013h (WS256N) 000Bh (WS128N) 0007h (WS064N)	Bank 0 Region Information. X = Number of sectors in bank
59h	0010h (WS256N) 0008h (WS128N) 0004h (WS064N)	Bank 1 Region Information. X = Number of sectors in bank
5Ah	0010h (WS256N) 0008h (WS128N) 0004h (WS064N)	Bank 2 Region Information. X = Number of sectors in bank
5Bh	0010h (WS256N) 0008h (WS128N) 0004h (WS064N)	Bank 3 Region Information. X = Number of sectors in bank
5Ch	0010h (WS256N) 0008h (WS128N) 0004h (WS064N)	Bank 4 Region Information. X = Number of sectors in bank
5Dh	0010h (WS256N) 0008h (WS128N) 0004h (WS064N)	Bank 5 Region Information. X = Number of sectors in bank
5Eh	0010h (WS256N) 0008h (WS128N) 0004h (WS064N)	Bank 6 Region Information. X = Number of sectors in bank
5Fh	0010h (WS256N) 0008h (WS128N) 0004h (WS064N)	Bank 7 Region Information. X = Number of sectors in bank
60h	0010h (WS256N) 0008h (WS128N) 0004h (WS064N)	Bank 8 Region Information. X = Number of sectors in bank
61h	0010h (WS256N) 0008h (WS128N) 0004h (WS064N)	Bank 9 Region Information. X = Number of sectors in bank
62h	0010h (WS256N) 0008h (WS128N) 0004h (WS064N)	Bank 10 Region Information. X = Number of sectors in bank
63h	0010h (WS256N) 0008h (WS128N) 0004h (WS064N)	Bank 11 Region Information. X = Number of sectors in bank
64h	0010h (WS256N) 0008h (WS128N) 0004h (WS064N)	Bank 12 Region Information. X = Number of sectors in bank
65h	0010h (WS256N) 0008h (WS128N) 0004h (WS064N)	Bank 13 Region Information. X = Number of sectors in bank
66h	0010h (WS256N) 0008h (WS128N) 0004h (WS064N)	Bank 14 Region Information. X = Number of sectors in bank
67h	0013h (WS256N) 000Bh (WS128N) 0007h (WS064N)	Bank 15 Region Information. X = Number of sectors in bank

14 Commonly Used Terms

Term	Definition
ACC	ACCelerate. A special purpose input signal which allows for faster programming or erase operation when raised to a specified voltage above V_{CC}. In some devices ACC may protect all sectors when at a low voltage.
A_{max}	Most significant bit of the address input [A23 for 256Mbit, A22 for128Mbit, A21 for 64Mbit]
A_{min}	Least significant bit of the address input signals (A0 for all devices in this document).
Asynchronous	Operation where signal relationships are based only on propagation delays and are unrelated to synchronous control (clock) signal.
Autoselect	Read mode for obtaining manufacturer and device information as well as sector protection status.
Bank	Section of the memory array consisting of multiple consecutive sectors. A read operation in one bank, can be independent of a program or erase operation in a different bank for devices that offer simultaneous read and write feature.
Boot sector	Smaller size sectors located at the top and or bottom of Flash device address space. The smaller sector size allows for finer granularity control of erase and protection for code or parameters used to initiate system operation after power-on or reset.
Boundary	Location at the beginning or end of series of memory locations.
Burst Read	*See synchronous read*.
Byte	8 bits
CFI	Common Flash Interface. A Flash memory industry standard specification [JEDEC 137-A and JESD68.01] designed to allow a system to interrogate the Flash to determine its size, type and other performance parameters.
Clear	Zero (Logic Low Level)
Configuration Register	Special purpose register which must be programmed to enable synchronous read mode
Continuous Read	Synchronous method of burst read whereby the device reads continuously until it is stopped by the host, or it has reached the highest address of the memory array, after which the read address wraps around to the lowest memory array address
Erase	Returns bits of a Flash memory array to their default state of a logical One (High Level).
Erase Suspend/Erase Resume	Halts an erase operation to allow reading or programming in any sector that is not selected for erasure
BGA	Ball Grid Array package. Spansion LLC offers two variations: Fortified Ball Grid Array and Fine-pitch Ball Grid Array. See the specific package drawing or connection diagram for further details.
Linear Read	Synchronous (burst) read operation in which 8, 16, or 32 words of sequential data with or without wraparound before requiring a new initial address.
MCP	Multi-Chip Package. A method of combining integrated circuits in a single package by *stacking* multiple die of the same or different devices.
Memory Array	The programmable area of the product available for data storage.
MirrorBit™ Technology	Spansion™ trademarked technology for storing multiple bits of data in the same transistor.

Term	Definition
Page	Group of words that may be accessed more rapidly as a group than if the words were accessed individually.
Page Read	Asynchronous read operation of several words in which the first word of the group takes a longer initial access time and subsequent words in the group take less *page* access time to be read. Different words in the group are accessed by changing only the least significant address lines.
Password Protection	Sector protection method which uses a programmable password, in addition to the Persistent Protection method, for protection of sectors in the Flash memory device.
Persistent Protection	Sector protection method that uses commands and only the standard core voltage supply to control protection of sectors in the Flash memory device. This method replaces a prior technique of requiring a 12V supply to control the protection method.
Program	Stores data into a Flash memory by selectively clearing bits of the memory array in order to leave a data pattern of *ones* and *zeros*.
Program Suspend/Program Resume	Halts a programming operation to read data from any location that is not selected for programming or erase.
Read	Host bus cycle that causes the Flash to output data onto the data bus.
Registers	Dynamic storage bits for holding device control information or tracking the status of an operation.
Secured Silicon	Secured Silicon. An area consisting of 256 bytes in which any word may be programmed once, and the entire area may be protected once from any future programming. Information in this area may be programmed at the factory or by the user. Once programmed and protected there is no way to change the secured information. This area is often used to store a software readable identification such as a serial number.
Sector Protection	Use of one or more control bits per sector to indicate whether each sector may be programmed or erased. If the Protection bit for a sector is set the embedded algorithms for program or erase ignores program or erase commands related to that sector.
Sector	An Area of the memory array in which all bits must be erased together by an erase operation.
Simultaneous Operation	Mode of operation in which a host system may issue a program or erase command to one bank, that embedded algorithm operation may then proceed while the host immediately follows the embedded algorithm command with reading from another bank. Reading may continue concurrently in any bank other than the one executing the embedded algorithm operation.
Synchronous Operation	Operation that progresses only when a timing signal, known as a clock, transitions between logic levels (that is, at a clock edge).
VersatileIO™ (V_{IO})	Separate power supply or voltage reference signal that allows the host system to set the voltage levels that the device generates at its data outputs and the voltages tolerated at its data inputs.
Unlock Bypass	Mode that facilitates faster program times by reducing the number of command bus cycles required to issue a write operation command. In this mode the initial two Unlock *write* cycles, of the usual 4 cycle Program command, are not required – reducing all Program commands to two bus cycles while in this mode.
Word	Two contiguous bytes (16 bits) located at an even byte boundary. A double word is two contiguous words located on a two word boundary. A quad word is four contiguous words located on a four word boundary.

Term	Definition
Wraparound	Special burst read mode where the read address *wraps* or returns back to the lowest address boundary in the selected range of words, after reading the last Byte or Word in the range, e.g. for a 4 word range of 0 to 3, a read beginning at word 2 would read words in the sequence 2, 3, 0, 1.
Write	Interchangeable term for a program/erase operation where the content of a register and or memory location is being altered. The term write is often associated with *writing command cycles* to enter or exit a particular mode of operation.
Write Buffer	Multi-word area in which multiple words may be programmed as a single operation. A Write Buffer may be 16 to 32 words long and is located on a 16 or 32 word boundary respectively.
Write Buffer Programming	Method of writing multiple words, up to the maximum size of the Write Buffer, in one operation. Using Write Buffer Programming results in ≥ 8 times faster programming time than by using single word at a time programming commands.
Write Operation Status	Allows the host system to determine the status of a program or erase operation by reading several special purpose register bits.

S29RS512N

512 Megabit (32 M x 16-Bit) CMOS 1.8 Volt-only Read/Write, Burst Mode, Mass Storage Flash Memory for Multi-Chip Products (MCP)

SPANSION™

DATA SHEET

Distinctive Characteristics

Architectural Advantages

- **Single 1.8 volt read, program and erase (1.65 to 1.95 volt)**
- **Manufactured on 0.11 µm MirrorBit™ process Read / Write operation**
  - Zero latency between read and write operations
- **Programable Burst Interface**
  - 2 Modes of Burst Read Operation
  - Linear Burst: 8, 16, and 32 words with or without wrap-around
  - Continuous Sequential Burst
- **Sector Architecture**
  - one-hundred-twenty-eight 256 Kword sectors
- **100,000 erase cycle per sector typical**
- **20-year data retention typical**

Performance Charcteristics

- **Read access times at 80 / 66 / 54 MHz**
  - Burst access times of 9.1/11.2/13.5 ns
  - Synchronous latency of 148 ns
  - Asynchronous random access times of 143 ns
- **High Performance**
  - Typical word programming time of 40 µs
  - Typical effective word programming time of 9.4 µs utilizing a 32-Word Write Buffer at Vcc Level
  - Typical effective word programming time of 6 µs utilizing a 32-Word Write Buffer at ACC Level
  - Typical 2 s sector erase time for 256 Kword sectors
- **Power dissipation (typical values, C_L = 30 pF) @ 80 MHz**
  - Continuous Burst Mode Read: 35 mA
  - Program: 19 mA
  - Erase: 19 mA
  - Standby mode: 20 µA

Hardware Features

- **Sector Protection**
  - Dynamic Protection Bits (DYB) are assigned to every sector
  - A command sector protection to lock/unlock combinations of individual sectors to prevent/allow program or erase operations within that sector.
- **Handshaking feature available**
  - Provides host system with minimum possible latency by monitoring RDY
- **ACC input: Acceleration function reduces programming time in a factory setting**
- **Low V_{CC} write inhibit**

Software Features

- **Software command set compatible with JEDEC 42.4 standards**
- **Data# Polling and toggle bits**
  - Provides a software method of detecting program and erase operation completion
- **Erase Suspend / Resume**
  - Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Program Suspend / Resume**
  - Suspends a programming operation to read data from a sector other than the one being programmed, then resume the programming operation
- **Unlock Bypass Program command**
  - Reduces overall programming time when issuing multiple program command sequences

Additional Features

- **Program Operation**
  - Ability to perform synchronous and asynchronous write operation independent of burst control register setting

Publication Number S75WS-N-00 **Revision** A **Amendment** 0 **Issue Date** February 17, 2005

General Description

The S29RS512N is a 512 Mbit, 1.8 Volt-only, simultaneous Read/Write, Burst Mode Flash memory device, organized as 33,554,432words of 16 bits each. This device uses a single V_{CC} of 1.65 to 1.95 V to read, program, and erase the memory array. A 9.0-volt V_{HH} on ACC may be used for faster program performance in a factory setting environment.

The device uses Chip Enable (CE#), Write Enable (WE#), Address Valid (AVD#) and Output Enable (OE#) to control asynchronous read and write operations. For burst operations, the device additionally requires Ready (RDY), and Clock (CLK). This implementation allows easy interface with minimal glue logic to a wide range of microprocessors/microcontrollers for high performance read operations.

The burst read mode feature gives system designers flexibility in the interface to the device. The user can preset the burst length and then wrap or non-wrap through the same memory space, or read the currently addressable flash array block in continuous mode.

The rising clock edge initiates burst accesses and determines when data will be output.

The device is entirely command set compatible with the **JEDEC 42.4 single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timing. Register contents serve as inputs to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm - an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster program times by requiring only two write cycles to program data instead of four. Additionally, **Write Buffer Programming** is available on this family of devices. This feature provides superior programming performance by grouping locations being programmed.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm - an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The **Program Suspend/Program Resume** feature enables the user to put program on hold to read data from any sector that is not selected for programming. If a read is needed from the Dynamic Protection area after a program suspend, then the user must use the proper command sequence to enter and exit this region. The program suspend/resume functionality is also available when programming in erase suspend (1 level depth only).

The **Erase Suspend/Erase Resume** feature enables the user to put erase on hold to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved. If a read is needed from the Dynamic Protection area, after an erase suspend, then the user must use the proper command sequence to enter and exit this region.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read boot-up firmware from the Flash memory device.

The host system can detect whether a memory array program or erase operation is complete by using the device status bit DQ7 (Data# Polling), DQ6/DQ2 (toggle bits), DQ5 (exceeded timing limit), DQ3 (sector erase start timeout state indicator), and DQ1 (write to buffer abort). After a program or erase cycle has been completed, the device automatically returns to reading array data.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors [The device is fully erased when shipped from the factory].

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions.

When the ACC pin = V_{IL}, the entire flash memory array is protected.

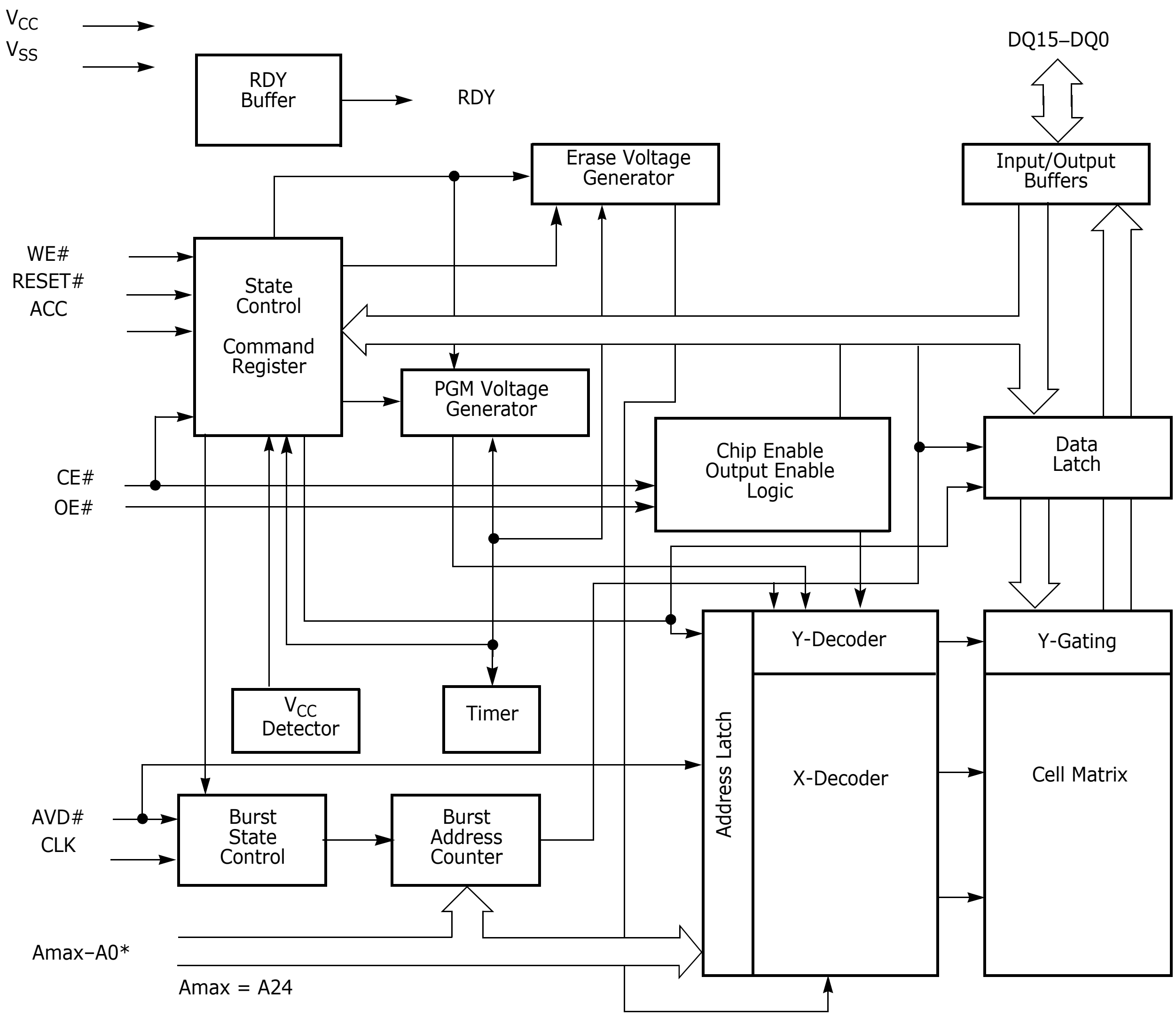
The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both modes.

Spansion's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector. The data is programmed using hot electron injection.

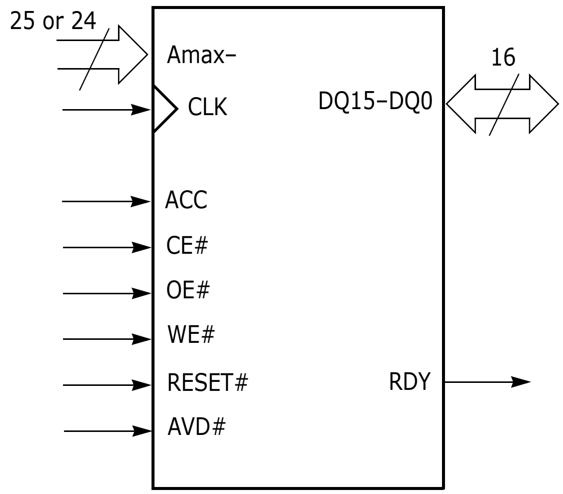
15 Product Selector Guide

S29RS512N					
Synchronous/Burst				Asynchronous	
Speed Option	80 MHz	66 MHz	54 MHz		
Max Latency, ns (t_{IACC})	148	160	160	Max Access Time, ns (t_{ACC})	143
Max Burst Access Time, ns (t_{BACC})	9.1	11.2	13.5	Max CE# Access, ns (t_{CE})	148
Max OE# Access, ns (t_{OE})	9.1	11.2	13.5	Max OE# Access, ns (t_{OE})	9.1

16 Block Diagram



17 Logic Symbol



Note: *Amax = A24 for 512Mb.*

18 Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 18.1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 18.1 Device Bus Operations

Operation	CE#	OE#	WE#	Addresses	DQ15–0	RESET#	CLK	AVD#
Asynchronous Read - Addresses Latched	L	L	H	Addr In	I/O	H	X	↓↑
Asynchronous Read - Addresses Steady State	L	L	H	Addr In	I/O	H	X	L
Asynchronous Write	L	H	L	Addr In	I/O	H	X	L
Synchronous Write	L	H	L	Addr In	I/O	H	↓↑	↓↑
Standby (CE#)	H	X	X	X	HIGH Z	H	X	X
Hardware Reset	X	X	X	X	HIGH Z	L	X	X
Burst Read Operations								
Load Starting Burst Address	L	X	H	Addr In	X	H	↑	↓↑
Advance Burst to next address with appropriate Data presented on the Data Bus	L	L	H	X	Burst Data Out	H	↑	H
Terminate current Burst read cycle	H	X	H	X	HIGH Z	H	↑	X
Terminate current Burst read cycle via RESET#	X	X	H	X	HIGH Z	L	X	X
Terminate current Burst read cycle and start new Burst read cycle	L	X	H	Addr In	I/O	H	↑	↓↑

Legend: *L = Logic 0, H = Logic 1, X = Don't Care.*

18.1 Requirements for Asynchronous Read Operation (Non-Burst)

To read data from the memory array, the system must first assert a valid address on Amax–A0, while driving AVD# and CE# to V_{IL}. WE# should remain at V_{IH}. The rising edge of AVD# latches the address. The data will appear on DQ15–DQ0.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from the stable CE# to valid data at the outputs. The output enable access time (t_{OE}) is the delay from the falling edge of OE# to valid data at the output.

The internal state machine is set for reading array data in asynchronous mode upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition.

18.2 Requirements for Synchronous (Burst) Read Operation

The device is capable of continuous sequential burst operation and linear burst operation of a preset length. When the device first powers up, it is enabled for asynchronous read operation.

Prior to entering burst mode, the system should determine how many wait states are desired for the initial word (t_{IACC}) of each burst access, what mode of burst operation is desired and how the RDY signal will transition with valid data. The system would then write the configuration register command sequence. See Set Configuration Register Command Sequence for further details.

Table 2-4 shows the address latency scheme for varying frequencies.

Table 18.2 Address Latency Scheme for < 56Mhz

Initial Addr	Cycle							
	X	X+1	X+2	X+3	**Add ws**	X+4	X+5	X+6
00	D0	D1	D2	D3	**0ws**	D4	D5	D6
01	D1	D2	D3	1ws	**0ws**	D4	D5	D6
10	D2	D3	1ws	1ws	**0ws**	D4	D5	D6
11	D3	1ws	1ws	1ws	**0ws**	D4	D5	D6

Table 18.3 Address Latency Scheme for < 70Mhz

Initial Addr	Cycle							
	X	X+1	X+2	X+3	**Add ws**	X+4	X+5	X+6
00	D0	D1	D2	D3	**1ws**	D4	D5	D6
01	D1	D2	D3	1ws	**1ws**	D4	D5	D6
10	D2	D3	1ws	1ws	**1ws**	D4	D5	D6
11	D3	1ws	1ws	1ws	**1ws**	D4	D5	D6

Table 18.4 Address Latency Scheme for < 84Mhz

Initial Addrs	Cycle							
	X	X+1	X+2	X+3	**Add ws**	X+4	X+5	X+6
00	D0	D1	D2	D3	**2ws**	D4	D5	D6
01	D1	D2	D3	1ws	**2ws**	D4	D5	D6
10	D2	D3	1ws	1ws	**2ws**	D4	D5	D6
11	D3	1ws	1ws	1ws	**2ws**	D4	D5	D6

Address Latency Scheme for < 84Mhz

The initial word is output t_{IACC} after the rising edge of the first CLK cycle. Subsequent words are output t_{BACC} after the rising edge of each successive clock cycle, which automatically increments the internal address counter. Note that the device has a fixed internal address boundary that occurs every 512 words **and there is a boundary crossing latency of 4/8 wait states, when the device is operating at frequencies lower than 56/80Mhz respectively.**

During the time the device is outputting data with the starting burst address not divisible by four, additional waits are required. For example, if the device is operating at frequency of 80Mhz and if the starting burst address is divisible by four A1:0 = 00, two additional wait state is required.

If the starting burst address is at address A1:0 = 01, 10, 11 then three, four or five wait states are required, respectively, until data D4 is read and burst sequence becomes linear. Please refer to Table 18.4 for further details. The RDY output indicates this condition to the system by deasserting.

18.2.1 Continuous Burst

The device will continue to output sequential burst data, wrapping around to address 000000h after it reaches the highest addressable memory location, until the system drives CE# high, RESET# low, or AVD# low in conjunction with a new address. See Table 18.1.

18.2.2 8-, 16-, and 32-Word Linear Burst with Wrap Around

The remaining three modes are of the linear wrap around design, in which a fixed number of words are read from consecutive addresses. In each of these modes, the burst addresses read are determined by the group within which the starting address falls. The groups are sized according to the number of words read in a single burst sequence for a given mode (see Table 18.5.).

Table 18.5 Burst Address Groups

Mode	Group Size	Group Address Ranges
8-word	8 words	0-7h, 8-Fh, 10-17h,...
16-word	16 words	0-Fh, 10-1Fh, 20-2Fh,...
32-word	32 words	00-1Fh, 20-3Fh, 40-5Fh,...

As an example: if the starting address in the 8-word mode is 3ch, the address range to be read would be 38-3Fh, and the burst sequence would be 3C, 3D, 3E, 3F, 38, 39, 3A, 3Bh. if wrap around is enable. The burst sequence begins with the starting address written to the device, but wraps back to the first address in the selected group and stops at the group size, terminating the burst read. In a similar fashion, the 16-word and 32-word Linear Wrap modes begin their burst sequence on the starting address written to the device, and then wrap back to the first address in the selected address group. **Note that in these three burst read modes the address pointer does not cross the boundary that occurs every 512 words; thus, no wait states are inserted (except during the initial access).** (see Figure 25.4)

18.2.3 8-, 16-, and 32-Word Linear Burst without Wrap Around

If wrap around is not enabled, 8-word, 16-word, or 32-word burst will execute linearly up to word boundary. The burst will stop after 8, 16, or 32 addresses and will not wrap around to the first address of the selected group. As an example: if the starting address in the 8-word mode is 3ch, the address range to be read would be 39-40h, and the burst sequence would be 3C, 3D-3E-3F-40-41-42-43h if wrap around is not enabled. The next address to be read will require a new address and AVD# pulse. The address range would stay within the address block, causing address FFFFh to be followed by 0000h. *Note that in this burst mode, the address pointer may cross the boundary that occurs every 128 words.*

18.3 Configuration Register

The device uses a configuration register to set the various burst parameters: number of wait states, burst read mode, RDY configuration, and synchronous mode active.

18.4 RDY: Ready

The RDY is a dedicated output that, when the device is configured in the Synchronous mode, indicates (when at logic low) the system should wait 1 clock cycle before expecting the next word of data. The RDY pin is only controlled by CE#. Using the RDY Configuration Command Sequence, RDY can be set so that a logic low indicates the system should wait 2 clock cycles before expecting valid data.

The following conditions cause the RDY output to be low: during the initial access (in burst mode), and at the boundary crossing, that occurs every 512 words beginning with address 1FFh.

18.5 Handshaking

The device is equipped with a handshaking feature that allows the host system to simply monitor the RDY signal from the device to determine when the burst data is ready to be read. The host system should use the programmable wait state configuration to set the number of wait states for optimal burst mode operation. The initial word of burst data is indicated by the rising edge of RDY after OE# goes low.

For optimal burst mode performance, the host system must set the appropriate number of wait states in the flash device depending on clock frequency. See Set Configuration Register Command Sequence and Requirements for Synchronous (Burst) Read Operation for more information.

18.6 Writing Commands/Command Sequences

The device has the capability of performing an asynchronous or synchronous write operation. While the device is configured in Asynchronous read it is able to perform Asynchronous write operations only. CLK is ignored when the device is configured in the Asynchronous mode. When in the Synchronous read mode configuration, the device is able to perform both Asynchronous and Synchronous write operations. CLK and AVD# address latch is supported in the Synchronous programming mode. During a synchronous write operation, to write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive AVD# and CE# to V_{IL}, and OE# to V_{IH} when providing an address to the device, and drive WE# and CE# to V_{IL}, and OE# to V_{IH}. when writing commands or data. During an asynchronous write operation, the system must drive CE# and WE# to V_{IL} and OE# to V_{IH} when providing an address, command, and data. Addresses are latched on the last falling edge of WE# or CE#, while data is latched on the 1st rising edge of WE# or CE# (see).

The device features an Unlock Bypass mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word, instead of four.

An erase operation can erase one sector, multiple sectors or the entire device. Table 19.6 indicates the address space that each sector occupies. A *sector address* is the address bits required to uniquely select a sector.

I_{CC2} in the DC Characteristics section represents the active current specification for the write mode. The AC Characteristics section contains timing specification tables and timing diagrams for write operations.

18.7 Accelerated Program/Chip Erase Operations

The device offers accelerated program and accelerated chip erase operations through the ACC functionACC is intended to allow faster manufacturing throughput at the factory and not to be used in system operations.

The system can use the Write Buffer Load command sequence. Note that if a *Write-to-Buffer-Abort Reset* is required, the **full 3-cycle RESET command sequence must be used to reset the device**. Removing V_{HH} from the ACC input, upon completion of the embedded program or erase operation, returns the device to normal operation. Note that sectors must be unlocked prior to raising ACC to V_{HH}. When at V_{IL}, ACC locks all sectors. ACC should be at V_{IH} for all other conditions.

number loaded = the number of locations to program minus 1. For example, if the system will program 6 address locations, then 05h should be written to the device.)

The system then writes the starting address/data combination. This starting address is the first address/data pair to be programmed, and selects the *write-buffer-page* address. All subsequent address/data pairs **must** fall within the *selected-write-buffer-page* where Amax = 24 for RS512N.

The *write-buffer-page* is selected by addresses Amax - A5.

The *write-buffer-page* addresses **must be the same for all address/data pairs loaded into the write buffer**. (This means Write Buffer Programming **cannot** be performed across multiple *write-buffer-page*s. This also means that Write Buffer Programming **cannot** be performed across multiple sectors. If the system attempts to load programming data outside of the selected *write-buffer-page*, the operation will ABORT.)

After writing the Starting Address/Data pair, the system then writes the remaining address/data paris into the write buffer. Write buffer locations may be loaded in any order.

Note that if a Write Buffer address location is loaded multiple times, the *address/data pair* counter **will be decremented for every data load operation**. Also, the **last data loaded** at a location before the *Program Buffer to Flash* confirm command will be programmed into the device. It is the software's responsibility to comprehend ramifications of loading a write-buffer location more than once. The counter decrements **for each data load operation**, ***not*** **for each unique write-buffer-address location**.

Once the specified number of write buffer locations have been loaded, the system must then write the *Program Buffer to Flash* command at the Sector Address. Any other address/data write combinations will abort the Write Buffer Programming operation. The device then *goes busy*. The Data Bar polling techniques should be used while monitoring the **last address location loaded into the write buffer**. This eliminates the need to store an address in memory because the system can load the last address location, issue the program confirm command at the last loaded address location, and then data bar poll at that same address. DQ7, DQ6, DQ5, DQ2, and DQ1 should be monitored to determine the device status during Write Buffer Programming.

The write-buffer *embedded* programming operation can be suspended using the standard suspend/resume commands. Upon successful completion of the Write Buffer Programming operation, the device will return to READ mode.

The Write Buffer Programming Sequence can be ABORTED in the following ways:

- Load a value that is greater than the page buffer size during the *Number of Locations to Program* step.
- Write to an address in a sector different than the one specified during the *Write-Buffer-Load* command.
- Write an Address/Data pair to a different write-buffer-page than the one selected by the *Starting Address* during the *write buffer data loading* stage of the operation.
- Write data other than the *Confirm Command* after the specified number of *data load* cycles.

The ABORT condition is indicated by DQ1 = 1, DQ7 = Data# (for the *last address location loaded*), DQ6 = TOGGLE, DQ5 = 0. This indicates that the Write Buffer Programming Operation was ABORTED. A *Write-to-Buffer-Abort reset* command sequence is required when using the Write-Buffer-Programming features in Unlock Bypass mode. **[Use of the write buffer is strongly recommended for programming when multiple words are to be programmed.]**

from the internal register (which is separate from the memory array)

18.8 Dynamic Sector Protection

The device offers data protection at the sector level and the DYB associated command sequences disables or re-enables both program and erase operations in any sector or sector group.

- Dynamically Locked—The sector is protected and can be changed by a simple command
- Unlocked—The sector is unprotected and can be changed by a simple command

18.8.1 Dynamic Protection Bit (DYB)

A volatile protection bit is assigned for each sector. After power-up or hardware reset, the contents of all DYBs is cleared *erased to 1*. In other words, the DYB powers-up in an unprotected state. Each DYB is individually modifiable through the DYB Write Command.

The Protection State for each sector is determined by the DYB related to that sector. The DYBs control whether or not the sector is protected or unprotected. By issuing the DYB Write command sequences, the DYBs will be set (programmed to *0*) or cleared (erased to *1*), thus placing each sector in the protected or unprotected state. These are the so-called Dynamic Locked or Unlocked states. They are called dynamic states because it is very easy to switch back and forth between the protected and unprotected conditions. This allows software to easily protect sectors against inadvertent changes yet does not prevent the easy removal of protection when changes are needed. The DYBs maybe set or cleared as often as needed.

18.9 Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# inputs are both held at V_{CC}. The device requires standard access time (t_{CE}) for read access, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in the DC Characteristics section represents the standby current specification.

18.10 Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. While in asynchronous mode, the device automatically enables this mode when addresses remain stable for t_{ACC} + 20 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. While in synchronous mode, the Automatic Sleep Mode is disabled. Note that a new burst operation is required to provide new data.

I_{CC6} in the DC Characteristics section represents the automatic sleep mode current specification.

18.11 RESET#: Hardware Reset Input

The RESET# input provides a hardware method of resetting the device to reading array data. When RESET# is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all outputs, resets the configuration register, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS}, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within V_{SS}, the standby current will be greater.

RESET# may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted t_{RP} operation, the device requires a time of t_{RH} + t_{RP} before the device is ready to read data again. If RESET# is asserted when a program or erase operation is not executing, the reset operation is completed within a time of t_{RP} (not during Embedded Algorithms). The system can read data t_{RH} after RESET# returns to V_{IH}.

Refer to the Synchronous/Burst Read section for RESET# parameters and to Figure 25.9 for the timing diagram.

18.12 Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The outputs are placed in the high impedance state.

18.13 Hardware Data Protection

The following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

18.13.1 Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to reading array data. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control inputs to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

18.13.2 Write Pulse *Glitch* Protection

Noise pulses do not initiate a write cycle.

18.13.3 Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

19 Sector Address / Memory Address Map

Table 19.6 Sector Address / Memory Address Map for the RS512N

Sector	Sector Size	(A24-A0) Address Range	Sector	Sector Size	(A24-A0) Address Range
SA0	256 Kwords	0000000h-003FFFFh	SA64	256 Kwords	1000000h-103FFFFh
SA1	256 Kwords	0040000h-007FFFFh	SA65	256 Kwords	1040000h-107FFFFh
SA2	256 Kwords	0080000h-00BFFFFh	SA66	256 Kwords	1080000h-10BFFFFh
SA3	256 Kwords	00C0000h-00FFFFFh	SA67	256 Kwords	10C0000h-10FFFFFh
SA4	256 Kwords	0100000h-013FFFFh	SA68	256 Kwords	1100000h-113FFFFh
SA5	256 Kwords	0140000h-017FFFFh	SA69	256 Kwords	1140000h-117FFFFh
SA6	256 Kwords	0180000h-01BFFFFh	SA70	256 Kwords	1180000h-11BFFFFh
SA7	256 Kwords	01C0000h-01FFFFFh	SA71	256 Kwords	11C0000h-11FFFFFh
SA8	256 Kwords	0200000h-023FFFFh	SA72	256 Kwords	1200000h-123FFFFh
SA9	256 Kwords	0240000h-027FFFFh	SA73	256 Kwords	1240000h-127FFFFh
SA10	256 Kwords	0280000h-02BFFFFh	SA74	256 Kwords	1280000h-12BFFFFh
SA11	256 Kwords	02C0000h-02FFFFFh	SA75	256 Kwords	12C0000h-12FFFFFh
SA12	256 Kwords	0300000h-033FFFFh	SA76	256 Kwords	1300000h-133FFFFh
SA13	256 Kwords	0340000h-037FFFFh	SA77	256 Kwords	1340000h-137FFFFh
SA14	256 Kwords	0380000h-03BFFFFh	SA78	256 Kwords	1380000h-13BFFFFh
SA15	256 Kwords	03C0000h-03FFFFFh	SA79	256 Kwords	13C0000h-13FFFFFh
SA16	256 Kwords	0400000h-043FFFFh	SA80	256 Kwords	1400000h-143FFFFh
SA17	256 Kwords	0440000h-047FFFFh	SA81	256 Kwords	1440000h-147FFFFh
SA18	256 Kwords	0480000h-04BFFFFh	SA82	256 Kwords	1480000h-14BFFFFh
SA19	256 Kwords	04C0000h-04FFFFFh	SA83	256 Kwords	14C0000h-14FFFFFh
SA20	256 Kwords	0500000h-053FFFFh	SA84	256 Kwords	1500000h-153FFFFh
SA21	256 Kwords	0540000h-057FFFFh	SA85	256 Kwords	1540000h-157FFFFh
SA22	256 Kwords	0580000h-05BFFFFh	SA86	256 Kwords	1580000h-15BFFFFh
SA23	256 Kwords	05C0000h-05FFFFFh	SA87	256 Kwords	15C0000h-15FFFFFh
SA24	256 Kwords	0600000h-063FFFFh	SA88	256 Kwords	1600000h-163FFFFh
SA25	256 Kwords	0640000h-067FFFFh	SA89	256 Kwords	1640000h-167FFFFh
SA26	256 Kwords	0680000h-06BFFFFh	SA90	256 Kwords	1680000h-16BFFFFh
SA27	256 Kwords	06C0000h-06FFFFFh	SA91	256 Kwords	16C0000h-16FFFFFh
SA28	256 Kwords	0700000h-073FFFFh	SA92	256 Kwords	1700000h-173FFFFh
SA29	256 Kwords	0740000h-077FFFFh	SA93	256 Kwords	1740000h-177FFFFh
SA30	256 Kwords	0780000h-07BFFFFh	SA94	256 Kwords	1780000h-17BFFFFh
SA31	256 Kwords	07C0000h-07FFFFFh	SA95	256 Kwords	17C0000h-17FFFFFh
SA32	256 Kwords	0800000h-083FFFFh	SA96	256 Kwords	1800000h-183FFFFh
SA33	256 Kwords	0840000h-087FFFFh	SA97	256 Kwords	1840000h-187FFFFh
SA34	256 Kwords	0880000h-08BFFFFh	SA98	256 Kwords	1880000h-18BFFFFh
SA35	256 Kwords	08C0000h-08FFFFFh	SA99	256 Kwords	18C0000h-18FFFFFh
SA36	256 Kwords	0900000h-093FFFFh	SA100	256 Kwords	1900000h-193FFFFh
SA37	256 Kwords	0940000h-097FFFFh	SA101	256 Kwords	1940000h-197FFFFh
SA38	256 Kwords	0980000h-09BFFFFh	SA102	256 Kwords	1980000h-19BFFFFh
SA39	256 Kwords	09C0000h-09FFFFFh	SA103	256 Kwords	19C0000h-19FFFFFh

Table 19.6 Sector Address / Memory Address Map for the RS512N (Continued)

Sector	Sector Size	(A24-A0) Address Range	Sector	Sector Size	(A24-A0) Address Range
SA40	256 Kwords	0A00000h-0A3FFFFh	SA104	256 Kwords	1A00000h-1A3FFFFh
SA41	256 Kwords	0A40000h-0A7FFFFh	SA105	256 Kwords	1A40000h-1A7FFFFh
SA42	256 Kwords	0A80000h-0ABFFFFh	SA106	256 Kwords	1A80000h-1ABFFFFh
SA43	256 Kwords	0AC0000h-0AFFFFFh	SA107	256 Kwords	1AC0000h-1AFFFFFh
SA44	256 Kwords	0B00000h-0B3FFFFh	SA108	256 Kwords	1B00000h-1B3FFFFh
SA45	256 Kwords	0B40000h-0B7FFFFh	SA109	256 Kwords	1B40000h-1B7FFFFh
SA46	256 Kwords	0B80000h-0BBFFFFh	SA110	256 Kwords	1B80000h-1BBFFFFh
SA47	256 Kwords	0BC0000h-0BFFFFFh	SA111	256 Kwords	1BC0000h-1BFFFFFh
SA48	256 Kwords	0C00000h-0C3FFFFh	SA112	256 Kwords	1C00000h-1C3FFFFh
SA49	256 Kwords	0C40000h-0C7FFFFh	SA113	256 Kwords	1C40000h-1C7FFFFh
SA50	256 Kwords	0C80000h-0CBFFFFh	SA114	256 Kwords	1C80000h-1CBFFFFh
SA51	256 Kwords	0CC0000h-0CFFFFFh	SA115	256 Kwords	1CC0000h-1CFFFFFh
SA52	256 Kwords	0D00000h-0D3FFFFh	SA116	256 Kwords	1D00000h-1D3FFFFh
SA53	256 Kwords	0D40000h-0D7FFFFh	SA117	256 Kwords	1D40000h-1D7FFFFh
SA54	256 Kwords	0D80000h-0DBFFFFh	SA118	256 Kwords	1D80000h-1DBFFFFh
SA55	256 Kwords	0DC0000h-0DFFFFFh	SA119	256 Kwords	1DC0000h-1DFFFFFh
SA56	256 Kwords	0E00000h-0E3FFFFh	SA120	256 Kwords	1E00000h-1E3FFFFh
SA57	256 Kwords	0E40000h-0E7FFFFh	SA121	256 Kwords	1E40000h-1E7FFFFh
SA58	256 Kwords	0E80000h-0EBFFFFh	SA122	256 Kwords	1E80000h-1EBFFFFh
SA59	256 Kwords	0EC0000h-0EFFFFFh	SA123	256 Kwords	1EC0000h-1EFFFFFh
SA60	256 Kwords	0F00000h-0F3FFFFh	SA124	256 Kwords	1F00000h-1F3FFFFh
SA61	256 Kwords	0F40000h-0F7FFFFh	SA125	256 Kwords	1F40000h-1F7FFFFh
SA62	256 Kwords	0F80000h-0FBFFFFh	SA126	256 Kwords	1F80000h-1FBFFFFh
SA63	256 Kwords	0FC0000h-0FFFFFFh	SA127	256 Kwords	1FC0000h-1FFFFFFh

19.1 Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data in asynchronous mode. The device is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector within the same device. After completing a programming operation in the Erase Suspend mode, the system may once again read array data from any non-erase-suspended sector within the same device. See the Erase Suspend/Erase Resume Commands section for more information.

After the device accepts a Program Suspend command, the device enters the program-suspend-read mode, after which the system can read data from any non-program-suspended sector within the device. See Program Suspend/Program Resume Commands for more information.

The system must issue the reset command to return device to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the device is in the autoselect mode. See the Reset Command section for more information. If DQ1 goes high during Write Buffer Programming, the system must issue the Write Buffer Abort Reset command.

See also the Requirements for Asynchronous Read Operation (Non-Burst) and the Requirements for Synchronous (Burst) Read Operation sections for more information. The Asynchronous Read and Synchronous/Burst Read tables provide the read parameters, Figure 25.2, Figure 25.3, and Figure 25.7 show the timings.

19.2 Set Configuration Register Command Sequence

The device uses a configuration register to set the various burst parameters: number of wait states, burst read mode, RDY configuration, and synchronous mode active. The configuration register must be set before the device will enter burst mode.

The configuration register is loaded with a four-cycle command sequence. The first two cycles are standard unlock sequences. On the third cycle, the data should be D0h and address bits should be 555h. During the fourth cycle, the configuration code should be entered onto the data bus with the address bus set to address 000h or 001h. Once the data has been programmed into the configuration register, a software reset command is required to set the device into the correct state. The device will power up or after a hardware reset with the default setting, which is in asynchronous mode. The register must be set before the device can enter synchronous mode. The configuration register can not be changed during device operations (program, erase, or sector lock).

19.3 Read Configuration Register Command Sequence

The configuration register can be read with a four-cycle command sequence. The first two cycles are standard unlock sequences. On the third cycle, the data should be C6h and address bits should be 555h. During the fourth cycle, the configuration code should be read out of the data bus with the address bus set to address 000h or 001h. Once the data has been read from the configuration register, a software reset command is required to set the device into array read mode.

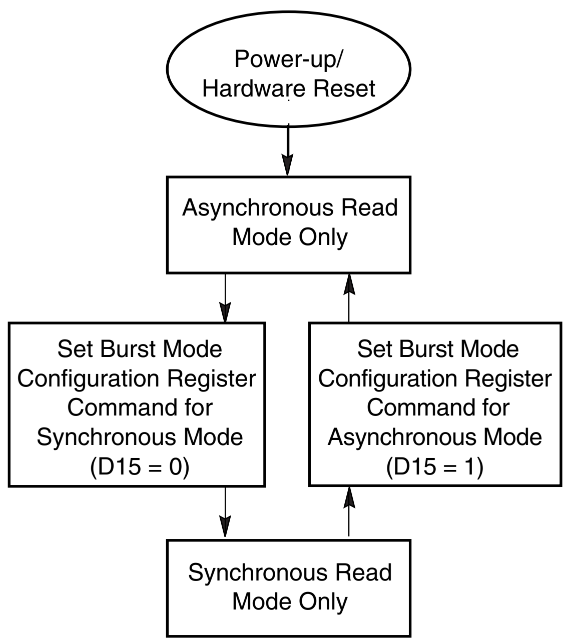


Figure 19.1 Synchronous/Asynchronous State Diagram

19.3.1 Read Mode Setting

On power-up or hardware reset, the device is set to be in asynchronous read mode. This setting allows the system to enable or disable burst mode during system operations. **Configuration Bit CR0.15** determines this setting: *1* for asynchronous mode, *0* for synchronous mode.

19.3.2 Programmable Wait State Configuration

The programmable wait state feature informs the device of the number of clock cycles that must elapse after AVD# is driven active before data will be available. This value is determined by the input frequency of the device. **Configuration Bit CR1.0 & CR0.13–CR0.11** determine the setting (see Table 19.7).

The wait state command sequence instructs the device to set a particular number of clock cycles for the initial access in burst mode. The number of wait states that should be programmed into the device is directly related to the clock frequency.

Table 19.7 Programmable Wait State Settings

CR1.0	CR0.13	CR0.12	CR0.11	Total Initial Access Cycles
0	0	0	0	Reserved
0	0	0	1	3
0	0	1	0	4
0	0	1	1	5
0	1	0	0	6
0	1	0	1	7
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12 (default)
1	1	0	1	13
1	1	1	0	Reserved
1	1	1	1	Reserved

Notes:

1. *Upon power-up or hardware reset, the default setting is twelve wait states.*
2. *All other but setting are reserved.*

It is recommended that the wait state command sequence be written, even if the default wait state value is desired, to ensure the device is set as expected. A hardware reset will set the wait state to the default setting.

19.3.3 Programmable Wait State

The host system should set **CR1.0 & CR0.13-CR0.11** to 1100/1010/1000 for a clock frequency of 80/66/54 MHz for the system/device to execute at maximum speed.

19.3.4 Boundary Crossing Latency

Additional wait states must be inserted to account for boundary crossing latency. This is done by setting **CR0.14** to a ‘1’ (default). If required, **CR0.14** can be changed to a ‘0’ to remove the boundary crossing latency.

19.3.5 Handshaking

For optimal burst mode performance, the host system must set the appropriate number of wait states in the flash device depending on the clock frequency.

The autoselect function allows the host system to determine whether the flash device is enabled for handshaking. See the Autoselect Command Sequence for more information.

19.3.6 Burst Length Configuration

The device supports four different read modes: continuous mode, and 8, 16, and 32 word linear with or without wrap around modes. A continuous sequence (default) begins at the starting address and advances the address pointer until the burst operation is complete. If the highest address in the device is reached during the continuous burst read mode, the address pointer wraps around to the lowest address.

For example, an eight-word linear read with wrap around begins on the starting address written to the device and then advances to the next 8 word boundary. The address pointer then returns to the 1st word after the previous eight word boundary, wrapping through the starting location. The sixteen- and thirty-two linear wrap around modes operate in a fashion similar to the eight-word mode.

Table 19.8 shows the **CR0.2-CR0.0** and settings for the four read modes.

Table 19.8 Burst Length Configuration

Burst Modes	Address Bits		
	CR0.2	CR0.1	CR0.0
Continuous	0	0	0
8-word linear	0	1	0
16-word linear	0	1	1
32-word linear	1	0	0

Note: *Upon power-up or hardware reset the default setting is continuous.*

19.3.7 Burst Wrap Around

By default, the device will perform burst wrap around with **CR0.3** set to a '1'. Changing the **CR0.3** to a '0' disables burst wrap around.

19.3.8 RDY Configuration

By default, the device is set so that the RDY pin will output V_{OH} whenever there is valid data on the outputs. The device can be set so that RDY goes active one data cycle before active data. **CR0.8** determines this setting; *1* for RDY active (default) with data, *0* for RDY active one clock cycle before valid data.

19.3.9 RDY Polarity

By default, the RDY pin will always indicate that the device is ready to handle a new transaction with **CR0.10** set to a '1'. In this case, the RDY pin is active high. Changing the **CR0.10** to a '0' sets the RDY pin to be active low. In this case, the RDY pin will always indicate that the device is ready to handle a new transaction when low.

19.4 Configuration Register

Table 19.9 shows the address bits that determine the configuration register settings for various device functions.

Table 19.9 Configuration Register

CR0. Bit	Function	Settings (Binary)
CR0.15	Set Device Read Mode	0 = Synchronous Read (Burst Mode) Enabled 1 = Asynchronous Mode (default)
CR0.14	Boundary Crossing	0 = No extra boundary crossing latency 1 = With extra boundary crossing latency (default)
CR1.0	Programmable Wait State	0000 = Reserved 0001 = Data is valid on the 4th active CLK edge after addresses are latched 0010 = Data is valid on the 5th active CLK edge after addresses are latched 0011 = Data is valid on the 6th active CLK edge after addresses are latched 0100 = Data is valid on the 7th active CLK edge after addresses are latched 0101 = Data is valid on the 8th active CLK edge after addresses are latched 0110 = Reserved 0111 = Reserved 1000 = Data is valid on the 9th active CLK edge after addresses are latched 1001 = Data is valid on the 10th active CLK edge after addresses are latched 1010 = Data is valid on the 11th active CLK edge after addresses are latched 1011 = Data is valid on the 12th active CLK edge after addresses are latched 1100 = Data is valid on the 13th active CLK edge after addresses are latched (default) 1101 = Data is valid on the 14th active CLK edge after addresses are latched 1110 = Reserved 1111 = Reserved
CR0.13		
CR0.12		
CR0.11		
CR0.10	RDY Polarity	0 = RDY signal is active low 1 = RDY signal is active high (default)
CR0.9	Reserved	1 = default
CR0.8	RDY	0 = RDY active one clock cycle before data 1 = RDY active with data (default)
CR0.7	Reserved	1 = default
CR0.6	Reserved	1 = default
CR0.5	Reserved	0 = default
CR0.4	Reserved	0 = default
CR0.3	Burst Wrap Around	0 = No Wrap Around Burst 1 = Wrap Around Burst (default)
CR0.2	Burst Length	000 = Continuous (default) 010 = 8-Word Linear Burst 011 = 16-Word Linear Burst 100 = 32-Word Linear Burst (All other bit settings are reserved)
CR0.1		
CR0.0		

Note: *3.Device will be in the default state upon power-up or hardware reset.*

19.5 Reset Command

Writing the reset command resets the device to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to which the system was writing to the read mode. [Once erasure begins, however, the device ignores reset commands until the operation is complete].

The reset command may be written between the sequence cycles in a program command sequence before programming begins (prior to the third cycle). This resets the device to which the system was writing to the read mode. If the program command sequence is written to the device that is in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If a device entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that device to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to the read mode (or erase-suspend-read mode if the device was in Erase Suspend and program-suspend-read mode if the device was in Program Suspend).

Note: If DQ1 goes high during a Write Buffer Programming operation, the system must write the *Write to Buffer Abort Reset* command sequence to RESET the device to reading array data. The standard RESET command will not work. See Table 19.9 for details on this command sequence.

19.6 Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. The Command Definitions table shows the address and data requirements. The autoselect command sequence may be written to an address within the device that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the autoselect command. The device then enters the autoselect mode. No subsequent data will be made available if the autoselect data is read in synchronous mode. The system may read at any address within the device any number of times without initiating another autoselect command sequence. The following table describes the address requirements for the various autoselect functions, and the resulting data. The device ID is read in three cycles.

Table 19.10 Autoselect Addresses

Description	Address	Read Data
Manufacturer ID	00h	01h
Device ID, Word 1	01h	227Eh
Device ID, Word 2	0Eh	2229 (RS512N)
Device ID, Word 3	0Fh	2201 (RS512N)
Indicator Bits	03h	DQ15 - DQ5 = 0 DQ4 & DQ3 = 11 DQ2 - DQ0 = 0

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the device was previously in Erase Suspend).

19.7 Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. The Command Definitions table shows the address and data requirements for the program command sequence.

When the Embedded Program algorithm is complete, the device then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by monitoring DQ7 or DQ6/DQ2. Refer to the "Write Operation Status" section for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a hardware reset immediately terminates the program operation. The program command sequence should be reinitiated once the device has returned to the read mode, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from *0* back to a *1*. Only erase operations can convert a *0* back to a *1*. Attempting to program a *1* over a *0* will result in a programming failure.**

Note: *See the Command Definitions table for program command sequence.*

Figure 19.2 Program Word Operation

19.8 Write Buffer Programming Command Sequence

Write Buffer Programming Sequence allows for faster programming as compared to the standard Program Command Sequence. See the Write Buffer Programming Operation section for the program command sequence.

Table 19.11 Write Buffer Command Sequence

Sequence	Address	Data	Comment
Unlock Command 1	555	00AA	Not required in the Unlock Bypass mode
Unlock Command 2	2AA	0055	Same as above
Write Buffer Load	Sector Address	0025h	
Specify the Number of Program Locations	Starting Address	Word Count	Number of locations to program minus 1
Load 1st data word	Starting Address	Program Data	All addresses must be within write-buffer-page boundaries, but do not have to be loaded in any order
Load next data word	Write Buffer Location	Program Data	Same as above
...	...	...	Same as above
Load last data word	Write Buffer Location	Program Data	Same as above
Write Buffer Program Confirm	Sector Address	0029h	This command must follow the last write buffer location loaded, or the operation will ABORT
Device goes busy			
Status monitoring through DQ pins (Perform Data Bar Polling on the **Last Loaded Address**)			

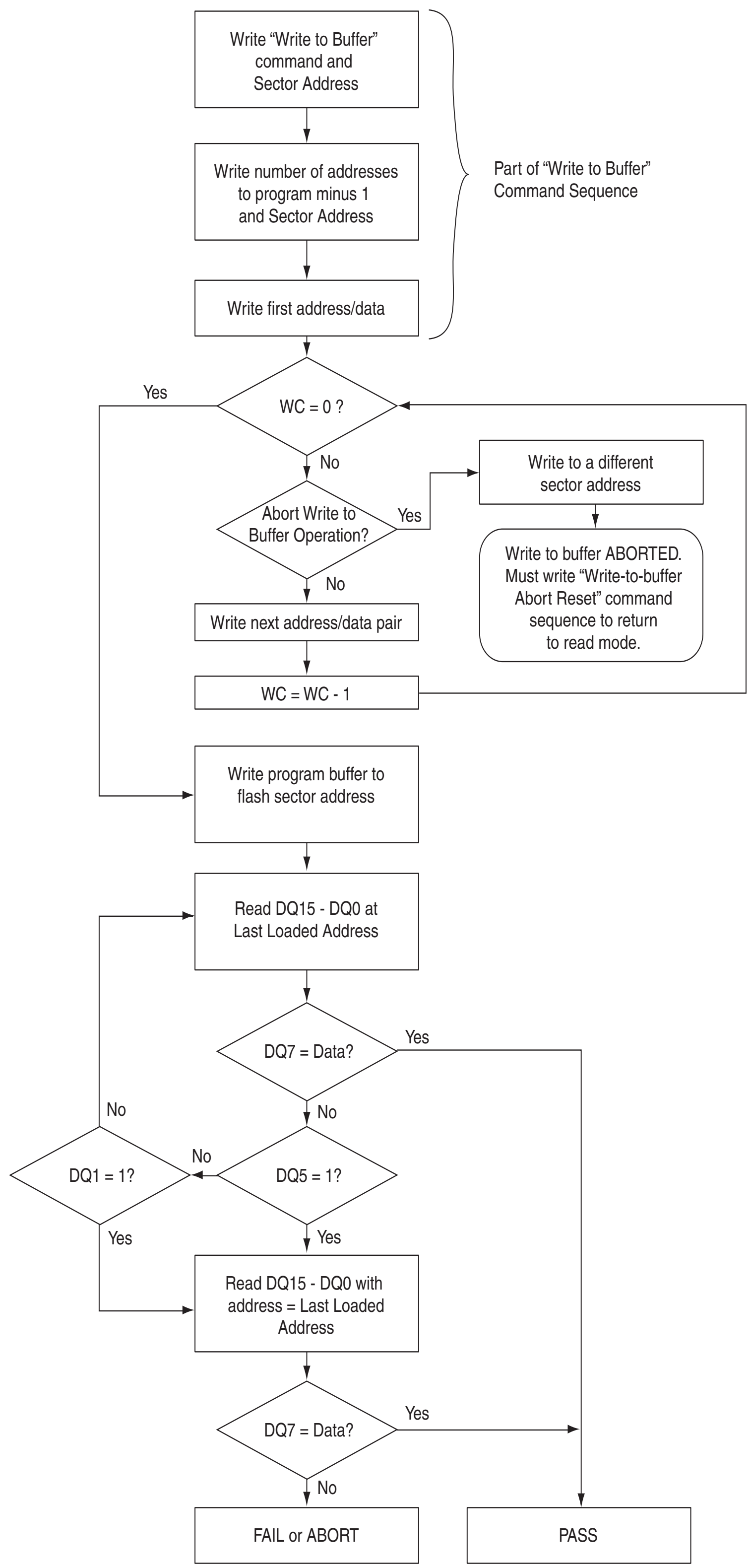


Figure 19.3 Write Buffer Programming Operation

19.8.1 Unlock Bypass Command Sequence

The unlock bypass feature allows the system to primarily program to the device faster than using the standard word program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time.

During the unlock bypass mode, only the Unlock Bypass Program command is valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h. The second cycle need only contain the data 00h. The device then returns to the read mode.

19.9 Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. The Command Definitions table shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, the device returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7 or DQ6/DQ2. Refer to the Write Operation Status section for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

Figure 20.4 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations table in the AC Characteristics section for parameters and timing diagrams.

19.10 Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. The Command Definitions table shows the address and data requirements for the sector erase command sequence.

The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of no less than 50 µs occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than

t_{SEA}. Any sector erase address and command following the exceeded time-out may or may not be accepted. Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to the read mode.

The system can monitor DQ3 to determine if the sector erase timer has timed out (See DQ3: Sector Erase Timer.) The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by reading DQ7 or DQ6/DQ2. Refer to the Write Operation Status section for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a hardware reset immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

Figure 20.4 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations table in the Erase/Program Operations section for parameters and timing diagrams.

19.10.1 Accelerated Sector Erase

Under certain conditions, the device can erase sectors in parallel. This method of erasing sectors is faster than the standard sector erase command sequence. Table 19.6lists the sectors.

The accelerated sector erase function must not be used more than 100 times per sector. In addition, accelerated sector erase should be performed at room temperature 30°C (+/-) 5°C.

Use the following procedure to perform accelerated sector erase:

1. Unlock all sectors in a sector to be erased using the sector lock/unlock command sequence. All sectors that remain locked will not be erased.
2. Apply 9 V to the ACC input. This voltage must be applied at least 1 µs before executing step 3.
3. Write 80h to any address within a sector to be erased.
4. Write 30h to any address within a sector to be erased.
5. Monitor status bits DQ2/DQ6 or DQ7 to determine when erasure is complete, just as in the standard erase operation. See the Write Operation Status section for further details.
6. Lower ACC from 9 V to V_{CC}.
7. Relock sectors as required.

20 Erase Suspend/Erase Resume Commands

Notes:
1. *See the Command Definitions table for erase command sequence.*
2. *See the section on DQ3 for information on the sector erase timer.*

Figure 20.4 Erase Operation

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the minimum t_{SEA} time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of t_{ESL} (Erase Suspend Latency) to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the device enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device *erase suspends* all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See Write Operation Status for information on these status bits.

After an erase-suspended program operation is complete, the device returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See Write Operation Status for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. See Write Buffer Programming Operation and Autoselect Command Sequence for details. To resume the sector erase operation, the system must write the Erase Resume command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

20.1 Program Suspend/Program Resume Commands

The Program Suspend command allows the system to interrupt a embedded programming operation or a *Write to Buffer* programming operation so that data can read from any non-suspended sector. When the Program Suspend command is written during a programming process, the device halts the programming operation within t_{PSL} (Program Suspend Latency) and updates the status bits. Addresses are *don't-cares* when writing the Program Suspend command.

After the programming operation has been suspended, the system can read array data from any non-suspended sector. The Program Suspend command may also be issued during a programming operation while an erase is suspended. In this case, data may be read from any addresses not in Erase Suspend or Program Suspend. If a read is needed from the SecSi Sector area (One Time Program area), then user must use the proper command sequences to enter and exit this region. The system may also write the autoselect command sequence when the device is in Program Suspend mode. The device allows reading autoselect codes in the suspended sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to Program Suspend mode, and is ready for another valid operation. See Autoselect Command Sequence for more information.

After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See Write Operation Status for more information. The system must write the Program Resume command (address bits are *don't care*) to exit the Program Suspend mode and continue the programming operation. Further writes of the Program Resume command are ignored. Another Program Suspend command can be written after the device has resume programming.

20.2 Volatile Sector Protection Command Set

The Volatile Sector Protection Command Set permits the user to set the Dynamic Protection Bit (DYB), clear the Dynamic Protection Bit (DYB), and read the logic state of the Dynamic Protection Bit (DYB).

The **Volatile Sector Protection Command Set Entry** command sequence must be issued prior to any of the commands listed following to enable proper command execution. Note that issuing the **Volatile Sector Protection Command Set Entry** command disables reads and writes for the device with the command.

- **DYB Set Command**
- **DYB Clear Command**
- **DYB Status Read Command**

The DYB Set/Clear command is used to set or clear a DYB for a given sector. The address bits are issued at the same time as the code 00h or 01h on DQ7-DQ0. All other DQ data bus pins are ignored during the data write cycle. The DYBs are modifiable at any time, regardless of the state of the PPB or PPB Lock Bit. The DYBs are cleared (erased to '1') at power-up or hardware reset and are thus in an unprotected state.

The programming state of the DYB for a given sector can be verified by writing a DYB Status Read Command to the device.

The **Volatile Sector Protection Command Set Exit** command must be issued after the execution of the commands listed previously to reset the device to read mode. Otherwise the device will hang.

Note that issuing the **Volatile Sector Protection Command Set Exit** command re-enables reads and writes for the device.

21 Command Definitions

Command Sequence (Note 1)		Cycles	Bus Cycles (Notes 1–6)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Asynchronous Read (7)		1	RA	RD										
Reset (8)		1	XXX	F0										
Autoselect (9)	Manufacturer ID	4	555	AA	2AA	55	555	90	X00	0001				
	Device ID (10)	6	555	AA	2AA	55	555	90	X01	(11)	X0E	(10)	X0F	(10)
	Indicator Bits	4	555	AA	2AA	55	555	90	X03	(11)				
Program		4	555	AA	2AA	55	555	A0	PA	Data				
Write to Buffer (18)		6	555	AA	2AA	55	SA	25	PA	WC	PA	PD	WBL	PD
Program Buffer to Flash		1	SA	29										
Write to Buffer Abort Reset (22)		3	555	AA	2AA	55	555	F0						
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase Suspend (15)		1	XXX	B0										
Erase Resume (15)		1	XXX	30										
Set Configuration Register (16)		4	555	AA	2AA	55	555	D0	X00 or X01	CR				
Read Configuration Register (17)		4	555	AA	2AA	55	555	C6	X00 or X01	CR				
Unlock Bypass Mode	Unlock Bypass Entry (21)	3	555	AA	2AA	55	555	20						
	Unlock Bypass Program (12, 13)	2	XX	A0	PA	PD								
	Unlock Bypass Reset	2	XX	90	XXX	00								
Volatile Sector Protection Command Set Definitions														
DYB	Volatile Sector Protection Command Set Entry	3	555	AA	2AA	55	555	E0						
	DYB Set	2	XX	A0	SA	00								
	DYB Clear	2	XX	A0	SA	01								
	DYB Status Read	1	SA	RD(0)										
	Volatile Sector Protection Command Set Exit	2	XX	90	XX	00								

Legend:
X = Don't care
RA = Address of the memory location to be read.
RD = Data read from location RA during read operation.
PA = Address of the memory location to be programmed. Addresses latch on the rising edge of the AVD# pulse or active edge of CLK which ever comes first.
PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.
SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits A24–A14 for the RS512N uniquely select any sector.
CR = Configuration Register data bits D15–D0.
WBL = Write Buffer Location. Address must be within the same write buffer page as PA.
WC = Word Count. Number of write buffer locations to load minus 1.

Notes:
1. *See Table 18.1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the following, all bus cycles are write cycle: read cycle, fourth through sixth cycles of the Autoselect commands, fourth cycle of the configuration register verify command, and any cycle reading at RD(0) and RD(1).*
4. *Data bits DQ15–DQ8 are don't care in command sequences, except for RD, PD, and WD.*
5. *Unless otherwise noted, address bits Amax–A12 are don't cares.*
6. *Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. The system must write the reset command to return the device to reading array data.*
7. *No unlock or command cycles required when device is reading array data.*
8. *The Reset command is required to return to reading array data (or to the erase-suspend-read mode if previously in Erase Suspend) when device is in the autoselect mode, or if DQ5 goes high (while the device is providing status information) or performing sector lock/unlock.*
9. *The fourth cycle of the autoselect command sequence is a read cycle. See the Autoselect Command Sequence* section.
10. *512 Mb: 0Eh = 29h and 0Fh = 01h.*
11. *See the Autoselect Command Sequence section.*
12. *The Unlock Bypass command sequence is required prior to this command sequence.*
13. *The Unlock Bypass Reset command is required to return to reading array data when the device is in the unlock bypass mode.*
14. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
15. *The Erase Resume command is valid only during the Erase Suspend mode*
16. *See the Set Configuration Register Command Sequence section.*
17. *See the Read Configuration Register Command Sequence section which further provides information on Reset Command to Configure the Configuration Register.*
18. *The total number of cycles in the command sequence is determined by the number of words written to the write buffer. The maximum number of cycles in the command sequence is 37.*
19. *ACC must be at V_{HH} during the entire operation of this command*
20. *Command sequence resets device for next command after write-to-buffer operation.*
21. *Entry commands are needed to enter a specific mode to enable instructions only available within that mode.*
22. *Write Buffer Programming can be initiated after Unlock Bypass Entry.*

22 Write Operation Status

The device provides several bits to determine the status of a program or erase operation: DQ1, DQ2, DQ3, DQ5, DQ6, and DQ7. Table 22.13 and the following subsections describe the function of these bits. DQ7 and DQ6 each offers a method for determining whether a program or erase operation is complete or in progress.

22.1 DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence. **Note that the Data# Polling is valid only for the last word being programmed in the write-buffer-page during Write Buffer Programming. Reading Data# Polling status on any word other than the last word to be programmed in the write-buffer-page will return false status information.**

During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately t_{PSP}, then the device returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a *0* on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a *1* on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately t_{ASP}, then the device returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ6–DQ0 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ6-DQ0 may be still invalid. Valid data on DQ7-D00 will appear on successive read cycles.

Table 22.13 shows the outputs for Data# Polling on DQ7. Figure 22.5 shows the Data# Polling algorithm. Figure 25.13 in the AC Characteristics section shows the Data# Polling timing diagram.

Notes:

1. *VA = Valid adntsbdress for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = 1 because DQ7 may change simultaneously with DQ5.*

Figure 22.5 Data# Polling Algorithm

22.2 DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address in the device, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately t_{ASP} (All Sectors Protected toggle time), then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately t_{PSP} after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

See the following for additional information: Figure 22.6, Figure 25.14 (toggle bit timing diagram), and Table 22.12.

Toggle Bit I on DQ6 requires either OE# or CE# to be deasserted and reasserted to show the change in state.

Note: *The system should recheck the toggle bit even if DQ5 = 1 because the toggle bit may stop toggling as DQ5 changes to 1. See the subsections on DQ6 and DQ2 for more information.*

Figure 22.6 Toggle Bit Algorithm

DQ2: Toggle Bit II

The *Toggle Bit II* on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. But DQ2 by itself cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 22.12 to compare outputs for DQ2 and DQ6.

See Figure 22.6 and Figure 25.14 for additional information.

22.3 Reading Toggle Bits DQ6/DQ2

Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle. (See Figure 22.6)

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation.

22.4 DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a *1*, indicating that the program or erase cycle was not successfully completed.

The device may output a *1* on DQ5 if the system tries to program a *1* to a location that was previously programmed to *0* Only an erase operation can change a *0* back to a *1*. Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a *1*.

Under both these conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if the device was previously in the erase-suspend-program mode).

22.5 DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a *0* to a *1*. If the time between additional sector erase commands from the system can be assumed to be less than t_{SEA}, the system need not monitor DQ3. See also the Sector Erase Command Sequence section.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is *1*, the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is *00* the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 22.13 shows the status of DQ3 relative to the other status bits.

22.6 DQ1: Write to Buffer Abort

DQ1 indicates whether a Write to Buffer operation was aborted. Under these conditions DQ1 produces a '1'. The system must issue the Write to Buffer Abort Reset command sequence to return the device to reading array data. See the Write Buffer Programming Operation section for more details.

3.
4. *DQ1 indicates the Write to Buffer ABORT status during Write Buffer Programming operations.*
5. *The data-bar polling algorithm should be used for Write Buffer Programming operations. Note that DQ7# during Write Buffer Programming indicates the data-bar for DQ7 data* ***for the LAST LOADED WRITE-BUFFER ADDRESS location****.*

ACC (Note 2) . . . . –0.5 V to +9.5 V

6. *Minimum DC input voltage on pin ACC is -0.5V. During voltage transitions, ACC may overshoot*

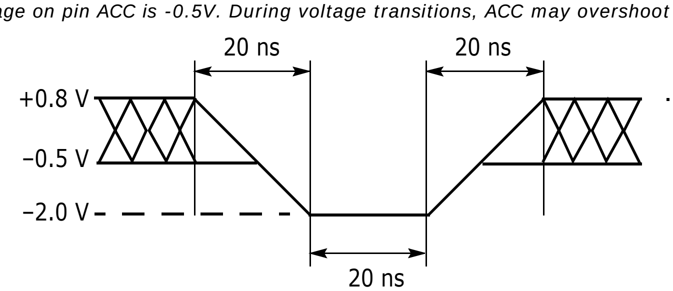


Table 22.1 Maximum Negative Overshoot Waveform

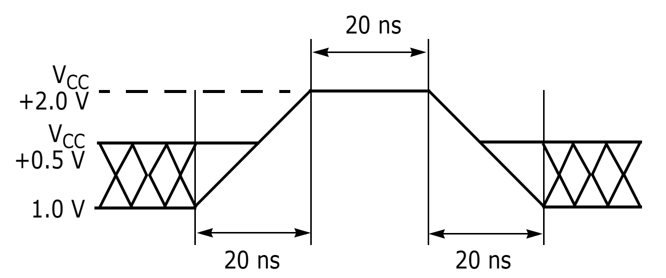


Figure 22.7 Maximum Positive Overshoot Waveform

23 DC Characteristics

23.1 CMOS Compatible

Parameter	Description	Test Conditions (Note 1)		Min	Typ (Note 7)	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}max$				±1	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}max$				±1	µA
I_{CCB}	V_{CC} Active burst Read Current	CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}, burst length = 8	80 MHz		30	66	mA
			66 MHz		28	60	
			54 MHz		27	54	
		CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}, burst length = 16	80 MHz		32	60	mA
			66 MHz		30	54	
			54 MHz		28	48	
		CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}, burst length = 32	80 MHz		34	54	mA
			66 MHz		32	48	
			54 MHz		29	42	
		CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}, burst length = Continuous	80 MHz		38	48	mA
			66 MHz		35	42	
			54 MHz		22	36	
I_{CC1}	V_{CC} Active Asynchronous Read Current (Note 2)	CE# = V_{IL}, OE# = V_{IH}, WE# = V_{IH}	10 MHz		27	36	mA
			5 MHz		13	18	mA
			1 MHz		3	4	mA
I_{CC2}	V_{CC} Active Write Current (Note 3)	CE# = V_{IL}, OE# = V_{IH}, ACC = V_{IH}	V_{CC}		<35	<50	mA
			V_{ACC}		20	30	µA
I_{CC3}	V_{CC} Standby Current (Note 6)	CE# = RESET# = $V_{CC} \pm 0.2$ V	V_{CC}		20	40	µA
			V_{ACC}		10	15	µA
I_{CC4}	V_{CC} Reset Current	RESET# = V_{IL}, CLK = V_{IL}			70	150	µA
I_{CC6}	V_{CC} Sleep Current	CE# = V_{IL}, OE# = V_{IH}			20	40	µA
I_{ACC}	Accelerated Program Current (Note 5)	CE# = V_{IL}, OE# = V_{IH}, V_{ACC} = 9.5 V	V_{CC}		<30	<40	mA
			V_{ACC}		<15	<20	mA
V_{IL}	Input Low Voltage			−0.5		0.4	V
V_{IH}	Input High Voltage			$V_{CC} - 0.4$		$V_{CC} + 0.4$	
V_{OL}	Output Low Voltage	I_{OL} = 100 µA, $V_{CC} = V_{CC}$ min				0.1	V
V_{OH}	Output High Voltage	I_{OH} = −100 µA, $V_{CC} = V_{CC}$ min		$V_{CC} - 0.1$			V
V_{HH}	Voltage for Accelerated Program			8.5		9.5	V
V_{LKO}	Low V_{CC} Lock-out Voltage			1.0		1.4	V

Notes:

1. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}$ max.*
2. *The I_{CC} current listed is typically less than 2-3 mA/MHz, with OE# at V_{IH}.*
3. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
4. *Device enters automatic sleep mode when addresses are stable for t_{ACC} + 20 ns. Typical sleep mode current is equal to I_{CC3}.*
5. *Total current during accelerated programming is the sum of V_{ACC} and V_{CC} currents.*
6. *$U_{IH} = V_{CC} \pm 0.2$ V and V_{IL} > -.1 V*
7. *Typical test conditions of room temperature and 1.8 V V_{CC}.*

24 Test Conditions

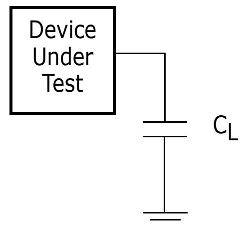
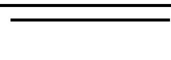
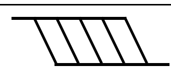
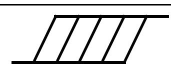
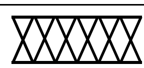
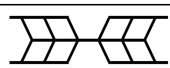


Figure 24.1 Test Setup

Table 24.1 Test Specifications

Test Condition	All Speed Options	Unit
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	2.5	ns
Input Pulse Levels	0.0–V_{CC}	V
Input timing measurement reference levels	$V_{CC}/2$	V
Output timing measurement reference levels	$V_{CC}/2$	V

Figure 24.2 Input Waveforms and Measurement Levels

Waveform	Inputs	Outputs
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don’t Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

25 AC Characteristics

25.1 V_{CC} Power-up

Parameter	Description	Test Setup	Speed	Unit
t_{VCS}	V_{CC} Setup Time	Min	1	ms

Notes:

1. *V_{CC} >= V_{IO} - 100mV and V_{CC} ramp rate is > 1V / 100µs*
2. *V_{CC} ramp rate <1V / 100µs, a Hardware Reset will be required.*

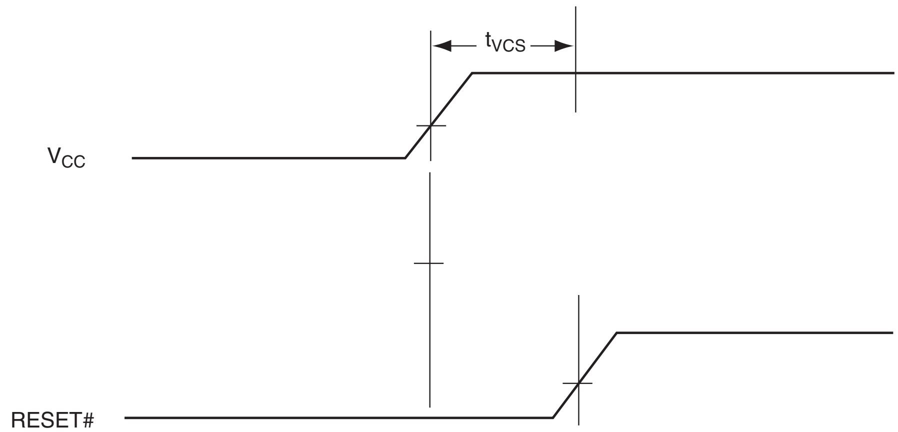


Figure 25.1 V_{CC} Power-up Diagram

25.2 CLK Characterization

Parameter	Description		80 MHz	66 MHz	54 MHz	Unit
f_{CLK}	CLK Frequency	Max	80	66	54	MHz
t_{CLK}	CLK Period	Min	12.5	15.1	18.5	ns
t_{CH}	CLK High Time	Min	3.5	6.1	7.40	ns
t_{CL}	CLK Low Time					
t_{CR}	CLK Rise Time	Max	2	3	3	ns
t_{CF}	CLK Fall Time					

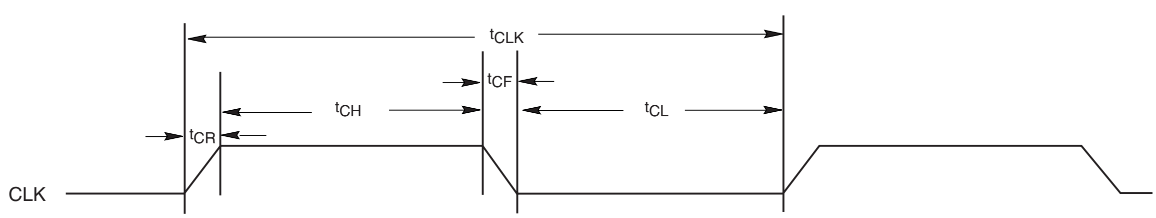


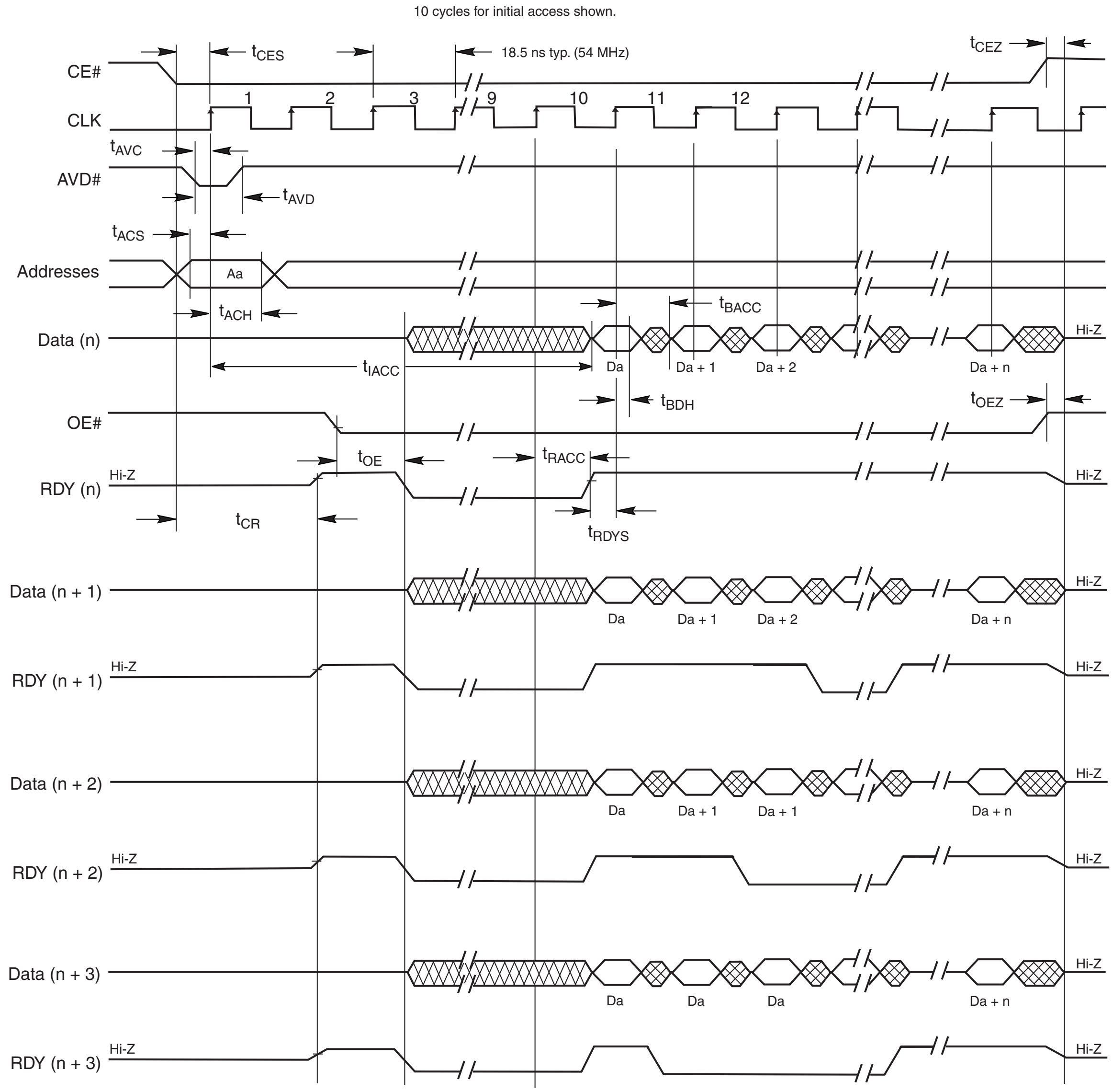
Figure 25.2 CLK Characterization

25.3 Synchronous/Burst Read

Parameter		Description		80 MHz	66 MHz	54 MHz	Unit
JEDEC	Standard						
	t_{IACC}	Latency	Max	148			ns
	t_{BACC}	Burst Access Time Valid Clock to Output Delay	Max	9.1	11.2	13.5	ns
	t_{ACS}	Address Setup Time to CLK (Note 1)	Min	4	4	5	ns
	t_{ACH}	Address Hold Time from CLK (Note 1)	Min	2	2	3	ns
	t_{BDH}	Data Hold Time from Next Clock Cycle	Min	4	4	5	ns
	t_{CR}	Chip Enable to RDY Valid	Max	9.1	11.2	13.5	ns
	t_{OE}	Output Enable to Output Valid	Max	9.1	11.2	13.5	ns
	t_{CEZ}	Chip Enable to High Z (Note 2)	Max	10	10	10	ns
	t_{OEZ}	Output Enable to High Z (Note 2)	Max	10	10	10	ns
	t_{CES}	CE# Setup Time to CLK	Min	4	4	4	ns
	t_{RDYS}	RDY Setup Time to CLK	Min	4	4	5	ns
	t_{RACC}	Ready Access Time from CLK	Max	9.1	11.2	13.5	ns
	t_{AAS}	Address Setup Time to AVD# (Note 1)	Min	4	4	5	ns
	t_{AAH}	Address Hold Time to AVD# (Note 1)	Min	2	2	3	ns
	t_{CAS}	CE# Setup Time to AVD#	Min	0	0	0	ns
	t_{AVC}	AVD# Low to CLK	Min	4	4	4	ns
	t_{AVD}	AVD# Pulse	Min	8	8	8	ns

Notes:

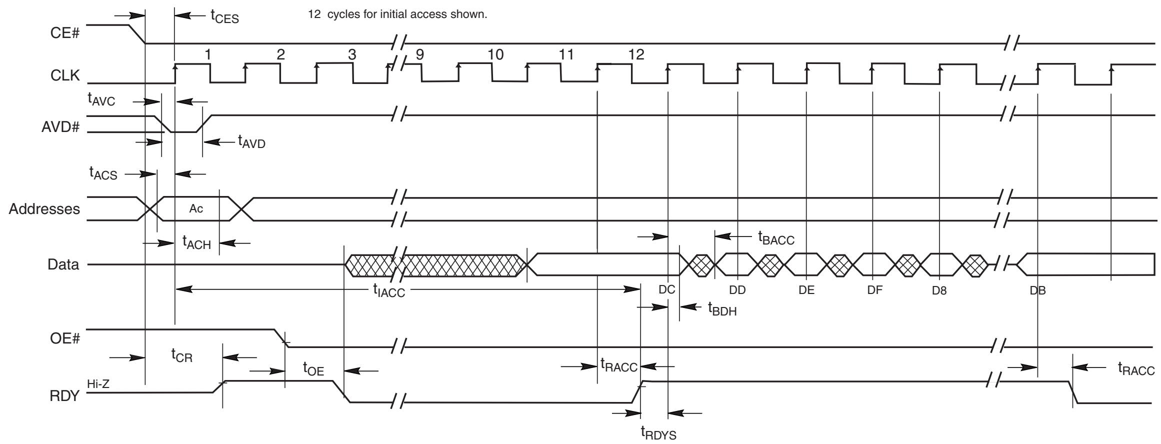
1. *Addresses are latched on the first rising edge of CLK.*
2. *Not 100% tested.*



Notes:

1. *Figure shows total number of wait states set to ten cycles. The total number of wait states can be programmed from three cycles to thirteen cycles.*
2. *If any burst address occurs at* address + 1, address + 2, ..., *or* address + 7, *additional clock delay cycles are inserted, and are indicated by RDY.*
3. *The device is in synchronous mode.*
4. *In order for the device to operate at 80Mhz/66Mhz/54Mhz, there is an additional wait state latency of 2/1/0 accordingly, every 4 clock cycles with the first data being read.*

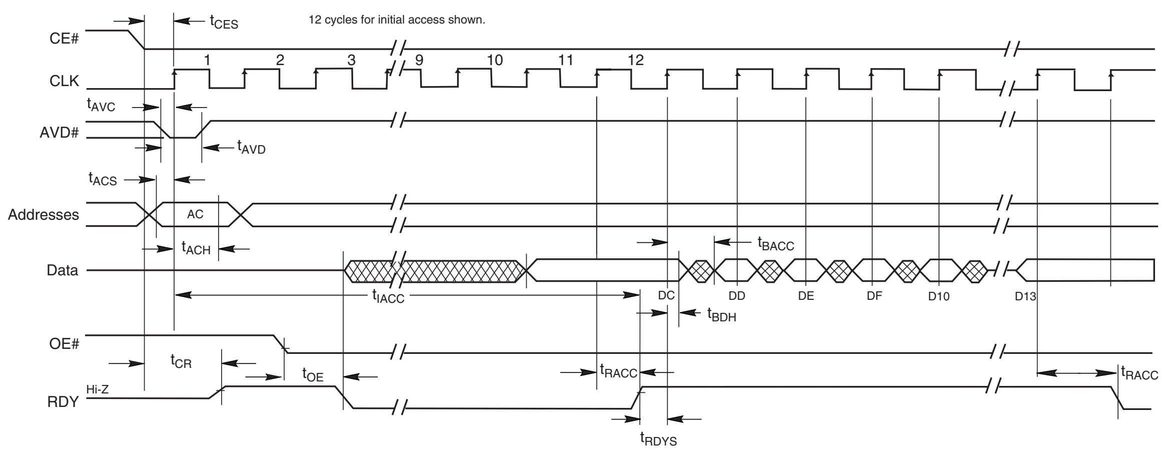
Figure 25.3 CLK Synchronous Burst Mode Read



Notes:

1. *Figure shows total number of wait states set to twelve cycles. The total number of wait states can be programmed from three cycles to thirteen cycles. Clock is set for active rising edge.*
2. *If any burst address occurs at* address + 1, address + 2, ..., *or* address + 7, *additional clock delay cycles are inserted, and are indicated by RDY. The device is in synchronous mode with wrap around.*
3. *In order for the device to operate at 80Mhz/66Mhz/54Mhz, there is an additional wait state latency of 2/1/0 accordingly, every 4 clock cycles with the first data being read.*
4. *D8–DF in data waveform indicate the order of data within a given 8-word address range, from lowest to highest. Starting address in figure is the 4th address in range (O-F).*

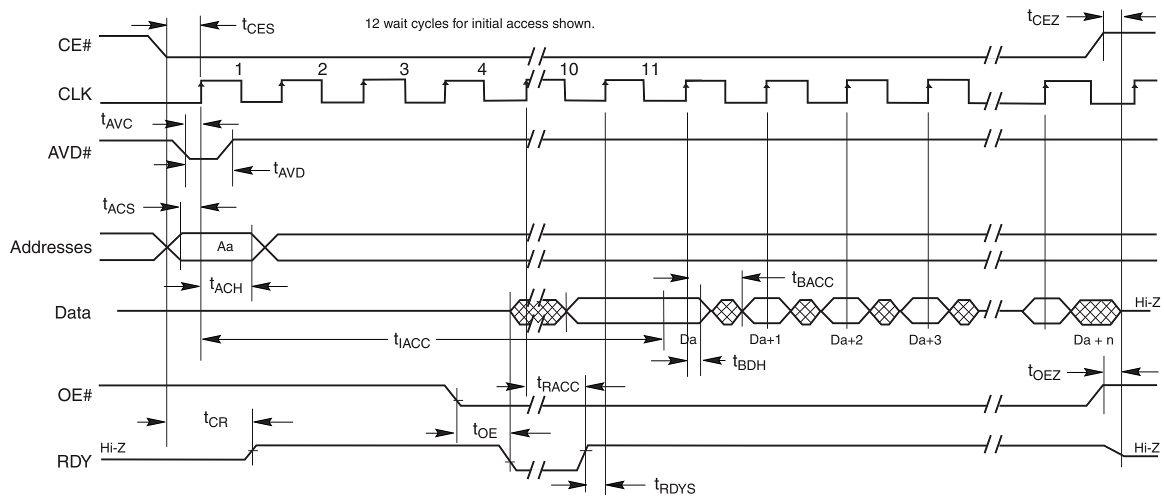
Figure 25.4 8-word Linear Burst with Wrap Around



Notes:

1. *Figure shows total number of wait states set to twelve cycles. The total number of wait states can be programmed from three cycles to thirteen cycles. Clock is set for active rising edge.*
2. *If any burst address occurs at* address + 1, address + 2, ..., *or* address + 7, *additional clock delay cycles are inserted, and are indicated by RDY.*
3. *In order for the device to operate at 80Mhz/66Mhz/54Mhz, there is an additional wait state latency of 2/1/0 accordingly, every 4 clock cycles with the first data being read.*
4. *DC–D13 in data waveform indicate the order of data within a given 8-word address range, from lowest to highest. Starting address in figure is the 4th address in range (C-13).*

Figure 25.5 8-word Linear Burst without Wrap Around



Notes:

1. *Figure assumes eleven wait states for initial access and synchronous read.*
2. *The Set Configuration Register command sequence has been written with A18=0; device will output RDY one cycle before valid data.*

Figure 25.6 Burst with RDY Set One Cycle Before Data

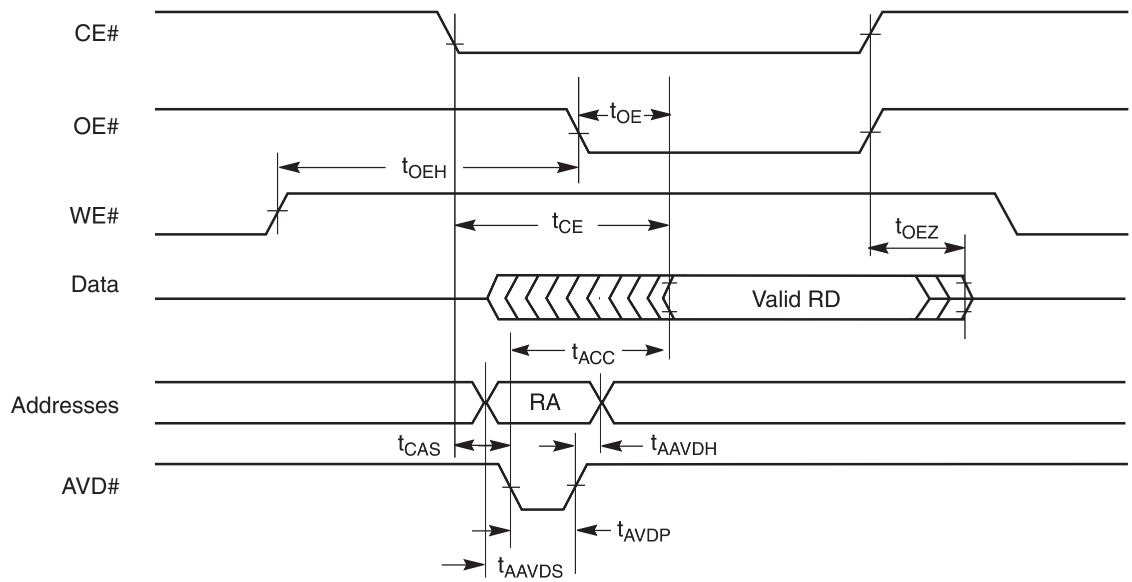
25.4 Asynchronous Mode Read @ VIO = 1.8 V

<table>
<tr><th colspan="2">Parameter</th><th colspan="2" rowspan="2">Description</th><th rowspan="2"></th><th rowspan="2">80 MHz</th><th rowspan="2">66 MHz</th><th rowspan="2">54 MHz</th><th rowspan="2">Unit</th></tr>
<tr><th>JEDEC</th><th>Standard</th></tr>
<tr><td></td><td>t_{CE}</td><td colspan="2">Access Time from CE# Low</td><td>Max</td><td colspan="3">148</td><td>ns</td></tr>
<tr><td></td><td>t_{ACC}</td><td colspan="2">Asynchronous Access Time (Note 1)</td><td>Max</td><td colspan="3">143</td><td>ns</td></tr>
<tr><td></td><td>t_{AVDP}</td><td colspan="2">AVD# Low Time</td><td>Min</td><td>8</td><td>8</td><td>10</td><td>ns</td></tr>
<tr><td></td><td>t_{AAVDS}</td><td colspan="2">Address Setup Time to Rising Edge of AVD#</td><td>Min</td><td>4</td><td>4</td><td>5</td><td>ns</td></tr>
<tr><td></td><td>t_{AAVDH}</td><td colspan="2">Address Hold Time from Rising Edge of AVD#</td><td>Min</td><td>2</td><td>2</td><td>3</td><td>ns</td></tr>
<tr><td></td><td>t_{OE}</td><td colspan="2">Output Enable to Output Valid</td><td>Max</td><td>9.1</td><td>11.2</td><td>13.5</td><td>ns</td></tr>
<tr><td rowspan="2"></td><td rowspan="2">t_{OEH}</td><td rowspan="2">Output Enable Hold Time</td><td>Read</td><td>Min</td><td>0</td><td>0</td><td>0</td><td>ns</td></tr>
<tr><td>Data# Polling</td><td>Min</td><td>10</td><td>10</td><td>10</td><td>ns</td></tr>
<tr><td></td><td>t_{OEZ}</td><td colspan="2">Output Enable to High Z (Note 2)</td><td>Max</td><td>10</td><td>10</td><td>10</td><td>ns</td></tr>
<tr><td></td><td>t_{CAS}</td><td colspan="2">CE# Setup Time to AVD#</td><td>Min</td><td>0</td><td>0</td><td>0</td><td>ns</td></tr>
</table>

Notes:

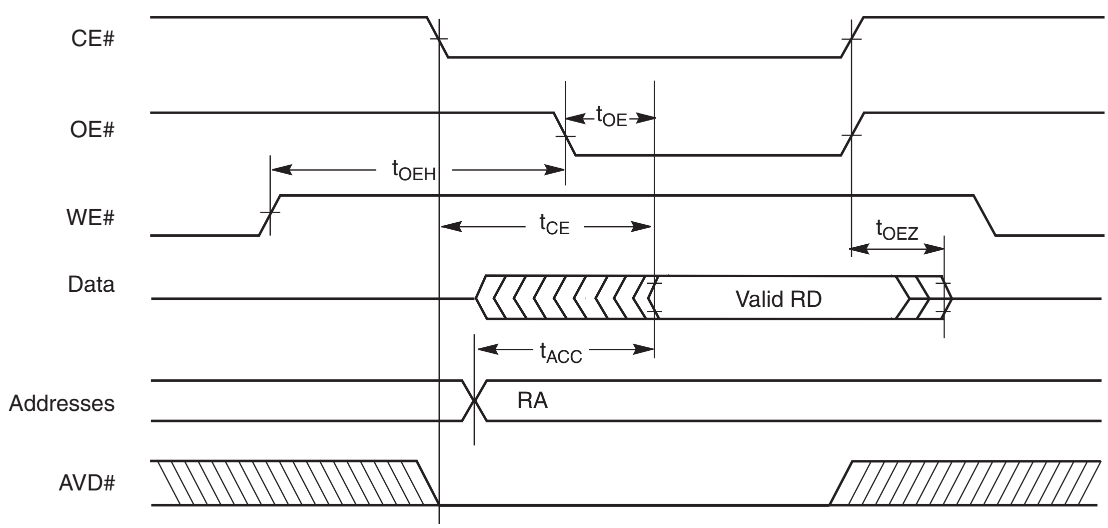
1. *Asynchronous Access Time is from the last of either stable addresses or the falling edge of AVD#.*
2. *Not 100% tested.*

25.5 Timing Diagrams



Note: *RA = Read Address, RD = Read Data.*

Figure 25.7 Asynchronous Mode Read with Latched Addresses



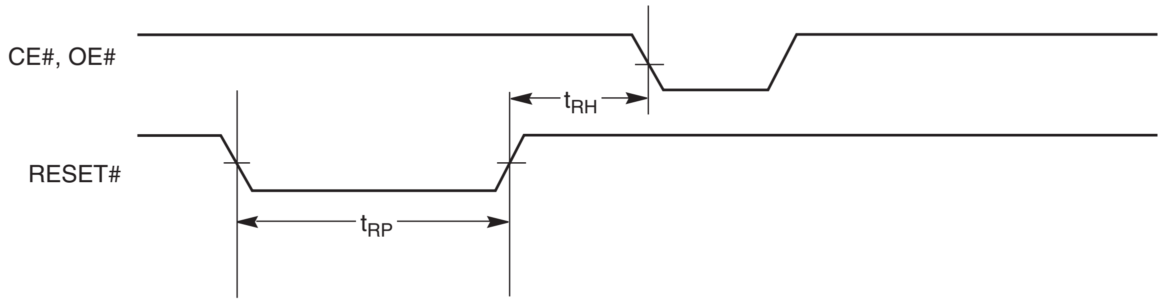
Note: *RA = Read Address, RD = Read Data.*

Figure 25.8 Asynchronous Mode Read

25.6 Hardware Reset (RESET#)

Parameter		Description		All Speeds	Unit
JEDEC	Std				
	t_{RP}	RESET# Pulse Width	Min	30	µs
	t_{RH}	Reset High Time Before Read to Read Mode	Min	300	µs
	t_{RPD}	RESET# Low to Standby Mode	Min	20	µs

Note: *Not 100% tested.*



Reset Timings

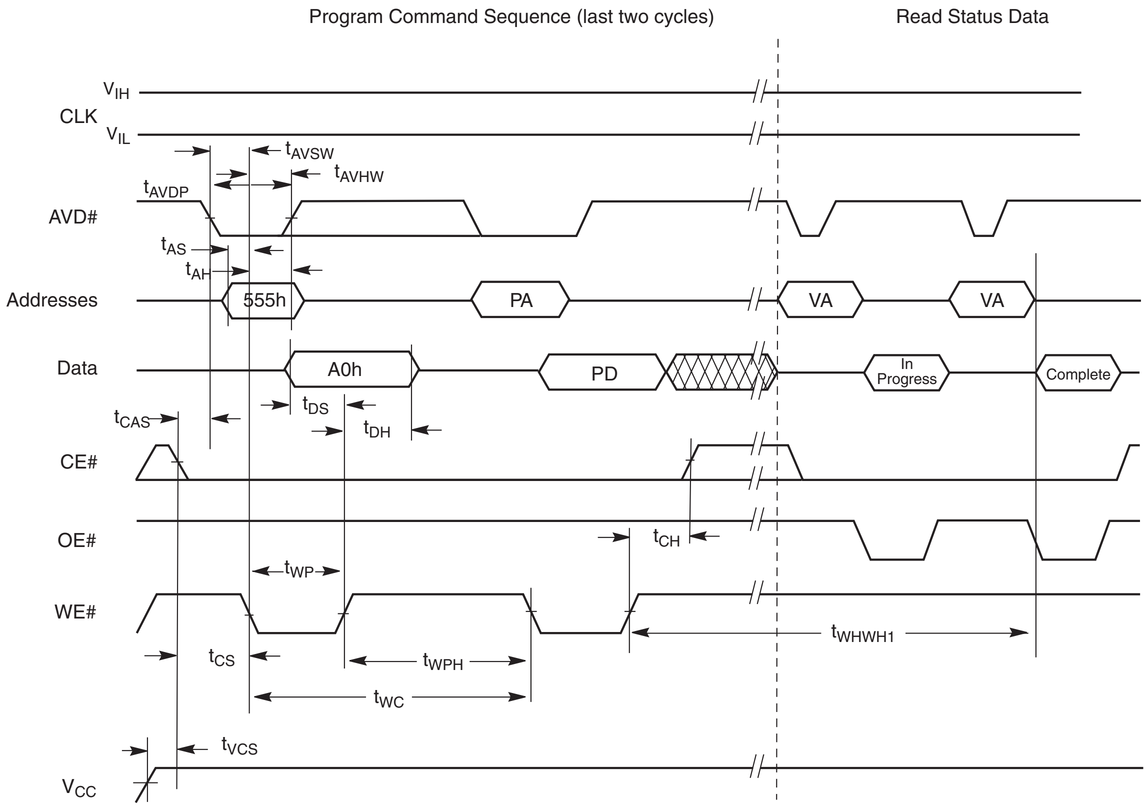
Figure 25.9 Reset Timings

25.7 Erase/Program Operations

Parameter JEDEC	Parameter Standard	Description			80 MHz	66 MHz	54 MHz	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	70			ns
t_{AVWL}	t_{AS}	Address Setup Time (Notes 2, 3)	Synchronous	Min	5			ns
			Asynchronous		0	0	0	
t_{WLAX}	t_{AH}	Address Hold Time (Notes 2, 3)	Synchronous	Min	2	2	3	ns
			Asynchronous		0	0	0	
	t_{AVDP}	AVD# Low Time		Min	8	8	8	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	20	20	25	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0	0	0	ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write		Min	0	0	0	ns
	t_{CAS}	CE# Setup Time to AVD#		Min	0	0	0	ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	30			ns
t_{WHWL}	t_{WPH}	Write Pulse Width Highs		Min	20	20	25	ns
	$t_{SR/W}$	Latency Between Read and Write Operations		Min	0	0	0	ns
	t_{VID}	V_{ACC} Rise and Fall Time		Min	500			ns
	t_{VIDS}	V_{ACC} Setup Time (During Accelerated Programming)		Min	1			µs
	t_{VCS}	V_{CC} Setup Time		Min	50			µs
t_{ELWL}	t_{CS}	CE# Setup Time to WE#		Min	5			ns
	t_{AVSW}	AVD# Setup Time to WE#		Min	5			ns
	t_{AVHW}	AVD# Hold Time to WE#		Min	2	2	3	ns
	t_{AVSC}	AVD# Setup Time to CLK		Min	5			ns
	t_{AVHC}	AVD# Hold Time to CLK		Min	2	2	3	ns
	t_{CSW}	Clock Setup Time to WE#		Min	5			ns
	t_{WEP}	Noise Pulse Margin on WE#		Max	3			ns
	t_{SEA}	Sector Erase Accept Time-out		Max	50			µs
	t_{ESL}	Erase Suspend Latency		Max	20			µs
	t_{PSL}	Program Suspend Latency		Max	20			µs
	t_{ASP}	Toggle Time During Sector Protection		Typ	100			µs
	t_{PSP}	Toggle Time During Programming Within a Protected Sector		Typ	1			µs

Notes:

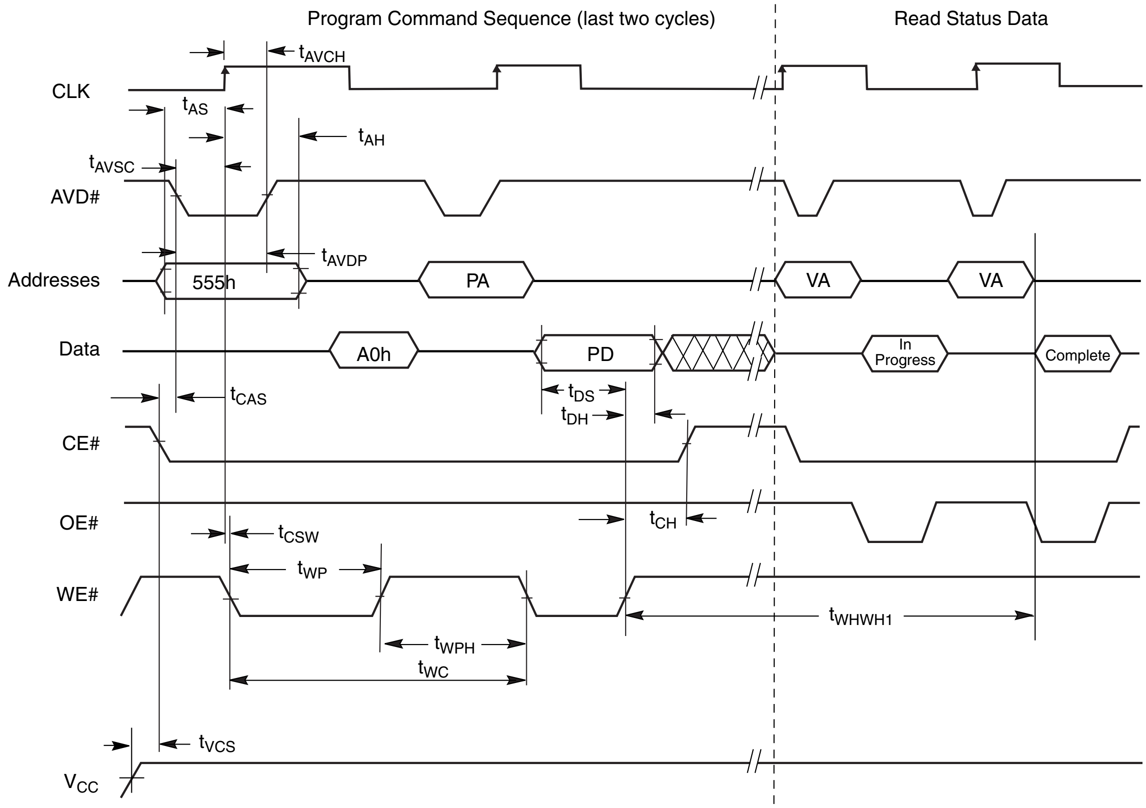
1. *Not 100% tested.*
2. *Asynchronous read mode allows Asynchronous program operation only. Synchronous read mode allows both Asynchronous and Synchronous program operation.*
3. *In asynchronous program operation timing, addresses are latched on the falling edge of WE#. In synchronous program operation timing, addresses are latched on the rising edge of CLK.*
4. *See the Erase and Programming Performance section for more information. Does not include the preprogramming time.*



Notes:

1. *PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.*
2. In progress *and* complete *refer to status of program operation.*
3. *Amax–A14 are don't care during command sequence unlock cycles.*
4. *CLK can be either* V_{IL} *or* V_{IH}*.*
5. *The Asynchronous programming operation is independent of the Set Device Read Mode bit in the Configuration Register.*

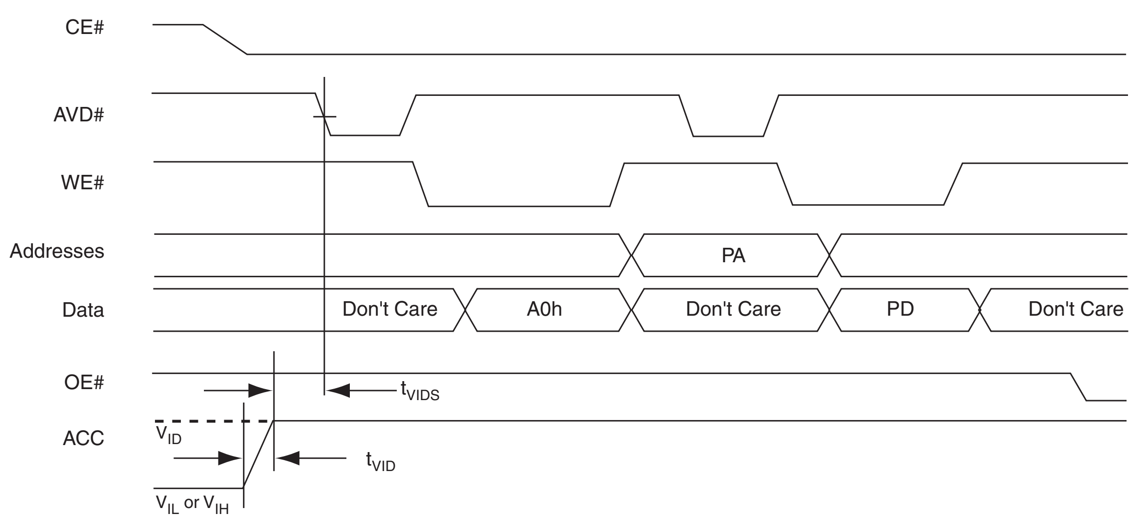
Figure 25.10 Asynchronous Program Operation Timings: WE# Latched Addresses



Notes:

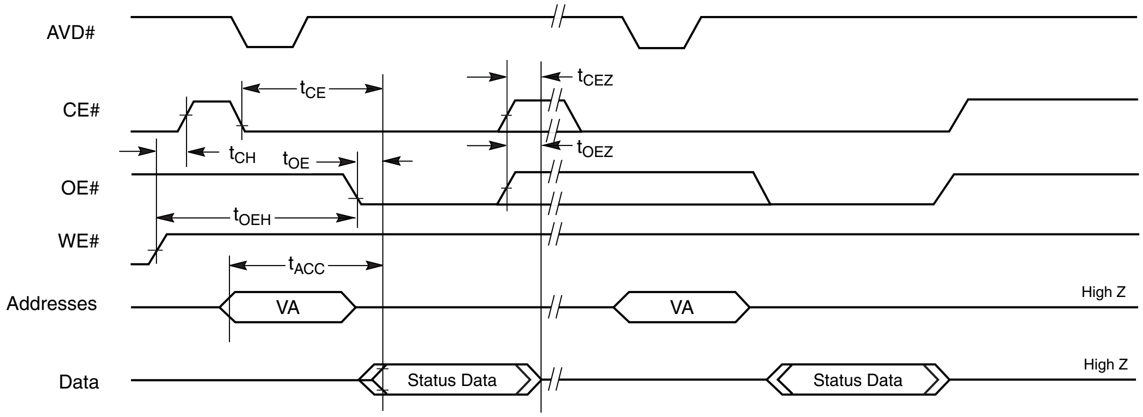
1. *PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.*
2. In progress *and* complete *refer to status of program operation.*
3. *Amax9–A14 are don't care during command sequence unlock cycles.*
4. *Addresses are latched on the rising edge of CLK.*
5. *Either CE# or AVD# is required to go from low to high in between programming command sequences.*
6. *The Synchronous programming operation is dependent of the Set Device Read Mode bit in the Configuration Register. The Configuration Register must be set to the Synchronous Read Mode.*

Figure 25.11 Synchronous Program Operation Timings: CLK Latched Addresses



Note: *Use setup and hold times from conventional program operation.*

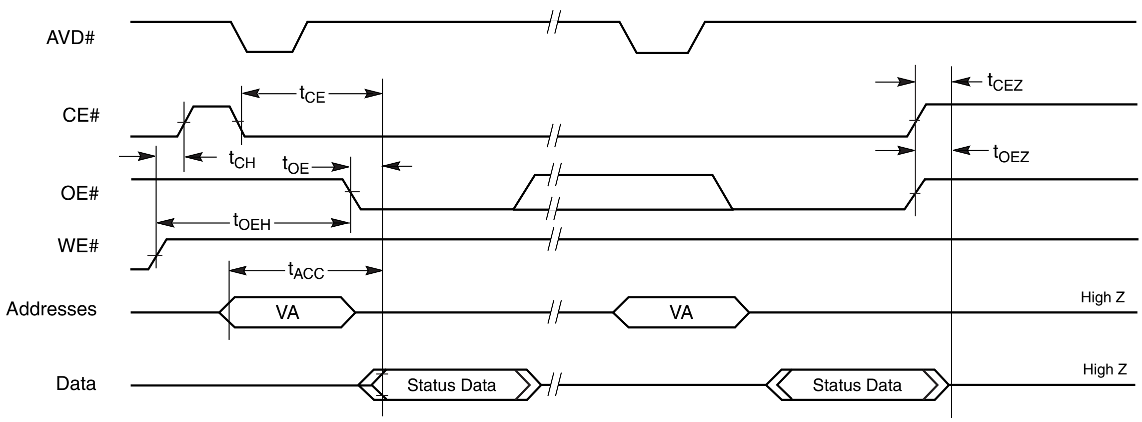
Figure 25.12 Accelerated Unlock Bypass Programming Timing



Notes:

1. *Status reads in figure are shown as asynchronous.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is completeData# Polling will output true data.*

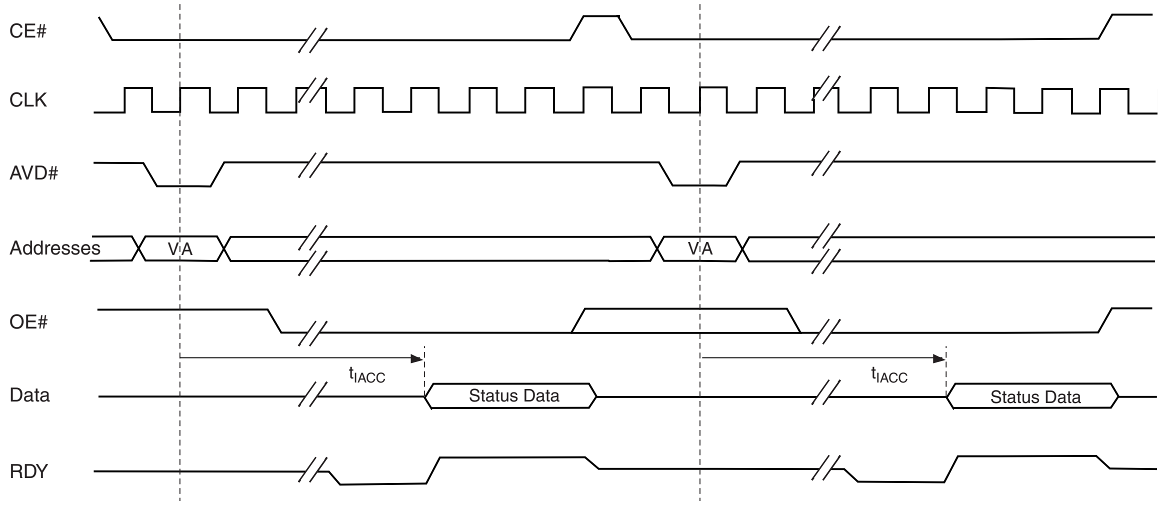
Figure 25.13 Data# Polling Timings (During Embedded Algorithm)



Notes:

1. *Status reads in figure are shown as asynchronous.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, .*

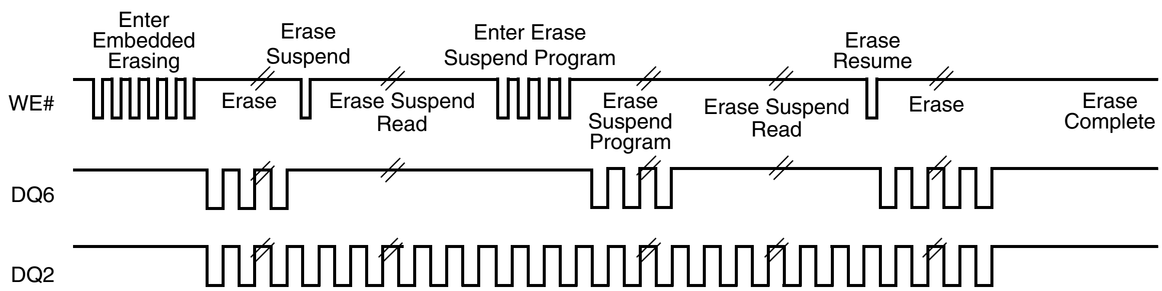
Figure 25.14 Toggle Bit Timings (During Embedded Algorithm)



Notes:

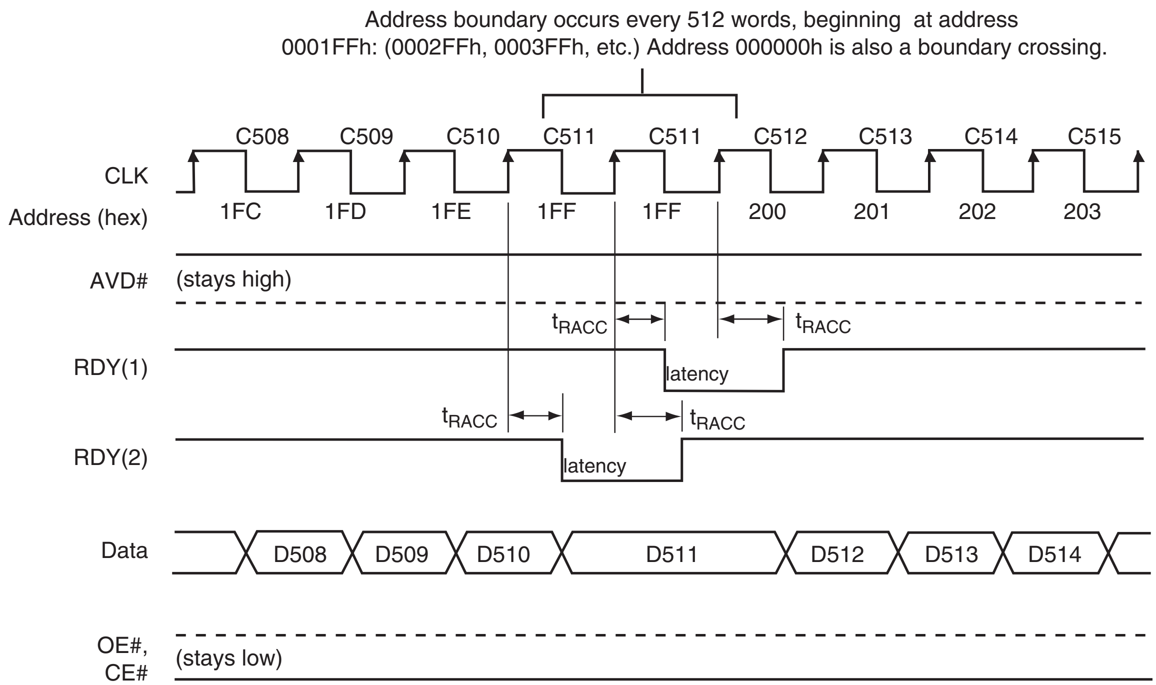
1. *The timings are similar to synchronous read timings.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, .*
3. *RDY is active with data (D8 = 0 in the Configuration Register). When D8 = 1 in the Configuration Register, RDY is active one clock cycle before data.*

Figure 25.15 Synchronous Data Polling Timings/Toggle Bit Timings



Note: *DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6.*

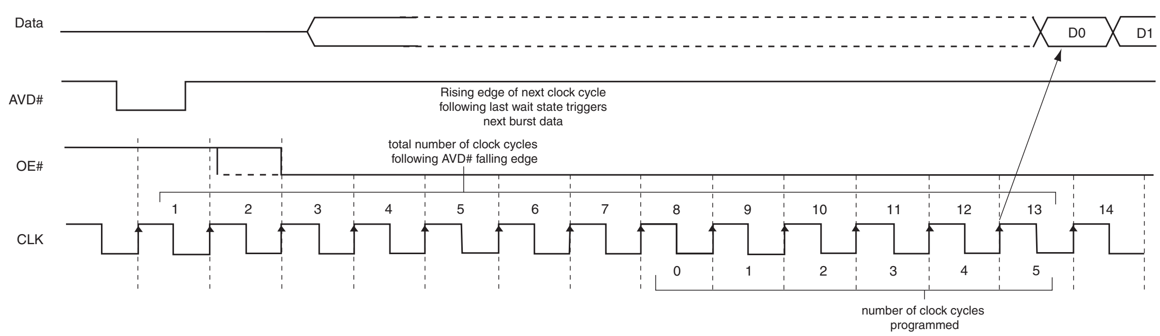
Figure 25.16 DQ2 vs. DQ6



Notes:

1. *RDY active with data (D8 = 0 in the Configuration Register).*
2. *RDY active one clock cycle before data (D8 = 1 in the Configuration Register).*
3. *Cxx indicates the clock that triggers Dxx on the outputs; for example, C60 triggers D60.*
4. *There will be an additional 4/8 wait state latency for 54/80 Mhz respectively.*

Figure 25.17 Latency with Boundary Crossing

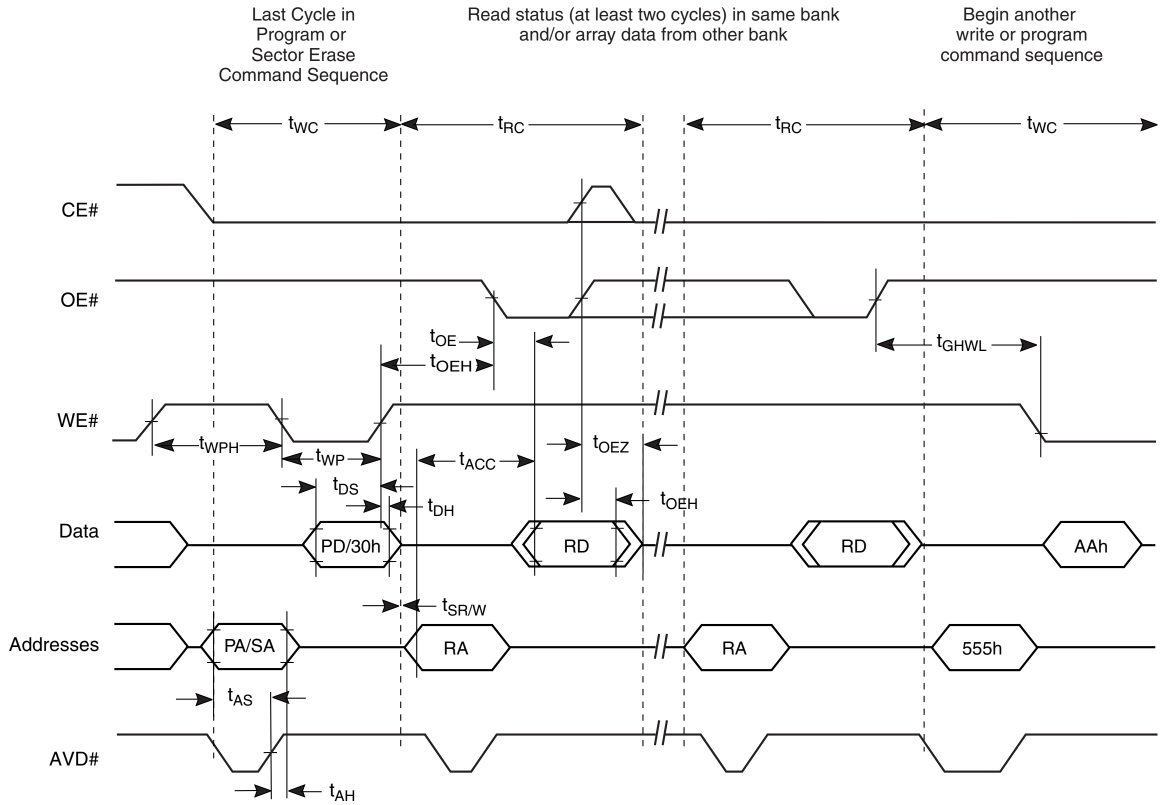


Wait State Configuration Register Setup

CR1.0, CR0.13, CR0.12, CR0.11= 1101 ⇒ *13 total*
CR1.0, CR0.13, CR0.12, CR0.11= 1100 ⇒ *12 total*
CR1.0, CR0.13, CR0.12, CR0.11= 1011 ⇒ *11 total*
CR1.0, CR0.13, CR0.12, CR0.11= 1010 ⇒ *10 total*
CR1.0, CR0.13, CR0.12, CR0.11= 1001 ⇒ *9 total*
CR1.0, CR0.13, CR0.12, CR0.11= 1000 ⇒ *8 total*
CR1.0, CR0.13, CR0.12, CR0.11= 0101 ⇒ *7 total*
CR1.0, CR0.13, CR0.12, CR0.11= 0100 ⇒ *6 total*
CR1.0, CR0.13, CR0.12, CR0.11= 0011 ⇒ *5 total*
CR1.0, CR0.13, CR0.12, CR0.11= 0010 ⇒ *4 total*
CR1.0, CR0.13, CR0.12, CR0.11= 0001 ⇒ *3 total*

Note: *Figure assumes address D0 is not at an address boundary.*

Figure 25.18 Example of Wait States Insertion



Note: *Breakpoints in waveforms indicate that system may alternately read the status of the program or erase operation in the device. The system should read status twice to ensure valid information.*

Figure 25.19 Back-to-Back Read/Write Cycle Timings

26 Erase and Programming Performance

Parameter			Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time	256 Kword	V_{CC}	2	20	s	Excludes 00h programming prior to erasure (Note 4)
		ACC	1	10		
Chip Erase Time		V_{CC}	308	616	s	
		ACC	262	524		
Word Programming Time		V_{CC}	<40	<400	µs	Excludes system level overhead (Note 5)
		ACC	<24	<240		
Effective Word Programming Time utilizing Program Write Buffer		V_{CC}	<9.4	<94	µs	
		ACC	<6	<60		
Total 32-Word BufferProgramming Time		V_{CC}	<300	<3000	µs	
		ACC	<192	<1920		
Chip Programming Time (Note 3)		V_{CC}	<314.6	<629.2	s	Excludes system level overhead (Note 5)
		ACC	<201.4	<402.6		

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 1.8 V V_{CC}, 100,000 cycles typical. Additionally, programming typically assumes a checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 1.65 V, 100,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all words are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See the Command Definitions table for further information on command definitions.*
6. *The device has a minimum erase and program cycle endurance of 100,000 cycles.*

CellularRAM

128/64/32 Megabit
Burst CellularRAM

Features

- **Single device supports asynchronous, page, and burst operations**
- **VCC Voltages**
  - 1.70V–1.95V V_{CC}
- **Random Access Time: 70ns**
- **Burst Mode Write Access**
  - Continuous burst
- **Burst Mode Read Access**
  - 4, 8, or 16 words, or continuous burst
- **Page Mode Read Access**
  - Sixteen-word page size
  - Interpage Read access: 70ns
  - Intrapage Read access: 20ns
- **Low-Power Consumption**
  - Asynchronous Read < 25mA
  - Intrapage Read < 15mA
  - Initial access, burst Read < 35mA
  - Continuous burst Read < 11mA
  - Standby: 180µA
  - Deep power-down < 10µA
- **Low-Power Features**
  - Temperature Compensated Refresh (TCR) On-chip sensor control
  - Partial Array Refresh (PAR)
  - Deep Power-Down (DPD) Mode

General Description

CellularRAM™ products are High-speed, CMOS dynamic random access memories developed for low-power, portable applications. These devices include an industry standard burst mode Flash interface that dramatically increases Read/Write bandwidth compared with other low-power SRAM or Pseudo SRAM offerings.

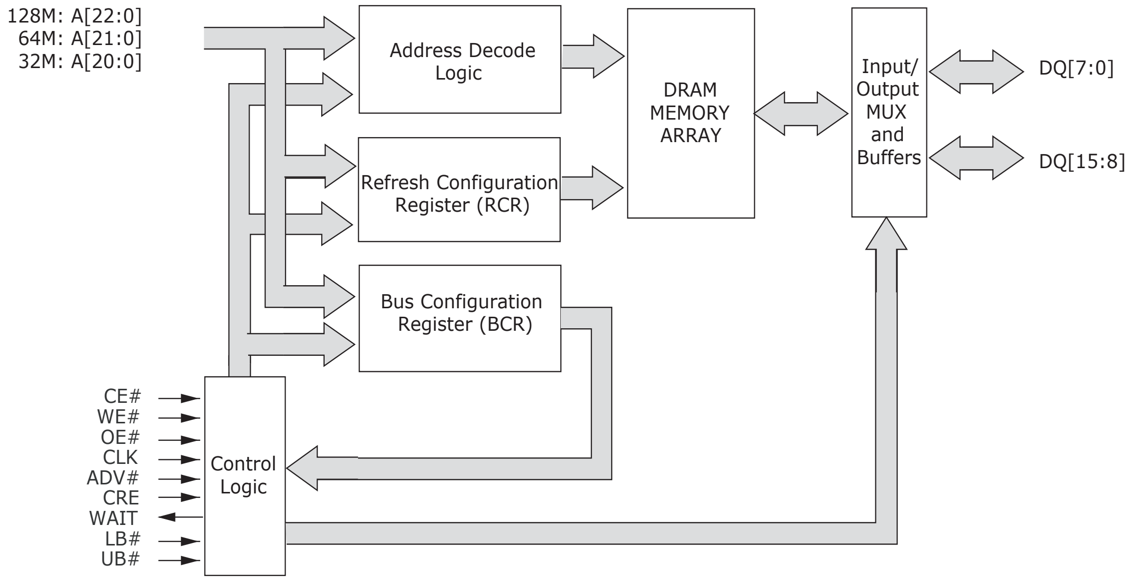
To operate seamlessly on a burst Flash bus, CellularRAM products incorporate a transparent self-refresh mechanism. The hidden refresh requires no additional support from the system memory controller and has no significant impact on device Read/Write performance.

Two user-accessible control registers define device operation. The bus configuration register (BCR) defines how the CellularRAM device interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up and can be updated anytime during normal operation.

Special attention has been focused on standby current consumption during self refresh. CellularRAM products include three mechanisms to minimize standby current. Partial array refresh (PAR) enables the system to limit refresh to only that part of the DRAM array that contains essential data. Temperature compensated refresh (TCR) adjusts the refresh rate to match the device temperature—the refresh rate decreases at lower temperatures to minimize current consumption during standby. Deep power-down (DPD) enables the system to halt the refresh operation altogether when no vital information is stored in the device. The system-configurable refresh mechanisms are accessed through the RCR.

Publication Number S75WS-N-00 **Revision** A **Amendment** 0 **Issue Date** February 17, 2005

27 Functional Block Diagram



***Note:** Functional block diagrams illustrate simplified device operation. See truth table, ball descriptions, and timing diagrams for detailed information.*

Figure 27.1 Functional Block Diagram

Table 27.1 Signal Descriptions

Symbol	Type	Description
128M: A[22:0] 64M: A[21:0] 32M: A[20:0]	Input	Address Inputs: Inputs for addresses during Read and Write operations. Addresses are internally latched during Read and Write cycles. The address lines are also used to define the value to be loaded into the BCR or the RCR.
CLK	Input	Clock: Synchronizes the memory to the system operating frequency during synchronous operations. When configured for synchronous operation, the address is latched on the first rising CLK edge when ADV# is active. CLK is static (High or Low) during asynchronous access Read and Write operations and during Page Read Access operations.
ADV#	Input	Address Valid: Indicates that a valid address is present on the address inputs. Addresses can be latched on the rising edge of ADV# during asynchronous Read and Write operations. ADV# can be held Low during asynchronous Read and Write operations.
CRE	Input	Configuration Register Enable: When CRE is High, Write operations load the RCR or BCR.
CE#	Input	Chip Enable: Activates the device when Low. When CE# is High, the device is disabled and goes into standby or deep power-down mode.
OE#	Input	Output Enable: Enables the output buffers when Low. When OE# is High, the output buffers are disabled.
WE#	Input	Write Enable: Determines if a given cycle is a Write cycle. If WE# is Low, the cycle is a Write to either a configuration register or to the memory array.
LB#	Input	Lower Byte Enable. DQ[7:0]
UB#	Input	Upper Byte Enable. DQ[15:8]
DQ[15:0]	Input/ Output	Data Inputs/Outputs.
Wait	Output	Wait: Provides data-valid feedback during burst Read and Write operations. The signal is gated by CE#. Wait is used to arbitrate collisions between refresh and Read/Write operations. Wait is asserted when a burst crosses a row boundary. Wait is also used to mask the delay associated with opening a new internal page. Wait is asserted and should be ignored during asynchronous and page mode operations. Wait is High-Z when CE# is High.
V_{CC}	Supply	Device Power Supply: (1.7V–1.95V) Power supply for device core operation.
$V_{CC}Q$	Supply	I/O Power Supply: (1.7V–1.95V) Power supply for input/output buffers.
V_{SS}	Supply	V_{SS} must be connected to ground.
$V_{SS}Q$	Supply	$V_{SS}Q$ must be connected to ground.

Note: *The CLK and ADV# inputs can be tied to V_{SS} if the device is always operating in asynchronous or page mode. Wait will be asserted but should be ignored during asynchronous and page mode operations.*

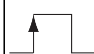
Table 27.2 Bus Operations—Asynchronous Mode

Mode	Power	Clk (Note 1)	ADV#	CE#	OE#	WE#	CRE	LB#/ UB#	Wait (Note 2)	DQ[15:0] (Note 3)	Notes
Read	Active	X	L	L	L	H	L	L	Low-Z	Data-Out	4
Write	Active	X	L	L	X	L	L	L	Low-Z	Data-In	4
Standby	Standby	X	X	H	X	X	L	X	High-Z	High-Z	5, 6
No Operation	Idle	X	X	L	X	X	L	X	Low-Z	X	4, 6
Configuration Register	Active	X	L	L	H	L	H	X	Low-Z	High-Z	
DPD	Deep Power-down	X	X	H	X	X	X	X	High-Z	High-Z	7

Notes:

1. *CLK may be High or Low, but must be static during synchronous Read, synchronous Write, burst suspend, and DPD modes; and to achieve standby power during standby and active modes.*
2. *The Wait polarity is configured through the bus configuration register (BCR[10]).*
3. *When LB# and UB# are in select mode (Low), DQ[15:0] are affected. When only LB# is in select mode, DQ[7:0] are affected. When only UB# is in the select mode, DQ[15:8] are affected.*
4. *The device will consume active power in this mode whenever addresses are changed.*
5. *When the device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.*
6. *V_{IN} = $V_{CC}Q$ or 0V; all device balls must be static (unswitched) to achieve standby current.*
7. *DPD is maintained until RCR is reconfigured.*

Table 27.3 Bus Operations—Burst Mode

Mode	Power	CLK (Note 1)	ADV#	CE#	OE#	WE#	CRE	LB#/ UB#	Wait (Note 2)	DQ[15:0] (Note 3)	Notes
Async Read	Active	X	L	L	L	H	L	L	Low-Z	Data-Out	4
Async Write	Active	X	L	L	X	L	L	L	Low-Z	Data-In	4
Standby	Standby	X	X	H	X	X	L	X	High-Z	High-Z	5, 6
No Operation	Idle	X	X	L	X	X	L	X	Low-Z	X	4, 6
Initial Burst Read	Active		L	L	X	H	L	L	Low-Z	Data-Out	4, 8
Initial Burst Write	Active		L	L	H	L	L	X	Low-Z	Data-In	4, 8
Burst Continue	Active		H	L	X	X	L	X	Low-Z	Data-In or Data-Out	4, 8
Burst Suspend	Active	X	X	L	H	X	L	X	Low-Z	High-Z	4, 8
Configuration Register	Active		L	L	H	L	H	X	Low-Z	High-Z	8
DPD	Deep Power-Down	X	X	H	X	X	X	X	High-Z	High-Z	7

Notes:

1. *CLK may be High or Low, but must be static during asynchronous Read, synchronous Write, burst suspend, and DPD modes; and to achieve standby power during standby and active modes.*
2. *The Wait polarity is configured through the bus configuration register (BCR[10]).*
3. *When LB# and UB# are in select mode (Low), DQ[15:0] are affected. When only LB# is in select mode, DQ[7:0] are affected. When only UB# is in the select mode, DQ[15:8] are affected.*
4. *The device will consume active power in this mode whenever addresses are changed.*
5. *When the device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.*
6. *V_{IN} = $V_{CC}Q$ or 0V; all device balls must be static (unswitched) to achieve standby current.*
7. *DPD is maintained until RCR is reconfigured.*
8. *Burst mode operation is initialized through the bus configuration register (BCR[15]).*

28 Functional Description

The CellularRAM bus interface supports both asynchronous and burst mode transfers. Page mode accesses are also included as a bandwidth-enhancing extension to the asynchronous Read protocol.

28.1 Power-Up Initialization

CellularRAM products include an on-chip voltage sensor used to launch the power-up initialization process. Initialization will configure the BCR and the RCR with their default settings (see Table 31.1 and Table 31.5). V_{CC} and V_{CCQ} must be applied simultaneously. When they reach a stable level at or above 1.7V, the device will require 150 µs to complete its self-initialization process. During the initialization period, CE# should remain High. When initialization is complete, the device is Ready for normal operation.

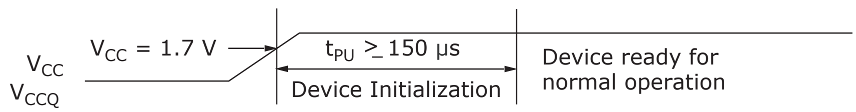


Figure 28.2 Power-Up Initialization Timing

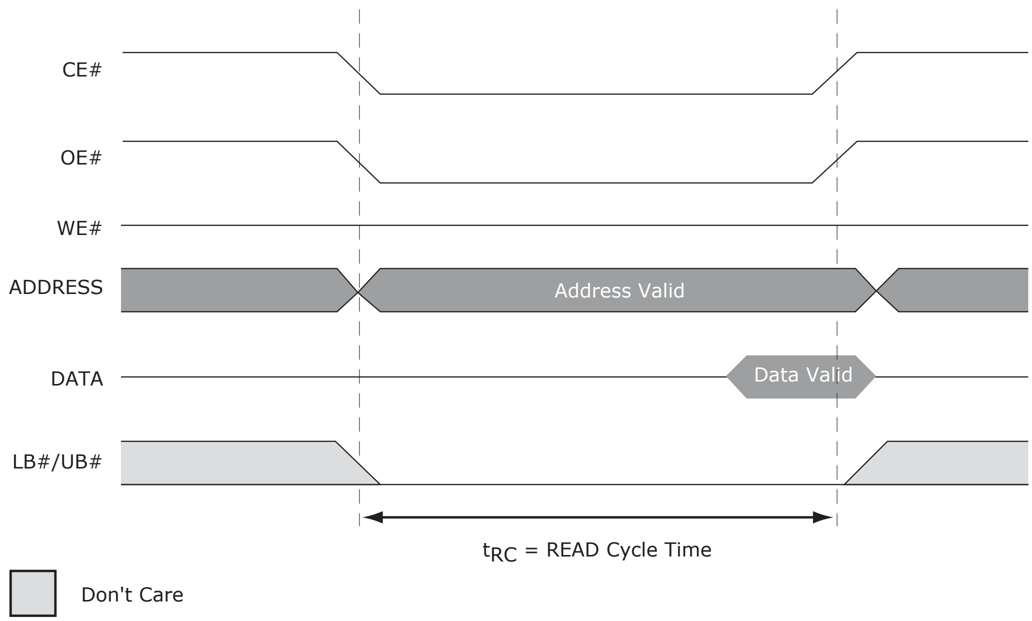
29 Bus Operating Modes

CellularRAM products incorporate a burst mode interface found on Flash products targeting low-power, wireless applications. This bus interface supports asynchronous, page mode, and burst mode Read and Write transfers. The specific interface supported is defined by the value loaded into the BCR. Page mode is controlled by the refresh configuration register (RCR[7]).

29.1 Asynchronous Mode

CellularRAM products power up in the asynchronous operating mode. This mode uses the industry standard SRAM control bus (CE#, OE#, WE#, LB#/ UB#). Read operations (Figure 29.1) are initiated by bringing CE#, OE#, and LB#/UB# Low while keeping WE# High. Valid data will be driven out of the I/Os after the specified access time has elapsed. Write operations (Figure 29.2) occur when CE#, WE#, and LB#/ UB# are driven Low. During asynchronous Write operations, the OE# level is a *don't care*, and WE# will override OE#. The data to be written is latched on the rising edge of CE#, WE#, or LB#/UB# (whichever occurs first). Asynchronous operations (page mode disabled) can either use the ADV input to latch the address, or ADV can be driven Low during the entire Read/Write operation.

During asynchronous operation, the CLK input must be held static (High or Low, no transitions). Wait will be driven while the device is enabled and its state should be ignored.



Note: *ADV must remain Low for page mode operation.*

Figure 29.1 Read Operation (ADV# Low)

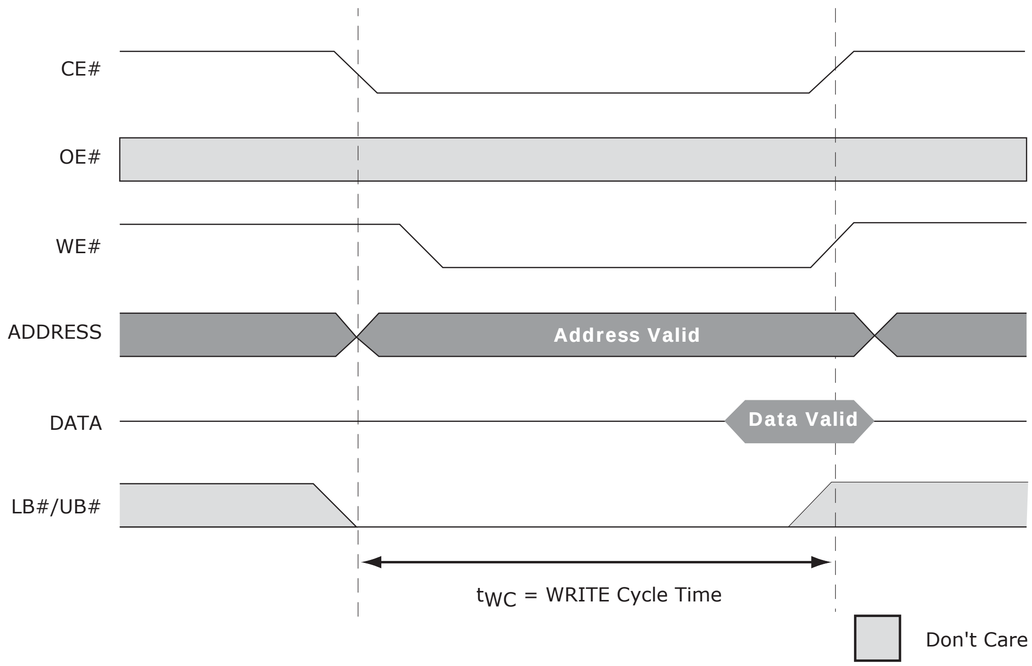


Figure 29.2 Write Operation (ADV# Low)

29.2 Page Mode Read Operation

Page mode is a performance-enhancing extension to the legacy asynchronous Read operation. In page mode-capable products, an initial asynchronous Read access is performed, then adjacent addresses can be Read quickly by simply changing the low-order address. Addresses A[3:0] are used to determine the members of the 16-address CellularRAM page. Addresses A[4] and higher must remain fixed during the entire page mode access. Figure 29.3 shows the timing for a page mode access. Page mode takes advantage of the fact that adjacent addresses can be Read in a shorter period of time than random addresses. Write operations do not include comparable page mode functionality.

During asynchronous page mode operation, the CLK input must be held Low. CE# must be driven High upon completion of a page mode access. Wait will be driven while the device is enabled and its state should be ignored. Page mode is enabled by setting RCR[7] to High. Write operations do not include comparable page mode functionality. ADV must be driven Low during all page mode Read accesses.

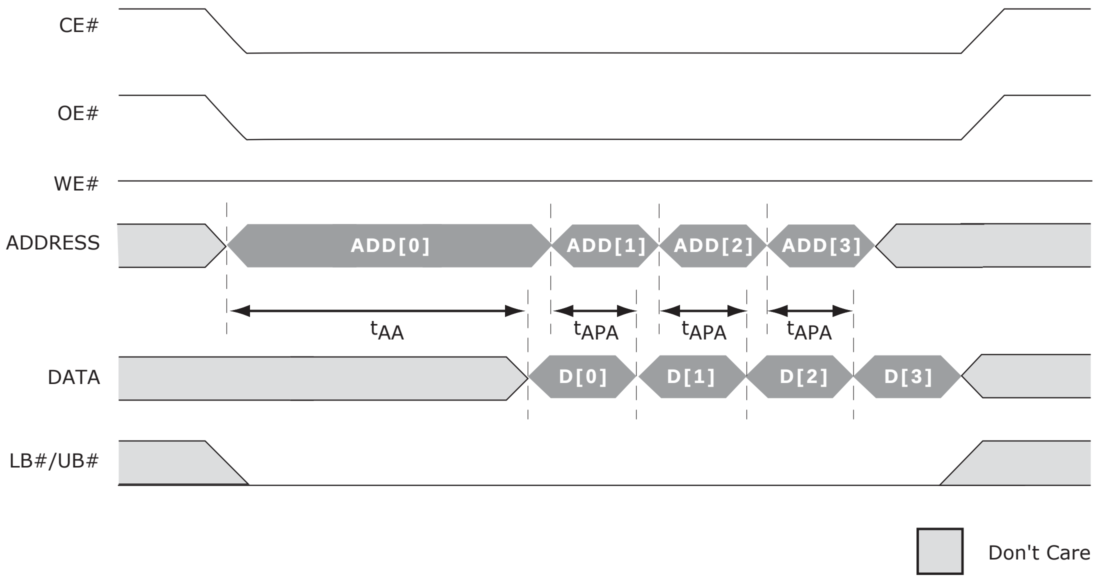


Figure 29.3 Page Mode Read Operation (ADV# Low)

29.3 Burst Mode Operation

Burst mode operations enable High-speed synchronous Read and Write operations. Burst operations consist of a multi-clock sequence that must be performed in an ordered fashion. After CE# goes Low, the address to access is latched on the rising edge of the next clock that ADV# is Low. During this first clock rising edge, WE# indicates whether the operation is going to be a Read (WE# = High, Figure 29.4) or Write (WE# = Low, Figure 29.5).

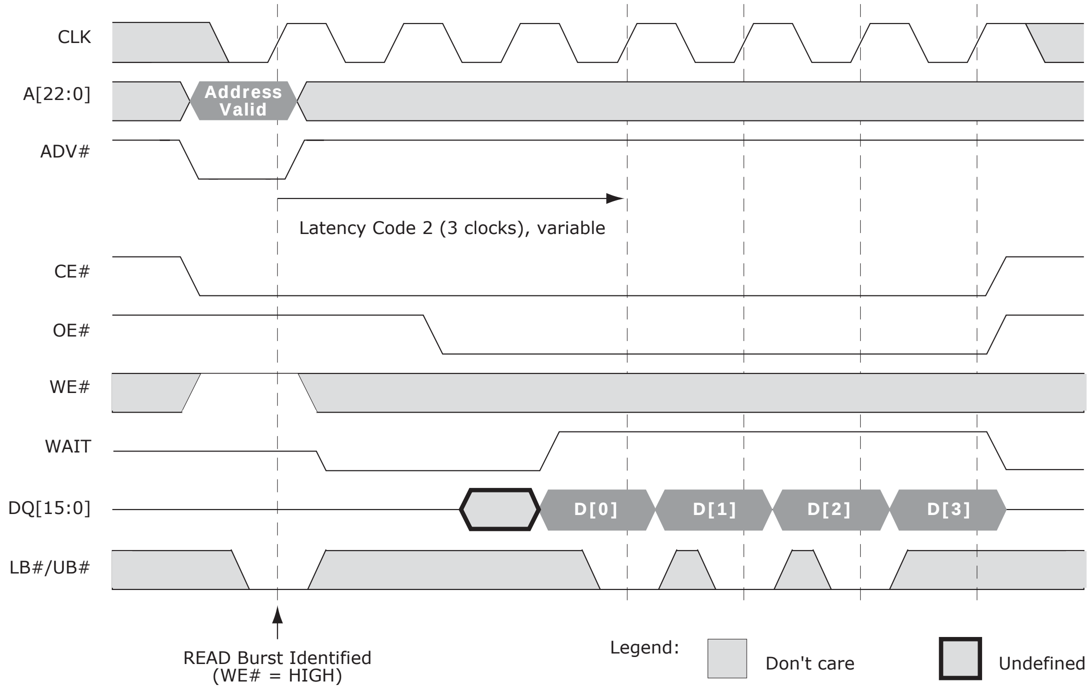
The size of a burst can be specified in the BCR either as a fixed length or continuous. Fixed-length bursts consist of four, eight, or sixteen words. Continuous bursts have the ability to start at a specified address and burst through the entire memory.

The latency count stored in the BCR defines the number of clock cycles that elapse before the initial data value is transferred between the processor and CellularRAM device.

The Wait output asserts as soon as a burst is initiated, and de-asserts to indicate when data is to be transferred into (or out of) the memory. Wait will again be asserted if the burst crosses a row boundary. Once the CellularRAM device has restored the previous row's data and accessed the next row, Wait will be deasserted and the burst can continue (see Figure 34.9).

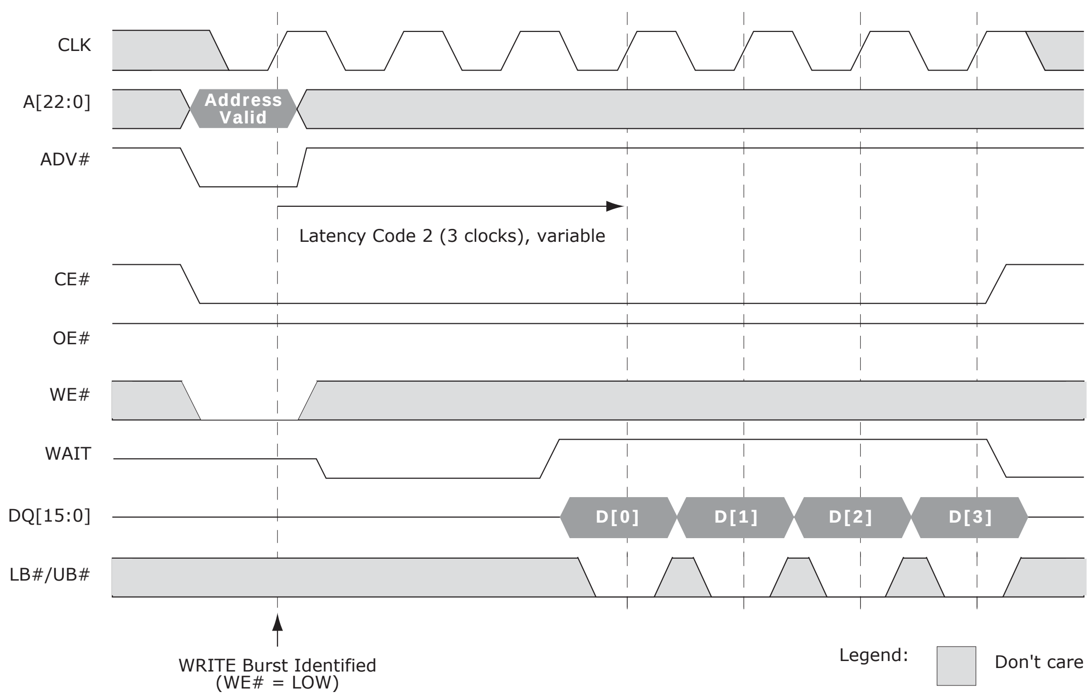
To access other devices on the same bus without the timing penalty of the initial latency for a new burst, burst mode can be suspended. Bursts are suspended by stopping CLK. CLK can be stopped High or Low. If another device will use the data bus while the burst is suspended, OE# should be taken High to disable the CellularRAM outputs; otherwise, OE# can remain Low. Note that the Wait output will continue to be active, and as a result no other devices should directly share the Wait connection to the controller. To continue the burst sequence, OE# is taken Low, then CLK is restarted after valid data is available on the bus.

See How Extended Timings Impact CellularRAM™ Operation for restrictions on the maximum CE# Low time during burst operations. If a burst suspension will cause CE# to remain Low for longer than t_{CEM}, CE# should be taken High and the burst restarted with a new CE# Low/ADV# low cycle.



Note: *Non-default BCR settings: Variable latency; latency code two (three clocks); Wait active Low; Wait asserted during delay.*

Figure 29.4 Burst Mode Read (4-word burst)



Note: *Non-default BCR settings: Variable latency; latency code two (three clocks); Wait active Low; Wait asserted during delay.*

Figure 29.5 Burst Mode Write (4-word burst)

29.4 Mixed-Mode Operation

The device can support a combination of synchronous Read and asynchronous Write operations when the BCR is configured for synchronous operation. The asynchronous Write operation requires that the clock (CLK) remain static (High or Low) during the entire sequence. The ADV# signal can be used to latch the target address, or it can remain Low during the entire Write operation. CE# can remain Low when transitioning between mixed-mode operations with fixed latency enabled. Note that the t_{CKA} period is the same as a Read or Write cycle. This time is required to ensure adequate refresh. Mixed-mode operation facilitates a seamless interface to legacy burst mode Flash memory controllers. See Figure 34.18, Asynchronous Write Followed by Burst Read (timing diagram).

29.5 Wait Operation

The Wait output on a CellularRAM device is typically connected to a shared, system-level Wait signal (Figure 29.6). The shared Wait signal is used by the processor to coordinate transactions with multiple memories on the synchronous bus.

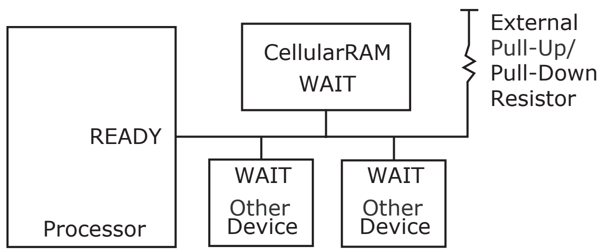


Figure 29.6 Wired or Wait Configuration

Once a Read or Write operation has been initiated, Wait goes active to indicate that the CellularRAM device requires additional time before data can be transferred. For Read operations, Wait will remain active until valid data is output from the device. For Write operations, Wait will indicate to the memory controller when data will be accepted into the CellularRAM device. When Wait transitions to an inactive state, the data burst will progress on successive clock edges.

CE# must remain asserted during Wait cycles (Wait asserted and Wait configuration BCR[8] = 1). Bringing CE# High during Wait cycles may cause data corruption. (Note that for BCR[8] = 0, the actual Wait cycles end one cycle after Wait de-asserts, and for row boundary crossings, start one cycle after the Wait signal asserts.)

When using variable initial access latency (BCR[14] = 0), the Wait output performs an arbitration role for Read or Write operations launched while an on-chip refresh is in progress. If a collision occurs, the Wait pin is asserted for additional clock cycles until the refresh has completed (Figure 29.7 and Figure 29.8). When the refresh operation has completed, the Read or Write operation will continue normally.

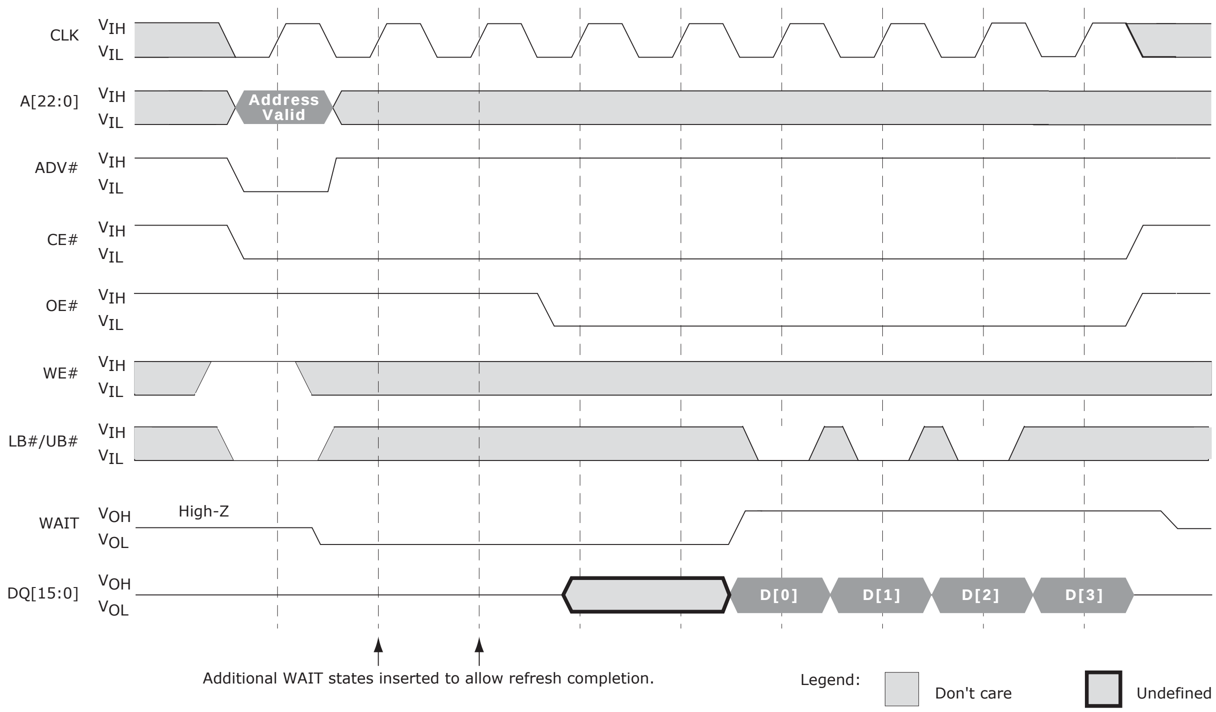
Wait is also asserted when a continuous Read or Write burst crosses the boundary between 128-word rows. The Wait assertion allows time for the new row to be accessed, and permits any pending refresh operations to be performed.

Wait will be asserted but should be ignored during asynchronous Read and Write, and page Read operations.

29.6 LB#/UB# Operation

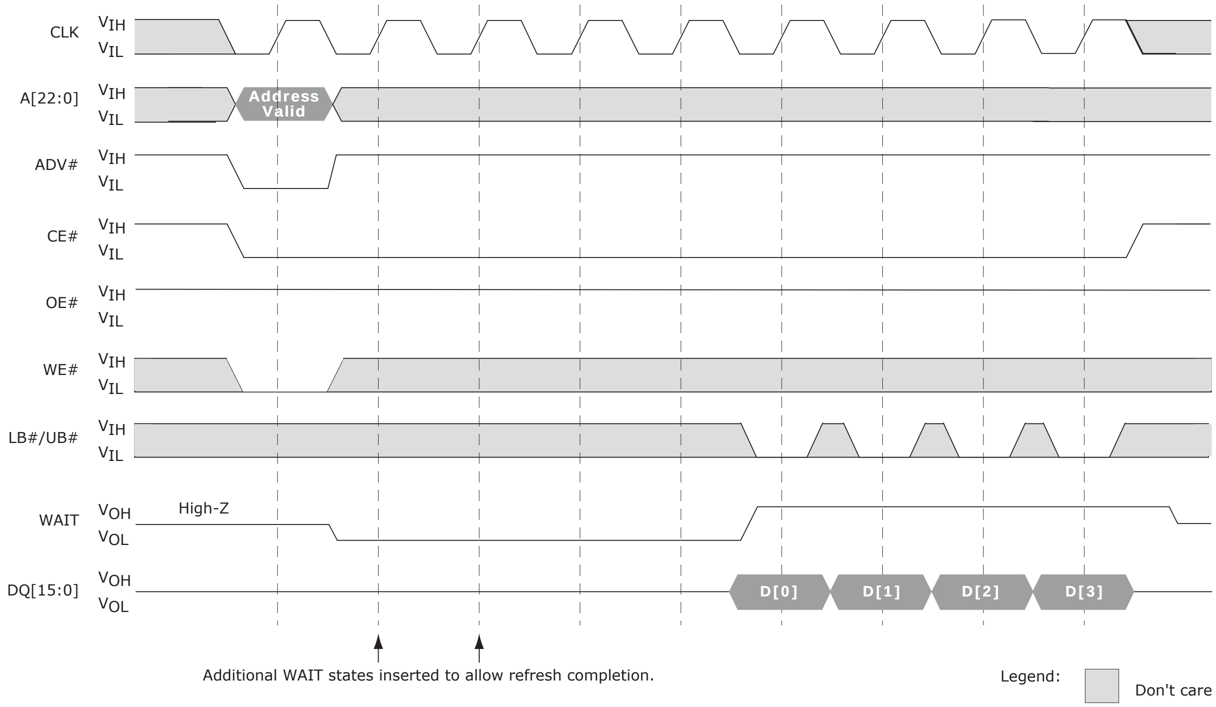
The LB# enable and UB# enable signals support byte-wide data transfers. During Read operations, the enabled byte(s) are driven onto the DQs. The DQs associated with a disabled byte are put into a High-Z state during a Read operation. During Write operations, any disabled bytes will not be transferred to the RAM array and the internal value will remain unchanged. During an asynchronous Write cycle, the data to be written is latched on the rising edge of CE#, WE#, LB#, or UB#, whichever occurs first.

When both the LB# and UB# are disabled (High) during an operation, the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, it remains in an active mode as long as CE# remains Low.



Note: *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*

Figure 29.7 Refresh Collision During Read Operation



Note: *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*

Figure 29.8 Refresh Collision During Write Operation

30 Low-Power Operation

30.1 Standby Mode Operation

During standby, the device current consumption is reduced to the level necessary to perform the DRAM refresh operation. Standby operation occurs when CE# is High.

The device will enter a reduced power state upon completion of a Read or Write operation, or when the address and control inputs remain static for an extended period of time. This mode will continue until a change occurs to the address or control inputs.

30.2 Temperature Compensated Refresh

Temperature compensated refresh (TCR) is used to adjust the refresh rate depending on the device operating temperature. DRAM technology requires increasingly frequent refresh operation to maintain data integrity as temperatures increase. More frequent refresh is required due to increased leakage of the DRAM capacitive storage elements as temperatures rise. A decreased refresh rate at lower temperatures will facilitate a savings in standby current.

TCR allows for adequate refresh at four different temperature thresholds (+15°C, +45°C, +70°C, and +85°C). The setting selected must be for a temperature higher than the case temperature of the CellularRAM device. For example, if the case temperature is 50°C, the system can minimize self refresh current consumption by selecting the +7°0C setting. The +15°C and +45°C settings would result in inadequate refreshing and cause data corruption.

30.3 Partial Array Refresh

Partial array refresh (PAR) restricts refresh operation to a portion of the total memory array. This feature enables the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, three-quarter array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map (Table 31.6). Read and Write operations to address ranges receiving refresh will not be affected. Data stored in addresses not receiving refresh will become corrupted. When re-enabling additional portions of the array, the new portions are available immediately upon writing to the RCR.

30.4 Deep Power-Down Operation

Deep power-down (DPD) operation disables all refresh-related activity. This mode is used if the system does not require the storage provided by the CellularRAM device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been re-enabled by rewriting the RCR, the CellularRAM device will require 150µs to perform an initialization procedure before normal operations can resume. During this 150µs period, the current consumption will be higher than the specified standby levels, but considerably lower than the active current specification.

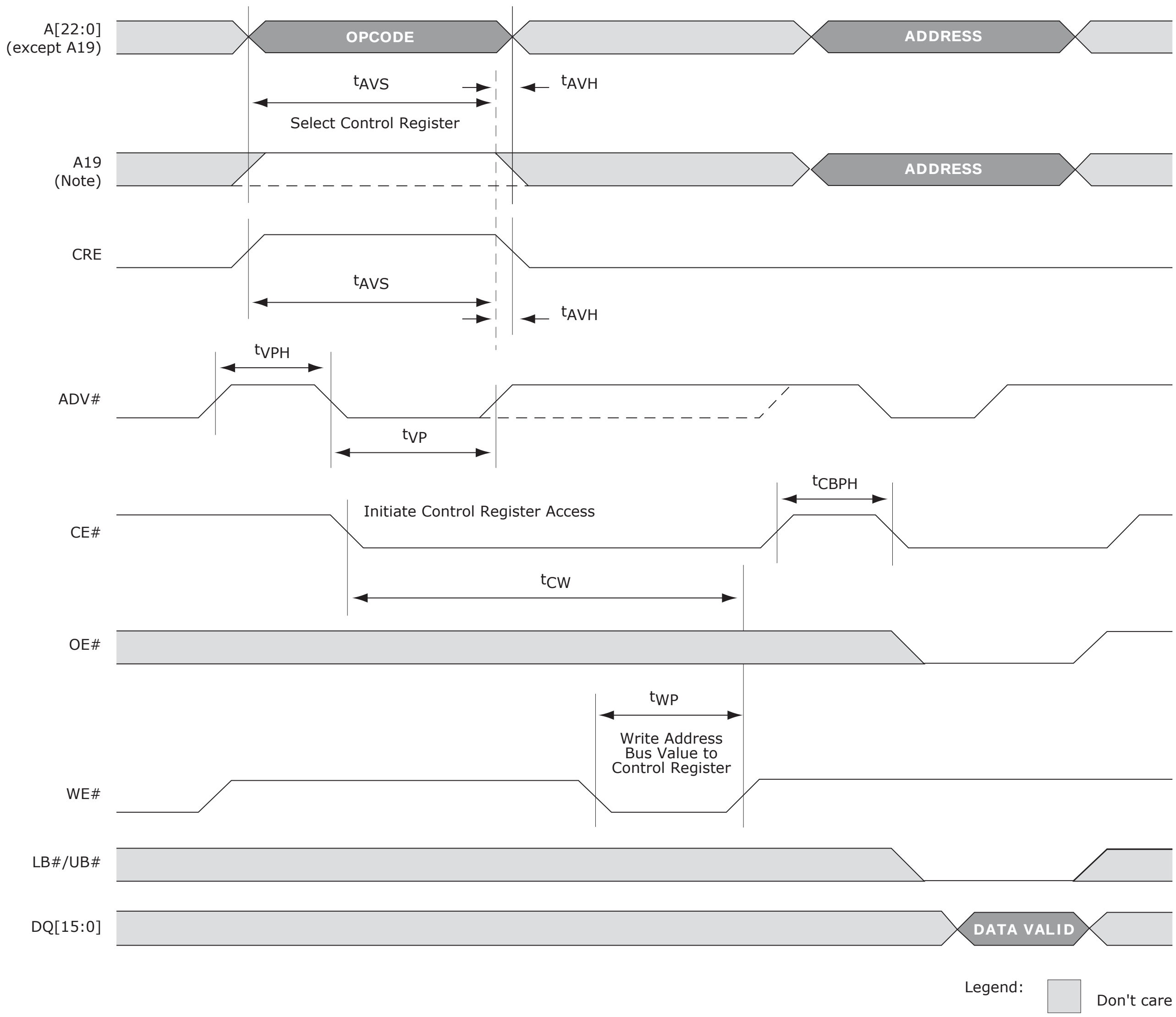
DPD cannot be enabled or disabled by writing to the RCR using the software access sequence; the RCR should be accessed using CRE instead.

31 Configuration Registers

Two user-accessible configuration registers define the device operation. The bus configuration register (BCR) defines how the CellularRAM interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up, and can be updated any time the devices are operating in a standby state.

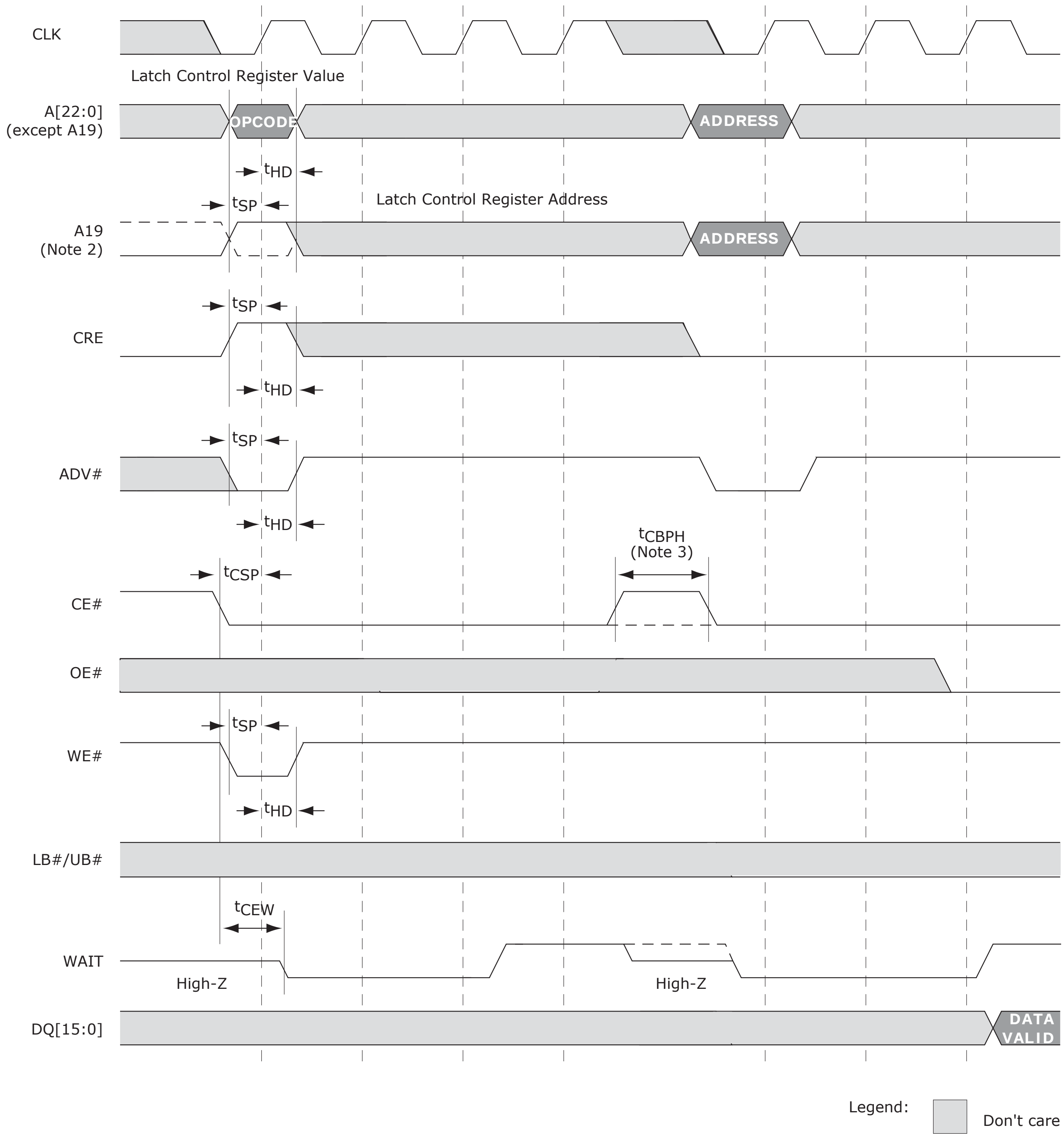
31.1 Access Using CRE

The configuration registers can be written to using either a synchronous or an asynchronous operation when the configuration register enable (CRE) input is High (see Figure 31.1 and Figure 31.2). When CRE is Low, a Read or Write operation will access the memory array. The register values are written via address pins A[21:0]. In an asynchronous Write, the values are latched into the configuration register on the rising edge of ADV#, CE#, or WE#, whichever occurs first; LB# and UB# are *Don't Care*. The BCR is accessed when A[19] is High; the RCR is accessed when A[19] is Low. For Reads, address inputs other than A[19] are *Don't Care*, and register bits 15:0 are output on DQ[15:0].



Note: *A[19] = Low to load RCR; A[19] = High to load BCR.*

Figure 31.1 Configuration Register Write, Asynchronous Mode Followed by Read



Notes:

1. *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*
2. *A[19] = Low to load RCR; A[19] = High to load BCR.*
3. *CE# must remain Low to complete a burst-of-one Write. Wait must be monitored—additional Wait cycles caused by refresh collisions require a corresponding number of additional CE# Low cycles.*

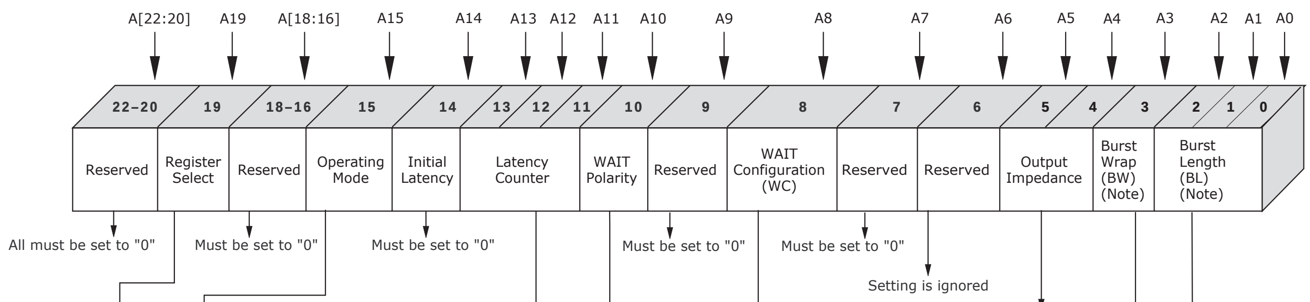
Figure 31.2 Configuration Register Write, Synchronous Mode Followed by Read0

31.2 Bus Configuration Register

The BCR defines how the CellularRAM device interacts with the system memory bus. Page mode operation is enabled by a bit contained in the RCR. Table 31.1 below describes the control bits in the BCR. At powerup, the BCR is set to 9D4Fh.

The BCR is accessed using CRE and A[19] High.

Table 31.1 Bus Configuration Register Definition



BCR[5]	BCR[4]	Output Impedance
0	0	Full Drive (default)
0	1	1/2 Drive
1	0	1/4 Drive
1	1	Reserved

BCR[13]	BCR[12]	BCR[11]	Latency Counter
0	0	0	Code 0–Reserved
0	0	1	Code 1–Reserved
0	1	0	Code 2
0	1	1	Code 3 (Default)
1	0	0	Code 4
1	0	1	Code 5
1	1	0	Code 6
1	1	1	Code 7–Reserved

BCR[3]	Burst Wrap (Note)
0	Burst wraps within the burst length
1	Burst no wrap (default)

BCR[8]	WAIT Configuration
0	Asserted during delay
1	Asserted one data cycle before delay (default)

BCR[10]	WAIT Polarity
0	Active LOW
1	Active HIGH (default)

BCR[15]	Operating Mode
0	Synchronous burst access mode
1	Asynchronous access mode (default)

BCR[2]	BCR[1]	BCR[0]	Burst Length (Note)
0	0	1	4 words
0	1	0	8 words
0	1	1	16 words
1	1	1	Continuous burst (default)
Others			Reserved

BCR[19]	Register Select
0	Select RCR
1	Select BCR

Note: *Burst wrap and length apply to Read operations only.*

Table 31.2 Sequence and Burst Length

Burst Wrap		Starting Address	4-word Burst Length	8-word Burst Length	16-word Burst Length	Continuous Burst
BCR[3]	Wrap	(Decimal)	Linear	Linear	Linear	Linear
0	Yes	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2-3-4-5-6-...
		1	1-2-3-0	1-2-3-4-5-6-7-0	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0	1-2-3-4-5-6-7-...
		2	2-3-0-1	2-3-4-5-6-7-0-1	2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1	2-3-4-5-6-7-8-...
		3	3-0-1-2	3-4-5-6-7-0-1-2	3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2	3-4-5-6-7-8-9-...
		4		4-5-6-7-0-1-2-3	4-5-6-7-8-9-10-11-12-13-14-15-0-1-2-3	4-5-6-7-8-9-10-...
		5		5-6-7-0-1-2-3-4	5-6-7-8-9-10-11-12-13-14-15-0-1-2-3-4	5-6-7-8-9-10-11-...
		6		6-7-0-1-2-3-4-5	6-7-8-9-10-11-12-13-14-15-0-1-2-3-4-5	6-7-8-9-10-11-12-...
		7		7-0-1-2-3-4-5-6	7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6	7-8-9-10-11-12-13-...
		...			...	...
		14			14-15-0-1-2-3-4-5-6-7-8-9-10-11-12-13	14-15-16-17-18-19-20-...
		15			15-0-1-2-3-4-5-6-7-8-9-10-11-12-13-14	15-16-17-18-19-20-21...
1	No	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2-3-4-5-6-...
		1	1-2-3-4	1-2-3-4-5-6-7-8	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-16	1-2-3-4-5-6-7-...
		2	2-3-4-5	2-3-4-5-6-7-8-9	2-3-4-5-6-7-8-9-10-11-12-13-14-15-16-17	2-3-4-5-6-7-8-...
		3	3-4-5-6	3-4-5-6-7-8-9-10	3-4-5-6-7-8-9-10-11-12-13-14-15-16-17-18	3-4-5-6-7-8-9-...
		4		4-5-6-7-8-9-10-11	4-5-6-7-8-9-10-11-12-13-14-15-16-17-18-19	4-5-6-7-8-9-10-...
		5		5-6-7-8-9-10-11-12	5-6-7-8-9-10-11-12-13-...-15-16-17-18-19-20	5-6-7-8-9-10-11...
		6		6-7-8-9-10-11-12-13	6-7-8-9-10-11-12-13-14-...-16-17-18-19-20-21	6-7-8-9-10-11-12...
		7		7-8-9-10-11-12-13-14	7-8-9-10-11-12-13-14-...-17-18-19-20-21-22	7-8-9-10-11-12-13...
		...			...	...
		14			14-15-16-17-18-19-...-23-24-25-26-27-28-29	14-15-16-17-18-19-20-...
		15			5-16-17-18-19-20-...-24-25-26-27-28-29-30	15-16-17-18-19-20-21-...

31.2.1 Burst Length (BCR[2:0]): Default = Continuous Burst

Burst lengths define the number of words the device outputs during burst Read operations. The device supports a burst length of 4, 8, or 16 words. The device can also be set in continuous burst mode where data is accessed sequentially without regard to address boundaries. Enabling burst no-wrap with BCR[3] = 1 overrides the burst-length setting.

31.2.2 Burst Wrap (BCR[3]): Default = No Wrap

The burst-wrap option determines if a 4-, 8-, or 16-word Read burst wraps within the burst length or steps through sequential addresses. If the wrap option is not enabled, the device accesses data from sequential addresses without regard to burst boundaries. When continuous burst operation is selected, the internal address wraps to 000000h if the burst goes past the last address. Enabling burst nowrap (BCR[3] = 1) overrides the burst-length setting.

31.2.3 Output Impedance (BCR[5:4]): Default = Outputs Use Full Drive Strength

The output driver strength can be altered to full, one-half, or one-quarter strength to adjust for different data bus loading scenarios. The reduced-strength options are intended for stacked chip (Flash + CellularRAM) environments when there is a dedicated memory bus. The reduced-drive-strength option minimizes the noise generated on the data bus during Read operations. Normal output drive strength should be selected when using a discrete CellularRAM device in a more heavily loaded data bus environment. Outputs are configured at full drive strength during testing.

Table 31.3 Output Impedance

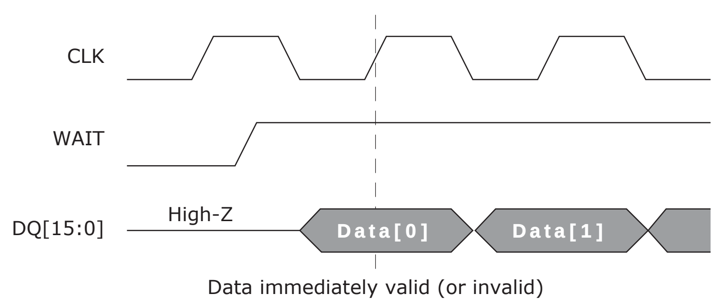
BCR[5]	BCR[4]	DRIVE STRENGTH
0	0	Full
0	1	1/2
1	0	1/4
1	1	Reserved

31.2.4 Wait Configuration (BCR[8]): Default = Wait Transitions One Clock Before Data Valid / Invalid

The Wait configuration bit is used to determine when Wait transitions between the asserted and the de-asserted state with respect to valid data presented on the data bus. The memory controller will use the Wait signal to coordinate data transfer during synchronous Read and Write operations. When BCR[8] = 0, data will be valid or invalid on the clock edge immediately after Wait transitions to the de-asserted or asserted state, respectively (Figure 31.3 and Figure 31.5). When A8 = 1, the Wait signal transitions one clock period prior to the data bus going valid or invalid (Figure 31.4).

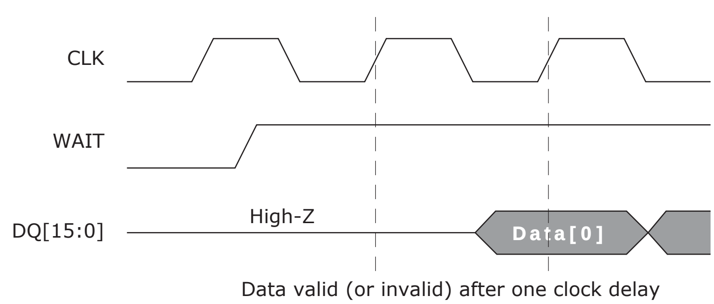
31.2.5 Wait Polarity (BCR[10]): Default = Wait Active High

The Wait polarity bit indicates whether an asserted Wait output should be High or Low. This bit will determine whether the Wait signal requires a pull-up or pull-down resistor to maintain the de-asserted state.



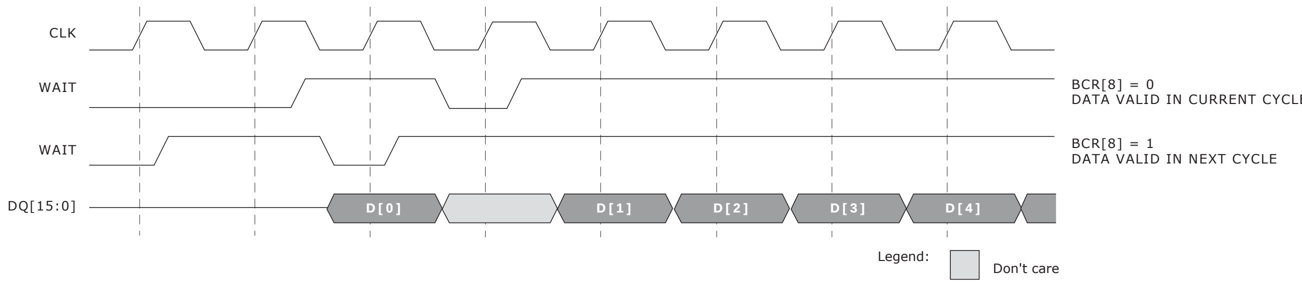
Note: *Data valid/invalid immediately after Wait transitions (BCR[8] = 0). See Figure 31.5.*

Figure 31.3 Wait Configuration (BCR[8] = 0)



Note: *Valid/invalid data delayed for one clock after Wait transitions (BCR[8] = 1). See Figure 31.5.*

Figure 31.4 Wait Configuration (BCR[8] = 1)



Note: *Non-default BCR setting: Wait active Low.*

Figure 31.5 Wait Configuration During Burst Operation

31.2.6 Latency Counter (BCR[13:11]): Default = Three-Clock Latency

The latency counter bits determine how many clocks occur between the beginning of a Read or Write operation and the first data value transferred. Latency codes from two (three clocks) to six (seven clocks) are allowed (see Table 31.4 and Figure 31.6 below).

Table 31.4 Variable Latency Configuration Codes

BCR[13:11]	Latency Configuration Code	Latency (Note)		Max Input Clk Frequency (MHz)	
		Normal	Refresh Collision	70 ns/80 MHz	85 ns/66 MHz
010	2 (3 clocks)	2	4	75 (13.0 ns)	44 (22.7 ns)
011	3 (4 clocks)—default	3	6	80 (12.5 ns)	66 (15.2 ns)
100	4 (5 clocks)	4	8		

Note: *Latency is the number of clock cycles from the initiation of a burst operation until data appears. Data is transferred on the next clock cycle.*

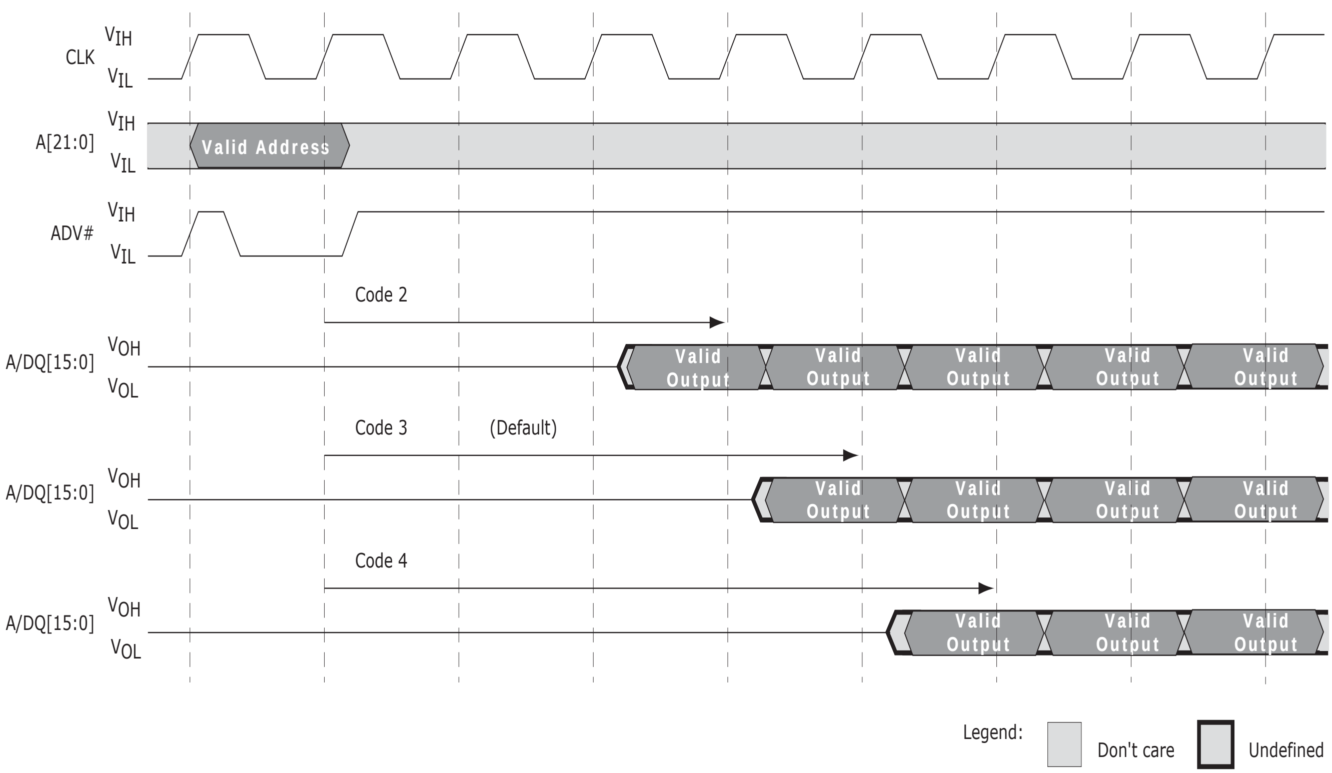


Figure 31.6 Latency Counter (Variable Initial Latency, No Refresh Collision)

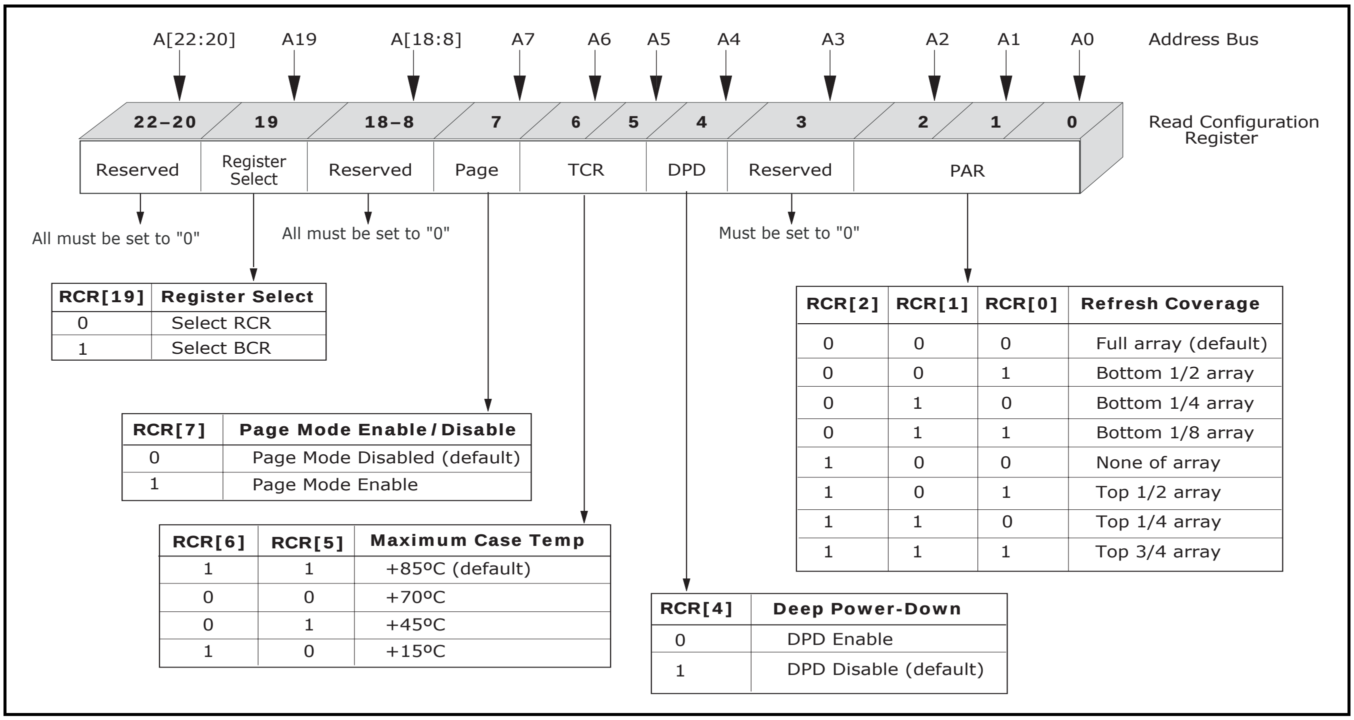
31.2.7 Operating Mode (BCR[15]): Default = Asynchronous Operation

The operating mode bit selects either synchronous burst operation or the default asynchronous mode of operation.

31.3 Refresh Configuration Register

The refresh configuration register (RCR) defines how the CellularRAM device performs its transparent self refresh. Altering the refresh parameters can dramatically reduce current consumption during standby mode. Page mode control is also embedded into the RCR. Table 31.5 below describes the control bits used in the RCR. At power-up, the RCR is set to 0070h. The RCR is accessed using CRE and A[19] Low.

Table 31.5 Refresh Configuration Register Mapping



RCR[19]	Register Select
0	Select RCR
1	Select BCR

RCR[7]	Page Mode Enable / Disable
0	Page Mode Disabled (default)
1	Page Mode Enable

RCR[6]	RCR[5]	Maximum Case Temp
1	1	+85ºC (default)
0	0	+70ºC
0	1	+45ºC
1	0	+15ºC

RCR[4]	Deep Power-Down
0	DPD Enable
1	DPD Disable (default)

RCR[2]	RCR[1]	RCR[0]	Refresh Coverage
0	0	0	Full array (default)
0	0	1	Bottom 1/2 array
0	1	0	Bottom 1/4 array
0	1	1	Bottom 1/8 array
1	0	0	None of array
1	0	1	Top 1/2 array
1	1	0	Top 1/4 array
1	1	1	Top 3/4 array

31.3.1 Partial Array Refresh (RCR[2:0]): Default = Full Array Refresh

The PAR bits restrict refresh operation to a portion of the total memory array. This feature allows the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, three-quarters array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map (see Table 31.6 through Table 31.8).

Table 31.6 128Mb Address Patterns for PAR (RCR[4] = 1)

RCR[2]	RCR[1]	RCR[0]	Active Section	Address Space	Size	Density
0	0	0	Full die	000000h–7FFFFFh	8 Meg x 16	128Mb
0	0	1	One-half of die	000000h–3FFFFFh	4 Meg x 16	64Mb
0	1	0	One-quarter of die	000000h–1FFFFFh	2 Meg x 16	32Mb
0	1	1	One-eighth of die	000000h–0FFFFFh	1 Meg x 16	16Mb
1	0	0	None of die	0	0 Meg x 16	0Mb
1	0	1	One-half of die	400000h–7FFFFFh	4 Meg x 16	64Mb

Table 31.6 128Mb Address Patterns for PAR (RCR[4] = 1) (Continued)

RCR[2]	RCR[1]	RCR[0]	Active Section	Address Space	Size	Density
1	1	0	One-quarter of die	600000h–7FFFFFh	2 Meg x 16	32Mb
1	1	1	One-eighth of die	700000h–7FFFFFh	1 Meg x 16	16Mb

Table 31.7 64Mb Address Patterns for PAR (RCR[4] = 1)

RCR[2]	RCR[1]	RCR[0]	Active Section	Address Space	Size	Density
0	0	0	Full die	000000h–3FFFFFh	4 Meg x 16	64Mb
0	0	1	One-half of die	000000h–2FFFFFh	3 Meg x 16	48Mb
0	1	0	One-quarter of die	000000h–1FFFFFh	2 Meg x 16	32Mb
0	1	1	One-eighth of die	000000h–0FFFFFh	1 Meg x 16	16Mb
1	0	0	None of die	0	0 Meg x 16	0Mb
1	0	1	One-half of die	100000h–3FFFFFh	3 Meg x 16	48Mb
1	1	0	One-quarter of die	200000h–3FFFFFh	2 Meg x 16	32Mb
1	1	1	One-eighth of die	300000h–3FFFFFh	1 Meg x 16	16Mb

Table 31.8 32Mb Address Patterns for PAR (RCR[4] = 1)

RCR[2]	RCR[1]	RCR[0]	ACTIVE SECTION	ADDRESS SPACE	SIZE	DENSITY
0	0	0	Full die	000000h–1FFFFFh	2 Meg x 16	32Mb
0	0	1	One-half of die	000000h–17FFFFh	1.5 Meg x 16	24Mb
0	1	0	One-quarter of die	000000h–0FFFFFh	1 Meg x 16	16Mb
0	1	1	One-eighth of die	000000h–07FFFFh	512K x 16	8Mb
1	0	0	None of die	0	0 Meg x 16	0Mb
1	0	1	One-half of die	080000h–1FFFFFh	1.5 Meg x 16	24Mb
1	1	0	One-quarter of die	100000h–1FFFFFh	1 Meg x 16	16Mb
1	1	1	One-eighth of die	180000h–1FFFFFh	512K x 16	8Mb

31.3.2 Deep Power-Down (RCR[4]): Default = DPD Disabled

The deep power-down bit enables and disables all refresh-related activity. This mode is used if the system does not require the storage provided by the CellularRAM device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been re-enabled, the Cellular-RAM device will require 150µs to perform an initialization procedure before normal operations can resume.

Deep power-down is enabled when RCR[4] = 0, and remains enabled until RCR[4] is set to *1*.

31.3.3 Temperature Compensated Refresh (RCR[6:5]): Default = +85°C Operation

The TCR bits allow for adequate refresh at four different temperature thresholds (+15ºC, +45ºC, +70ºC, and +85ºC). The setting selected must be for a temperature higher than the case temperature of the CellurlarRAM device. If the case temperature is +50ºC, the system can minimize self refresh current consumption by selecting the +70ºC setting. The +15ºC and +45ºC settings would result in inadequate refreshing and cause data corruption.

31.3.4 Page Mode Operation (RCR[7]): Default = Disabled

The page mode operation bit determines whether page mode is enabled for asynchronous Read operations. In the power-up default state, page mode is disabled.

32 Absolute Maximum Ratings

Voltage to Any Ball Except V_{CC}, $V_{CC}Q$
. . . . Relative to V_{SS}-0.50V to (4.0V or $V_{CC}Q$ + 0.3V, whichever is less)
Voltage on V_{CC} Supply Relative to V_{SS} . . . . -0.2V to +2.45V
Voltage on $V_{CC}Q$ Supply Relative to V_{SS} . . . . -0.2V to +2.45V
Storage Temperature (plastic) . . . . -55ºC to +150ºC
Operating Temperature (case)
. . . . Wireless-25ºC to +85ºC

Note: **Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.*

33 DC Characteristics

Table 33.1 Electrical Characteristics and Operating Conditions

Description	Conditions	Symbol		Min	Max	Units	Notes
Supply Voltage		V_{CC}		1.70	1.95	V	
I/O Supply Voltage		$V_{CC}Q$	W: 1.8V	1.70	1.95	V	
			J: 1.5V	1.35	1.65	V	
Input High Voltage		V_{IH}		$V_{CC}Q$ - 0.4	$V_{CC}Q$ + 0.2	V	2
Input Low Voltage		V_{IL}		-0.20	0.4	V	3
Output High Voltage	I_{OH} = -0.2mA	V_{OH}		0.80 $V_{CC}Q$		V	4
Output Low Voltage	I_{OL} = +0.2mA	V_{OL}			0.20 $V_{CC}Q$	V	4
Input Leakage Current	V_{IN} = 0 to $V_{CC}Q$	I_{LI}			1	µA	
Output Leakage Current	OE# = V_{IH} or Chip Disabled	I_{LO}			1	µA	
Operating Current							
Asynchronous Random Read	V_{IN} = $V_{CC}Q$ or 0V Chip Enabled, IOUT = 0	$I_{CC}1$	-70		25	mA	5
			-85		20		
Asynchronous Page Read			-70		15		
			-85		12		
Initial Access, Burst Read	V_{IN} = $V_{CC}Q$ or 0V Chip Enabled, IOUT = 0	$I_{CC}1$	80 MHz		35	mA	5
			66 MHz		30		
Continuous Burst Read			80 MHz		18		
			66 MHz		15		
Write Operating Current	V_{IN} = $V_{CC}Q$ or 0V Chip Enabled	$I_{CC}2$	-70		25	mA	
			-85		20		
Standby Current	V_{IN} = $V_{CC}Q$ or 0V CE# = $V_{CC}Q$	I_{SB}	128 M		180	µA	6
			64 M		120		
			32 M		110		

Notes:

1. *Wireless Temperature (-25°C < TC < +85°C); Industrial Temperature (-40°C < TC < +85°C).*
2. *Input signals may overshoot to $V_{CC}Q$ + 1.0V for periods less than 2ns during transitions.*
3. *Input signals may undershoot to V_{SS} - 1.0V for periods less than 2ns during transitions.*
4. *BCR[5:4] = 00b.*
5. *This parameter is specified with the outputs disabled to avoid external loading effects. The user must add the current required to drive output capacitance expected in the actual system.*
6. *ISB (MAX) values measured with PAR set to FULL ARRAY and TCR set to +85°C. To achieve Low standby current, all inputs must be driven to either $V_{CC}Q$ or V_{SS}.*

Table 33.2 Temperature Compensated Refresh Specifications and Conditions

Description	Conditions	Symbol	Density	Max Case Temperature	Standard Power (No Desig.)	Units
Temperature Compensated Refresh Standby Current	$V_{IN} = V_{CC}Q$ or 0V, CE# = $V_{CC}Q$	I_{TCR}	64 Mb	+85°C	120	µA
				+70°C	105	
				+45°C	85	
				+15°C	70	
			32 Mb	+85°C	110	
				+70°C	95	
				+45°C	80	
				+15°C	70	

Note: *I_{PAR} (MAX) values measured with TCR set to 85°C.*

Table 33.3 Partial Array Refresh Specifications and Conditions

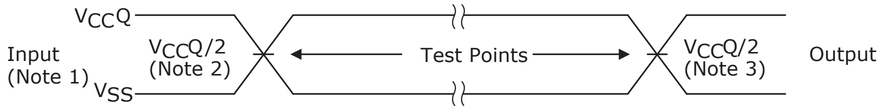
Description	Conditions	Symbol	Density	Array Partition	Standard Power (No Desig.)	Units
Partially Array Refresh Standby Current	$V_{IN} = V_{CC}Q$ or 0V, CE# = $V_{CC}Q$	I_{PAR}	64 Mb	Full	120	µA
				1/2	115	
				1/4	110	
				1/8	105	
				0	70	
			32 Mb	Full	110	
				1/2	105	
				1/4	100	
				1/8	95	
				0	70	
			128 Mb	Full	180	
				0	50	

Note: I_{PAR} (MAX) values measured with TCR set to 85°C.

Table 33.4 Deep Power-Down Specifications

Description	Conditions	Symbol	Typ	Units
Deep Power-down	$V_{IN} = V_{CC}Q$ or 0V; +25°C; V_{CC} = 1.8V	I_{ZZ}	10	µA

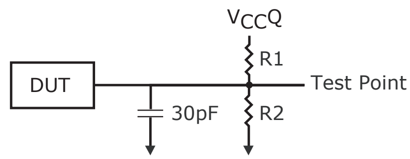
34 AC Characteristics



Notes:

1. *AC test inputs are driven at $V_{CC}Q$ for a logic 1 and V_{SS} for a logic 0. Input rise and fall times (10% to 90%) < 1.6ns.*
2. *Input timing begins at $V_{CC}Q/2$.*
3. *Output timing ends at $V_{CC}Q/2$.*

Figure 34.1 AC Input/Output Reference Waveform



Note: *All tests are performed with the outputs configured for full drive strength (BCR[5] = 0).*

Figure 34.2 Output Load Circuit

Table 34.1 Output Load Circuit

$V_{CC}Q$	R1/R2
1.8V	2.7K Ω

Table 34.2 Asynchronous Read Cycle Timing Requirements

Parameter	Symbol	85ns/66 MHz		70ns/80 MHz		Units	Notes
		Min	Max	Min	Max		
Address Access Time	t_{AA}		85		70	ns	
ADV# Access Time	t_{AADV}		85		70	ns	
Page Access Time	t_{APA}		25		20	ns	
Address Hold from ADV# High	t_{AVH}	5		5		ns	
Address Setup to ADV# High	t_{AVS}	10		10		ns	
LB#/UB# Access Time	t_{BA}		85		70	ns	
LB#/UB# Disable to DQ High-Z Output	t_{BHZ}		8		8	ns	4
LB#/UB# Enable to Low-Z Output	t_{BLZ}	10		10		ns	3
CE# High between Subsequent Mixed-Mode Operations	t_{CBPH}	5		5		ns	
Maximum CE# Pulse Width	t_{CEM}		4		4	µs	2
CE# Low to Wait Valid	t_{CEW}	1	7.5	1	7.5	ns	
Chip Select Access Time	t_{CO}		85		70	ns	
CE# Low to ADV# High	t_{CVS}	10		10		ns	
Chip Disable to DQ and Wait High-Z Output	t_{HZ}		8		8	ns	4
Chip Enable to Low-Z Output	t_{LZ}	10		10		ns	3
Output Enable to Valid Output	t_{OE}		20		20	ns	
Output Hold from Address Change	t_{OH}	5		5		ns	
Output Disable to DQ High-Z Output	t_{OHZ}		8		8	ns	4
Output Enable to Low-Z Output	t_{OLZ}	5		5		ns	3
Page Cycle Time	t_{PC}	25		20		ns	
Read Cycle Time	t_{RC}	85		70		ns	
ADV# Pulse Width Low	t_{VP}	10		10		ns	
ADV# Pulse Width High	t_{VPH}	10		10		ns	

Notes:

1. *All tests are performed with the outputs configured for full drive strength (BCR[5] = 0).*
2. *See How Extended Timings Impact CellularRAM™ Operation below.*
3. *High-Z to Low-Z timings are tested with the circuit shown in Figure 34.2. The Low-Z timings measure a*
4. *100mV transition away from the High-Z ($V_{CC}Q/2$) level toward either V_{OH} or V_{OL}.*
5. *Low-Z to High-Z timings are tested with the circuit shown in Figure 34.2. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward $V_{CC}Q/2$.*

Table 34.3 Burst Read Cycle Timing Requirements

Parameter	Symbol	70ns/80 MHz		85ns/66 MHz		Units	Notes
		Min	Max	Min	Max		
Burst to Read Access Time (Variable Latency)	t_{ABA}		35		55	ns	
CLK to Output Delay	t_{ACLK}		9		11	ns	
Address Setup to ADV# High	t_{AVS}	10		10		ns	
Burst OE# Low to Output Delay	t_{BOE}		20		20	ns	
CE# High between Subsequent Mixed-Mode Operations	t_{CBPH}	5		5		ns	
CE# Low to Wait Valid	t_{CEW}	1	7.5	1	7.5	ns	
CLK Period	t_{CLK}	12.5		15		ns	
CE# Setup Time to Active CLK Edge	t_{CSP}	4		5		ns	
Hold Time from Active CLK Edge	t_{HD}	2		2		ns	
Chip Disable to DQ and Wait High-Z Output	t_{HZ}		8		8	ns	2
CLK Rise or Fall Time	t_{KHKL}		1.6		1.6	ns	
CLK to Wait Valid	t_{KHTL}		9		11	ns	
CLK to DQ High-Z Output	t_{KHZ}	3	8	3	8	ns	
CLK to Low-Z Output	t_{KLZ}	2	5	2	5	ns	
Output Hold from CLK	t_{KOH}	2		2		ns	
CLK High or Low Time	t_{KP}	3		3		ns	
Output Disable to DQ High-Z Output	t_{OHZ}		8		8	ns	2
Output Enable to Low-Z Output	t_{OLZ}	5		5		ns	3
Setup Time to Active CLK Edge	t_{SP}	3		3		ns	

Notes:

1. *All tests are performed with the outputs configured for full drive strength (BCR[5] = 0).*
2. *Low-Z to High-Z timings are tested with the circuit shown in Figure 34.2. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward $V_{CC}Q/2$.*
3. *High-Z to Low-Z timings are tested with the circuit shown in Figure 34.2. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CC}Q/2$) level toward either V_{OH} or V_{OL}.*

Table 34.4 Asynchronous Write Cycle Timing Requirements

Parameter	Symbol	70 ns/80 MHz		85 ns/66 MHz		Units	Notes
		Min	Max	Min	Max		
Address and ADV# Low Setup Time	t_{AS}	0		0		ns	
Address Hold from ADV# Going High	t_{AVH}	5		5		ns	
Address Setup to ADV# Going High	t_{AVS}	10		10	ns		
Address Valid to End of Write	t_{AW}	70		85		ns	
LB#/UB# Select to End of Write	t_{BW}	70		85		ns	
Maximum CE# Pulse Width	t_{CEM}		4		4	µs	1
CE# Low to Wait Valid	t_{CEW}	1	7.5	1	7.5	ns	
Async Address-to-Burst Transition Time	t_{CKA}	70		85		ns	
CE# Low to ADV# High	t_{CVS}	10		10		ns	
Chip Enable to End of Write	t_{CW}	70		85		ns	
Data Hold from Write Time	t_{DH}	0		0		ns	
Data Write Setup Time	t_{DW}	23		23		ns	1
Chip Disable to Wait High-Z Output	t_{HZ}		8		8	ns	
Chip Enable to Low-Z Output	t_{LZ}	10		10		ns	3
End Write to Low-Z Output	t_{OW}	5		5		ns	3
ADV# Pulse Width	t_{VP}	10		10		ns	
ADV# Pulse Width High	t_{VPH}	10		10		ns	
ADV# Setup to End of Write	t_{VS}	70		85		ns	
Write Cycle Time	t_{WC}	70		85		ns	
Write to DQ High-Z Output	t_{WHZ}		8		8	ns	2
Write Pulse Width	t_{WP}	46		55		ns	1
Write Pulse Width High	t_{WPH}	10		10		ns	
Write Recovery Time	t_{WR}	0		0		ns	

Notes:

1. *See How Extended Timings Impact CellularRAM™ Operation below.*
2. *Low-Z to High-Z timings are tested with the circuit shown in Figure 34.2. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward $V_{CC}Q/2$.*
3. *High-Z to Low-Z timings are tested with the circuit shown in Figure 34.2. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CC}Q/2$) level toward either V_{OH} or V_{OL}.*

Table 34.5 Burst Write Cycle Timing Requirements

Parameter	Symbol	70ns/80 MHz		85ns/66 MHz		Units	Notes
		Min	Max	Min	Max		
CE# High between Subsequent Mixed-Mode Operations	t_{CBPH}	5		5		ns	
CE# Low to Wait Valid	t_{CEW}	1	7.5	1	7.5	ns	
Clock Period	t_{CLK}	12.5		15		ns	
CE# Setup to CLK Active Edge	t_{CSP}	4		5		ns	
Hold Time from Active CLK Edge	t_{HD}	2		2		ns	
Chip Disable to Wait High-Z Output	t_{HZ}		8		8	ns	
CLK Rise or Fall Time	t_{KHKL}		1.6		1.6	ns	
Clock to Wait Valid	t_{KHTL}		9		11	ns	
CLK High or Low Time	t_{KP}	3		3		ns	
Setup Time to Activate CLK Edge	t_{SP}	3		3		ns	

34.1 Timing Diagrams

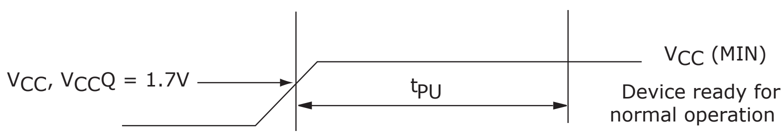


Figure 34.3 Initialization Period

Table 34.1 Initialization Timing Parameters

Parameter	Symbol	70ns/80 MHz		85ns/66 MHz		Units	Notes
		Min	Max	Min	Max		
Initialization Period (required before normal operations)	t_{PU}		150		150	µs	

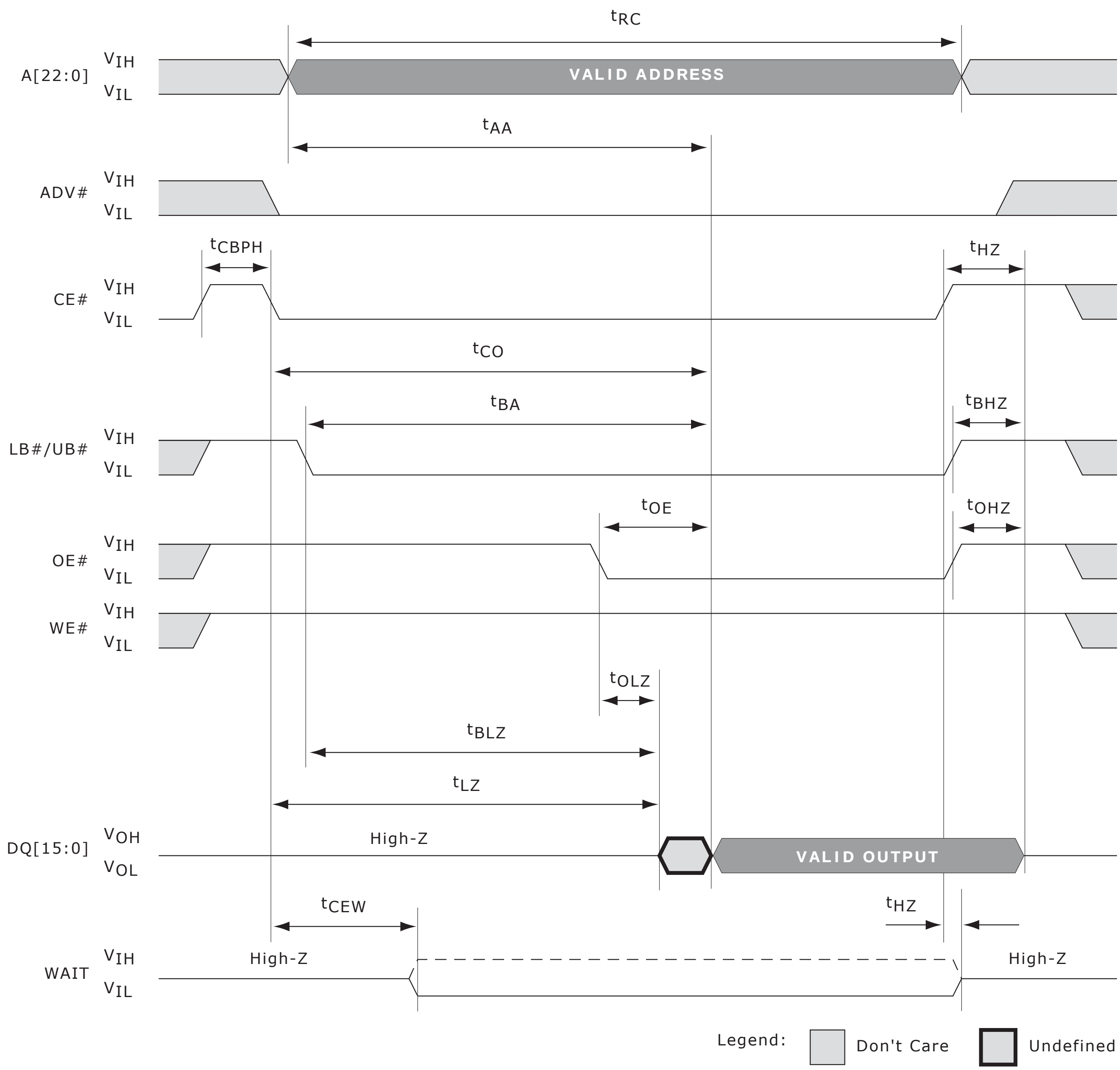


Figure 34.4 Asynchronous Read

Table 34.2 Asynchronous Read Timing Parameters

Symbol	70ns/80 MHz		85ns/66 MHz		Units
	Min	Max	Min	Max	
t_{AA}		70		85	ns
t_{BA}		70		85	ns
t_{BHZ}		8		8	ns
t_{BLZ}	10		10		ns
t_{CBPH}	5		5		ns
t_{CEW}	1	7.5	1	7.5	ns
t_{CO}		70			ns
t_{HZ}		8		8	ns
t_{LZ}	10		10		ns
t_{OE}		20		20	ns
t_{OHZ}		8		8	ns
t_{OLZ}	5		5		ns
t_{RC}	70		85		ns

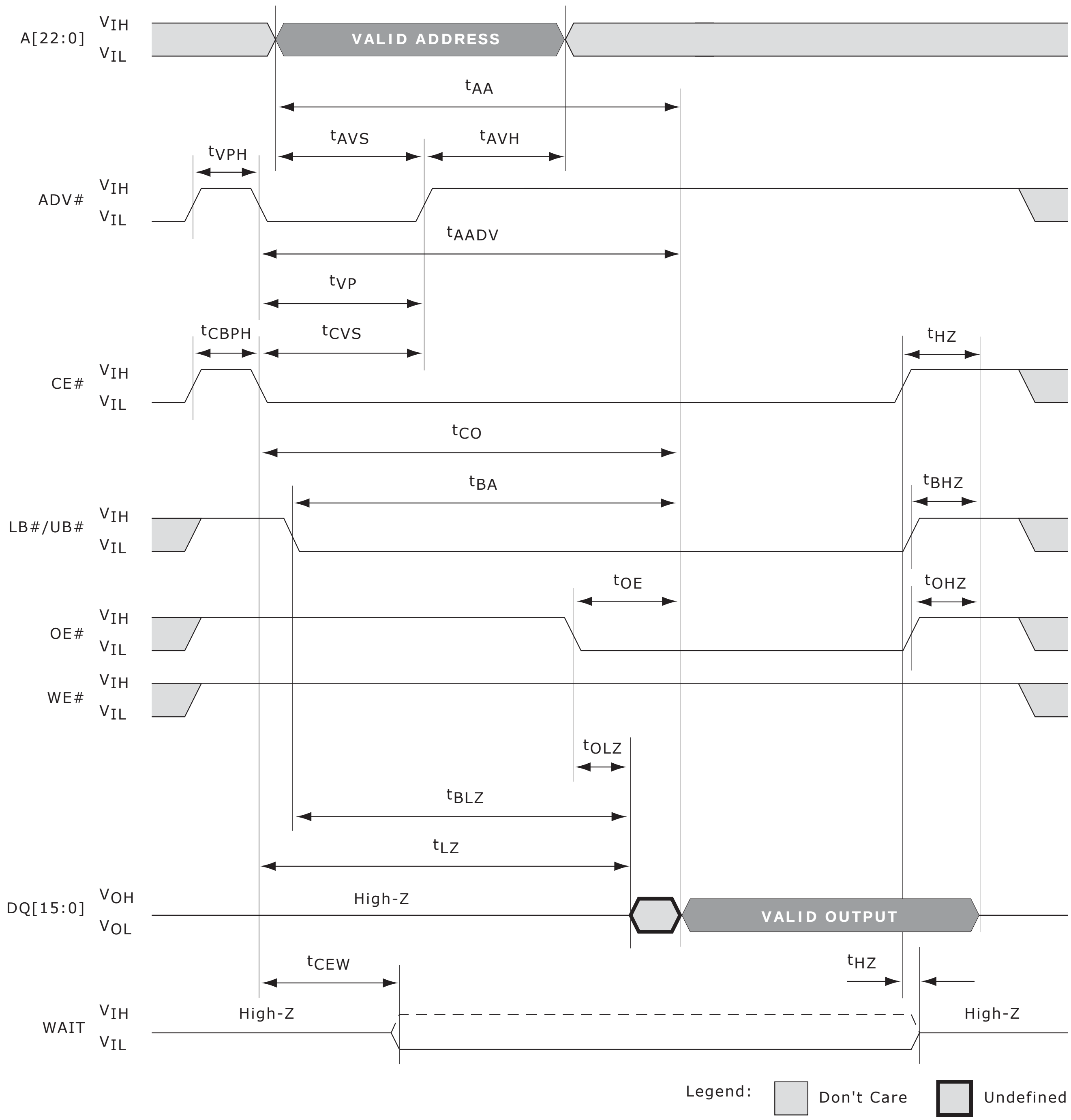


Figure 34.5 Asynchronous Read Using ADV#

Table 34.3 Asynchronous Read Timing Parameters Using ADV#

Symbol	70ns/80 MHz		85ns/66 MHz		Units
	Min	Max	Min	Max	
t_{AA}		70		85	ns
t_{AADV}		70		85	ns
t_{CVS}	10		10		ns
t_{AVH}	5		5		ns
t_{AVS}	10		10		ns
t_{BA}		70		85	ns
t_{BHZ}		8		8	ns
t_{BLZ}	10		10		ns
t_{CBPH}	5		5		ns
t_{CEW}	1	7.5	1	7.5	ns
t_{CO}		70		85	ns
t_{CVS}	10		10		ns
t_{HZ}		8		8	ns
t_{LZ}	10		10		ns
t_{OE}		20		20	ns
t_{OHZ}		8		8	ns
t_{OLZ}	5		5		ns
t_{VP}	10		10		ns
t_{VPH}	10		10		ns

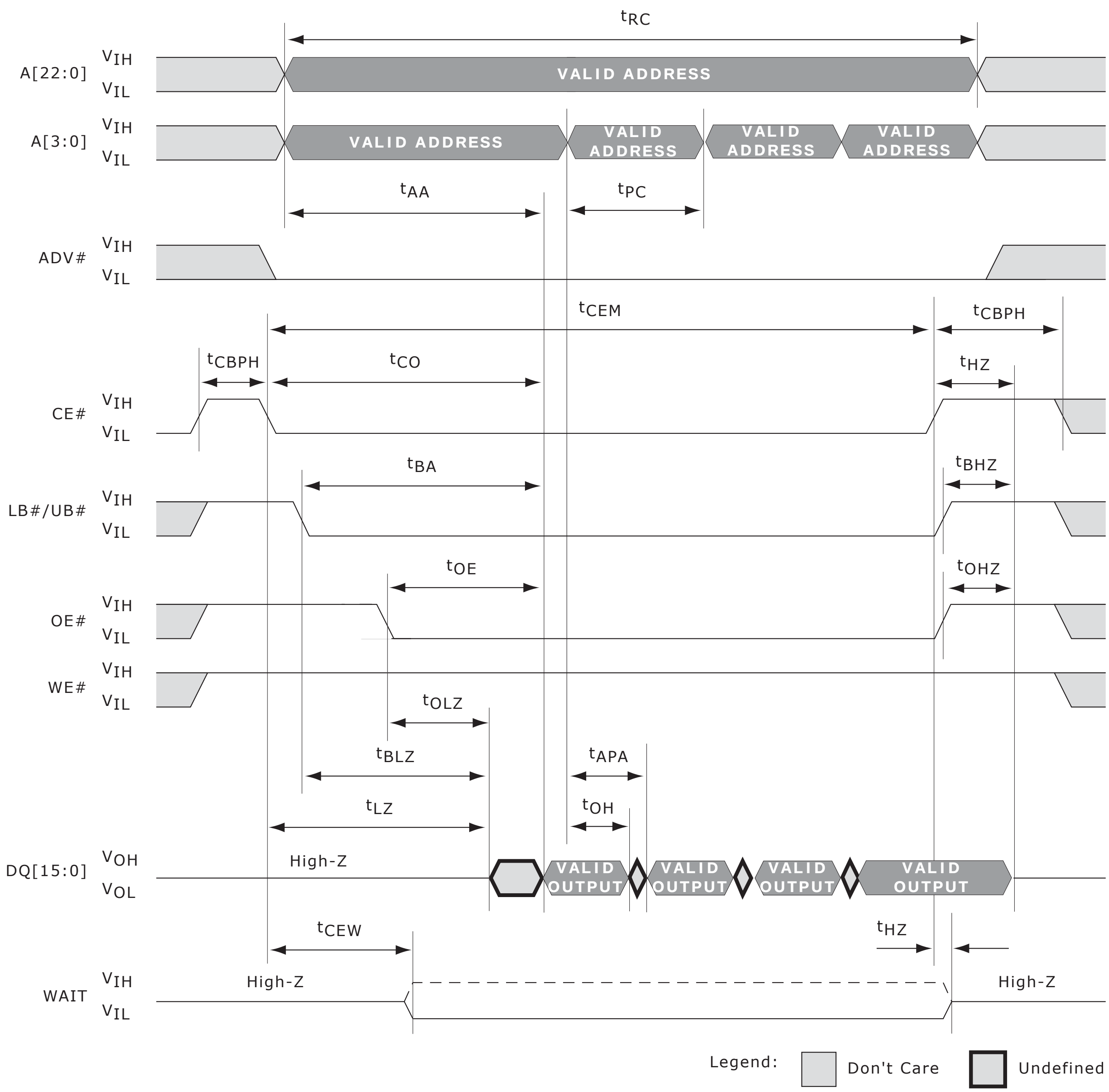
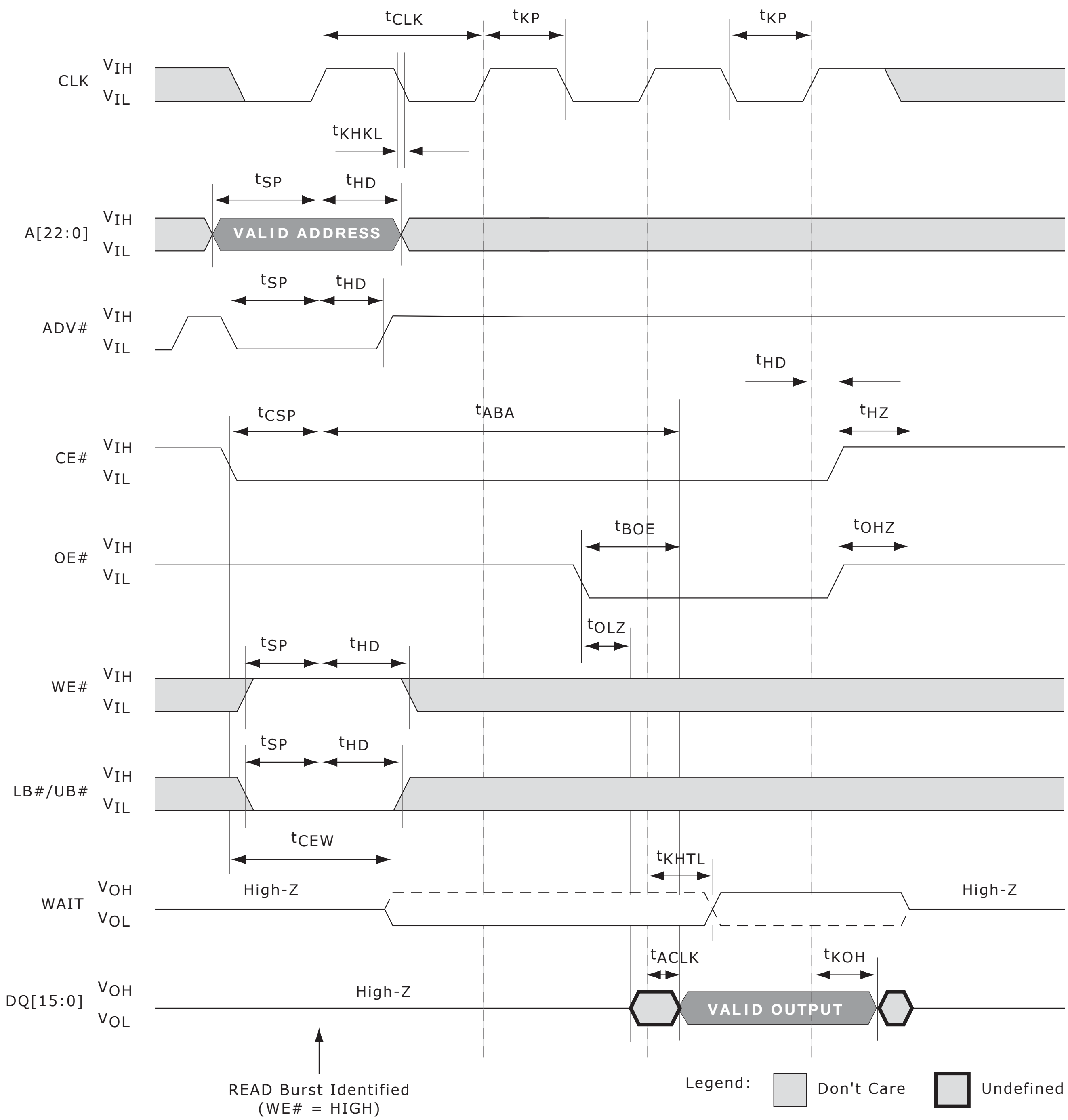


Figure 34.6 Page Mode Read

Table 34.4 Asynchronous Read Timing Parameters—Page Mode Operation

Symbol	70ns/80 MHz		85ns/66 MHz		Units
	Min	Max	Min	Max	
t_{AA}		70		85	ns
t_{APA}		20		25	ns
t_{BA}		70		85	ns
t_{BHZ}		8		8	ns
t_{BLZ}	10		10		ns
t_{CBPH}	5		5		ns
t_{CEM}		4		4	µs
t_{CEW}	1	7.5	1	7.5	ns
t_{CO}		70		85	ns
t_{HZ}		8		8	ns
t_{LZ}	10		10		ns
t_{OE}		20		20	ns
t_{OH}	5		5		ns
t_{OHZ}		8		8	ns
t_{OLZ}	5		5		ns
t_{PC}	20		25		ns
t_{RC}	70		85		ns

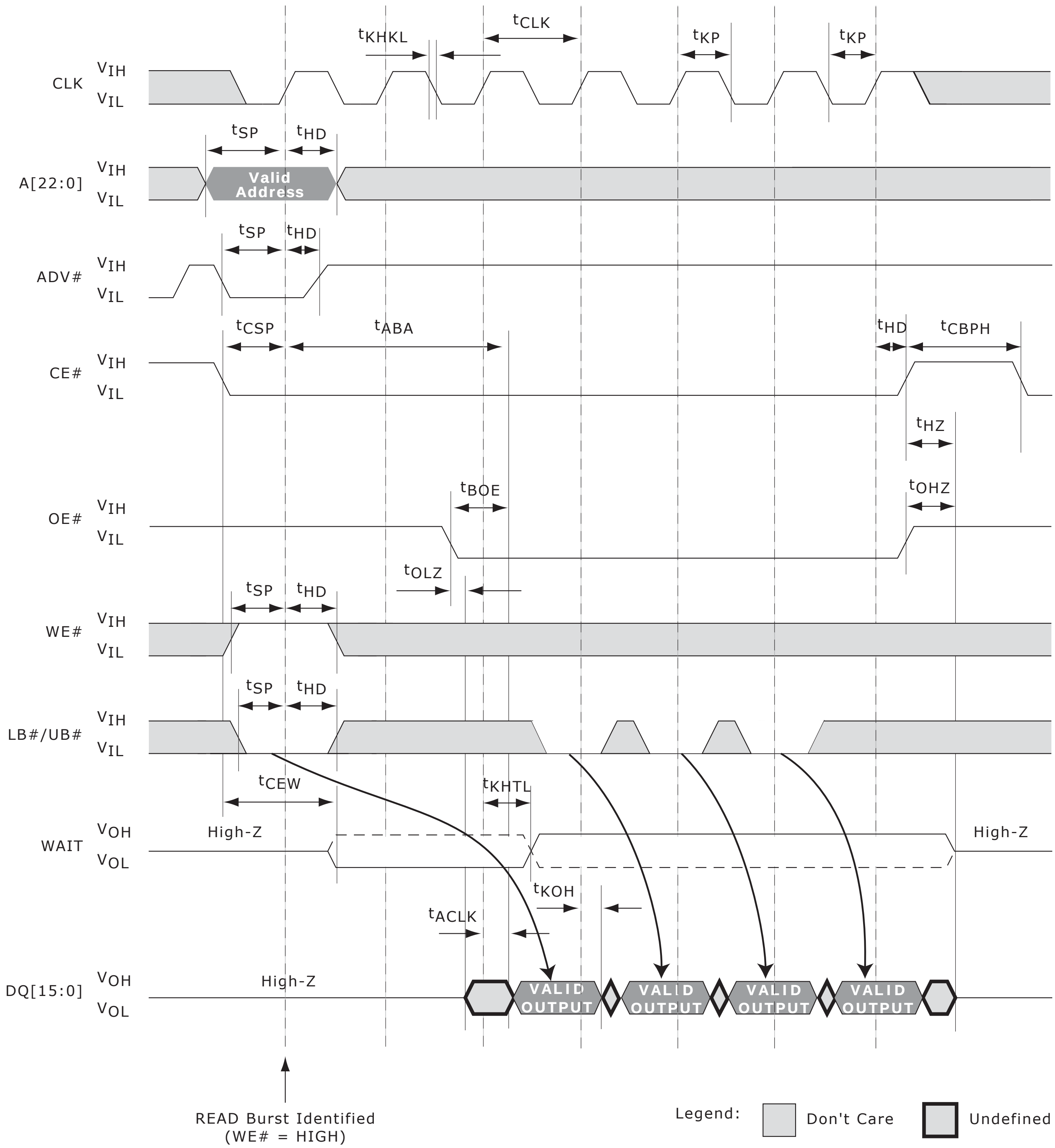


Note: *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*

Figure 34.7 Single-Access Burst Read Operation—Variable Latency

Table 34.5 Burst Read Timing Parameters—Single Access, Variable Latency

Symbol	70ns/80 MHz		85ns/66 MHz		Units
	Min	Max	Min	Max	
t_{ABA}		35		55	ns
t_{ACLK}		9		11	ns
t_{BOE}		20		20	ns
t_{CEW}	1	7.5	1	7.5	ns
t_{CLK}	12.5		15		ns
t_{CSP}	4		5		ns
t_{HD}	2		2		ns
t_{HZ}		8		8	ns
t_{KHKL}		1.6		1.6	ns
t_{KHTL}		9		11	ns
t_{KOH}	2		2		ns
t_{KP}	3		3		ns
t_{OHZ}		8		8	ns
t_{OLZ}	5		5		ns
t_{SP}	3		3		ns

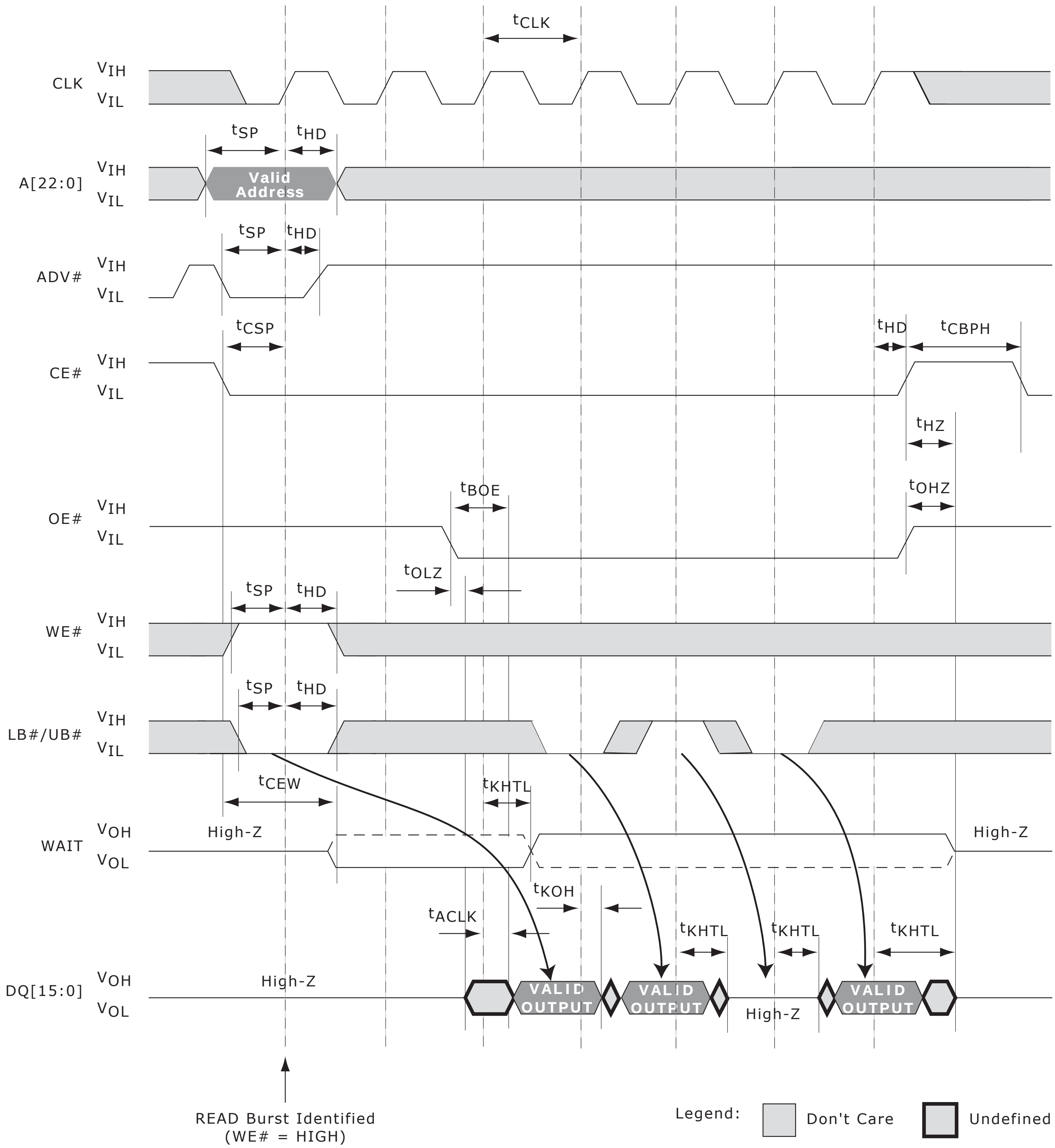


Note: *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*

Figure 34.8 Four-word Burst Read Operation—Variable Latency

Table 34.6 Burst Read Timing Parameters—4-word Burst

Symbol	70ns/80 MHz		85ns/66 MHz		Units
	Min	Max	Min	Max	
t_{ABA}		35		55	ns
t_{ACLK}		9		11	ns
t_{BOE}		20		20	ns
t_{CBPH}	5		5		ns
t_{CEW}	1	7.5	1	7.5	ns
t_{CLK}	12.5		15		ns
t_{CSP}	4		5		ns
t_{HD}	2		2		ns
t_{HZ}		8		8	ns
t_{KHKL}		1.6		1.6	ns
t_{KHTL}		9		11	ns
t_{KOH}	2		2		ns
t_{KP}	3		3		ns
t_{OHZ}		8		8	ns
t_{OLZ}	5		5		ns
t_{SP}	3		3		ns

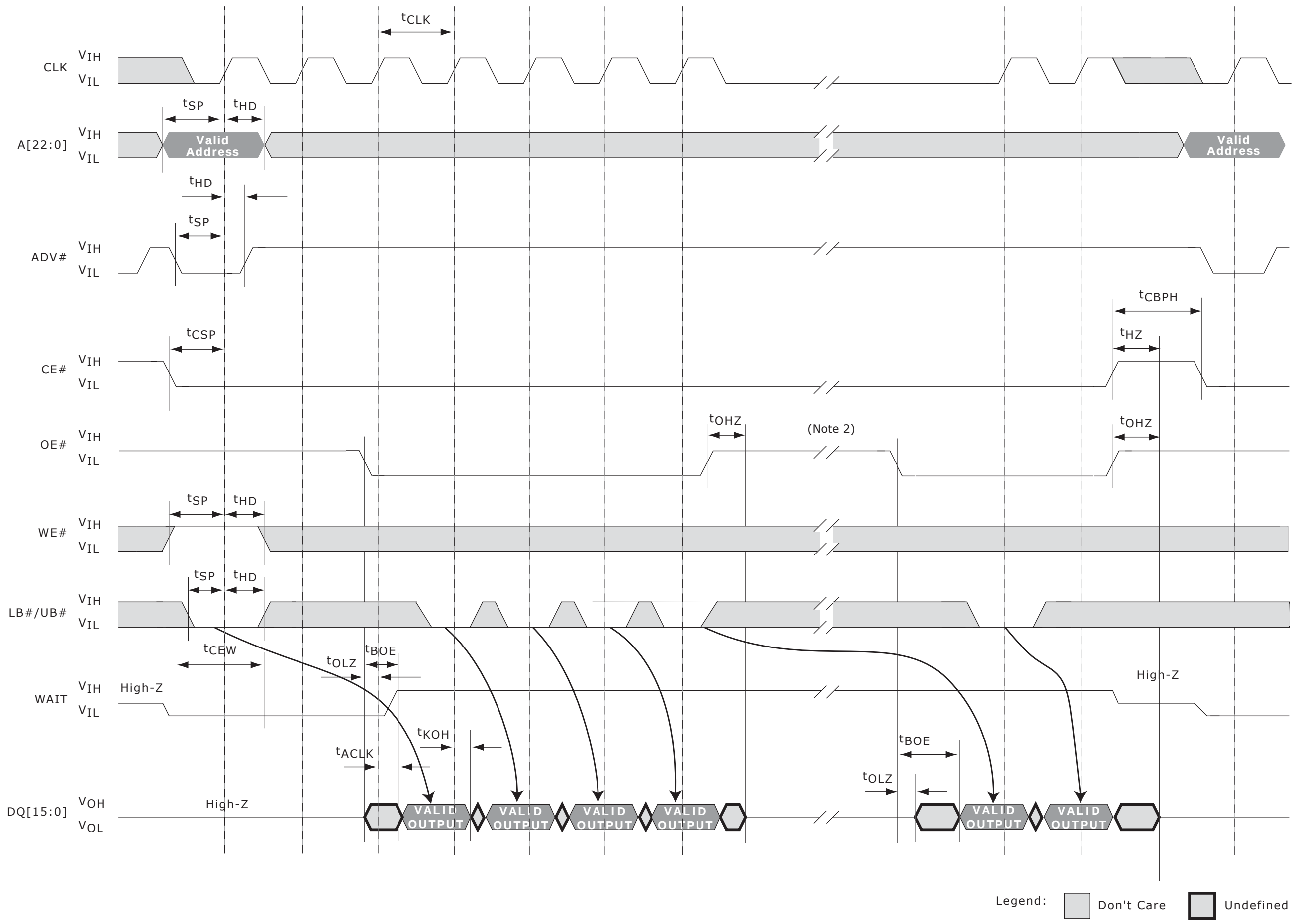


Note: *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*

Figure 34.9 Four-word Burst Read Operation (with LB#/UB#)

Table 34.7 Burst Read Timing Parameters—4-word Burst with LB#/UB#

Symbol	70ns/80 MHz		85ns/66 MHz		Units
	Min	Max	Min	Max	
t_{ACLK}		9		11	ns
t_{BOE}		20		20	ns
t_{CBPH}	5		5		ns
t_{CEW}	1	7.5	1	7.5	ns
t_{CLK}	12.5		15		ns
t_{CSP}	4		5		ns
t_{HD}	2		2		ns
t_{HZ}		8		8	ns
t_{KHTL}		9		11	ns
t_{KHZ}	3	8	3	8	ns
t_{KLZ}	2	5	2	5	ns
t_{KOH}	2		2		ns
t_{OHZ}		8		8	ns
t_{OLZ}	5		5		ns
t_{SP}	3		3		ns



Notes:

1. *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*
2. *OE# can stay Low during burst suspend. If OE# is Low, DQ[15:0] will continue to output valid data.*

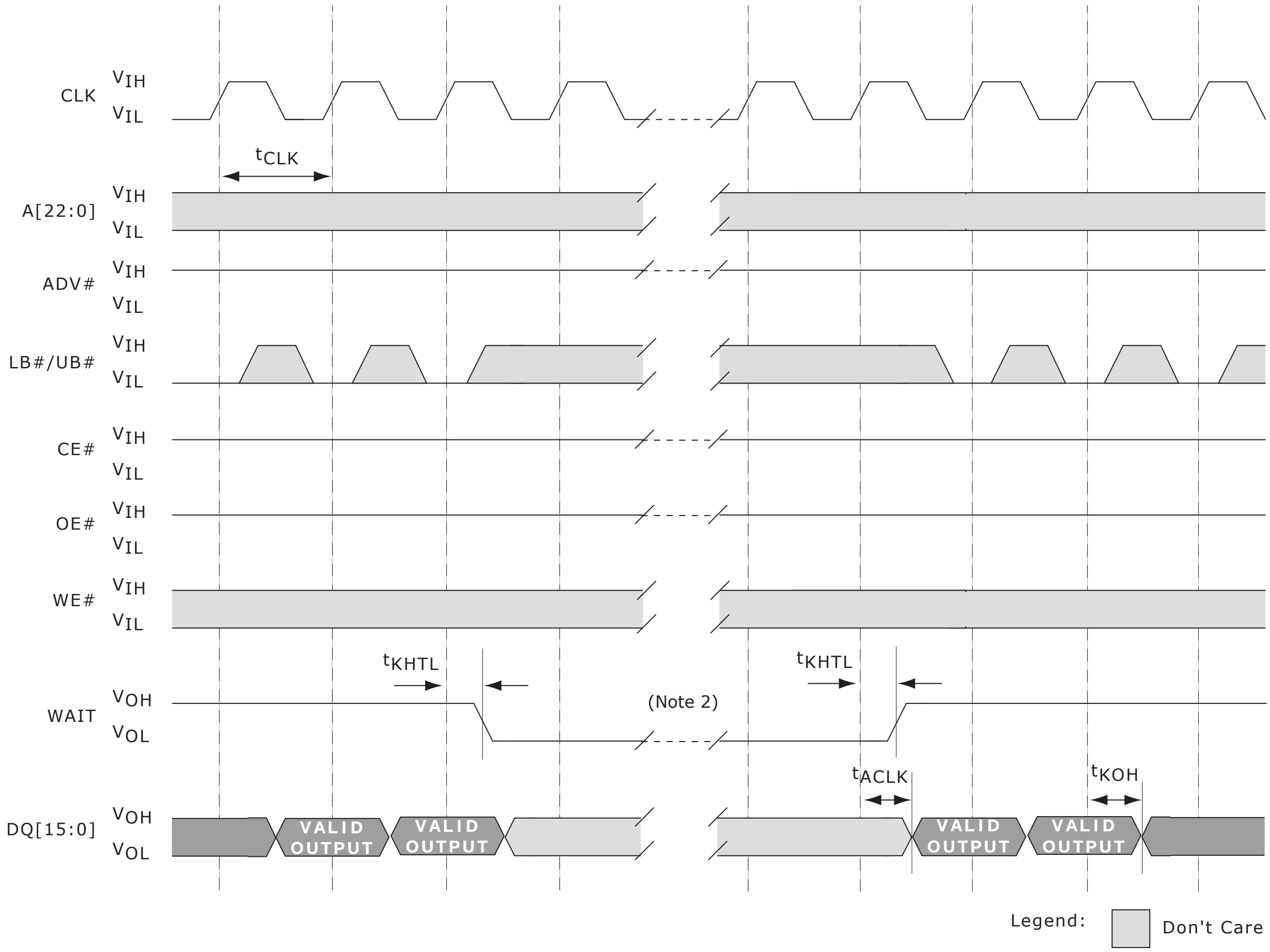
Figure 34.10 Refresh Collision During Write Operation

Table 34.8 Burst Read Timing Parameters—Burst Suspend

Symbol	70ns/80 MHz		85ns/66 MHz		Units
	Min	Max	Min	Max	
t_{ACLK}		9		11	ns
t_{BOE}		20		20	ns
t_{CBPH}	5		5		ns
t_{CLK}	12.5		15		ns
t_{CSP}	4		5		ns
t_{HD}	2		2		ns
t_{HZ}		8		8	ns
t_{KOH}	2		2		ns
t_{OHZ}		8		8	ns
t_{OLZ}	5		5		ns

Table 34.8 Burst Read Timing Parameters—Burst Suspend (Continued)

Symbol	70ns/80 MHz		85ns/66 MHz		Units
	Min	Max	Min	Max	
t_{SP}	3		3		ns



Notes:
1. *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*
2. *Wait will assert LC + 1 or 2LC + 1 cycles for variable latency (depending upon refresh status).*

Figure 34.9. Continuous Burst Read Showing an Output Delay with BCR[8] = 0 for End-of-Row Condition

Table 34.10 Burst Read Timing Parameters—BCR[8] = 0

Symbol	70ns/80 MHz		85ns/66 MHz		Units
	Min	Max	Min	Max	
t_{ACLK}		9		11	ns
t_{CLK}	12.5		15		ns
t_{KHTL}		9		11	ns
t_{KOH}	2		2		ns

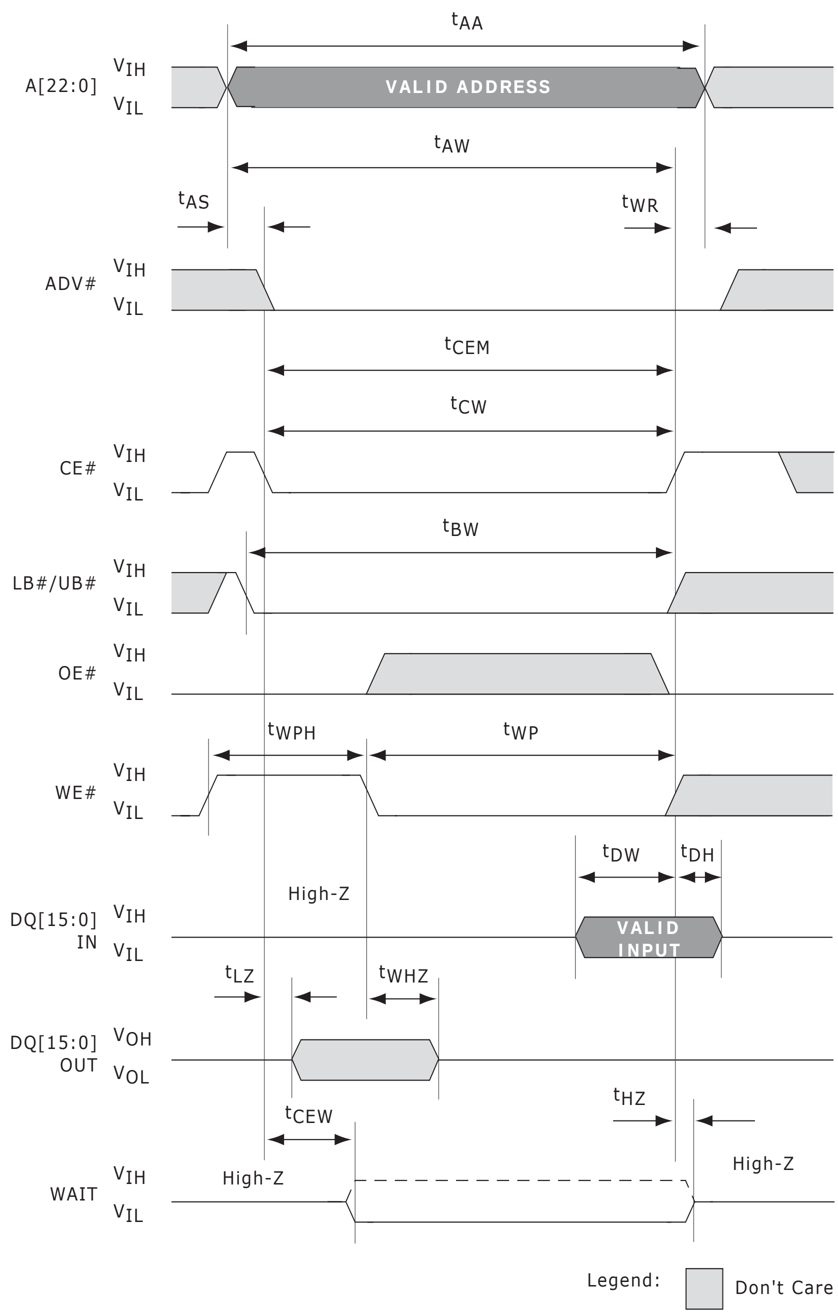


Figure 34.11 CE#-Controlled Asynchronous Write

Table 34.11 Asynchronous Write Timing Parameters—CE#-Controlled

Symbol	70ns/80 MHz		85ns/66 MHz		Units
	Min	Max	Min	Max	
t_{AS}	0		0		ns
t_{AW}	70		85		ns
t_{BW}	70		85		ns
t_{CEM}		4		4	µs
t_{CEW}	1	7.5	1	7.5	ns
t_{CW}	70		85		ns
t_{DH}	0		0		ns
t_{DW}	23		23		ns
t_{HZ}		8		8	ns
t_{LZ}	10		10		ns
t_{WC}	70		85		ns
t_{WHZ}		8		8	ns
t_{WP}	46		55		ns
t_{WPH}	10		10		ns
t_{WR}	0		0		ns

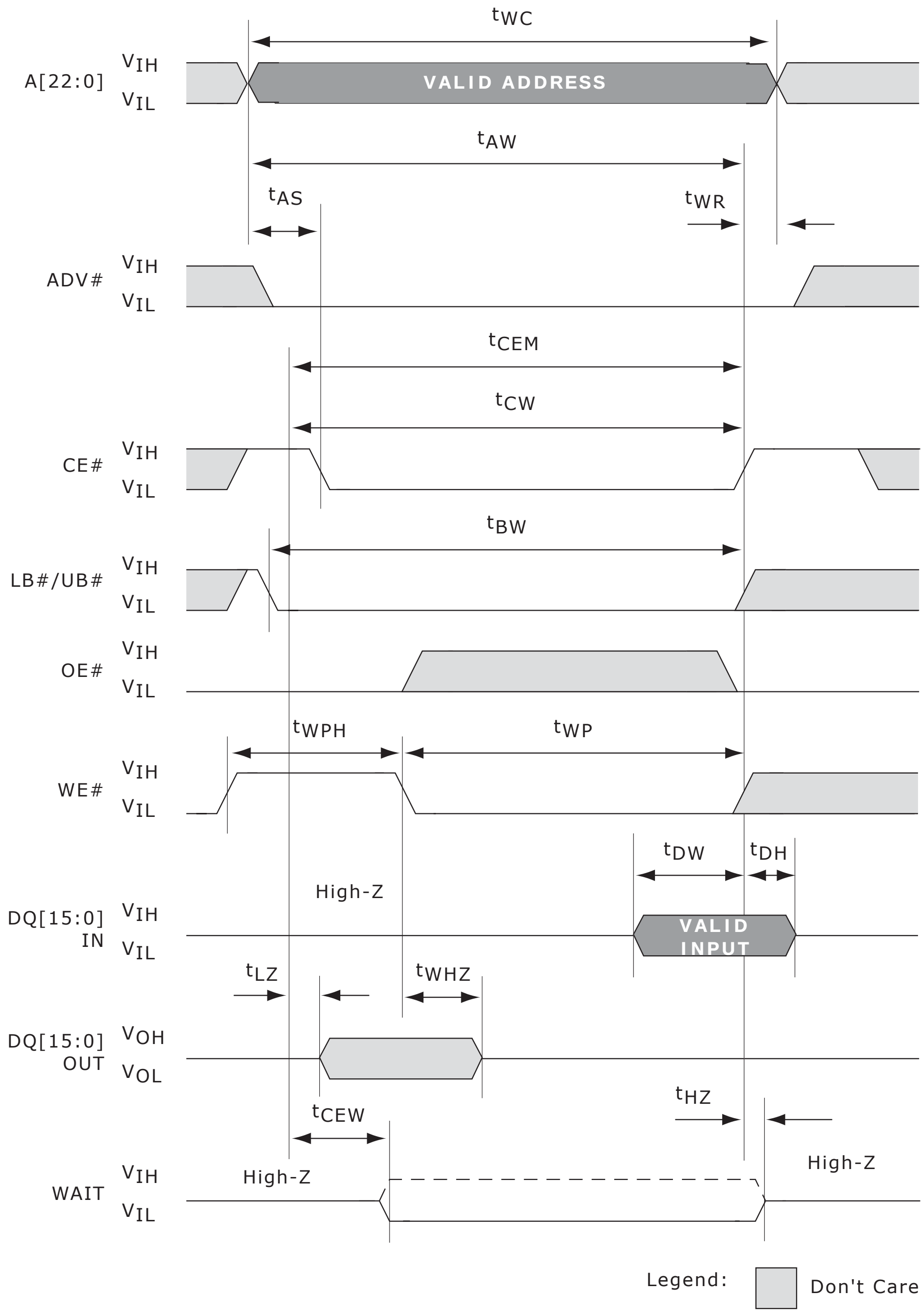


Figure 34.12 LB#/UB#-Controlled Asynchronous Write

Table 34.12 Asynchronous Write Timing Parameters—LB#/UB#-Controlled

Symbol	70ns/80 MHz		85ns/66 MHz		Units
	Min	Max	Min	Max	
t_{AS}	0		0		ns
t_{AW}	70		85		ns
t_{BW}	70		85		ns
t_{CEM}		4		4	µs
t_{CEW}	1	7.5	1	7.5	ns
t_{CW}	70		85		ns
t_{DH}	0		0		ns
t_{DW}	23		23		ns
t_{HZ}		8		8	ns
t_{LZ}	10		10		ns
t_{WC}	70		85		ns
t_{WHZ}		8		8	ns
t_{WP}	46		55		ns
t_{WPH}	10		10		ns
t_{WR}	0		0		ns

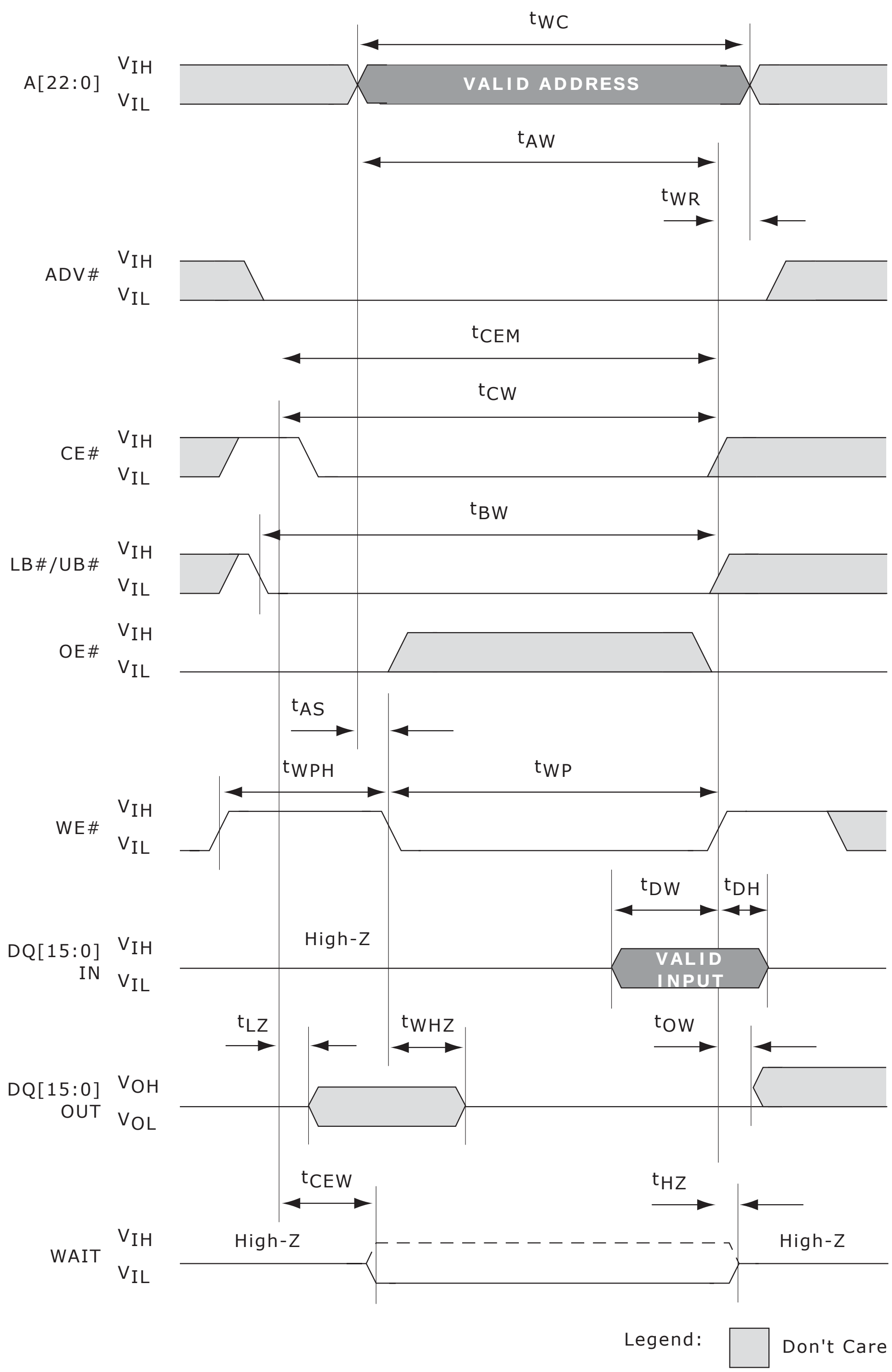


Figure 34.13 WE#-Controlled Asynchronous Write

Table 34.13 Asynchronous Write Timing Parameters—WE#-Controlled

Symbol	70ns/80 MHz		85ns/66 MHz		Units
	Min	Max	Min	Max	
t_{AS}	0		0		ns
t_{AW}	70		85		ns
t_{BW}	70		85		ns
t_{CEM}		4		4	µs
t_{CEW}	1	7.5	1	7.5	ns
t_{CW}	70		85		ns
t_{DH}	0		0		ns
t_{DW}	23		23		ns
t_{HZ}		8		8	ns
t_{LZ}	10		10		ns
t_{OW}	5		5		ns
t_{WC}	70		85		ns
t_{WHZ}		8		8	ns
t_{WP}	46		55		ns
t_{WPH}	10		10		ns
t_{WR}	0		0		ns

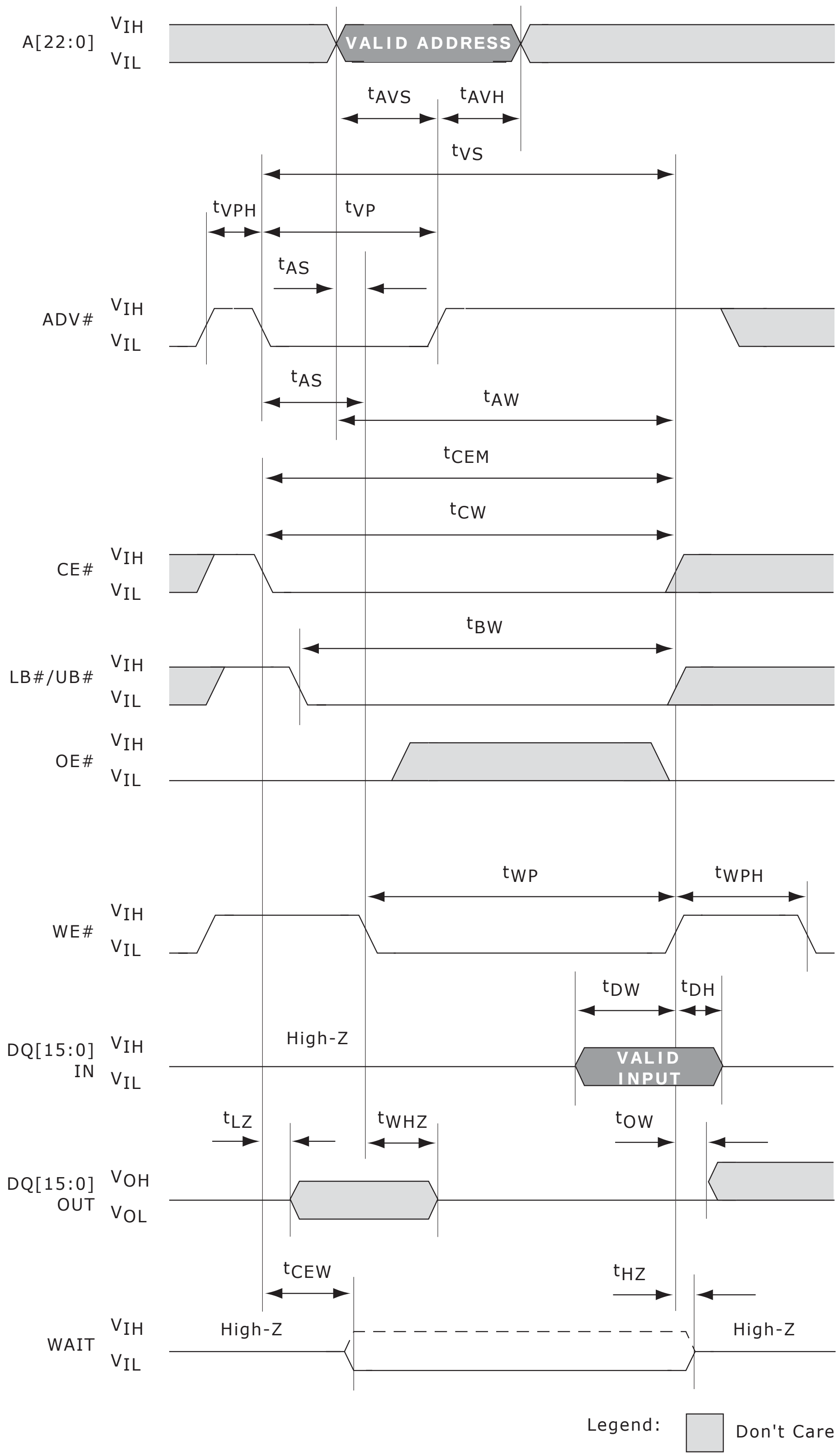
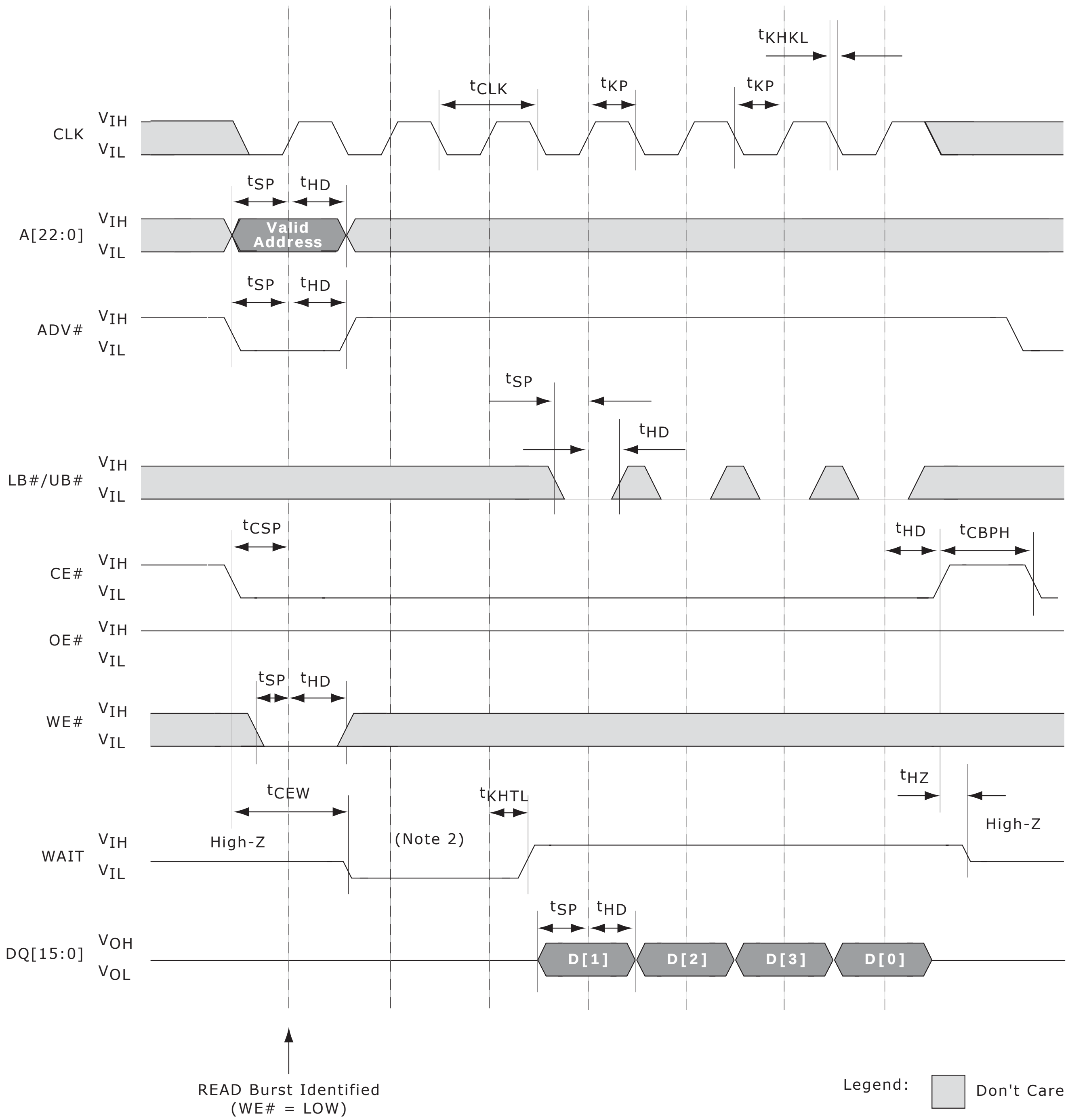


Figure 34.14 Asynchronous Write Using ADV#

Table 34.14 Asynchronous Write Timing Parameters Using ADV#

Symbol	70ns/80 MHz		85ns/66 MHz		Units
	Min	Max	Min	Max	
t_{AS}	0		0		ns
t_{AVH}	5		5		ns
t_{AVS}	10		10		ns
t_{AW}	70		85		ns
t_{BW}	70		85		ns
t_{CEM}		4		4	µs
t_{CEW}	1	7.5	1	7.5	ns
t_{CW}	70		85		ns
t_{DH}	0		0		ns
t_{DW}	23		23		ns
t_{HZ}		8		8	ns
t_{LZ}	10		10		ns
t_{OW}	5		5		ns
t_{AS}	0		0		ns
t_{VP}	10		10		ns
t_{VPH}	10		10		ns
t_{VS}	70		85		ns
t_{WHZ}		8		8	ns
t_{WP}	46		55		ns
t_{WPH}	10		10		ns



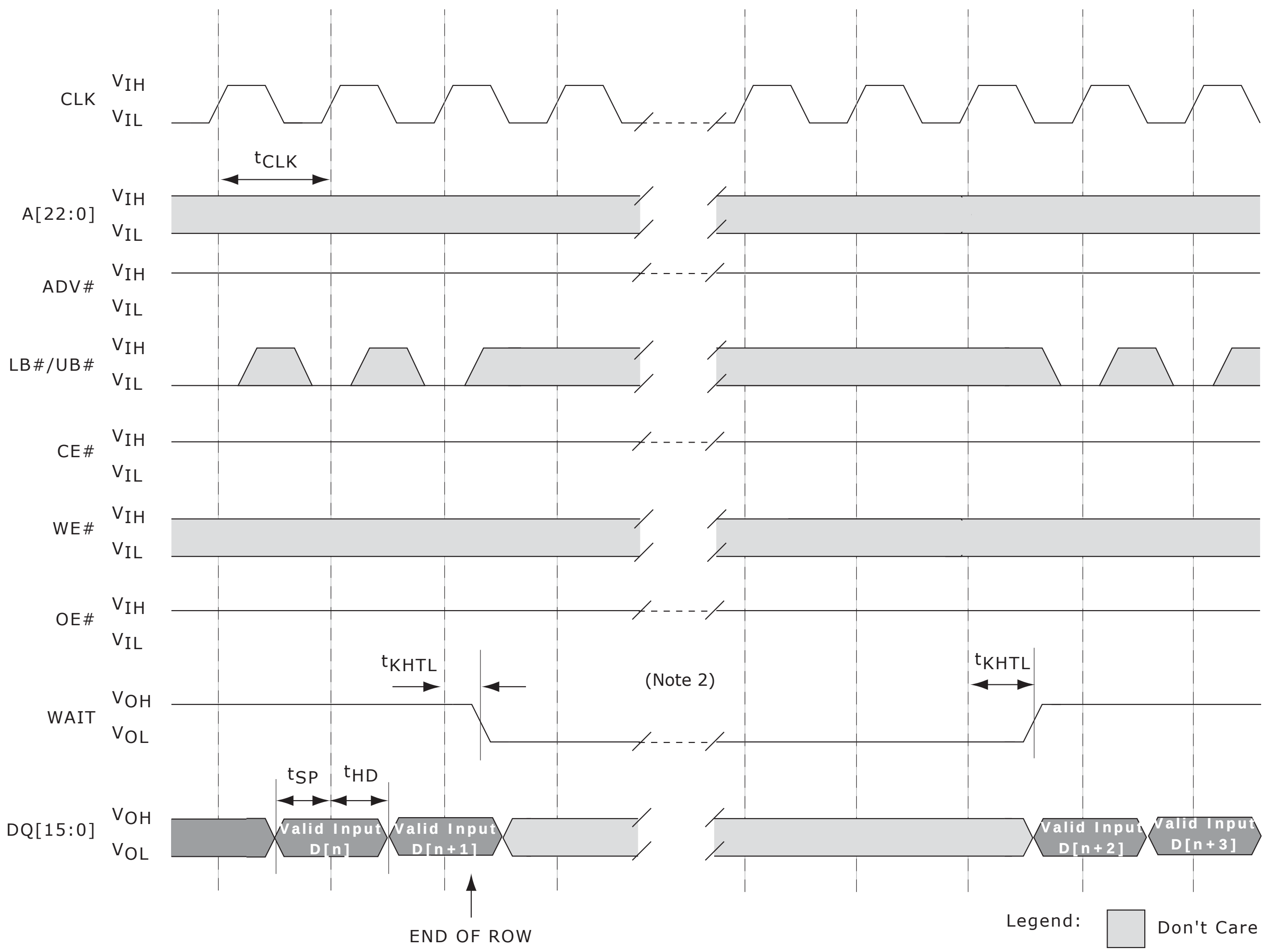
Notes:

1. *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay; burst length four; burst wrap enabled.*

Figure 34.15 Burst Write Operation

Table 34.15 Burst Write Timing Parameters

Symbol	70ns/80 MHz		85ns/66 MHz		Units
	Min	Max	Min	Max	
t_{CBPH}	5		5		ns
t_{CEW}	1	7.5	1	7.5	ns
t_{CLK}	12.5		15		ns
t_{CSP}	4		5		ns
t_{HD}	2		2		ns
t_{HZ}		8		8	ns
t_{KHKL}		1.6		1.6	ns
t_{KHTL}		9		11	ns
t_{KP}	3		3		ns
t_{SP}	3		3		ns



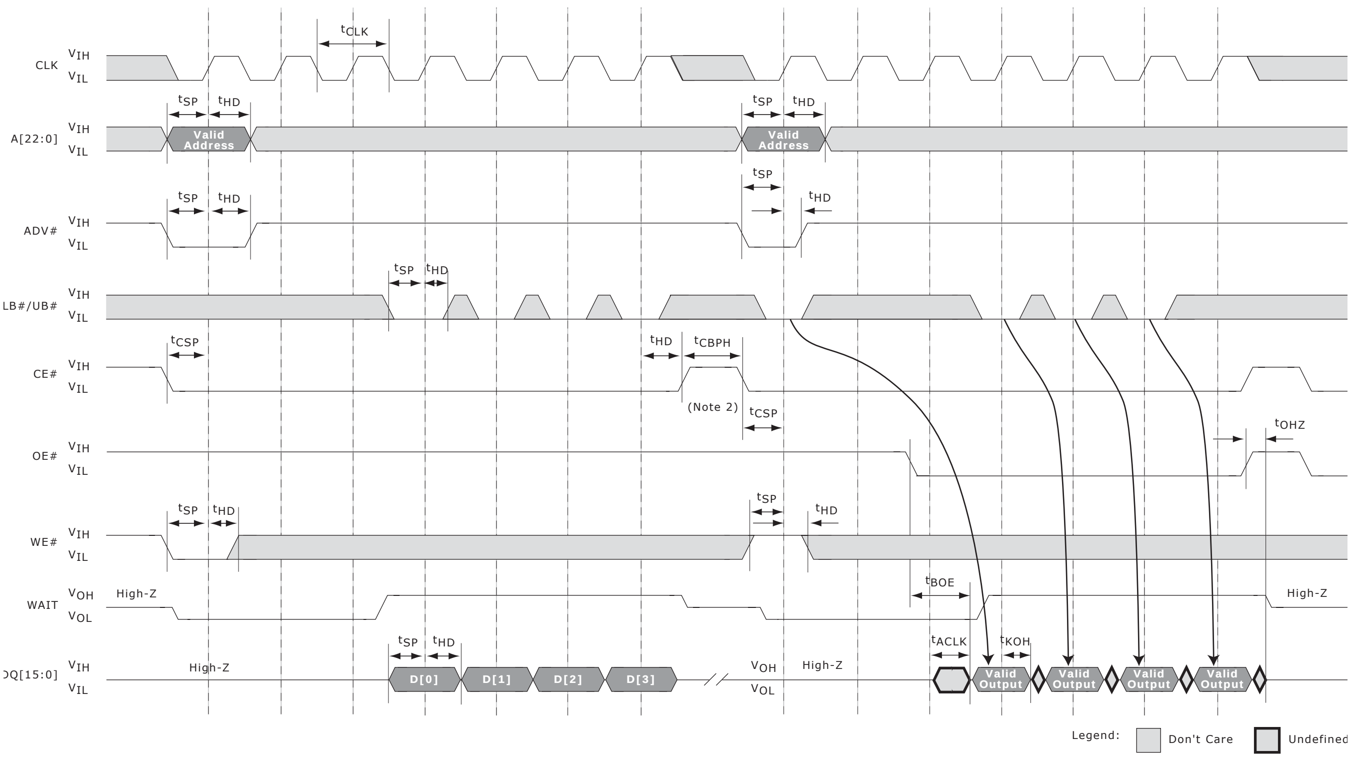
Notes:

1. *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*
2. *Wait will assert LC + 1 or 2LC + 1 cycles for variable latency (depending upon refresh status).*

Figure 34.16 Continuous Burst Write Showing an Output Delay with BCR[8] = 0 for End-of-Row Condition

Table 34.16 Burst Write Timing Parameters—BCR[8] = 0

Symbol	70ns/80 MHz		85ns/66 MHz		Units
	Min	Max	Min	Max	
t_{CLK}	12.5		15		ns
t_{HD}	2		2		ns
t_{KHTL}		8		11	ns
t_{SP}		3		3	ns



Notes:

1. Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.
1. To allow self-refresh operations to occur between transactions, CE# must remain High for at least 5ns (t_{CBPH}) to schedule the appropriate internal refresh operation. CE# can stay Low between burst Read and burst Write operations. See How Extended Timings Impact CellularRAM™ Operation for restrictions on the maximum CE# Low time (t_{CEM}).

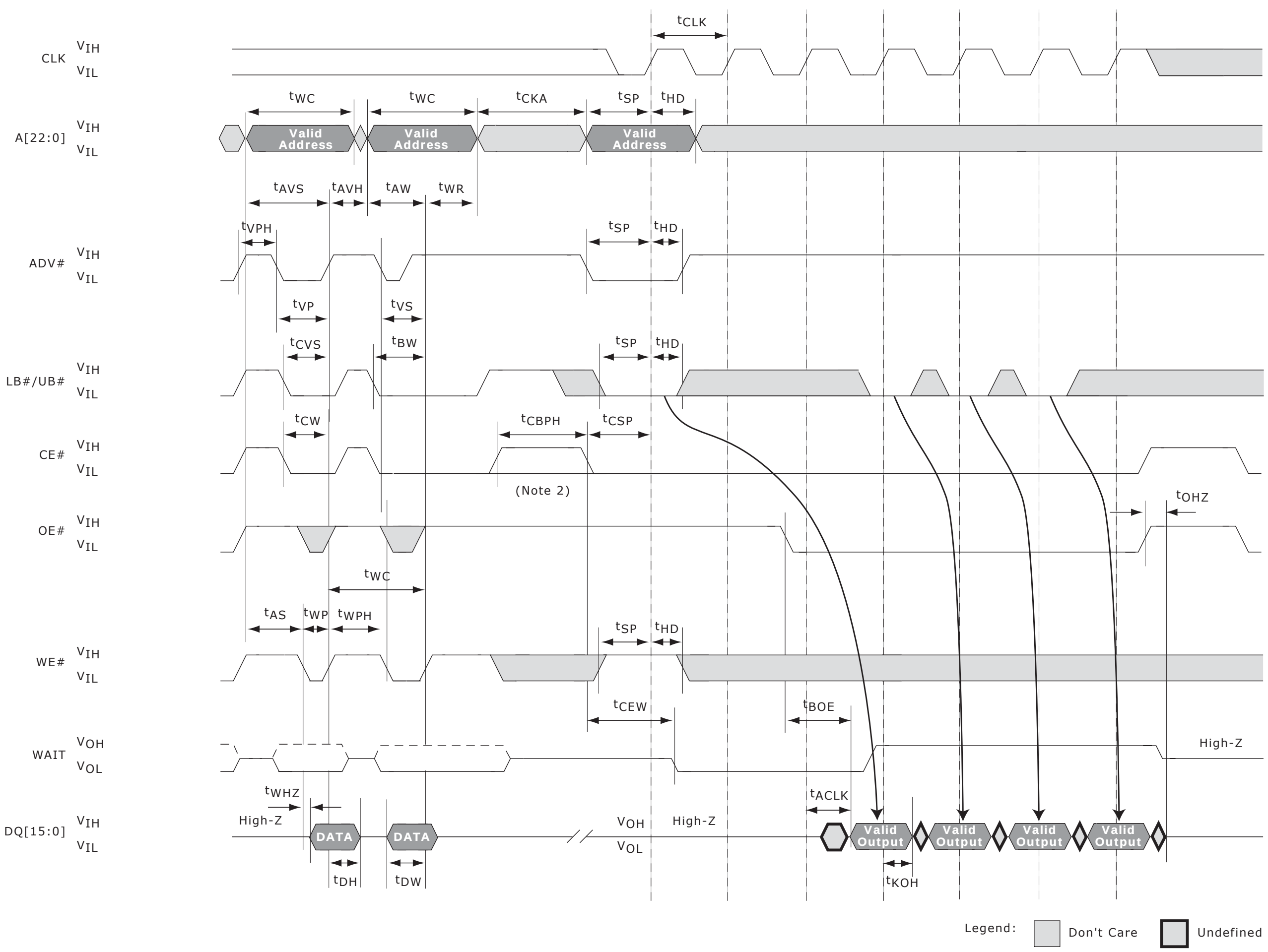
Figure 34.17 Burst Write Followed by Burst Read

Table 34.17 Write Timing Parameters—Burst Write Followed by Burst Read

Symbol	70ns/80 MHz		85ns/66 MHz		Units
	Min	Max	Min	Max	
t_{CBPH}	5		5		ns
t_{CLK}	12.5	20	15	20	ns
t_{CSP}	4	20	5	20	ns
t_{HD}	2		2		ns
t_{SP}	3		3		ns

Table 34.18 Read Timing Parameters—Burst Write Followed by Burst Read

Symbol	70ns/80 MHz		85ns/66 MHz		Units
	Min	Max	Min	Max	
t_{ACLK}	9		11	ns	
t_{BOE}		20		20	ns
t_{CLK}	12.5		15		ns
t_{CSP}	4		5		ns
t_{HD}	2		2		ns
t_{KOH}	2		2		ns
t_{OHZ}		8		8	ns
t_{SP}	3		3		ns



Notes:

1. *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*
1. *When transitioning between asynchronous and variable-latency burst operations, CE# must go High. If CE# goes High, it must remain High for at least 5ns (t_{CBPH}) to schedule the appropriate internal refresh operation. See How Extended Timings Impact CellularRAM™ Operation for restrictions on the maximum CE# Low time (t_{CEM}).*

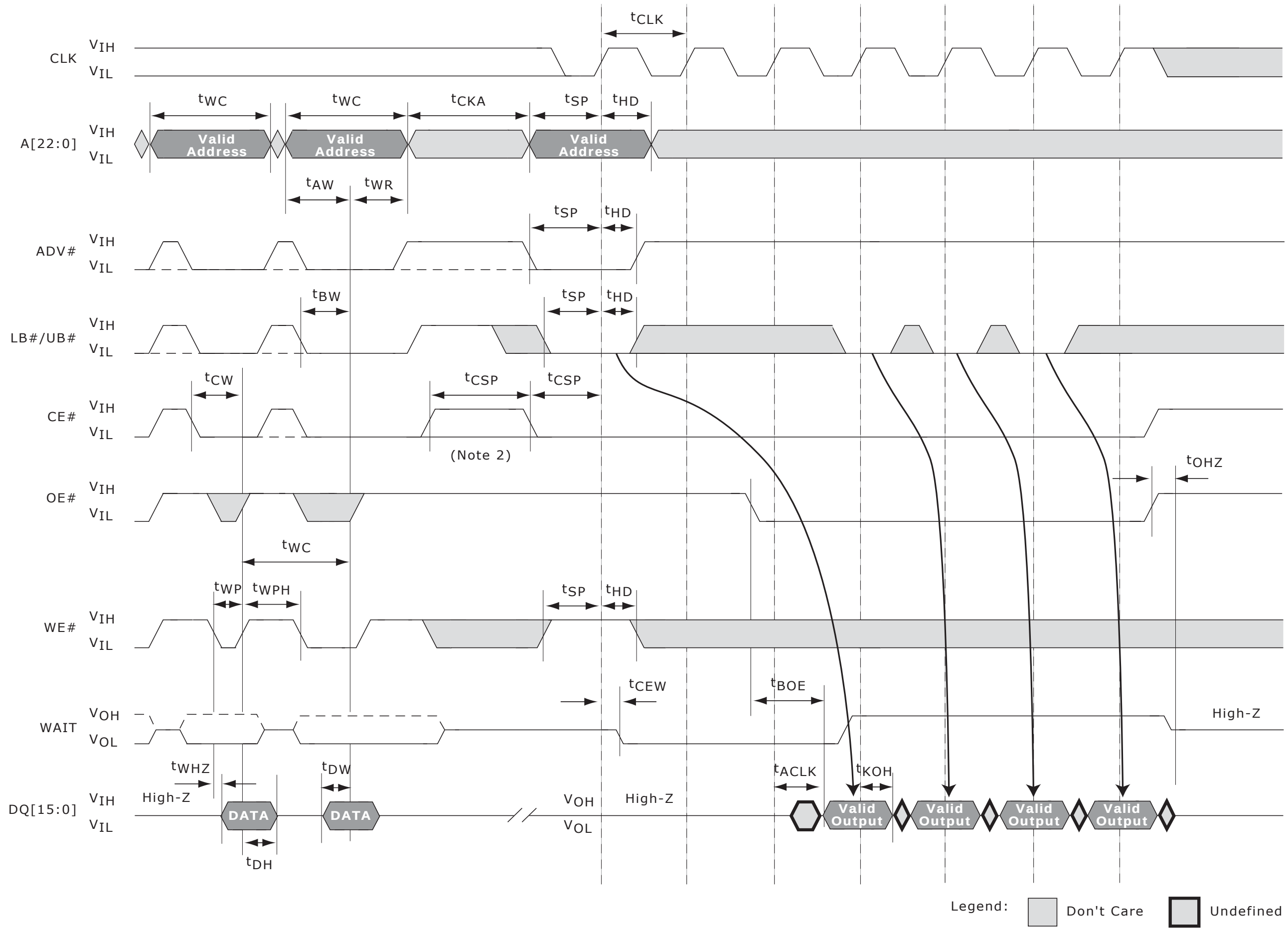
Figure 34.18 Asynchronous Write Followed by Burst Read

Table 34.19 Write Timing Parameters—Asynchronous Write Followed by Burst Read

Symbol	70ns/80 MHz		85ns/66 MHz		Units
	Min	Max	Min	Max	
t_{AVH}	5		5		ns
t_{AS}	0		0		ns
t_{AVS}	10		10		ns
t_{AW}	70		85		ns
t_{BW}	70		85		ns
t_{CKA}	70		85		ns
t_{CVS}	10		10		ns
t_{CW}	70		85		ns
t_{DH}	0		0		ns
t_{DW}	20		23		ns
t_{VP}	10		10		ns
t_{VPH}	10		10		ns
t_{VS}	70		85		ns
t_{WC}	70		85		ns
t_{WHZ}		8		8	ns
t_{WP}	46		55		ns
t_{WPH}	10		10		ns
t_{WR}	0		0		ns

Table 34.20 Read Timing Parameters—Asynchronous Write Followed by Burst Read

Symbol	70ns/80 MHz		85ns/66 MHz		Units
	Min	Max	Min	Max	
t_{ACLK}		9		11	ns
t_{BOE}		20		20	ns
t_{CBPH}	5		5		ns
t_{CEW}	1	7.5	1	7.5	ns
t_{CLK}	12.5		15		ns
t_{CSP}	4		5		ns
t_{HD}	2		2		ns
t_{KOH}	2		2		ns
t_{OHZ}		8		8	ns
t_{SP}	3		3		ns



Notes:

1. *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*
2. *When transitioning between asynchronous and variable-latency burst operations, CE# must go High. If CE# goes High, it must remain High for at least 5ns (t_{CBPH}) to schedule the appropriate internal refresh operation. See How Extended Timings Impact CellularRAM™ Operation for restrictions on the maximum CE# Low time (t_{CEM}).*

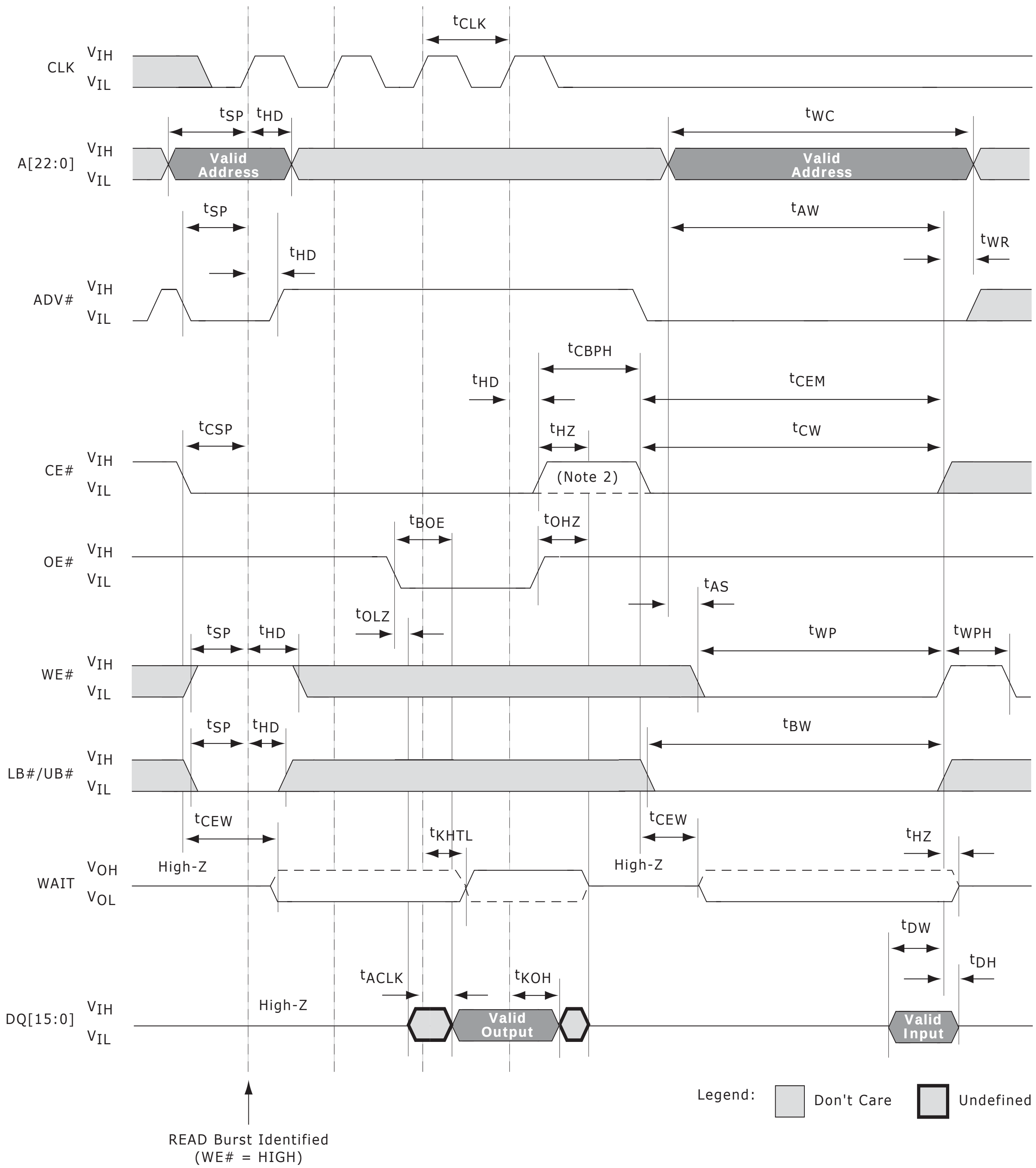
Figure 34.19 Asynchronous Write (ADV# Low) Followed By Burst Read

Table 34.21 Asynchronous Write Timing Parameters—ADV# Low

Symbol	70ns/80 MHz		85ns/66 MHz		Units
	Min	Max	Min	Max	
t_{AW}	70		85		ns
t_{BW}	70		85		ns
t_{CKA}	70		85		ns
t_{CW}	70		85		ns
t_{DH}	0		0		ns
t_{DW}	23		23		ns
t_{WC}	70		85		ns
t_{WHZ}		8		8	ns
t_{WP}	46		55		ns
t_{WPH}	10		10		ns
t_{WR}	0		0		ns

Table 34.22 Burst Read Timing Parameters

Symbol	70ns/80 MHz		85ns/66 MHz		Units
	Min	Max	Min	Max	
t_{ACLK}		9		11	ns
t_{BOE}		20		20	ns
t_{CBPH}	5		5		ns
t_{CEW}	1	7.5	1	7.5	ns
t_{CLK}	12.5		15		ns
t_{CSP}	4		5		ns
t_{HD}	2		2		ns
t_{KOH}	2		2		ns
t_{OHZ}		8		8	ns
t_{SP}	3		3		ns



Notes:

1. *Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.*
2. *When transitioning between asynchronous and variable-latency burst operations, CE# must go High. If CE# goes High, it must remain High for at least 5ns (t_{CBPH}) to schedule the appropriate internal refresh operation. See How Extended Timings Impact CellularRAM™ Operation for restrictions on the maximum CE# Low time (t_{CEM}).*

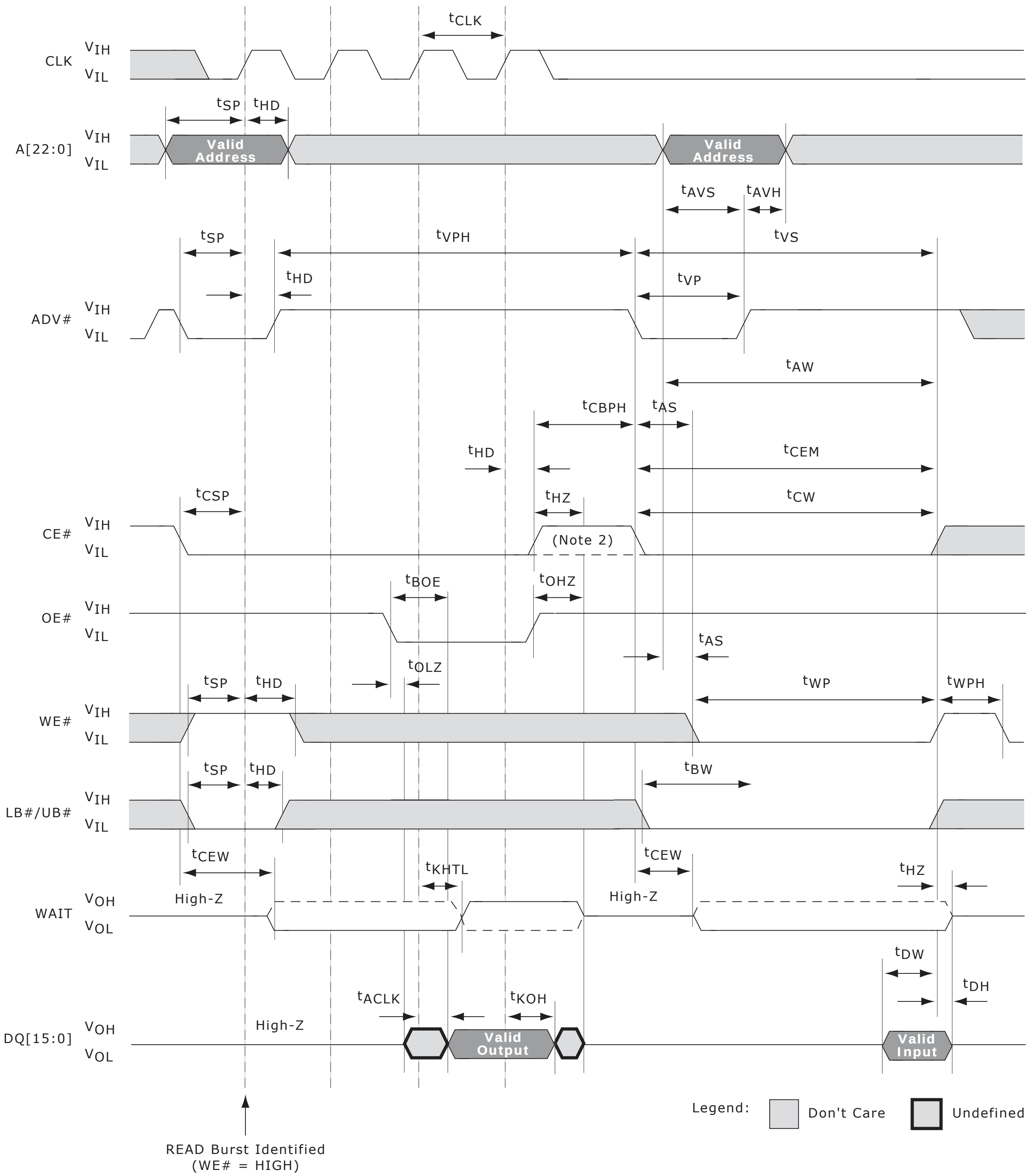
Figure 34.23. Burst Read Followed by Asynchronous Write (WE#-Controlled)

Table 34.24 Burst Read Timing Parameters

Symbol	70ns/80 MHz		85ns/66 MHz		Units
	Min	Max	Min	Max	
t_{ACLK}		9		11	ns
t_{BOE}		20		20	ns
t_{CBPH}	5		5		ns
t_{CEW}	1	7.5	1	7.5	ns
t_{CLK}	12.5		15		ns
t_{CSP}	4		5		ns
t_{HD}	2		2		ns
t_{HZ}		8		8	ns
t_{KHKL}		1.6		1.6	ns
t_{KHTL}		9		11	ns
t_{KOH}	2		2		ns
t_{KP}	3		3		ns
t_{OHZ}		8		8	ns

Table 34.25 Asynchronous Write Timing Parameters—WE# Controlled

Symbol	70ns/80 MHz		85ns/66 MHz		Units
	Min	Max	Min	Max	
t_{AS}	0			0	ns
t_{AW}	70		85		ns
t_{BW}	70		85		ns
t_{CEM}		4		4	µs
t_{CW}	70		85		ns
t_{DH}	0		0		ns
t_{DW}	23		23		ns
t_{HZ}		8		8	ns
t_{WC}	70		85		ns
t_{WP}	46		55		ns
t_{WPH}	10		10		ns
t_{WR}	0		0		ns



Notes:

1. Non-default BCR settings: Latency code two (three clocks); Wait active Low; Wait asserted during delay.
2. When transitioning between asynchronous and variable-latency burst operations, CE# must go High. If CE# goes High, it must remain High for at least 5ns (t_{CBPH}) to schedule the appropriate internal refresh operation. See How Extended Timings Impact CellularRAM™ Operation for restrictions on the maximum CE# Low time (t_{CEM}).

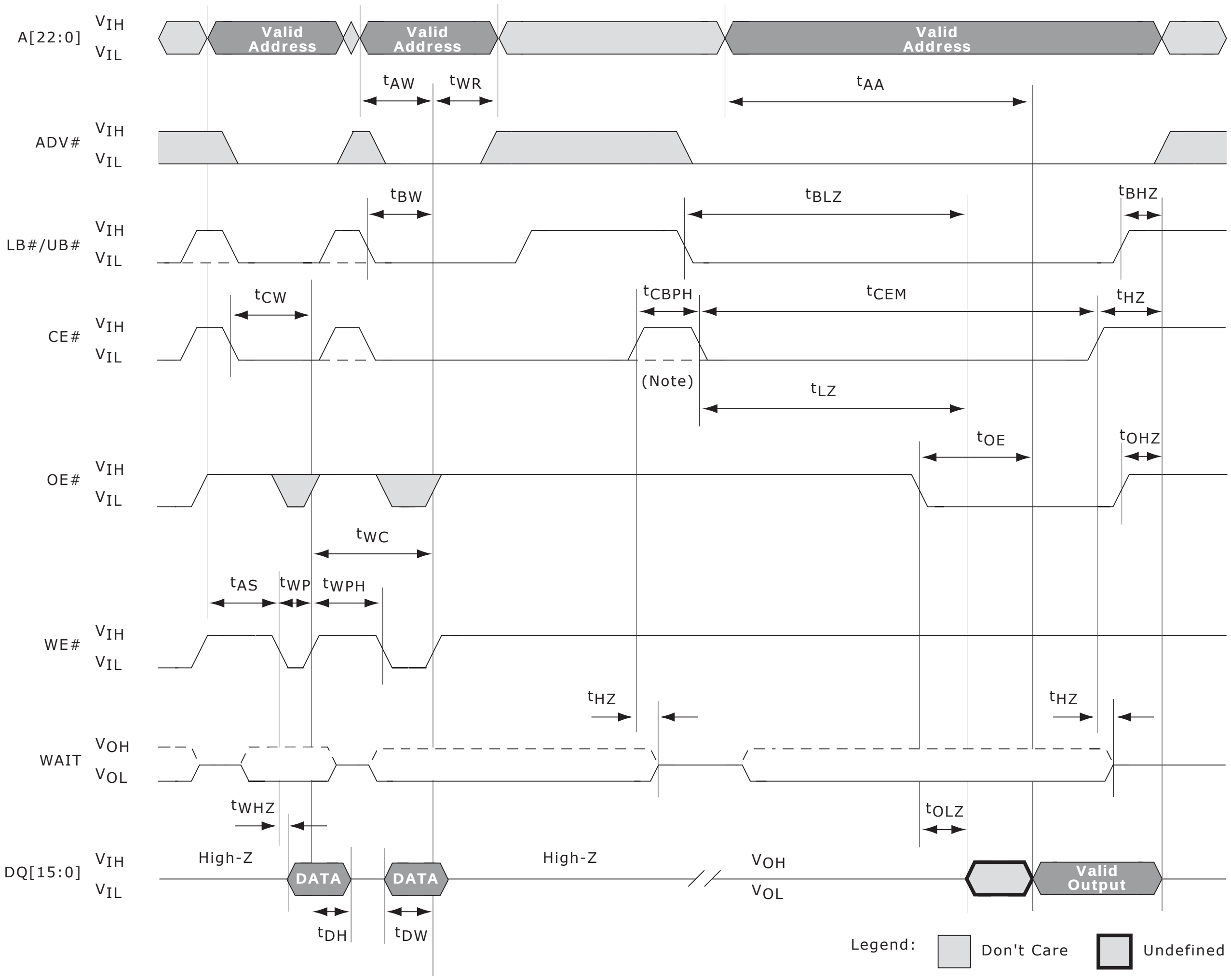
Figure 34.26. Burst Read Followed by Asynchronous Write Using ADV#

Table 34.27 Burst Read Timing Parameters

Symbol	70ns/80 MHz		85ns/66 MHz		Units
	Min	Max	Min	Max	
t_{ACLK}		9		11	ns
t_{BOE}		20		20	ns
t_{CBPH}	5		5		ns
t_{CEW}	1	7.5	1	7.5	ns
t_{CLK}	12.5		15		ns
t_{CSP}	4		5		ns
t_{HD}	2		2		ns
t_{HZ}		8		8	ns
t_{KHKL}		1.6		1.6	ns
t_{KHTL}		9		11	ns
t_{KOH}	2		2		ns
t_{KP}	3		3		ns
t_{OHZ}		8		8	ns

Table 34.28 Asynchronous Write Timing Parameters Using ADV#

Symbol	70ns/80 MHz		85ns/66 MHz		Units
	Min	Max	Min	Max	
t_{AS}	0		0		ns
t_{AVH}	5		5		ns
t_{AVS}	10		10		ns
t_{AW}	70		85		ns
t_{BW}	70		85		ns
t_{CEM}		4		4	µs
t_{CEW}	1	7.5	1	7.5	ns
t_{CW}	70		85		ns
t_{DH}	0		0		ns
t_{DW}	23		23		ns
t_{HZ}		8		8	ns
t_{VP}	10		10		ns
t_{VPH}	10		10		ns
t_{VS}	70		85		ns
t_{WP}	46		55		ns
t_{WPH}	10		10		ns
t_{WR}	0		0		ns



Note: *CE# can stay Low when transitioning between asynchronous operations. If CE# goes High, it must remain High for at least 5ns (t_{CBPH}) to schedule the appropriate internal refresh operation. See How Extended Timings Impact CellularRAM™ Operation for restrictions on the maximum CE# Low time (t_{CEM}).*

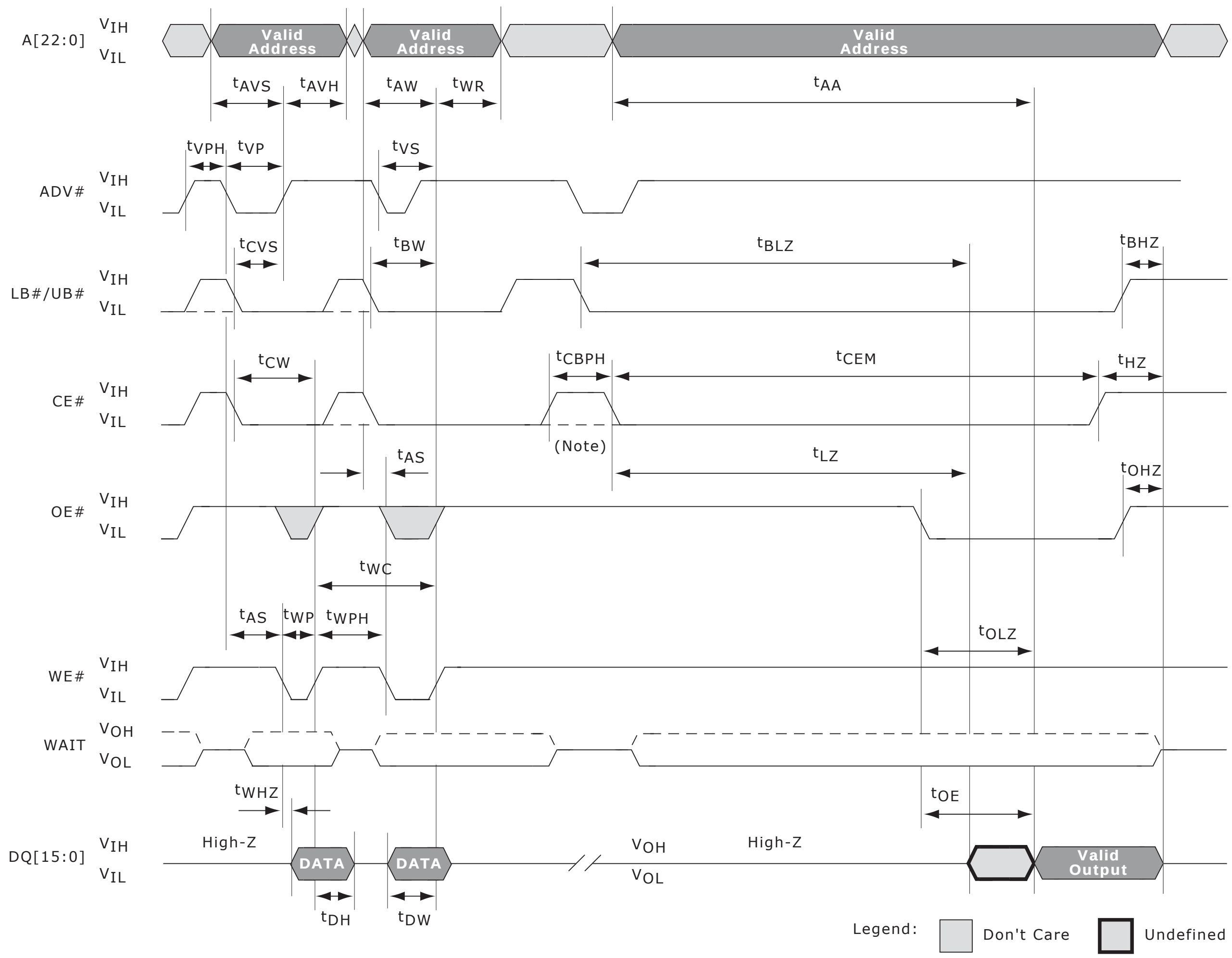
Figure 34.29. Asynchronous Write Followed by Asynchronous Read—ADV# Low

Table 34.30 Write Timing Parameters—ADV# Low

Symbol	70ns/80 MHz		85ns/66 MHz		Units
	Min	Max	Min	Max	
t_{AS}	0		0		ns
t_{AW}	70		85		ns
t_{BW}	70		85		ns
t_{CW}	70		85		ns
t_{DH}	0		0		ns
t_{DW}	23		23		ns
t_{HZ}		8		8	ns
t_{WC}	70		85		ns
t_{WHZ}		8		8	ns
t_{WP}	46		55		ns
t_{WPH}	10		10		ns
t_{WR}	0		0		ns

Table 34.31 Read Timing Parameters—ADV# Low

Symbol	70ns/80 MHz		85ns/66 MHz		Units
	Min	Max	Min	Max	
t_{AA}		70		85	ns
t_{BHZ}		8		8	ns
t_{BLZ}	10		10		ns
t_{CBPH}	5		5		ns
t_{CEM}		4		4	µs
t_{HZ}		8		8	ns
t_{LZ}	10		10		ns
t_{OE}		20		20	ns
t_{OHZ}		8		8	ns
t_{OLZ}	5		5		ns



Note: *CE# can stay Low when transitioning between asynchronous operations. If CE# goes High, it must remain High for at least 5ns (t_{CBPH}) to schedule the appropriate internal refresh operation. See How Extended Timings Impact CellularRAM™ Operation for restrictions on the maximum CE# Low time (t_{CEM}).*

Figure 34.32. Asynchronous Write Followed by Asynchronous Read

Table 34.33 Write Timing Parameters—Asynchronous Write Followed by Asynchronous Read

Symbol	70ns/80 MHz		85ns/66 MHz		Units
	Min	Max	Min	Max	
t_{AS}	0		0		ns
t_{AVH}	5		5		ns
t_{AVS}	10		10		ns
t_{AW}	70		85		ns
t_{BW}	70		85		ns
t_{CVS}	10		10		ns
t_{CW}	70		85		ns
t_{DH}	0		0		ns
t_{DW}	23		23		ns
t_{VP}	10		10		ns
t_{VPH}	10		10		ns
t_{VS}	70		85		ns
t_{WC}	70		85		ns
t_{WHZ}		8		8	ns
t_{WP}	46		55		ns
t_{WPH}	10		10		ns
t_{WR}	0		0		ns

Table 34.34 Read Timing Parameters—Asynchronous Write Followed by Asynchronous Read

Symbol	70ns/80 MHz		85ns/66 MHz		Units
	Min	Max	Min	Max	
t_{AA}		70		85	ns
t_{BHZ}		8		8	ns
t_{BLZ}	10		10		ns
t_{CBPH}	5		5		ns
t_{CEM}		4		4	µs
t_{HZ}		8		8	ns
t_{LZ}	10		10		ns
t_{OE}		20		20	ns
t_{OHZ}		8		8	ns
t_{OLZ}	5		5		ns

35 How Extended Timings Impact CellularRAM™ Operation

35.1 Introduction

This section describes CellularRAM™ timing requirements in systems that perform extended operations.

CellularRAM products use a DRAM technology that periodically requires refresh to ensure against data corruption. CellularRAM devices include on-chip circuitry that performs the required refresh in a manner that is completely transparent in systems with normal bus timings. The refresh circuitry imposes constraints on timings in systems that take longer than 4µs to complete an operation. Write operations are affected if the device is configured for asynchronous operation. Both Read and Write operations are affected if the device is configured for page or burst-mode operation.

35.2 Asynchronous Write Operation

The timing parameters provided in Figure 34.4 require that all Write operations must be completed within 4µs. After completing a Write operation, the device must either enter standby (by transitioning CE# High), or else perform a second operation (Read or Write) using a new address. Figure 35.1 and Figure 35.2 demonstrate these constraints as they apply during an asynchronous (page-mode-disabled) operation. Either the CE# active period (t_{CEM} in Figure 35.1) or the address valid period (t_{TM} in Figure 35.2) must be less than 4µs during any Write operation, otherwise, the extended Write timings must be used.

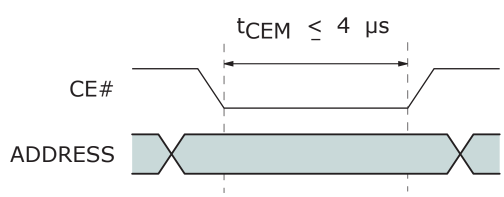


Figure 35.1 Extended Timing for t_{CEM}

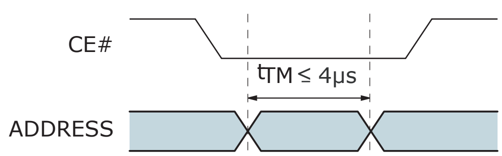


Figure 35.2 Extended Timing for t_{TM}

Table 35.1 Extended Cycle Impact on Read and Write Cycles

Page Mode	Timing Constraint	Read Cycle	Write Cycle
Asynchronous Page Mode Disabled	t_{CEM} and t_{TM} > 4µs (See Figure 35.1 and Figure 35.2.)	No impact.	Must use extended Write timing. (See Figure 35.2)
Asynchronous Page Mode Enabled	t_{CEM} > 4µs (See Figure 35.1.)	All following intrapage Read access times are t_{AA} (not t_{APA}).	Must use extended Write timing. (See Figure 35.3)
Burst	t_{CEM} > 4µs (See Figure 35.1.)	Burst must cross a row boundary within 4µs.	

35.2.1 Extended Write Timing— Asynchronous Write Operation

Modified timings are required during extended Write operations (see Figure 35.3). An extended Write operation requires that both the Write pulse width (t_{WP}) and the data valid period (t_{DW}) be lengthened to at least the minimum Write cycle time (t_{WC} [MIN]). These increased timings ensure that time is available for both a refresh operation and a successful completion of the Write operation.

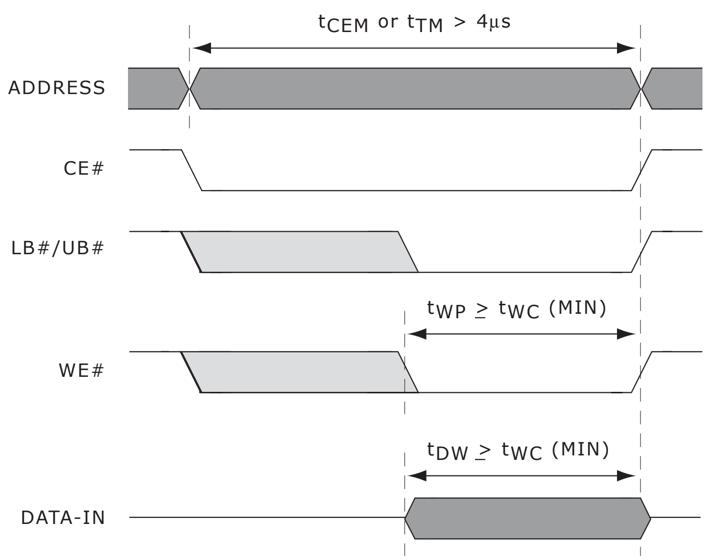


Figure 35.3 Extended Write Operation

35.3 Page Mode Read Operation

When a CellularRAM device is configured for page mode operation, the address inputs are used to accelerate Read accesses and cannot be used by the on-chip circuitry to schedule refresh. If CE# is Low longer than the t_{CEM} maximum time of 4µs during a Read operation, the system must allow t_{AA} (not t_{APA}, as would otherwise be expected) for all subsequent intrapage accesses until CE# goes High.

35.4 Burst-Mode Operation

When configured for burst-mode operation, it is necessary to allow the device to perform a refresh within any 4µs window. One of two conditions will enable the device to schedule a refresh within 4µs. The first condition is when all burst operations complete within 4µs. A burst completes when the CE# signal is registered High on a rising clock edge. The second condition that allows a refresh is when a burst access crosses a row boundary. The row-boundary crossing causes Wait to be asserted while the next row is accessed and enables the scheduling of refresh.

35.5 Summary

CellularRAM products are designed to ensure that any possible asynchronous timings do not cause data corruption due to lack of refresh. Slow bus timings on asynchronous Write operations require that t_{WP} and t_{DW} be lengthened. Slow bus timings during asynchronous page Read operations cause the next intrapage Read data to be delayed to t_{AA}.

Burst mode timings must allow the device to perform a refresh within any 4µs period. A burst operation must either complete (CE# registered High) or cross a row boundary within 4µs to ensure successful refresh scheduling. These timing requirements are likely to have little or no impact when interfacing a CellularRAM device with a low-speed memory bus.

36 Revisions

Revision A0 (February 17, 2005)

Initial Release

Colophon

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