PBL 386 15/1 Subscriber Line Interface Circuit

Description

The PBL 386 15/1 Subscriber Line Interface Circuit (SLIC) is a 90 V bipolar integrated circuit for use in ISDN Network Terminal Adapters, DAML, FITL and other short loop telecommunication equipment which often are remote powered, and by that, the available power is limited. The PBL 386 15/1 has been optimized for low total line interface cost, low power and requires a minimum of external components.
The PBL 386 15/1 has constant current feed, programmable to max 30mA. The SLIC uses a first battery voltage for On-hook . A second battery voltage is used for Off-hook and must be connected, to reduce short loop power dissipation. The SLIC automatically switches between the two battery supply voltages without need for external components or external control. The loop current controls the switching between On-hook and Off-hook battery.
The SLIC incorporates loop current, ground key and ring trip detection functions. The PBL 386 15/1 is compatible with loop start signalling. Two- to four-wire and four- to two-wire voice frequency (vf) signal conversion is accomplished by the SLIC in conjunction with either a conventional CODEC/filter or with a programmable CODEC/filter, e.g. SLAC, SiCoFi, Combo II. The programmable line terminating impedance could be complex or real to fit every market. Longitudinal voltages are suppressed by a feedback loop in the SLIC and the longitudinal balance specifications meet Bellcore TR909 requirements.
The PBL 386 15/1 package is a very PCB space efficient 28-pin SSOP.

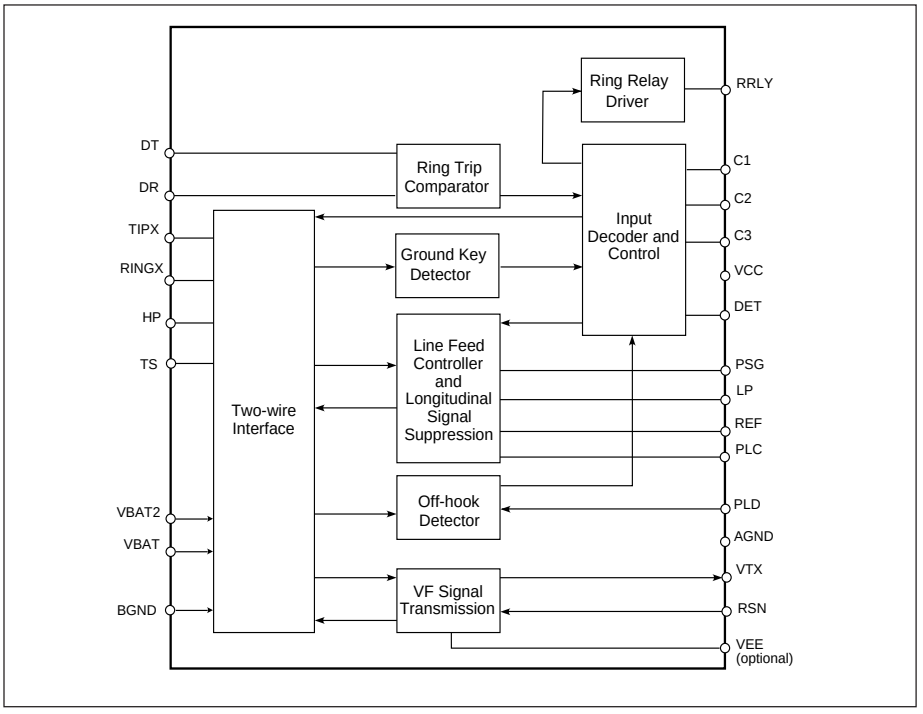


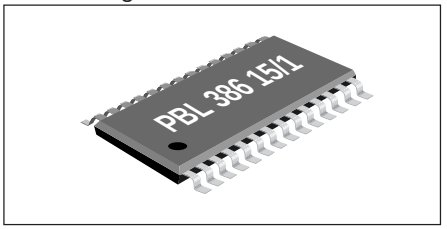
Figure 1. Block diagram.

Applications

- ISDN Network terminals
- DAML
- FITL
- Shortloop applications

Key Features

- Small footprint with SSOP package
- On-hook and Off-hook battery with automatic switching, controlled by loop current
- On-hook battery current is limited to 6 mA
- 37 mW on-hook power dissipation in active state
- Metering 0.5 Vrms (0.7 Vpeak)
- Adaptive Overhead Voltage
  The overhead voltage follows 1Vpeak<signals<2.5Vpeak
- Battery supply as low as -10V
- Only +5V in addition to GND and battery (VEE optional)
- Open loop voltage tracks On-hook battery
- Full longitudinal current capability during On-hook
- 43.5V open loop voltage @ -48V battery feed
- Automatic compensation for line leakage up to 5 mA
- On-hook transmission
- Programmable loop & ring-trip detector threshold
- Ground key detector
- Analog temperature guard with status exclusively viewed at detector output
- Integrated Ring Relay Driver
- Silent polarity reversal
- Linevoltage measurement



Package: 28-pin SSOP

Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Temperature, Humidity				
Storage temperature range	T_{Stg}	-55	+150	°C
Operating temperature range	T_{Amb}	-40	+110	°C
Operating junction temperature range, Note 1	T_J	-40	+140	°C
Power supply, -40°C ≤ T_{Amb} ≤ +85°C				
V_{CC} with respect to AGND	V_{CC}	-0.4	6.5	V
V_{EE} with respect to AGND	V_{EE}	V_{Bat}	0.4	V
V_{Bat2} with respect to A/BGND	V_{Bat2}	V_{Bat}	0.4	V
V_{Bat} with respect to BGND, continuous	V_{Bat}	-75	0.4	V
V_{Bat2} with respect to BGND, 10 ms	V_{Bat2}	-80	0.4	V
Power dissipation				
Continuous power dissipation at T_{Amb} ≤ +85 °C	P_D		0.8	W
Ground				
Voltage between AGND and BGND	V_G	-5	VCC	V
Relay Driver				
Ring relay supply voltage			BGND +13	V
Ring relay current			75 mA	
Ring trip comparator				
Input voltage	V_{DT}, V_{DR}	V_{Bat}	V_{CC}	V
Input current	I_{DT}, I_{DR}	-5	5	mA
Digital inputs, outputs (C1, C2, C3, DET)				
Input voltage	V_{ID}	-0.4	V_{CC}	V
Output voltage (DET not active)	V_{OD}	-0.4	V_{CC}	V
Output current (DET)	I_{OD}		30	mA
TIPX and RINGX terminals, -40°C < T_{Amb} < +85°C, V_{Bat} = -50 V				
TIPX or RINGX current	I_{TIPX}, I_{RINGX}	-110	+110	mA
TIPX or RINGX voltage, continuous (referenced to AGND), Note 2	V_{TA}, V_{RA}	V_{Bat}	2	V
TIPX or RINGX, pulse < 10 ms, t_{Rep} > 10 s, Note 2	V_{TA}, V_{RA}	V_{Bat} - 20	5	V
TIPX or RINGX, pulse < 1 µs, t_{Rep} > 10 s, Note 2	V_{TA}, V_{RA}	V_{Bat} - 40	10	V
TIP or RING, pulse < 250 ns, t_{Rep} > 10 s, Note 3	V_{TA}, V_{RA}	V_{Bat} - 70	15	V

Recommended Operating Condition

Parameter	Symbol	Min	Max	Unit
Ambient temperature	T_{Amb}	-40	+85	°C
V_{CC} with respect to AGND	V_{CC}	4.75	5.25	V
V_{EE} with respect to AGND	V_{EE}	V_{Bat}	-4.75	V
V_{Bat} with respect to BGND	V_{Bat}	-58	-10	V
V_{Bat2} with respect to BGND	V_{Bat2}	V_{Bat}	-10	V

Notes

1. The circuit includes thermal protection. Operation above max. junction temperature may degrade device reliability.
2. A diode in series with the VBat input increases the permitted continuous voltage and pulse < 10 ms to -85 V. A pulse ≤1µs is increased to the greater of |-70V| and |VBat -40V|.
3. R_{F1} and R_{F2} ≥ 20 Ω is also required. Pulse is supplied to TIP and RING outside R_{F1} and R_{F2}.

Electrical Characteristics

-40 °C ≤ T_{Amb} ≤ +85 °C, V_{CC} = +5V ±5 %, V_{EE} = -5V ± 5%, V_{Bat} = -58V to -40V, V_{Bat2} = -22V, R_{LC}=18.7kΩ (I_L = 27 mA), R_L = 600 Ω, R_{LD} = 50 kΩ, R_{F1}, R_{F2} = 0 Ω, R_{Ref} = 15kΩ, C_{HP} = 68nF, C_{LP}=0.47 µF, R_T = 120 kΩ, R_{RX} = 120 kΩ, Current definition: current is positive if flowing into a pin. Active state includes active normal and active reverse states unless otherwise specified. Battery definition: V_{Bat} = On-hook battery, V_{Bat2} = Off-hook battery.

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Two-wire port						
Overload level, V_{TRO}	2	Active state				
Off-Hook, I_{LDC} ≥ 10 mA		1% THD, Note 1	1.0			V_{Peak}
On-Hook, I_{LDC} ≤ 5 mA			1.0			V_{Peak}
Metering I_{LDC} ≥ 10 mA		Z_{LTTX} = 200 Ω, f = 16 kHz		0.7		V_{Peak}
Input impedance, Z_{TR}		Note 2		Z_T/200		
Longitudinal impedance, Z_{LoT}, Z_{LoR}		0 < f < 100 Hz		20	35	Ω/wire
Longitudinal current limit, I_{LoT}, I_{LoR}		active state	12			mA_{rms}/wire
Longitudinal to metallic balance, B_{LM}		IEEE standard 455-1985, ZTRX = 736 Ω				
		0.2 kHz < f < 1.0 kHz	53	70		dB
		1.0 kHz < f < 3.4 kHz	53	70		dB
Longitudinal to metallic balance, B_{LME}	3	active state				
$B_{LME} = 20 \bullet Log\left\lvert\frac{E_{Lo}}{V_{TR}}\right\rvert$		0.2 kHz ≤ f ≤ 1.0 kHz	53	70		dB
		1.0 kHz < f < 3.4 kHz	53	70		dB
Longitudinal to four-wire balance, B_{LFE}	3	active state				
$B_{LFE} = 20 \bullet Log\left\lvert\frac{E_{Lo}}{V_{TX}}\right\rvert$		0.2 kHz ≤ f ≤ 1.0 kHz	59	70		dB
		1.0 kHz < f < 3.4 kHz	59	70		dB
Metallic to longitudinal balance, B_{MLE}	4	active state				
$B_{MLE} = 20 \bullet Log\left\lvert\frac{V_{TR}}{V_{Lo}}\right\rvert$;E_{RX} = 0		0.2 kHz < f < 3.4 kHz	40	58		dB

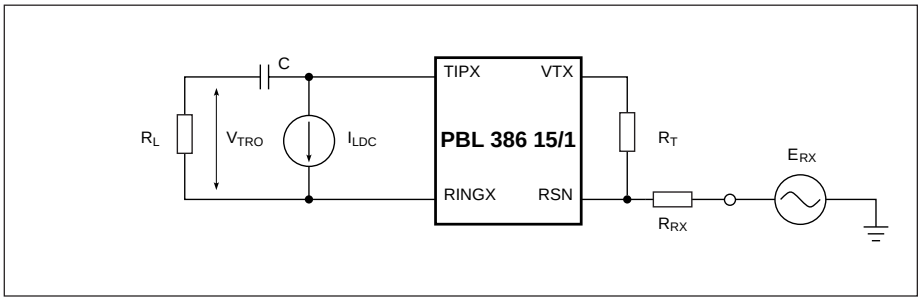


Figure 2. Overload level, V_{TRO}, two-wire port

$\frac{1}{wC}$ << R_L, R_L= 600 Ω

R_T = 120 kΩ, R_{RX} = 120 kΩ

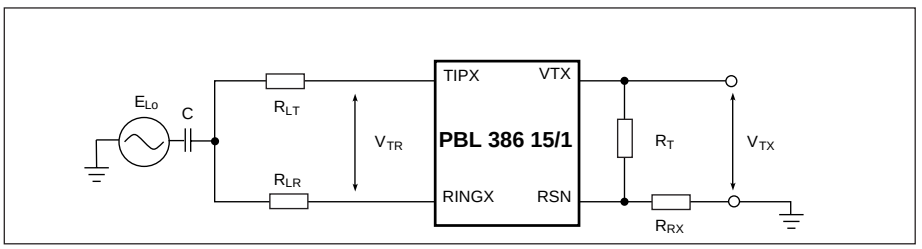


Figure 3. Longitudinal to metallic (B_{LME}) and Longitudinal to four-wire (B_{LFE}) balance

$\frac{1}{wC}$ << 150 Ω, R_{LR} = R_{LT} = R_L /2= 300Ω

R_T = 120 kΩ, R_{RX} = 120 kΩ

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Four-wire to longitudinal balance, B_{FLE}	4	active state $B_{FLE} = 20 \bullet Log \left\lvert \frac{E_{RX}}{V_{Lo}} \right\rvert$				
		0.2 kHz < f < 3.4 kHz	40	58		dB
Two-wire return loss, r		$r = 20 \bullet Log \frac{\lvert Z_{TR} + Z_L \rvert}{\lvert Z_{TR} - Z_L \rvert}$				
		0.2 kHz < f < 0.5 kHz	25			dB
		0.5 kHz < f < 1.0 kHz	27			dB
		1.0 kHz < f < 3.4 kHz, Note 3	23			dB
TIPX idle voltage, V_{Ti}		active normal, $I_L = 0$		- 1.3		V
RINGX idle voltage, V_{Ri}		active normal, $I_L = 0$		V_{Bat} +3.1		V
$\lvert V_{TR} \rvert$		active, $I_L = 0$	$\lvert V_{Bat} +5.5 \rvert$	$\lvert V_{Bat} + 4.5 \rvert$		V
Four-wire transmit port (V_{TX})						
Overload level, V_{TXO}	5					
Off-hook, $I_L \geq 10$mA		Load impedance > 20 kΩ,	0.5			V_{Peak}
On-hook, $I_L \leq 5$mA		1% THD, Note 4	0.5			V_{Peak}
Output offset voltage, ΔV_{TX}			-60		60	mV
Output impedance, z_{TX}		0.2 kHz < f < 3.4 kHz		5	20	Ω
Four-wire receive port (RSN)						
Receive summing node (RSN) dc voltage		$I_{RSN} = 0$ mA		GND ±25		mV
Receive summing node (RSN) impedance		0.2 kHz < f < 3.4 kHz		10	50	Ω
Receive summing node (RSN) current (I_{RSN}) to metallic loop current (I_L) gain, α_{RSN}		0.3 kHz < f < 3.4 kHz		400		ratio
Frequency response						
Two-wire to four-wire, g_{2-4}	6	relative to 0 dBm, 1.0 kHz. $E_{RX} = 0$ V				
		0.3 kHz < f < 3.4 kHz	-0.15		0.15	dB
		f = 8.0 kHz, 12 kHz, 16 kHz	-0.5	0	0.1	dB

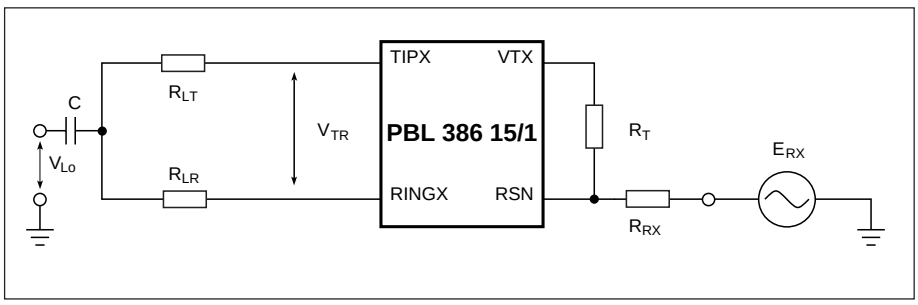


Figure 4. Metallic to longitudinal and four-wire to longitudinal balance

$\frac{1}{\omega C} << 150\ \Omega$, $R_{LT} = R_{LR} = R_L / 2 = 300\Omega$

$R_T = 120$ kΩ, $R_{RX} = 120$ kΩ

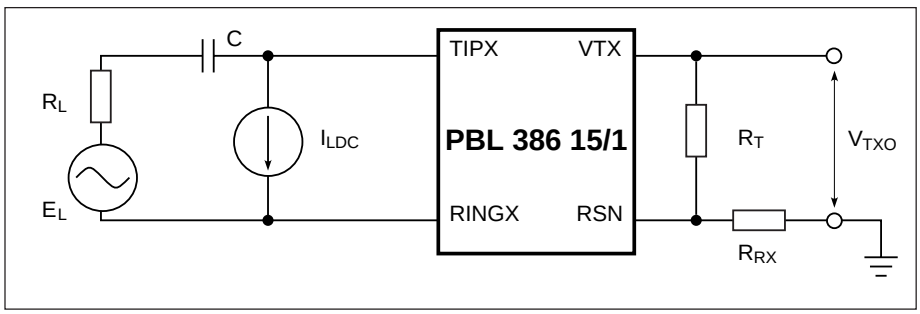


Figure 5. Overload level, V_{TXO}, four-wire transmit port

$\frac{1}{\omega C} << R_L$, $R_L = 600\ \Omega$

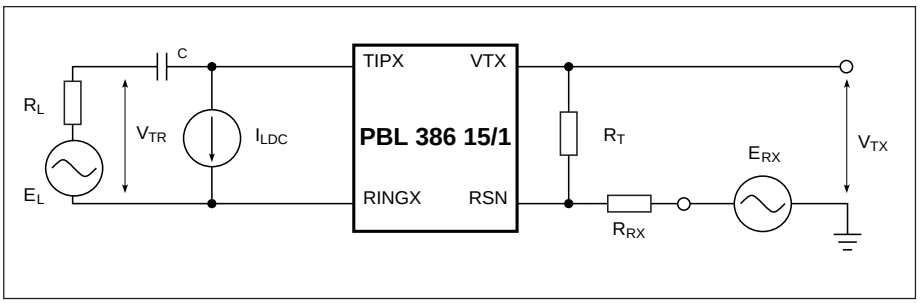
$R_T = 120$ kΩ, $R_{RX} = 120$ kΩ

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Four-wire to two-wire, g_{4-2}	6	relative to 0 dBm, 1.0 kHz. E_L = 0 V				
		0.3 kHz < f < 3.4 kHz	-0.15		0.15	dB
		f = 8 kHz, 12 kHz,	-1.0	-0.2	0	dB
		16 kHz	-1.0	-0.3	0	dB
Four-wire to four-wire, g_{4-4}	6	relative to 0 dBm, 1.0 kHz. E_L = 0 V				
		0.3 kHz < f < 3.4 kHz	-0.15		0.15	dB
Insertion loss						
Two-wire to four-wire, G_{2-4}	6	0 dBm, 1.0 kHz, Note 5				
		$G_{2-4} = 20 \bullet \text{Log} \left\lvert \frac{V_{TX}}{V_{TR}} \right\rvert, E_{RX} = 0$	-6.22	-6.02	-5.82	dB
Four-wire to two-wire, G_{4-2}	6	0 dBm, 1.0 kHz, Notes 5, 6				
		$G_{4-2} = 20 \bullet \text{Log} \left\lvert \frac{V_{TR}}{E_{RX}} \right\rvert, E_G = 0$	-0.2		0.2	dB
Gain tracking						
Two-wire to four-wire $R_{LDC} \leq 2k\Omega$	6	Ref. -10 dBm, 1.0 kHz, Note 7				
		-40 dBm to +3 dBm	-0.1		0.1	dB
		-55 dBm to -40 dBm	-0.2		0.2	dB
Four-wire to two-wire $R_{LDC} \leq 2k\Omega$	6	Ref. -10 dBm, 1.0 kHz, Note 7				
		-40 dBm to +3 dBm	-0.1		0.1	dB
		-55 dBm to -40 dBm	-0.2		0.2	dB
Noise						
Idle channel noise at two-wire		C-message weighting		7	12	dBrnC
(TIPX-RINGX)		Psophometrical weighting		-83	-78	dBmp
		Note 8				
Harmonic distortion						
Two-wire to four-wire	6	0 dBm, 1.0 kHz test signal			-50	dB
Four-wire to two-wire		0.3 kHz < f < 3.4 kHz			-50	dB
Battery feed characteristics						
Constant loop current, I_{LConst}	13	$I_{LProg} = \frac{500}{R_{LC}}$				
		18 < I_{LProg} < 30 mA	0.95 I_{LProg}	I_{LProg}	1.05 I_{LProg}	mA

Figure 6.
Frequency response, insertion loss, gain tracking.

$\frac{1}{\omega C}$ << R_L, R_L = 600 Ω

R_T = 120 kΩ, R_{RX} = 120 kΩ



Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Loop current detector						
Programmable threshold, I_{DET} I_{LTh} > 10 mA		$I_{LTh} = \frac{500}{R_{LD}}$	0.9•I_{LTh}	I_{LTh}	1.1•I_{LTh}	mA
Ground key detector						
Ground key detector threshold I_{LTIPX} and I_{LRINGX} current difference to trigger ground key det.			11	15	19	mA
Ring trip comparator						
Offset voltage, ΔV_{DTDR}		Source resistance, R_S = 0 Ω	-20	0	20	mV
Input bias current, I_B		$I_B = (I_{DT} + I_{DR})/2$	-50	-20		nA
Input common mode range, V_{DT}, V_{DR}			V_{Bat}+1		-1	V
Ring relay driver						
Saturation voltage, V_{OL}		I_{OL} = 50 mA		0.2	0.5	V
Off state leakage current, I_{Lk}		V_{OH} = 12 V			100	µA
Digital inputs (C1, C2, C3)						
Input low voltage, V_{IL}			0		0.5	V
Input high voltage, V_{IH}			2.5		V_{CC}	V
Input low current, $\|I_{IL}\|$		V_{IL} = 0.5			200	µA
Input high current, I_{IH}		V_{IH} = 2.5 V			200	µA
Detector output (DET)						
Output low voltage, V_{OL}		I_{OL} = 1 mA		0.1	0.6	V
Internal pull-up resistor to V_{CC}				10		kΩ
Power dissipation (V_{Bat} = -48V, V_{Bat2} = -22V, note 9)						
P_1		Open circuit state		15	18	mW
P_2 @ VEE=-5V		Active State I_{Lo} = 0 mA, I_L = 0 mA		37	44	mW
P_3 @ VEE=VB2		Active State I_{Lo} = 0 mA, I_L = 0 mA		40	47	mW
P_4 @ VEE = -5V		Active R_L = 300Ω (off-hook)		415		mW
P_5 @ VEE = -5V		Active R_L = 600Ω (off-hook)		200		mW
Power supply currents (V_{Bat} = -48V)						
V_{CC} current, I_{CC}		Open circuit state		1.3		mA
V_{EE} current, I_{EE}		Open circuit state	-0.2	-0.1		mA
V_{Bat} current, I_{Bat}		Open circuit state	-0.2	-0.1		mA
V_{CC} current, I_{CC}		Active State I_{Lo}= 0 mA, I_L = 0 mA		2.1	3.5	mA
V_{EE} current, I_{EE}		Active State I_{Lo}= 0 mA, I_L = 0 mA		0.1	0.3	mA
V_{Bat} current, I_{Bat} , On-hook		Active State I_{Lo}= 0 mA, I_L = 0 mA	-0.8	-0.5		mA
Power supply rejection ratios						
V_{CC} to 2- or 4-wire port		Active State, f = 1 kHz, V_n = 100mV	30	45		dB
V_{EE} to 2- or 4-wire port		Active State, f = 1 kHz, V_n = 100mV	28.5	55		dB
V_{Bat} to 2- or 4-wire port		Active State, f = 1 kHz, V_n = 100mV	45	60		dB
V_{Bat2} to 2- or 4-wire port		Active State, f = 1 kHz, V_n = 100mV	28.5	60		dB
Temperature guard						
Junction threshold temperature, T_{JG}			140			°C
Thermal resistance						
28-pin SSOP, $\theta_{JP28SSOP}$				55		°C/W

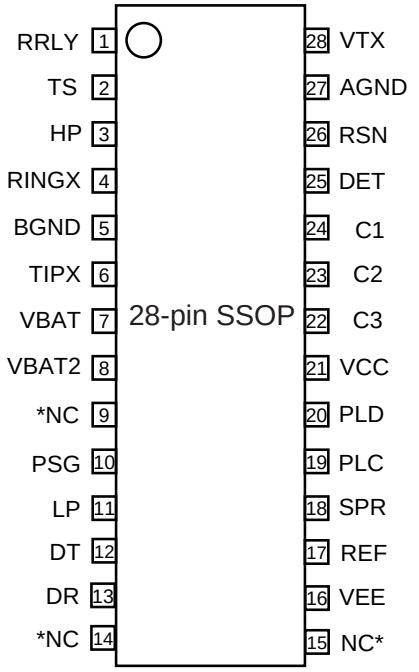
Notes

1. The overload level is automatically expanded to 2.5 V_{Peak} when the signal level > 1.0 V_{Peak} and is specified at the two-wire port with the signal source at the four-wire receive port.
2. The two-wire impedance is programmable by selection of external component values according to:
   $Z_{TR} = Z_T/|G_{2\text{-}4S}\,\alpha_{RSN}|$ where:
   Z_{TR} = impedance between the TIPX and RINGX terminals
   Z_T = programming network between the VTX and RSN terminals
   $G_{2\text{-}4S}$ = transmit gain, nominally = -0.5
   α_{RSN} = receive current gain, nominally = 400 (current defined as positive flowing into the receivesumming node, RSN, and when flowing from tip to ring).
3. Higher return loss values can be achieved by adding a reactive component to R_T, the two-wire terminating impedance programming resistance, e.g. by dividing R_T into two equal halves and connecting a capacitor from the common point to ground.
4. The overload level is automatically expanded as needed up to 1.25 V_{Peak} when the signal level >0.5 V_{Peak} and is specified at the four-wire transmit port, VTX, with the signal source at the two-wire port. Note that the gain from the two-wire port to the four-wire transmit port is $G_{2\text{-}4S}$ = -0.5.
5. Secondary protection resistors R_F impact the insertion loss. The specified insertion loss is for R_F = 0.
6. The specified insertion loss tolerance does not include errors caused by external components.
7. The level is specified at the four-wire receive port and referenced to a 600 Ω programmed two-wire impedance level.
8. The two-wire idle noise is specified with the four-wire receive port grounded (E_{RX} = 0; see figure 6).
   The four-wire idle noise at VTX is the two-wire value -6 dB and is specified with the two-wire port terminated in 600 Ω (R_L). The noise specification is referenced to a 600 Ω programmed two-wire impedance level at VTX. The four-wire receive port is grounded (E_{RX} = 0).
9. The V_{Bat2} voltage is optimized for R_L=600 Ω with a programmed linecurrent, I_L=27 mA. This gives V_{Bat2}=22 V at the terminal (e.g. calculated to 21.9V).

Pin Description

Refer to figure 7.

SSOP	Symbol	Description
1	RRLY	**R**ing **Re**l**a**y driver output.
2	TS	**T**ip **S**ense should be connected to TIPX.
3	HP	**H**igh **P**ass connection for ac/dc separation capacitor C_{HP}. Other end of C_{HP} connects to RINGX (pin 26).
4	RINGX	The TIPX and RINGX pins connect to the tip and ring leads of the two-wire interface via overvoltage protection components and ring relay (and optional test relay).
5	BGND	**B**attery **G**rou**nd**, should be tied together with AGND.
6	TIPX	The TIPX and RINGX pins connect to the tip and ring leads of the two-wire interface via overvoltage protection components and ring relay (and optional test relay).
7	VBAT	**On-hook** battery voltage. Negative with respect to BGND.
8	VBAT2	**Off-hook** battery voltage, connected in series with a diode.
9	NC	**N**o **C**onnect. Must be left open.
10	PSG	**P**rogrammable **S**aturation **G**uard. Must be connected to VBAT2.
11	LP	**L**ow **P**ass saturation guard filter capacitor connected here to filter out noise and improve PSRR. Other end of C_{LP} connects to VBAT2.
12	DT	Input to the ring trip comparator. With DR more positive than DT the detector output, DET, is at logic level low, indicating off-hook condition. The ring trip network connects to this input.
13	DR	Input to the ring trip comparator. With DR more positive than DT the detector output, DET, is at logic level low, indicating off-hook condition. The ring trip network connects to this input.
14	NC	**N**o **C**onnect. Must be left open.
15	NC	**N**o **C**onnect. Must be left open.
16	VEE	-5V power supply, if not -5 V available connect to VB2 or VBAT (VB2 lower power dissipation than VBAT).
17	REF	A 15kΩ resistor must be connected between this pin and AGND.
18	SPR	**S**ilent **P**olarity **R**eversal. The polarity reversal time can be adjusted with a capasitor connected to AGND.
19	PLC	**P**rog. **L**ine **C**urrent, the constant current part of the DC feed characteristic is programmed by a resistor connected from this pin to AGND.
20	PLD	**P**rogrammable **L**oop **D**etector threshold. The loop detection threshold is programmed by a resistor connected from this pin to AGND.
21	VCC	+5 V power supply.
22	C3	C1, C2 and C3 are digital inputs **C**ontrolling the SLIC operating states. Refer to section Operating states for details.
23	C2	
24	C1	
25	DET	**Det**ector output. Active low when indicating loop or ring trip detection, active high when indicating ground key detection, active low when indicating temperature alarm.
26	RSN	**R**eceive **S**umming **N**ode. 400 times the current flowing into this pin equals the metallic (transversal) current flowing from TIPX to RINGX. Programming networks for two-wire impedance and receive gain connect to the receive summing node.
27	AGND	**A**nalog **G**rou**nd**, should be tied together with BGND.
28	VTX	Transmit vf output. The ac voltage difference between TIPX and RINGX, the ac metallic voltage, is reproduced as an unbalanced GND referenced signal at VTX with a gain of -0.5. The two-wire impedance programming network connects between VTX and RSN.



***** Pins must be left open.

Figure 7. Pin configuration 28 pin SSOP package, top view.

SLIC Operating States

State	C3	C2	C1	SLIC operating state	Active detector
0	0	0	0	Open circuit	Detector is set high
1	0	0	1	Ringing state	Ring trip detector (active low)
2	0	1	0	Active state	Loop detector (active low)
3	0	1	1	Active state	Line Voltage measurament (pulse train)
4	1	0	0	Active state	Temperature guard (active low)
5	1	0	1	Active state	Ground key detector (active high)
6	1	1	0	Active reverse	Loop detector (active low)
7	1	1	1	Active reverse	Ground key detector (active high)

Table 1. SLIC operating states.

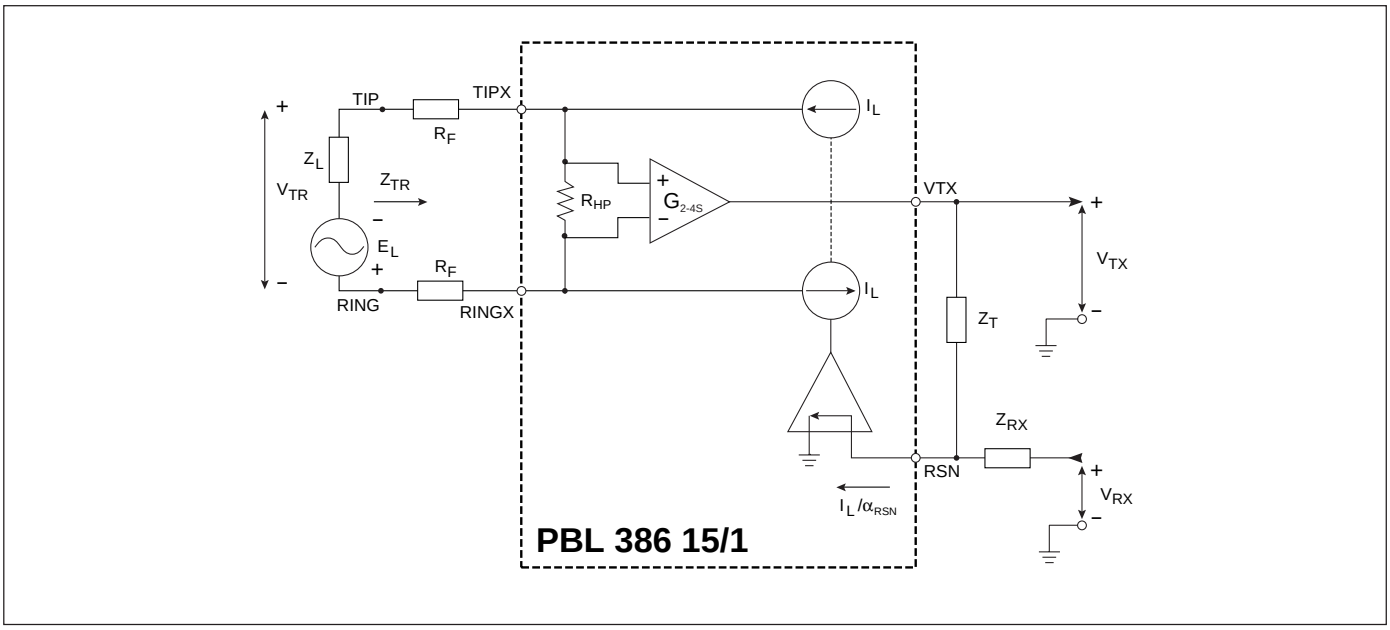


Figure 9. Simplified AC transmission circuit.

Functional Description and Applications Information Transmission

General

A simplified AC model of the transmission circuits is shown in figure 9. Circuit analysis yields:

$$V_{TR} = \frac{V_{TX}}{G_{2\text{-}4S}} - I_L \cdot 2R_F \qquad (1)$$

$$\frac{V_{TX}}{Z_T} + \frac{V_{RX}}{Z_{RX}} = \frac{I_L}{\alpha_{RSN}} \qquad (2)$$

$$V_{TR} = I_L \cdot Z_L - E_L \qquad (3)$$

where:

V_{TX} is a ground referenced version of the ac metallic voltage between the TIPX and RINGX terminals.

V_{TR} is the ac metallic voltage between tip and ring.

E_L is the line open circuit ac metallic voltage.

I_L is the ac metallic current.

R_F is a fuse resistor.

$G_{2\text{-}4S}$ is the SLIC two-wire to four-wire gain (transmit direction) with a nominal value of -0.5. (phase shift 180°.)

Z_L is the line impedance.

Z_T determines the SLIC TIPX to RINGX impedance for signal in the 0 - 20kHz frequency range.

Z_{RX} controls four- to two-wire gain.

V_{RX} is the analogue ground referenced receive signal.

α_{RSN} is the receive summing node current to metallic loop current gain. The nominal value of $\alpha_{RSN} = 400$

R_{HP} Internal resistor appprox. 180 kΩ

Two-Wire Impedance

To calculate Z_{TR}, the impedance presented to the two-wire line by the SLIC including the fuse resistor R_F, let $V_{RX} = 0$.

From (1) and (2):

$$Z_{TR} = \left| \frac{Z_T}{\alpha_{RSN} \cdot G_{2\text{-}4S}} - 2R_F \right|$$

Thus with Z_{TR}, $G_{2\text{-}4S}$, α_{RSN}, and R_F known:

$$Z_T = \alpha_{RSN} \cdot G_{2\text{-}4S} \cdot (2R_F - |Z_{TR}|)$$

Two-Wire to Four-Wire Gain

From (1) and (2) with $V_{RX} = 0$:

$$G_{2\text{-}4} = \frac{V_{TX}}{V_{TR}} = \frac{Z_T/\alpha_{RSN}}{\frac{Z_T}{\alpha_{RSN} \cdot G_{2\text{-}4S}} - 2R_F}$$

Four-Wire to Two-Wire Gain

From (1), (2) and (3) with $E_L = 0$:

$$G_{4\text{-}2} = \frac{V_{TR}}{V_{RX}} = \frac{Z_T}{Z_{RX}} \cdot \frac{Z_L}{\frac{Z_T}{\alpha_{RSN}} - G_{2\text{-}4S} \cdot (Z_L + 2R_F)}$$

In applications where $2R_F - Z_T/(\alpha_{RSN} \cdot G_{2\text{-}4S})$ is chosen to be equal to Z_L, the expression for $G_{4\text{-}2}$ simplifies to:

$$G_{4\text{-}2} = -\frac{Z_T}{Z_{RX}} \cdot \frac{1}{2 \cdot G_{2\text{-}4S}}$$

Four-Wire to Four-Wire Gain

From (1), (2) and (3) with $E_L = 0$:

$$G_{4\text{-}4} = \frac{V_{TX}}{V_{RX}} = \frac{Z_T}{Z_{RX}} \cdot \frac{G_{2\text{-}4S} \cdot (Z_L + 2R_F)}{\frac{Z_T}{\alpha_{RSN}} - G_{2\text{-}4S} \cdot (Z_L + 2R_F)}$$

Hybrid Function

The hybrid function can easily be implemented utilizing the uncommitted amplifier in conventional CODEC/filter combinations. Please, refer to figure 10. Via impedance Z_B a current proportional to V_{RX} is injected into the summing node of the combination CODEC/filter amplifier. As can be seen from the expression for the four-wire to four-wire gain a voltage proportional to V_{RX} is returned to V_{TX}. This voltage is converted by R_{TX} to a current flowing into the same summing node. These currents can be made to cancel by letting:

$$\frac{V_{TX}}{R_{TX}} + \frac{V_{RX}}{Z_B} = 0 \ (E_L = 0)$$

The four-wire to four-wire gain, $G_{4\text{-}4}$, includes the required phase shift and thus the balance network Z_B can be calculated from:

$$Z_B = - R_{TX} \cdot \frac{V_{RX}}{V_{TX}} =$$

$$- R_{TX} \cdot \frac{Z_{RX}}{Z_T} \cdot \frac{\frac{Z_T}{\alpha_{RSN}} - G_{2\text{-}4S} \cdot (Z_L + 2R_F)}{G_{2\text{-}4S} \cdot (Z_L + 2R_F)}$$

When choosing R_{TX}, make sure the output load of the VTX terminal is (R_{TX}//R_T in figure 15) > 20 kΩ.

If calculation of the Z_B formula above yields a balance network containing an inductor, an alternate method is recommended.

The PBL 386 15/1 SLIC may also be used together with programmable CODEC/filters. The programmable CODEC/filter allows for system controller adjustment of hybrid balance to accommodate different line impedances without change of hardware. In addition, the transmit and receive gain may be adjusted. Please, refer to the programmable CODEC/filter data sheets for design information.

Longitudinal Impedance

A feed back loop counteracts longitudinal voltages at the two-wire port by injecting longitudinal currents in opposing phase.

Thus longitudinal disturbances will appear as longitudinal currents and the TIPX and RINGX terminals will experience very small longitudinal voltage excursions, leaving metallic voltages well within the SLIC common mode range.

The SLIC longitudinal impedance per wire, Z_{LoT} and Z_{LoR}, appears as typically 20 Ω to longitudinal disturbances. It should be noted that longitudinal currents may exceed the dc loop current without disturbing the vf transmission.

Capacitors C_{TC} and C_{RC}

If RFI filtering is needed, the capacitors designated C_{TC} and C_{RC} in figure 13, connected between TIPX and ground as well as between RINGX and ground, may be mounted.

C_{TC} and C_{RC} work as RFI filters in conjunction with suitable series impedances (i.e. resistances, inductances). Resistors R_{F1} and R_{F2} may be sufficient, but series inductances can be added to form a second order filter. Current-compensated inductors are suitable since they suppress common-mode signals with minimum influence on return loss. Recommended values for C_{TC} and C_{RC} are below 1 nF. Lower values impose smaller degradation on return loss and longitudinal balance, but also attenuate radio frequencies to a smaller extent. The influence on the impedance loop must also be taken into consideration when programming the CODEC. C_{TC} and C_{RC} contribute to a metallic impedance of $1/(\pi \cdot f \cdot C_{TC}) = 1/(\pi \cdot f \cdot C_{RC})$, a TIPX to ground impedance of $1/(2 \cdot \pi \cdot f \cdot C_{TC})$ and a RINGX to ground impedance of $1/(2 \cdot \pi \cdot f \cdot C_{RC})$.

AC - DC Separation Capacitor, C_{HP}

The high pass filter capacitor connected between terminals HP and RINGX provides the separation of the ac and dc signals. C_{HP} positions the low end frequency response break point of the ac loop in the SLIC. Refer to table 1 for recommended value of C_{HP}.

Example: A C_{HP} value of 68 nF will position the low end frequency response 3dB break point of the ac loop at 13 Hz (f_{3dB}) according to $f_{3dB} = 1/(2 \cdot \pi \cdot R_{HP} \cdot C_{HP})$ where R_{HP} = 180 kΩ.

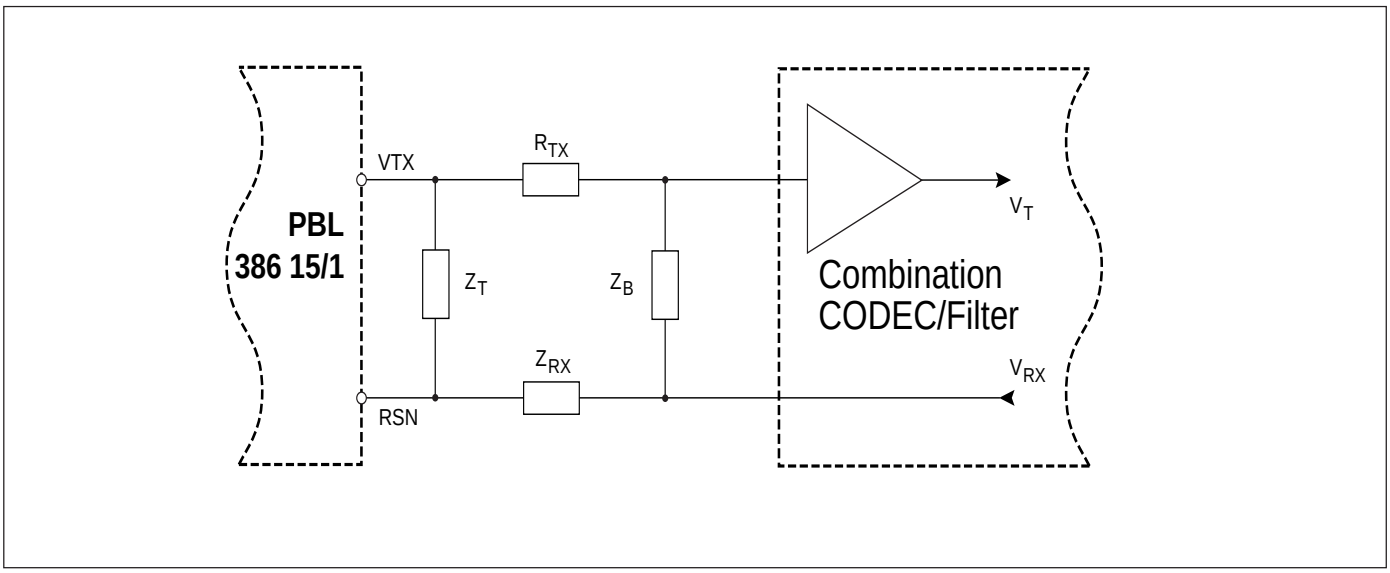


Figure 10. Hybrid function.

High-Pass Transmit Filter

When CODEC/filter with a single 5 V power supply is used, it is necessary to separate the different signal reference voltages between the SLIC and the CODEC/filter. In the transmit direction this can be done by connecting a capacitor between the VTX output of the SLIC and the CODEC/filter input. This capacitor will also form, together with R_{TX} and/or the input impedance of the CODEC/filter, a high-pass RC filter. It is recommended to position the 3 dB break point of this filter between 30 and 80 Hz to get a fast enough response for the dc steps that may occur with DTMF signaling.

Capacitor C_{LP}

The capacitor C_{LP}, which connects between the terminals LP and VBAT2, positions the high end frequency break point of the low pass filter in the dc loop in the SLIC. C_{LP} together with C_{HP} and Z_T (see section Two-Wire Impedance) forms the total two wire output impedance of the SLIC.

R_{FEED} [Ω]	C_{LP} [nF]	C_{HP} [nF]
2•25	470	68

Table 1. C_{LP} and C_{HP} values.

Adaptive Overhead Voltage, AOV

The Adaptive Overhead Voltage feature minimizes the power dissipation and at the same time provides a flexible solution for different system requirements and possible future changes concerning voice, metering and other signal levels. This is done by using an overhead voltage which automatically adapts to the signal level (voice + metering).
The PBL38615/1 will behave as a SLIC with fixed overhead for signals in the 0-20kHz range and with an amplitude less than $1V_{peak}$. For signal amplitudes between $1V_{Peak}$ and $2.5V_{Peak}$ the adaptive overhead function will expand the overhead voltage making it possible for the signal to propagate through the SLIC without distortion (This is the total sum of voice and metering signal). The expansion of the overhead occurs instantaneously. When the signal amplitude decreases, the overhead returns to its initial value with a time constant of approximately one second (see figure 11).

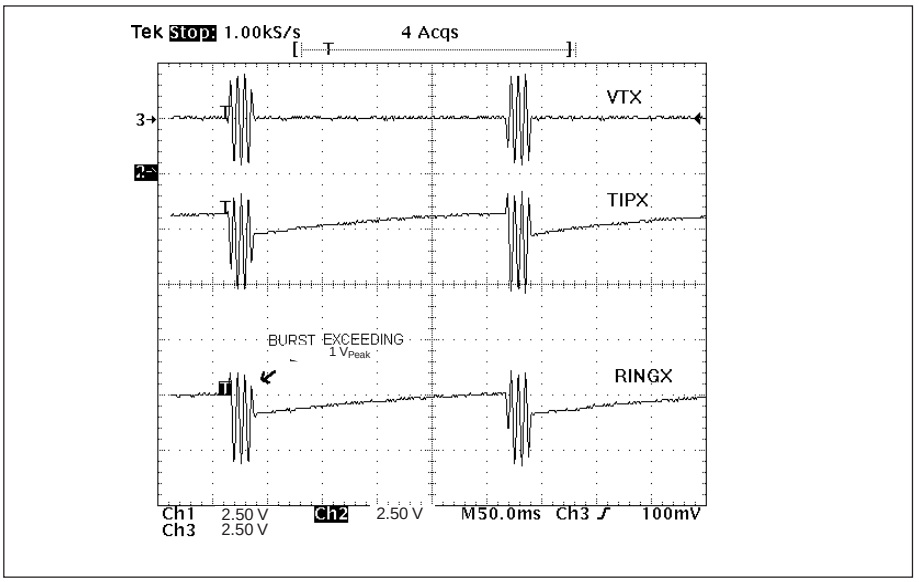


Figure 11. The AOV funktion when the AOV-pin is left open. (Observe, burst undersampled).

During operation the influence of the adaptive overhead function will not effect the SLIC performance in the constant current region of operation (see figure 11). If, however, the SLIC is in the off-hook, constant voltage region of operation then the influence of the adaptive headroom will be apparent as a slight decrease in line voltage (and hence line current) as the SLIC adjusts to accommodate the larger (voice + metering) signal.

Line Feed

If V_{TR} < | VBAT2 | -5.7 approx (See formula C in figure 17). the PBL 386 15/1 SLIC will emulate constant current feed. (references A-C in figure 17). The constant current region is adjustable between 18 mA and 30 mA.

If V_{TR} > | VBAT2 | -5.7 approx (See formula C in figure 17). the PBL 38615/1 SLIC will emulate a constant voltage feed with 2 x 25 Ω source impedance (references C-E in figure 17). This section is made as steep as possible to switch battery faster.

If the loop current is less than 5.5mA then the SLIC will automatically switch to supply the DC feed via Vbat rather than Vbat2 (references E in figure 17). This will not give any disturbances on the line.

The open loop voltage, V_{TRMAX}, measured between the TIPX and RINGX terminals tracks the battery voltage VBAT(references J in figure 17). According to the formula:

$$V_{TRMAX} = | VBAT | -4.6$$

When the line current is approaching open loop conditions (references G in figure 17) the overhead voltage is reduced. The line voltage is kept nearly constant with a steep slope corresponding to 2x25 Ω (references H in figure 17), to ensure maximum open loop voltage, even with a leaking telephone line.

Constant Current Region

The constant current (reference A-C in figure 17) is adjusted by connecting a resistor, R_{LC}, between terminal PLC and ground according to the equation:

$$R_{LC} = \frac{500}{I_{LProg}} - \frac{10.4 \cdot \ln(I_{LProg} \cdot 32)}{I_{LProg}}$$

Can simplifies to:

$$R_{LC} = \frac{500}{I_{LProg}}$$

Battery Switch

To reduce short loop power dissipation, a second battery voltage, Off-hook, must be connected to the device via an external diode at terminal VBAT2. The SLIC automatically switches between the two battery supply voltages without need for external control. The silent battery switching to VBAT occurs when the line current is below 5.5 mA. This means that the current in the On-hook battery is limited to 6 mA. To calculate the switching voltage use this formula (See formula C in figure 17):

$$V_{TR} = | VB2 | -4.4 - 50 \cdot I_{LProg}$$

If metering is used see section Metering Applications down below.

Connect the terminal VBAT2 to the second power supply via the diode D_{B2} in figure 15. A diode D_{BB} connected between VB and the VB2 power supply, see figure 15, will make sure that the SLIC continues to work on the second battery even if the first battery voltage disappears.

The current commute between the different batteries as shown in figure 12, note that some current is sourced from VB (typ. 0.5 mA, internal bias current) when the line current is sourced from VB2. The next chart (figure 13) is showing what power dissipation the SLIC is using with different batteries and variation of the line.

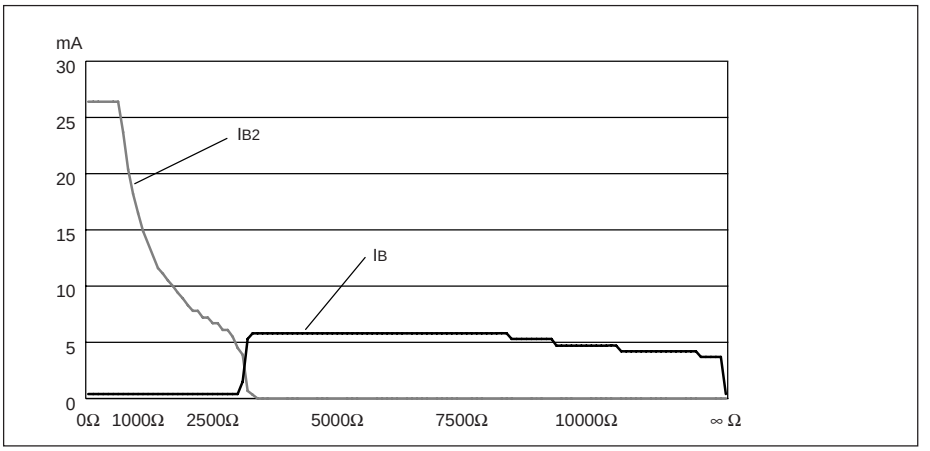


Figure 12. Chart describing current in Vbat and Vbat2.

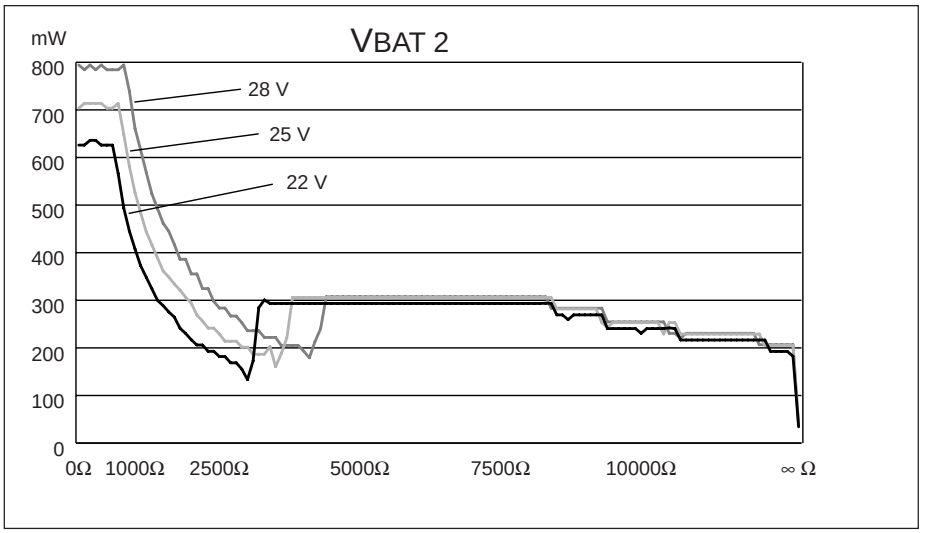


Figure 13. Chart describing Power dissipation with different Vbat2.

Metering Applications, TTX

It is very easy to use PBL 386 15/1 in metering applications; simply connect a suitable resistor (R_{TTX}) in series with a capacitor (C_{TTX}) between pin RSN and the metering source. Capacitor C_{TTX} decouples all DC-voltages that may be superimposed on the metering signal. The metering signal gain can be calculated from the equation:

$$G_{4\text{-}2TTX} = \frac{V_{TR}}{V_{TTX}} =$$

$$\frac{Z_T}{R_{TTX}} \cdot \frac{Z_{LTTX}}{\frac{Z_T}{\alpha_{RSN}} + G_{2\text{-}4S} \cdot (Z_{LTTX} + 2R_F)}$$

where:

V_{TTX} is the wanted metering voltage between the TIP and RING terminals

Z_{LTTX} is the line impedance seen by the 12 or 16 kHz metering signal,

$G_{2\text{-}4S}$ is the transmit gain through the SLIC, i e 0.5.

It is possible to mix voice voltage and metering voltage up to 2.5 Vpeak (1.7 Vrms), using AOV. Use following formula to calculate the switching voltage of the Battery Switch to get enough signal space.

$$V_{TR} = | VB2 | -3.4 - V_{voice} - V_{TTX} - 50 \cdot I_{LProg}$$

where:

V_{voice} is the voice voltage, normaly 1 V_{peak}

V_{TTX} is the the metering voltage in peak.

Silent Polarity Reversal

The reversal time is set by a capacitor, $C_{sprv,}$ between the pin SPR and AGND. The reversal has a setup time and reversal time see figure 14.

The setup time is different in Active- to Reversal-state and Reversal- to Active state but the silent polarity reversal time is the same Active- to Reversal-state and Reversal- to Active state. To calculate the silent polarity reversal time use following formula:

$t_r = C_{SPR} \cdot 9500$

Active- to Reversal-state and Reversal- to Active state and the setup time use following formulas.

Active → Reversal:
$t_{Act \rightarrow Rev} = C_{SPR} \cdot 17500$

Reversal → Active:
$t_{Rev \rightarrow Act} = C_{SPR} \cdot 15500$

The time is measured between 10% and 90% of the line voltage. The reversal time is independent of line load and line current.

Analog Temperature Guard

The widely varying environmental conditions in which SLICs operate may lead to the chip temperature limitations being exceeded. The PBL 386 15/1 SLIC reduces the dc line current and the longitudinal current limit when the chip temperature reaches approximately 145°C and increases it again automatically when the temperature drops.

The detector output, DET, is forced to a logic low level when the temperature guard is active.

The Active state temperature guard is exclusively viewed at detector output see section Active Temperature guard.

Loop Monitoring Functions

The loop current, ground key and ring trip detectors report their status through a common output, DET. The status of the detector pin, DET, is selected via the three bit control interface C1, C2 and C3. Please refer to section Control Inputs for a description of the control interface.

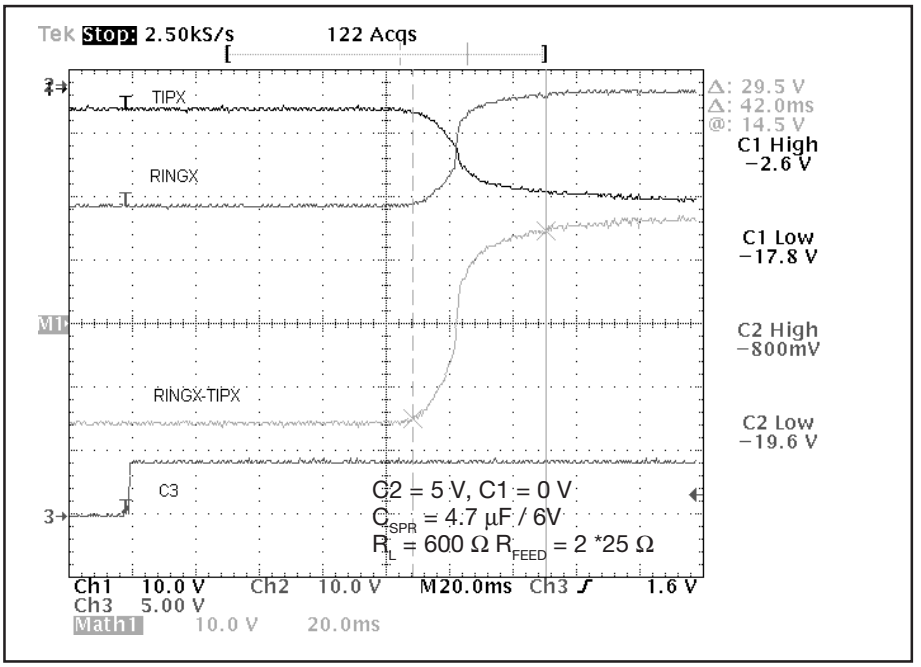


Figure 14. Silent Polarity Reversal

Loop Current Detector

The loop current detector indicates that the telephone is off hook and that DC current is flowing in the loop by putting the output pin DET, to a logic low level when selected. The loop current detector threshold value, I_{LTh}, where the loop current detector changes state, is programmable with the R_{LD} resistor. R_{LD} connects between pin PLD and ground and is calculated according to:

$$R_{LD} = \frac{500}{I_{LTh}}$$

Ground Key Detector

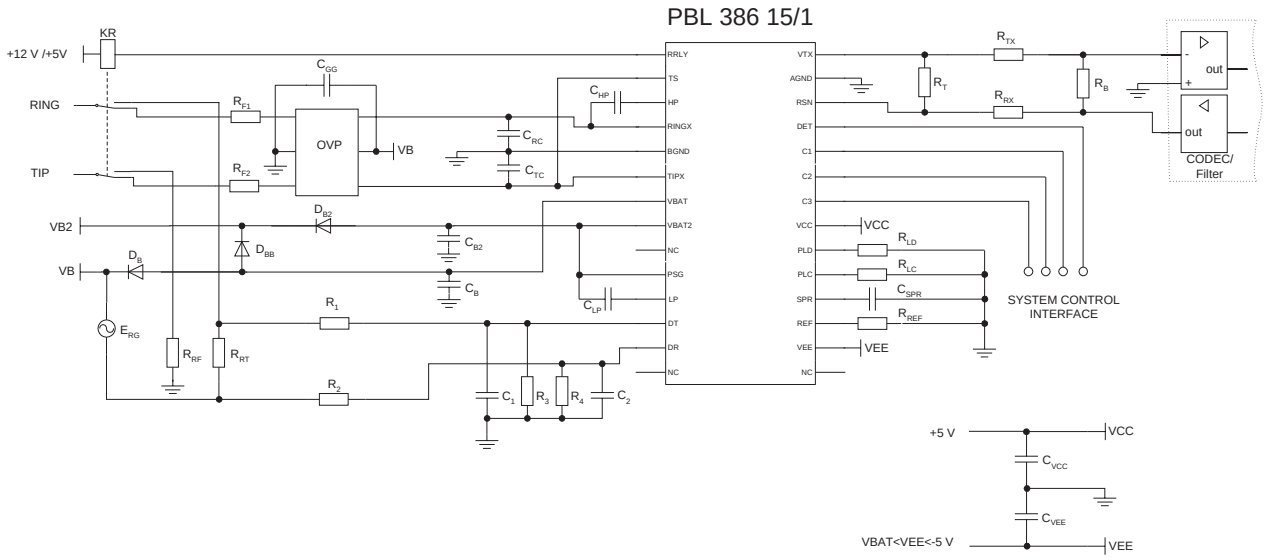
The ground key detector indicates when the ground key is pressed (active) by putting the output pin DET to a logic high level when selected. The ground key detector circuit senses the difference between TIPX and RINGX currents. The detector is triggered when the difference exceeds the current threshold.

Ring Trip Detector

Ring trip detection is accomplished by connecting an external network to a comparator in the SLIC with inputs DT and DR. The ringing source can be balanced or unbalanced e g superimposed on the battery voltage or ground. The unbalanced ringing source may be applied to either the ring lead or the tip lead with return via the other wire. A ring relay driven by the SLIC ring relay driver connects the ringing source to tip and ring.

The ring trip function is based on a polarity change at the comparator input when the line goes off-hook. In the on-hook state no dc current flows through the loop and the voltage at comparator input DT is more positive than the voltage at input DR. When the line goes off-hook, while the ring relay is energized, dc current flows and the comparator input voltage reverses polarity.

Figure 15 gives an example of a ring trip detection network. This network is applicable, when the ring voltage superimposed on the battery voltage is injected on the ring lead of the two-wire port. The dc voltage across sense resistor R_{RT} is monitored by the ring trip comparator input DT and DR via the filter network R_1, R_2, R_3, R_4, C_1 and C_2. DT is more positive than DR, with the line on-hook (no dc current). The DET output will report logic level high, i.e. the detector is not tripped. When the line goes off-hook, while ringing, a dc current will flow



RESISTORS (values according to IEC-63 E96 series):

R_{LD}	= 49.9 kΩ	1%	1/10 W
R_{LC}	= 18.7 kΩ	1%	1/10 W
R_{REF}	= 15 kΩ	1%	1/10 W
R_T	= 105 kΩ	1%	1/10 W
R_{TX}	= 32.4 kΩ	1%	1/10 W
R_B	= 57.6 kΩ	1%	1/10 W
R_{RX}	= 105 kΩ	1%	1/10 W
R_1	= 604 kΩ	1%	1/10 W
R_2	= 604 kΩ	1%	1/10 W
R_3	= 249 kΩ	1%	1/10 W
R_4	= 280 kΩ	1%	1/10 W
R_{RT}	= 332 Ω	5%	2 W
R_{RF}	= 332 Ω	5%	2 W
R_{F1}, R_{F2}	= Line resistor, 40 Ω 1% match		

CAPACITORS: (values according to IEC-63 E6 series):

C_B	= 100 nF	100 V 20%
C_{B2}	= 150 nF	100 V 20%
C_{VCC}	= 100 nF	10 V 20%
C_{VEE}	= 100 nF	10 V* 20%
C_{TC}	= 1.0 nF	100 V 20%
C_{RC}	= 1.0 nF	100 V 20%
C_{HP}	= 68 nF	100 V 20%
C_{LP}	= 470 nF	100 V 20%
C_{GG}	= 220 nF	100 V 20%
C_1	= 330 nF	63 V 10%
C_2	= 330 nF	63 V 10%
C_{SPR}	= optional	10 V 20%

*100V if VEE pin connected to VBAT, VBAT2

DIODES:

D_B	= 1N4448
D_{B2}	= 1N4448
D_{BB}	= 1N4448

OVP:
Secondary protection (e g Power Innovations TISP PBL2). The ground terminals of the secondary protection should be connected to the common ground on the Printed Board Assembly with a track as short and wide as possible, preferably a groundplane.

Figure 15. Single-channel subscriber line interface with PBL 386 15/1 and combination CODEC/filter

through the loop including sense resistor R_{RT} and will cause the input DT to become more negative than input DR. This changes the output on the DET pin to logic level low, i.e. tripped detector condition. The system controller (or line card processor) responds by de-energizing the ring relay via the SLIC, i.e. ring trip.

Complete filtering of the 20 Hz ac component at terminals DT and DR is not necessary. A toggling DET output can be examined by a software routine to determine the duty cycle. Off-hook condition is indicated when the DET output is at logic level low for more than half the time.

Detector Output (DET)

The PBL 386 15/1 SLIC incorporates a detector output driver designed as open collector (npn) with a current sinking capability of min 3 mA, and a 10 kΩ pull-up resistor. The emitter of the drive transistor is connected to AGND. A LED can be connected in series with a resistor (≈1 kΩ) at the DET output to visualize, for example loop status.

Relay driver

The PBL 386 15/1 SLIC incorporates a ring relay driver designed as open collector (npn) with a current sinking capability of 50 mA.The emitter of the drive transistor is connected to BGND. The relay driver has an internal zener diode clamp to protect the SLIC from inductive kick-back voltages. No external clamp is needed.

Control Inputs

The PBL 386 15/1 SLIC has three digital control inputs, C1, C2 and C3.
A decoder in the SLIC interprets the control input condition and sets up the commanded operating state.
C1 to C3 are internal pull-up inputs.

Open Circuit State

In the Open Circuit State the TIPX and RINGX line drive amplifiers as well as other circuit blocks are powered down. This causes the SLIC to present a high impedance to the line. Power dissipation is at a minimum and no detectors are active.

Ringing State

In the ringing state the SLIC will behave as in the active state with the exception that the ring relay driver and the ring trip detector are activated. The ring trip detector will indicate off hook with a logic low level at the detector output.

Active State

TIPX is the terminal closest to ground and sources loop current while RINGX is the more negative terminal and sinks loop current. The loop current or the ground key detector is activated. The loop current detector indicates off hook with a logic low level and the ground key detector indicates active ground key with a logic high level present at the detector output.

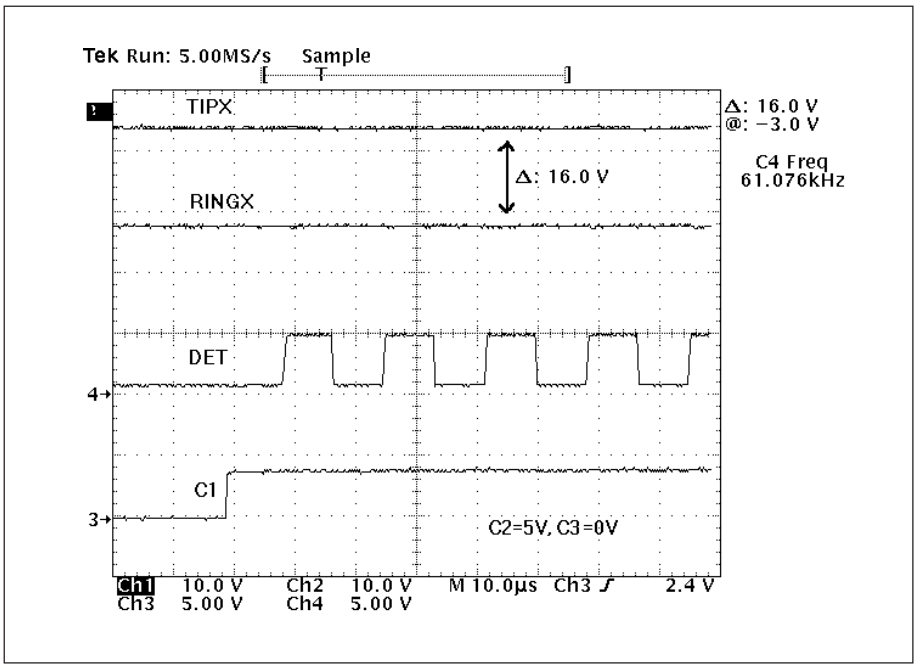


Figure 16. Line voltage measurment

Active Polarity Reversal State

TIPX and RINGX polarity is reversed compared to the Active State: RINGX is the terminal closest to ground and sources loop current while TIPX is the more negative terminal and sinks current. The loop current or the ground key detector is activated. The loop current detector will indicate off hook with a logic low level and the ground key detector will indicate active ground key with a logic high level present at the detector output.

Active Temperature guard state

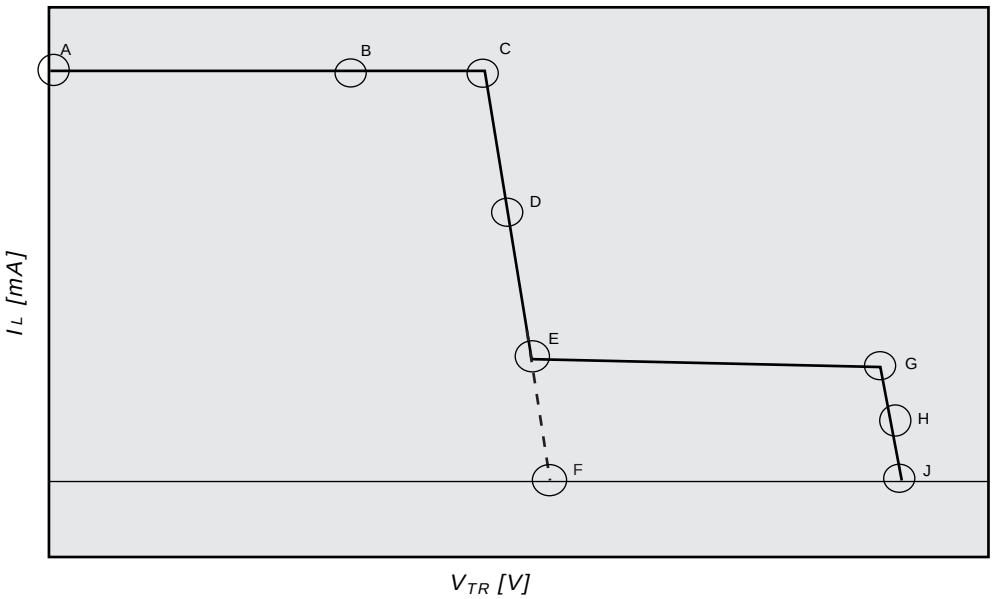
The temperature guard indicates if an error has occurred and the temperature guard is activated. The output pin DET is forced to a logic low level when activated .

Line Voltage measurement

The line voltage is presented on the detector output as a pulse train (see figure 16) with a frequency inversely proportional to the voltage according to the equation:

$$freq = \frac{10^6}{|V_{TR}| + 1} \text{ [Hz]}$$

The line voltage measurement will be started when entering this state from any other state and the SLIC will be as in active state except for the detector. The data can be used in variety of ways, for example to set transmission parameters in a programmable CODEC, in line testing where short circuits on the line can be detected and to control the metering signal amplitude.



A: I_L (@ V_{TR} = 0) = I_{LConst} I_{LConst} (typ) = I_{LProg} = $\frac{500}{R_{LC}}$ (13)

B,C: $I_L = I_{LConst}$, V_{TR}(@C)= V_{App} - R_{Feed} · I_{LProg}

D: R_{Feed} = 2 x 25 Ω

E: $I_L \approx$ 5.5 mA , V_{TR}= V_{App} - R_{Feed} · 5.5 mA

F: V_{APP} (@I_L =0) = V_{B2} - V_F^*-3.7 * Is the forward voltage of diode D_{VBAT2}.

G: $I_L \approx$ 5 mA

H: R_{Feed} = 2 x 25 Ω

J: V_{TRMAX} = |V_{Bat}| - 4.6 @ I_L = 0 mA

Figure 17. Battery feed characteristics (without the protection resistors on the line).

Overvoltage Protection

PBL 386 15/1 must be protected against overvoltages on the telephone line. The overvoltages could be caused for instance by lightning, ac power contact and induction. Refer to Maximum Ratings, TIPX and RINGX terminals, for maximum continuous and transient voltages.

Secondary Protection

The circuit shown in figure 15 utilizes series resistors together with a programmable overvoltage protector (e g Power Innovations TISP PBL2), serving as a secondary protection.

The TISP PBL2 is a dual forward-conducting buffered p-gate overvoltage protector. The protector gate references the protection (clamping) voltage to negative supply voltage (i.e. the battery voltage, V_B). As the protection voltage will track the negative supply voltage the overvoltage stress on the SLIC is minimized.

Positive overvoltages are clamped to ground by a diode. Negative overvoltages are initially clamped close to the SLIC negative supply rail voltage and the protector will crowbar into a low voltage on-state condition, by firing an internal thyristor.

A gate decoupling capacitor, C_{GG}, is needed to carry enough charge to supply a high enough current to quickly turn on the thyristor in the protector. C_{GG} should be placed close to the overvoltage protection device. Without the capacitor even the low inductance in the track to the V_B supply will limit the current and delay the activation of the thyristor clamp.

The fuse resistors R_F serve the dual purposes of being non- destructive energy dissipators, when transients are clamped and of being fuses, when the line is exposed to a power cross. If a PTC is chosen for R_F , note that it is important to always use the PTC´s in series with resistors not sensitive to temperature, as the PTC will act as a capacitance for fast transients and therefore will not protect the TISP.

Power-up Sequence

No special power-up sequence is necessary except that ground has to be present before all other power supply voltages.

The digital inputs C1 to C3 are internal pull-up terminals.

Printed Circuit Board Layout

Care in Printed Circuit Board (PCB) layout is essential for proper function;

The components connecting to the RSN input should be placed in close proximity to that pin, such that no interference is injected into the RSN pin. Ground plane surrounding the RSN pin is advisable.

Analog ground (AGND) should be connected to battery ground (BGND) on the PCB in one point.

R_{LC} and R_{REF} should be connected to AGND with short leads. Pin LP and pin PSG are sensitive to leakage currents.

R_{SG} and C_{LP} connections to VBAT2 should be short and very close to each other.

C_B and C_{B2} must be connected with short wide leads.

Ordering Information

Package	Temp. Range	Part No.
28pin SSOP Tape & Reel	-40° - + 85 °C	PBL 386 15/1 SHT

Ericsson Microelectronics
SE-164 81 Kista-Stockholm, Sweden
Telephone: +46 8 757 50 00