# SYNCHRONOUS SRAM MODULE

# 32K, 64K x 64 SRAM

**with Tag RAM**

256KB/512KB, 3.3V, FLOW-THROUGH OR PIPELINED SYNCHRONOUS BURST, SECONDARY CACHE MODULES

## FEATURES

- 160-lead, dual-in-line memory module (DIMM) for Intel 82430FX Triton PCIset
- Fast access times: 9, 11 and 12ns burst, 7 and 8ns pipelined burst
- Fast OE# access times: 5 and 6ns
- Single +3.3V +10%/-5% power supply
- Individual BYTE WRITE control
- Clock controlled, registered, address, data and control
- Internally self-timed WRITE cycle
- Low capacitive bus loading
- High 30pF output drive capability at rated access time

## OPTIONS — MARKING

| OPTIONS | MARKING |
|---|---|
| • Timing (Burst) | |
| 9ns access/15ns cycle/66 MHz | -9 |
| 11ns access/15ns cycle/60 MHz | -11 |
| 12ns access/20ns cycle/50 MHz | -12 |
| • Timing (Pipelined Burst) | |
| 7ns access/15ns cycle/66 MHz or 60 MHz | -7 |
| 8ns access/20ns cycle/50 MHz | -8 |
| • Packages | |
| 160-lead DIMM (gold) | G |

## VALID PART NUMBERS

| PART NUMBER | DESCRIPTION |
|---|---|
| MT3LST3264G-xx | 32K x 64, Burst |
| MT5LST6464G-xx | 64K x 64, Burst |
| MT3LST3264PG-xx | 32K x 64, Pipelined Burst |
| MT5LST6464PG-xx | 64K x 64, Pipelined Burst |

## GENERAL DESCRIPTION

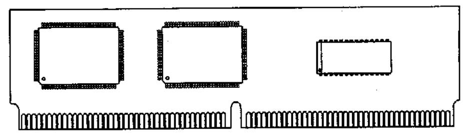
The Micron SyncBurst SRAM module family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using an advanced CMOS process.

The MT3LST3264 module integrates two 32K x 32 synchronous SRAMs and 32K x 8 Tag RAM. The MT5LST6464 integrates four 32K x 32 synchronous SRAMs and 32K x 8 Tag RAM. All synchronous inputs pass through registers controlled by positive-edge-triggered clock inputs (CLK0 and CLK1). The synchronous inputs include all addresses, data inputs, active LOW chip enable (CS#), burst control

## PIN ASSIGNMENT (Front View)

**160-Pin DIMM**

(SB-1) 32K x 64
(SB-2) 64K x 64



| PIN # | SYMBOL | PIN # | SYMBOL | PIN # | SYMBOL | PIN # | SYMBOL |
|---|---|---|---|---|---|---|---|
| 1 | Vss | 41 | DQ58 | 81 | Vss | 121 | DQ59 |
| 2 | TDQ0 | 42 | DQ56 | 82 | TDQ1 | 122 | DQ57 |
| 3 | TDQ2 | 43 | Vss | 83 | TDQ7 | 123 | Vss |
| 4 | TDQ6 | 44 | DQ54 | 84 | TDQ5 | 124 | DQ55 |
| 5 | TDQ4 | 45 | DQ52 | 85 | TDQ3 | 125 | DQ53 |
| 6 | RSVD | 46 | DQ50 | 86 | RSVD | 126 | DQ51 |
| 7 | Vcc | 47 | DQ48 | 87 | RSVD | 127 | DQ49 |
| 8 | TWE# | 48 | Vss | 88 | RSVD | 128 | Vss |
| 9 | ADSC# | 49 | DQ46 | 89 | ADV# | 129 | DQ47 |
| 10 | Vss | 50 | DQ44 | 90 | Vss | 130 | DQ45 |
| 11 | CWE4# | 51 | DQ42 | 91 | COE# | 131 | DQ43 |
| 12 | CWE6# | 52 | Vcc | 92 | CWE5# | 132 | RSVD |
| 13 | CWE0# | 53 | DQ40 | 93 | CWE7# | 133 | DQ41 |
| 14 | CWE2# | 54 | DQ38 | 94 | CWE1# | 134 | DQ39 |
| 15 | Vcc | 55 | DQ36 | 95 | RSVD | 135 | DQ37 |
| 16 | CS# | 56 | Vss | 96 | CWE3# | 136 | Vss |
| 17 | GWE# | 57 | DQ34 | 97 | RSVD | 137 | DQ35 |
| 18 | BWE# | 58 | DQ32 | 98 | RSVD | 138 | DQ33 |
| 19 | Vss | 59 | DQ30 | 99 | Vss | 139 | DQ31 |
| 20 | A3 | 60 | Vcc | 100 | RSVD | 140 | RSVD |
| 21 | A7 | 61 | DQ28 | 101 | A4 | 141 | DQ29 |
| 22 | A5 | 62 | DQ26 | 102 | A6 | 142 | DQ27 |
| 23 | A11 | 63 | DQ24 | 103 | A8 | 143 | DQ25 |
| 24 | A16 | 64 | Vss | 104 | A10 | 144 | Vss |
| 25 | Vcc | 65 | DQ22 | 105 | RSVD | 145 | DQ23 |
| 26 | A18 | 66 | DQ20 | 106 | A17 | 146 | DQ21 |
| 27 | Vss | 67 | DQ18 | 107 | Vss | 147 | DQ19 |
| 28 | A12 | 68 | Vcc | 108 | A9 | 148 | RSVD |
| 29 | A13 | 69 | DQ16 | 109 | A14 | 149 | DQ17 |
| 30 | ADSP# | 70 | DQ14 | 110 | A15 | 150 | DQ15 |
| 31 | ECS1# | 71 | DQ12 | 111 | RSVD | 151 | DQ13 |
| 32 | ECS2# | 72 | Vss | 112 | PD0 | 152 | Vss |
| 33 | PD1 | 73 | DQ10 | 113 | PD2 | 153 | DQ11 |
| 34 | PD3 | 74 | DQ8 | 114 | PD4 | 154 | DQ9 |
| 35 | Vss | 75 | DQ6 | 115 | Vss | 155 | DQ7 |
| 36 | CLK1 | 76 | Vcc | 116 | CLK0 | 156 | RSVD |
| 37 | Vss | 77 | DQ4 | 117 | Vss | 157 | DQ5 |
| 38 | DQ62 | 78 | DQ2 | 118 | DQ63 | 158 | DQ3 |
| 39 | Vcc | 79 | DQ0 | 119 | RSVD | 159 | DQ1 |
| 40 | DQ60 | 80 | Vss | 120 | DQ61 | 160 | Vss |

## GENERAL DESCRIPTION (continued)

inputs (ADSC#, ADSP#, ADV#) and byte write enables (CWE0#-7#).

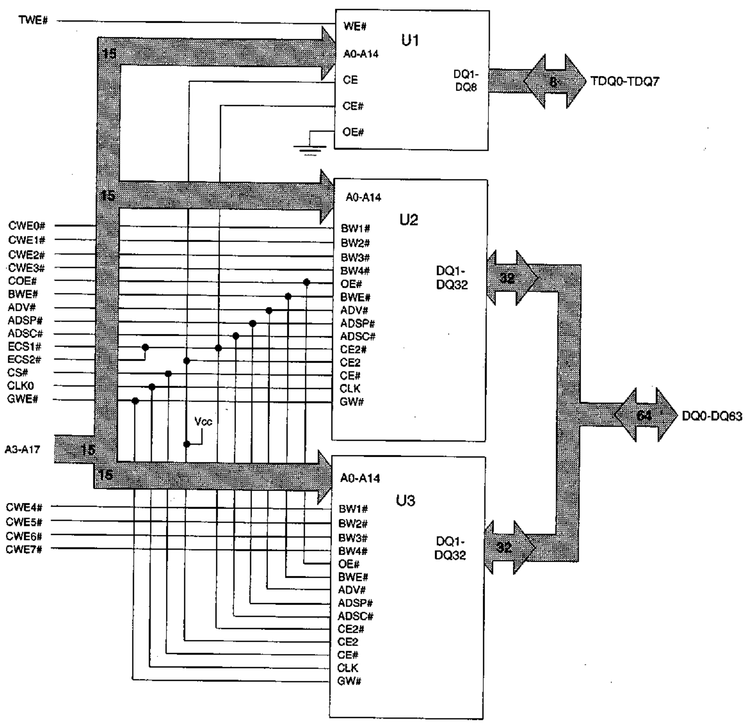
Asynchronous inputs include the output enable (COE#) and the clocks (CLK0 and CLK1). The data-out (Q), enabled by COE#, is also asynchronous. WRITE cycles can be from 1 to 8 bytes wide as controlled by the byte write enables.

Burst operation can be initiated with either address status processor (ADSP#) or address status controller (ADSC#) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pins (ADV#).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. CWE0# controls DQ0-DQ7, CWE1# controls DQ8-DQ15, CWE2# controls DQ16-DQ23, CWE3# controls DQ24-DQ31 and so forth.

The module operates from a +3.3V power supply and all inputs and outputs are TTL-compatible and 5V-tolerant. This module is ideally suited to Pentium™ systems and those systems which benefit from a very wide data bus. For additional functional and timing information consult Micron's MT58LC32K32B3 and MT58LC32K32D8 data sheets.

### FUNCTIONAL BLOCK DIAGRAM
### 256KB
### (32K x 64)

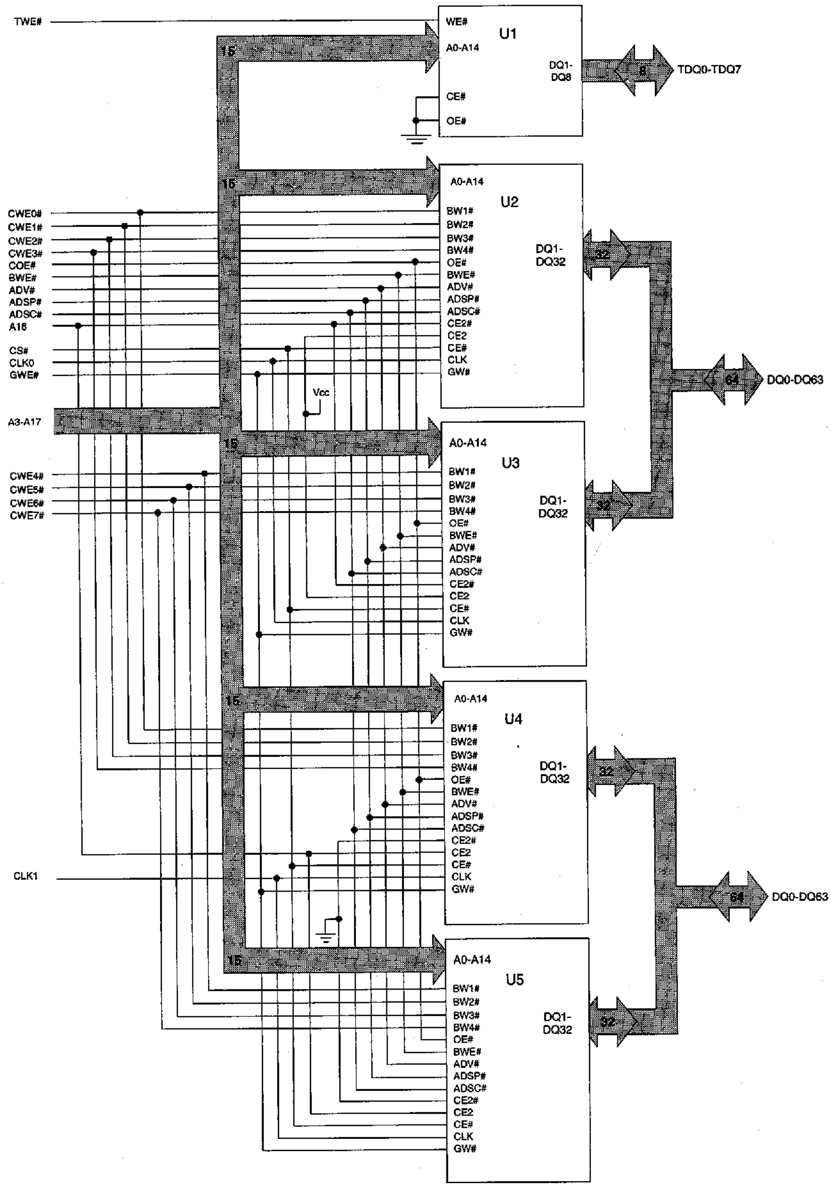



U1= 32K x 8
U2-U3 = MT58LC32K32B3LG (Burst)
U2-U3 = MT58LC32K32D8LG (Pipelined Burst)

**NOTE:** 1. Functional Block Diagrams illustrate simplified module operation. See Truth Table, Pin Descriptions and timing diagrams for detailed information.

SYNCHRONOUS SRAM MODULE

## FUNCTIONAL BLOCK DIAGRAM
## 512KB
## (64K x 64)




U1= 32K x 8
U2-U5 = MT58LC32K32B3LG (Burst)
U2-U3 = MT58LC32K32D8LG (Pipelined Burst)

SYNCHRONOUS SRAM MODULE

## PIN DESCRIPTIONS

| MODULE PINS | SYMBOL | TYPE | DESCRIPTION |
|---|---|---|---|
| 20-24, 26, 28-29, 101-104, 106, 108-110 | A3-A18 | Input | Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. |
| 11-14, 92-94, 96 | CWE0#-7# | Input | Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A BYTE WRITE enable is LOW for a WRITE cycle and HIGH for a READ cycle. CWE0# controls DQ0-DQ7 and DQP0. CWE1# controls DQ8-DQ15 and DQP1. CWE2# controls DQ16-DQ23 and DQP2. CWE3# controls DQ24-DQ31 and DQP3, and so forth. Data I/O are tristated if any of these eight inputs are LOW. |
| 18 | BWE# | Input | Byte Write Enable: This active LOW input permits byte write operations and must meet the setup and hold times around the rising edge of CLK0-1. |
| 8 | TWE# | Input | Tag RAM Write Enable: This active LOW input controls the Tag portion of the module. |
| 17 | GWE# | Input | Global Write Enable: This active LOW input allows a full 64-bit WRITE to occur independent of the CWEn# and BWE# lines and must meet the setup and hold times around the rising edge of CLK0-1. |
| 36, 116 | CLK0-CLK1 | Input | Clock: This signal latches the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge. (CLK1 used on 64K x 64 only). |
| 16 | CS# | Input | Synchronous Chip Enable: This active LOW input is used to enable the devices and conditions the internal use of ADSP#. This input is sampled only when a new external address is loaded. |
| 91 | COE# | Input | Output Enable: This active LOW asynchronous input enables the data I/O output drivers. |
| 89 | ADV# | Input | Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an ADSP# cycle is initiated if a WRITE cycle is desired (to ensure use of correct address). |
| 30 | ADSP# | Input | Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be latched. A READ is performed using the new address, independent of the byte write enables and ADSC#. ADSP# is ignored if CE# is HIGH. |
| 9 | ADSC# | Input | Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst and causes a new external address to be latched. A READ or WRITE is performed using the new address if all chip enables are active. Power-down state is entered if one or more chip enables are inactive. |

## PIN DESCRIPTIONS (continued)

| MODULE PINS | SYMBOL | TYPE | DESCRIPTION |
|---|---|---|---|
| 31-32 | ECS1#-ECS2# | Input | Expansion Chip Selects: These active LOW inputs allow expansion of a 32K x 64 module with another 32K x 64 module. These pins are used internal to the module on the 64K x 64, and therefore are no connects on the edge connector. |
| 38, 40-42, 44-47, 49-51, 53-55, 57-59, 61-63, 65-67, 69-71, 73-75, 77-79, 118, 120-122, 124-127, 129-131, 133-135, 137-139, 141-143, 145-147, 149-151, 153-155, 157-159 | DQ0-DQ63 | Input/ Output | SRAM Data I/O: Byte 1 is DQ0-DQ7; Byte 2 is DQ8-DQ15; Byte 3 is DQ16-DQ23; Byte 4 is DQ24-DQ31 and so forth. Input data must meet setup and hold times around the rising edge of CLK. |
| 2-5, 82-85 | TDQ0-TDQ7 | Input/ Output | Tag Data I/O |
| 33-34, 112-114 | PD0-PD4 | Output | Presence Detect: These pins are configured based on the size and type of the DIMM. |
| 7, 15, 25, 39, 52, 60, 68, 76 | Vcc | Supply | Power Supply: +3.3V ±5% |
| 1, 10, 19, 27, 35, 37, 43, 48, 56, 64, 72, 80, 81, 90, 99, 107, 115, 117, 123, 128, 136, 144, 152, 160 | Vss | Supply | Ground: GND |
| 6, 86, 88, 97-98, 100, 111 | RSVD | - | No Connect: These pins are reserved. |

## INTERLEAVED BURST ADDRESS TABLE

| First Address (External) | Second Address (Internal) | Third Address (Internal) | Fourth Address (Internal) |
|---|---|---|---|
| X...X00 | X...X01 | X...X10 | X...X11 |
| X...X01 | X...X00 | X...X11 | X...X10 |
| X...X10 | X...X11 | X...X00 | X...X01 |
| X...X11 | X...X10 | X...X01 | X...X00 |

## PRESENCE-DETECT TABLE

| CACHE SIZE/TYPE | PD4 | PD3 | PD2 | PD1 | PD0 |
|---|---|---|---|---|---|
| 256KB/Burst | Vss | NC | Vss | NC | Vss |
| 256KB/Pipelined Burst | Vss | NC | Vss | NC | NC |
| 512KB/Burst | Vss | Vss | NC | NC | Vss |
| 512KB/Pipelined Burst | Vss | Vss | NC | NC | NC |
| 512KB/2-Bank Pipelined Burst | Vss | Vss | NC | Vss | Vss |

## TRUTH TABLE

| OPERATION | ADDRESS USED | CS# | CE2# | CE2 | ADSP# | ADSC# | ADV# | WRITE# | COE# | CLK0-1 | DQ0-63 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Deselected Cycle, Power-down | None | H | X | X | X | L | X | X | X | L-H | High-Z |
| Deselected Cycle, Power-down | None | L | X | L | L | X | X | X | X | L-H | High-Z |
| Deselected Cycle, Power-down | None | L | H | X | L | X | X | X | X | L-H | High-Z |
| Deselected Cycle, Power-down | None | L | X | L | H | L | X | X | X | L-H | High-Z |
| Deselected Cycle, Power-down | None | L | H | X | H | L | X | X | X | L-H | High-Z |
| READ Cycle, Begin Burst | External | L | L | H | L | X | X | X | L | L-H | Q |
| READ Cycle, Begin Burst | External | L | L | H | L | X | X | X | H | L-H | High-Z |
| WRITE Cycle, Begin Burst | External | L | L | H | H | L | X | L | X | L-H | D |
| READ Cycle, Begin Burst | External | L | L | H | H | L | X | H | L | L-H | Q |
| READ Cycle, Begin Burst | External | L | L | H | H | L | X | H | H | L-H | High-Z |
| READ Cycle, Continue Burst | Next | X | X | X | H | H | L | H | L | L-H | Q |
| READ Cycle, Continue Burst | Next | X | X | X | H | H | L | H | H | L-H | High-Z |
| READ Cycle, Continue Burst | Next | H | X | X | X | H | L | H | L | L-H | Q |
| READ Cycle, Continue Burst | Next | H | X | X | X | H | L | H | H | L-H | High-Z |
| WRITE Cycle, Continue Burst | Next | X | X | X | H | H | L | L | X | L-H | D |
| WRITE Cycle, Continue Burst | Next | H | X | X | X | H | L | L | X | L-H | D |
| READ Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | L | L-H | Q |
| READ Cycle, Suspend Burst | Current | X | X | X | H | H | H | H | H | L-H | High-Z |
| READ Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | L | L-H | Q |
| READ Cycle, Suspend Burst | Current | H | X | X | X | H | H | H | H | L-H | High-Z |
| WRITE Cycle, Suspend Burst | Current | X | X | X | H | H | H | L | X | L-H | D |
| WRITE Cycle, Suspend Burst | Current | H | X | X | X | H | H | L | X | L-H | D |

**NOTE:**

1. X means "don't care." H means logic HIGH. L means logic LOW. WRITE#=L means any one or more byte write enable signals (CWE0#-CWE7#) and BWE# are LOW or GWE# is LOW. WRITE#=H means all byte write enable signals are HIGH.
2. CWE0# enables WRITEs to DQ0-DQ7, CWE1# enables WRITEs to DQ8-DQ15, and so forth.
3. All inputs except COE# must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a WRITE operation following a READ operation, COE# must be HIGH before the input data setup time and held HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. ADSP# LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and BWE# LOW or GWE# LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

## ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss ........ -0.5V to +4.6V
$V_{IN}$ ........................................................ -0.5V to Vcc +0.5V
Storage Temperature (plastic) .................... -55°C to +125°C
Short Circuit Output Current .................................. 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Vcc = +3.3V +10%/-5% unless otherwise noted)

| DESCRIPTION | CONDITIONS | | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Input High (Logic 1) Voltage | | | $V_{IH}$ | 2.0 | Vcc +0.3V | V | 1, 2 |
| Input Low (Logic 0) Voltage | | | $V_{IL}$ | -0.3 | 0.8 | V | 1, 2 |
| Input Leakage Current | $0V \leq V_{IN} \leq V_{CC}$ | ECS1#-ECS2# | $I_{LI1}$ | -3 | 3 | µA | |
| | | A3-A17 | $I_{LI2}$ | -5 | 5 | µA | |
| | | TWE# | $I_{LI3}$ | -1 | 1 | µA | |
| | | All other inputs | $I_{LI4}$ | -2 | 2 | µA | |
| Output Leakage Current | Output(s) Disabled, $0V \leq V_{OUT} \leq V_{CC}$ | | $I_{LO}$ | -2 | 2 | µA | |
| Output High Voltage | $I_{OH}$ = -4.0mA | | $V_{OH}$ | 2.4 | | V | 1 |
| Output Low Voltage | $I_{OL}$ = 8.0mA | | $V_{OL}$ | | 0.4 | V | 1 |
| Supply Voltage | | | $V_{CC}$ | 3.135 | 3.6 | V | 1 |

| DESCRIPTION | CONDITIONS | SYM | SIZE | TYP | MAX -7 | MAX -8 | MAX -9 | MAX -11 | MAX -12 | UNITS | NOTES |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Power Supply Current: Operating | Device selected; all inputs $\leq V_{IL}$ or $\geq V_{IH}$; cycle time $\geq {}^tKC$ MIN; Vcc = MAX; outputs open | $I_{CC1}$ | 256KB<br>512KB | 300<br>575 | 725<br>1,325 | 625<br>1,125 | 625<br>1,125 | 570<br>1,020 | 510<br>910 | mA<br>mA | 3, 5, 6 |
| Power Supply Current: Idle | Device selected; Vcc = MAX; ADSC#, ADSP#, ADV# $\geq V_{IH}$; all inputs $\leq$ Vss +0.2 or $\geq$ Vcc -0.2; cycle time $\geq {}^tKC$ MIN | $I_{CC2}$ | 256KB<br>512KB | 77<br>137 | 190<br>350 | 180<br>330 | 180<br>330 | 180<br>330 | 170<br>310 | mA<br>mA | 5, 6 |
| CMOS Standby | Device deselected; Vcc = MAX; all inputs $\leq$ Vss +0.2 or $\geq$ Vcc -0.2; all inputs static; CLK frequency = 0 | $I_{SB1}$ | 256KB<br>512KB | 2.0<br>3.0 | 13<br>23 | 13<br>23 | 13<br>23 | 13<br>23 | 13<br>23 | mA<br>mA | 5, 6 |
| TTL Standby | Device deselected; Vcc = MAX; all inputs $\leq V_{IL}$ or $\geq V_{IH}$; all inputs static; CLK frequency = 0 | $I_{SB2}$ | 256KB<br>512KB | 47<br>77 | 80<br>130 | 75<br>125 | 80<br>130 | 75<br>125 | 75<br>125 | mA<br>mA | 5, 6 |
| Clock Running | Device deselected; Vcc = MAX; all inputs $\leq$ Vss +0.2 or $\geq$ Vcc -0.2; CLK cycle time $\geq {}^tKC$ MIN | $I_{SB3}$ | 256KB<br>512KB | 77<br>137 | 190<br>350 | 180<br>330 | 180<br>330 | 180<br>330 | 170<br>310 | mA<br>mA | 5, 6 |

## CAPACITANCE

| DESCRIPTION | CONDITIONS | SYMBOL | MAX 256KB | MAX 512KB | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Capacitance: A3-A17, ECS1#-ECS2# | $T_A$ = 25°C; f = 1 MHz | $C_{I1}$ | 18 | 26 | pF | 4 |
| Input Capacitance: ADSP#, ADV#, CLK0-1, COE#, TWE#, ADSC#, BWE#, GWE#, A18 | Vcc = 3.3V | $C_{I2}$ | 10 | 20 | pF | 4 |
| Input Capacitance: CWE0#-CWE7# | | $C_{I3}$ | 5 | 10 | pF | 4 |
| Input/Output Capacitance: DQ0-63, TDQ0-7 | | $C_O$ | 10 | 20 | pF | 4 |

## NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +4.6V$ for $t \leq {}^tKC/2$ for $I \leq 20mA$
   Undershoot: $V_{IL} \geq -0.7V$ for $t \leq {}^tKC/2$ for $I \leq 20mA$
   Power-up: $V_{IH} \leq +3.6V$ and $V_{CC} \leq 3.135V$ for $t \leq 200ms$
3. Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. "Device deselected" means device is in POWER-DOWN mode as defined in the truth table. "Device selected" means device is active (not in POWER-DOWN mode).
6. Typical values are measured at 3.3V, 25°C and 20ns cycle time.

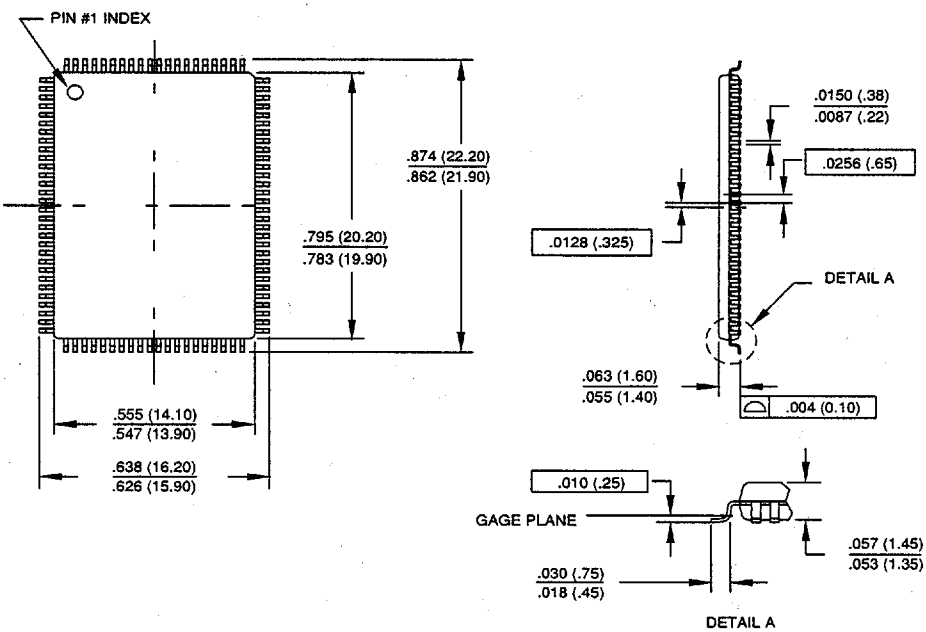
SYNCHRONOUS SRAM MODULE

# PACKAGE SELECTION GUIDE

| PACKAGE TYPE | REFERENCE CODE | PIN COUNT | WIDTH | PAGE |
|---|---|---|---|---|
| TQFP | | | | |
| | SA | 100 | 14.0 mm x 20.0 mm | 7-1 |

| PACKAGE TYPE | REFERENCE CODE | PIN COUNT | HEIGHT | PAGE |
|---|---|---|---|---|
| MODULE DIMM | | | | |
| | SB | 160 | 1.150" | 7-2 |

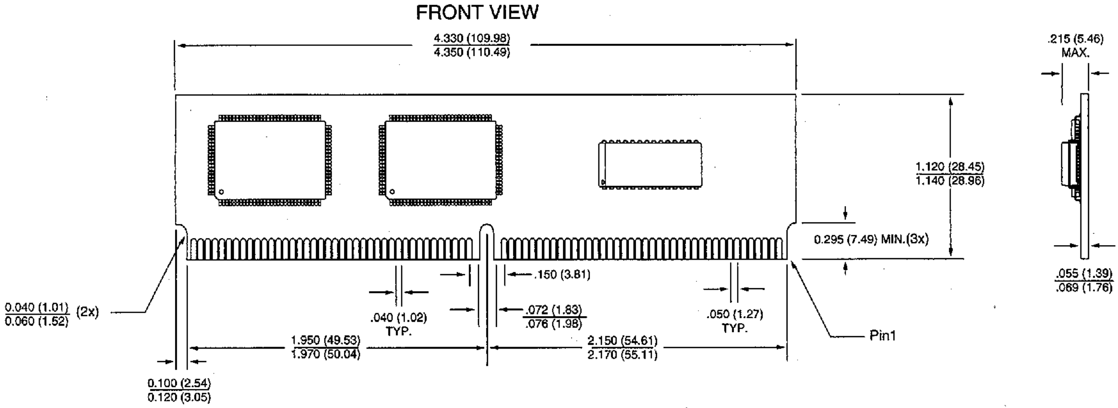
## 100-PIN TQFP
SA-1



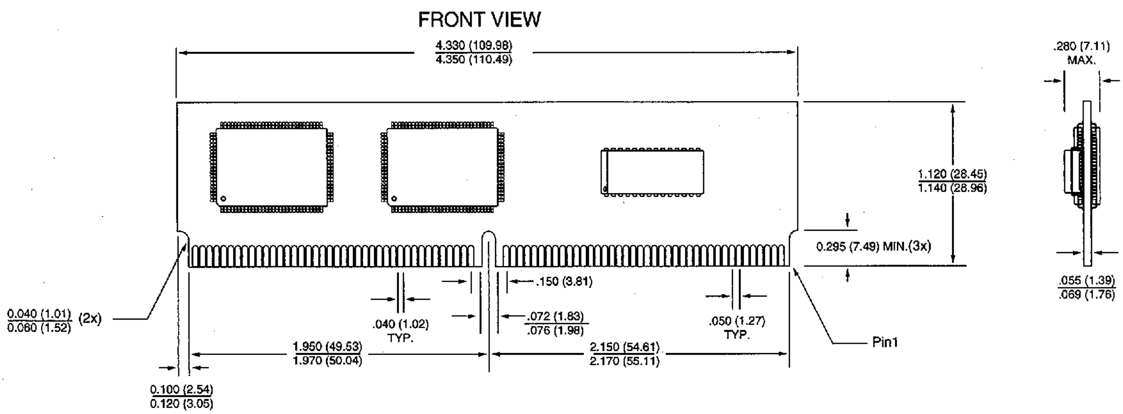

**NOTE:** 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

## 160-PIN MODULE DIMM
SB-1

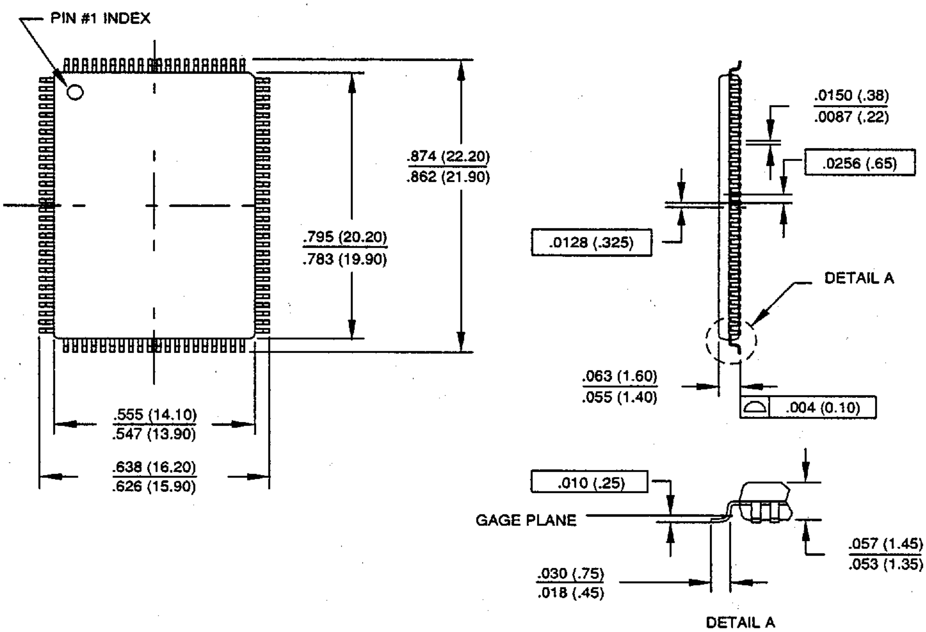



## 160-PIN MODULE DIMM
SB-2




**NOTE:** 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

## 100-PIN TQFP
SA-1



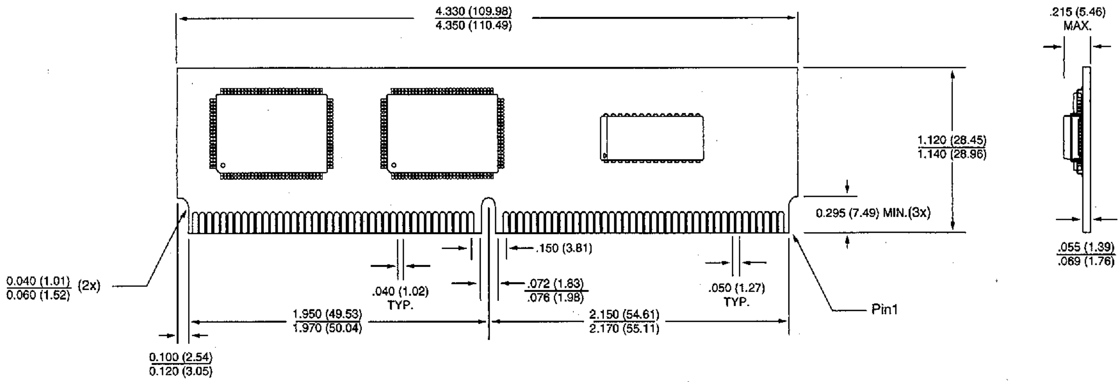

**NOTE:** 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

## 160-PIN MODULE DIMM

### SB-1

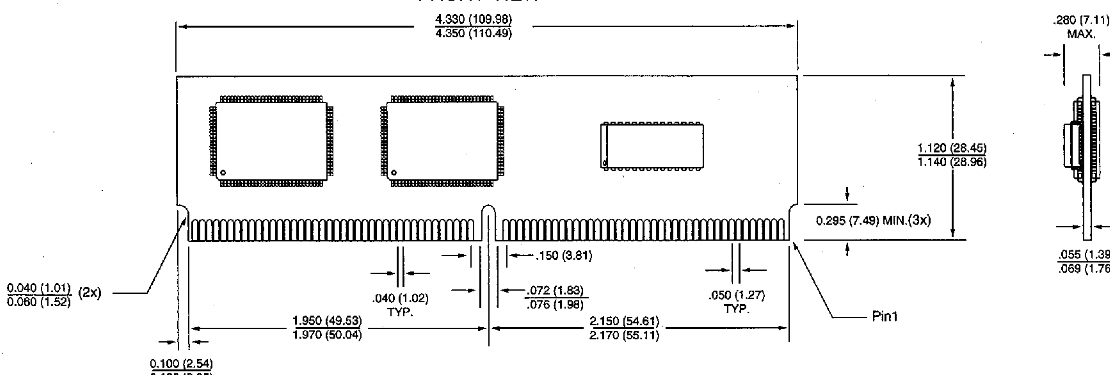
FRONT VIEW




## 160-PIN MODULE DIMM

### SB-2

FRONT VIEW




**NOTE:** 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.