

## Features

64Kx32 bit CMOS Static

Random Access Memory

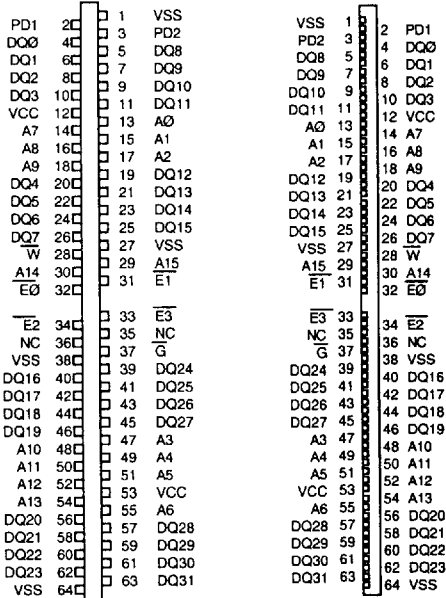
- Access Times 15 thru 35ns
- Individual Byte Selects
- Output Enable Function
- Fully Static, No Clocks
- TTL Compatible I/O

High Density Packaging

- 64 Pin SIMM, No. 30-Straight
- 64 Pin SIMM, No. 342 Angled
- 64 Pin ZIP, No. 87
- JEDEC Standard Pinout
- Common Data Inputs and Outputs

Single +5V (±10%) Supply Operation

## Pin Configurations and Block Diagram



PD1 - Open  
PD2 - VSS

## 64Kx32 Static RAM CMOS, High Speed Module

The ED18F3265C is a high speed 2 megabit Static RAM module organized as 64Kx32. This module is constructed from eight 64Kx4 Static RAMs in SOJ packages on an epoxy laminate (FR4) board.

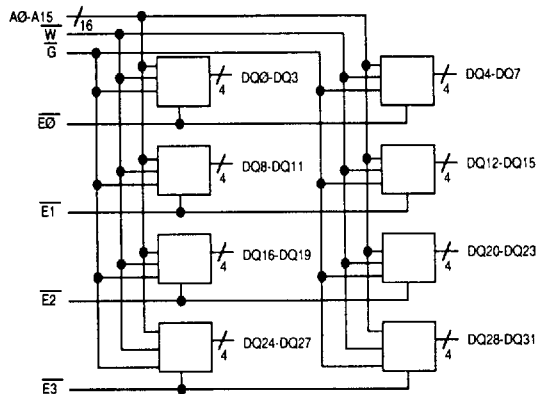
Four chip Enables ( $\overline{E0}$ - $\overline{E3}$ ) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

The ED18F3265C is offered in a both 64 lead SIMM and 64 pin ZIP packages, which enable two megabits of memory to be placed in less than 1.2 square inches of board space.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation and providing equal access and cycle times for ease of use.

### Pin Names

A0-A15	Address Inputs
$\overline{E0}$ - $\overline{E3}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQ0-DQ3	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection



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### Absolute Maximum Ratings\*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Storage Temperature	
Plastic	-55°C to +125°C
Power Dissipation	8.0 Watt
Output Current	20 mA

\*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

### AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	1TTL, CL = 30pF

(note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF)

### DC Electrical Characteristics

Parameter	Sym	Conditions	ns	Min	Typ*	Max	Units
Operating Power	ICC1	$\bar{W}, \bar{E} = VIL, I/O = 0mA$	15ns	--	880	1120	mA
Supply Current		Min Cycle	20-35ns		740	980	mA
Standby (TTL) Power	ICC2	$\bar{E} \geq VIH, VIN \leq VIL$		--	150	280	mA
Supply Current		$VIN \geq VIH$					
Full Standby Power	ICC3	$\bar{E} \geq VCC-0.2V$		--	80	160	mA
Supply Current		$VIN \geq VCC-0.2V$ or					
CMOS		$VIN \leq 0.2V$					
Input Leakage Current	ILI	$VIN = 0V$ to VCC		--	--	±20	µA
Output Leakage Current	ILO	$V I/O = 0V$ to VCC		--	--	±80	µA
Output High Voltage	VOH	$I/OH = -4.0mA$		2.4	--	--	V
Output Low Voltage	VOL	$I/O L = 8.0mA$		--	--	0.4	V

\*Typical: TA = 25°C, VCC = 5.0V

### Truth Table

$\bar{G}$	$\bar{E}$	$\bar{W}$	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOU $\bar{T}$	ICC1
X	L	L	Write	DIN	ICC1

### Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Input Capacitance (Except DQ Pins)	CI	60	pF
Capacitance (DQ Pins)	CD/Q	20	pF
Input (E)	CC	20	pF
Input (W) Line (G)	CW	60	pF

These parameters are sampled, not 100% tested.

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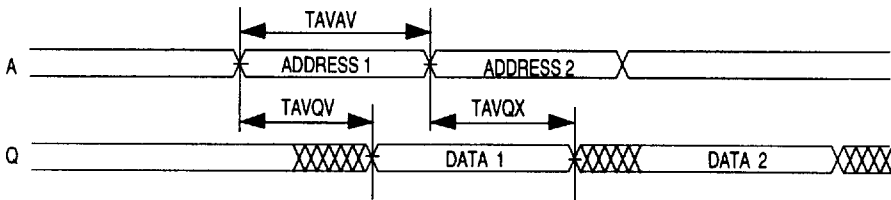
**ED18F3265C**  
64Kx32 SRAM Module

**AC Characteristics Read Cycle**

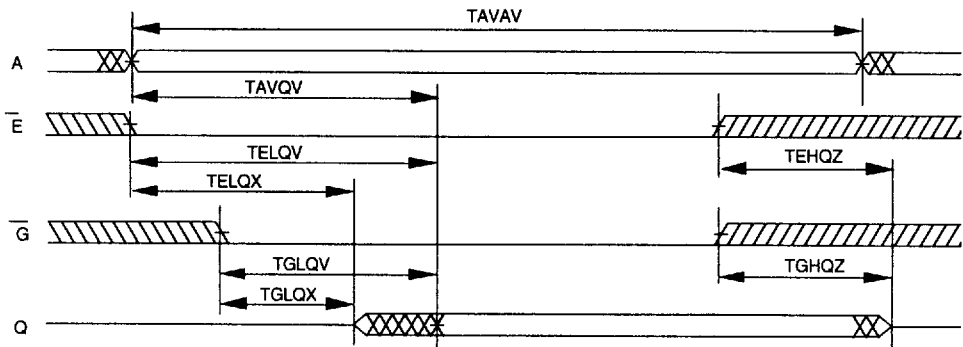
	Symbol		15ns		20ns		25ns		35ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	TRC	15		20		25		35		ns
Address Access Time	TAVQV	TAA		15		20		25		35	ns
Chip Enable Access Time	TELQV	TACS		15		20		25		35	ns
Chip Enable to Output in Low Z(1)	TELOX	TCLZ		3		3		3		3	ns
Chip Disable to Output in High Z(1)	TEHQZ	TCHZ	0	8	0	10	0	12	0	15	ns
Output Hold from Address Change	TAVQX	TOH		3		3		3		3	ns
Output Enable to Output Valid	TGLQV	TOE		8		10		15		20	ns
Output Enable to Output in Low Z(1)	TGLQX	TOLZ		0		0		0		0	ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ	0	6	0	8	0	10	0	12	ns

Note 1: Parameter guaranteed, but not tested.

**Read Cycle 1 - W High, G, E Low**



**Read Cycle 2 - W High**



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### AC Characteristics Write Cycle

Parameter	Symbol		15ns		20ns		25ns		35ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV	TWC	15		20		25		35		ns
Chip Enable to End of Write	TELWH	TCW	10		15		20		30		ns
Address Setup Time	TELEH	TCW	10		15		20		30		ns
	TAVWL	TAS	0		2		2		2		ns
Address Valid to End of Write	TAVEL	TAS	0		2		2		2		ns
	TAVWH	TAW	13		15		20		25		ns
Write Pulse Width	TAVEH	TAW	13		15		20		25		ns
	TWLWH	TWP	13		15		20		25		ns
Write Recovery Time	TWLEH	TWP	13		15		20		25		ns
	TWHAX	TWR	2		2		2		2		ns
Data Hold Time	TEHAX	TWR	2		2		2		2		ns
	TWHDX	TDH	3		1		1		1		ns
Write to Output in High Z (1)	TEHDX	TDH	3		1		1		1		ns
	TWLQZ	TWHZ	0	8	0	10	0	12	0	15	ns
Data to Write Time	TDVWH	TDW	10		12		15		20		ns
	TDVEH	TDW	10		12		15		20		ns
Output Active from End of Write (1)	TWHQX	TWLZ	3		3		3		3		ns

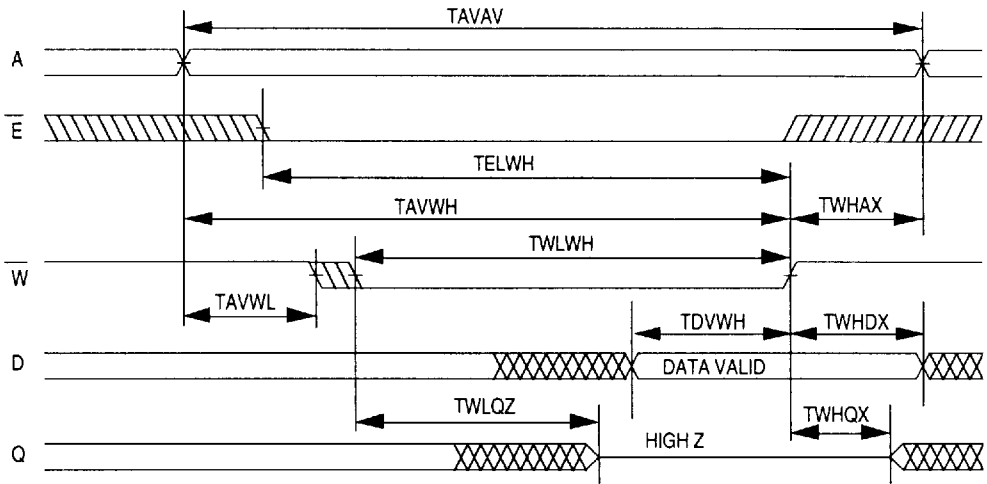
Note 1: Parameter guaranteed, but not tested.

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**ED18F3265C**

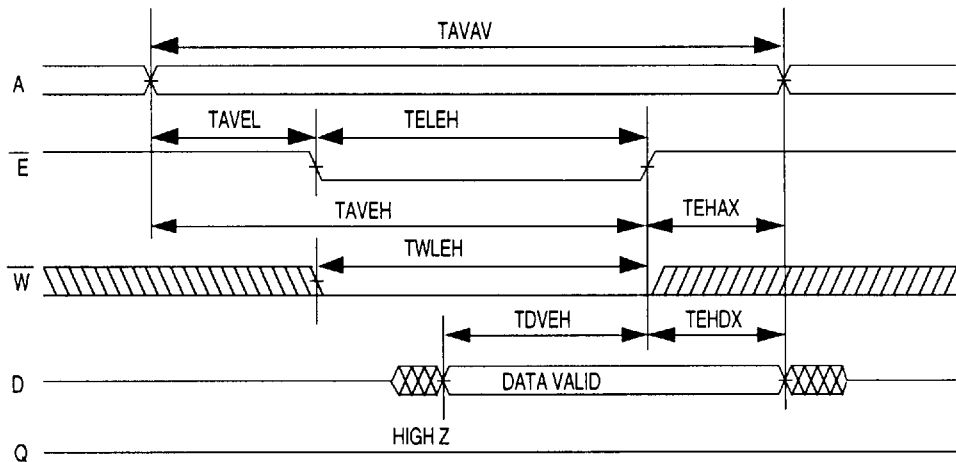
64Kx32 SRAM Module

**Write Cycle 1 - W Controlled**



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**Write Cycle 2 - E Controlled**



### Ordering Information

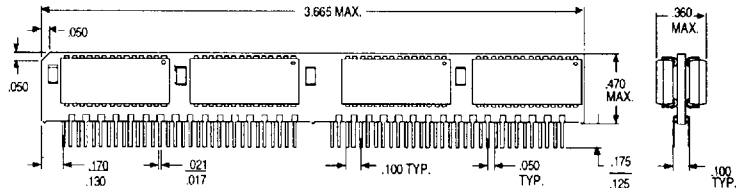
Part Number	Speed (ns)	Package No.
EDI8F3265C15MZC	15	87
EDI8F3265C20MZC	20	87
EDI8F3265C25MZC	25	87
EDI8F3265C35MZC	35	87

Part Number	Speed (ns)	Package No.
EDI8F3265C15MMC	15	30
EDI8F3265C20MMC	20	30
EDI8F3265C25MMC	25	30
EDI8F3265C35MMC	35	30
EDI8F3265C15MNC	15	342
EDI8F3265C20MNC	20	342
EDI8F3265C25MNC	25	342
EDI8F3265C35MNC	35	342

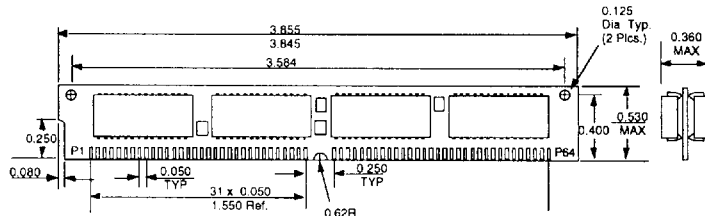
Note: To order an Industrial grade product substitute the letter C in the Suffix with the letter I, eg. EDI8F3265C20MZC becomes EDI8F3265C20MI.

### Package Description

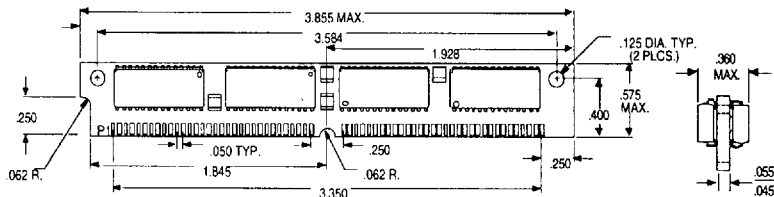
#### Package No. 87 64 Pin ZIP



#### Package No. 30 64 Pin SIMM Straight



#### Package No. 342 64 Pin SIMM Angled



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