

CY7C1061AV33

16-Mbit (1 M × 16) Static RAM

Features

- High speed
 □ t_{AA} = 10 ns
- Low active power 990 mW (max)
- Operating voltages of 3.3 ± 0.3 V
- 2.0 V data retention
- Automatic power down when deselected
- TTL compatible inputs and outputs
- Easy memory expansion with \overline{CE}_1 and CE_2 features
- Available in Pb-free and non Pb-free 54-pin TSOP II package and non Pb-free 60-ball fine pitch ball grid array (FBGA) package

Functional Description

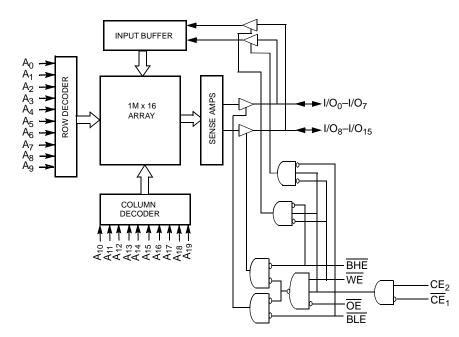
The CY7C1061AV33 is a high performance CMOS Static RAM organized as 1,048,576 words by 16 bits.

To write to the device, enable the chip (\overline{CE}_1 LOW and CE_2 HIGH) while forcing the Write Enable (\overline{WE}) input LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₉). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₉).

To read from the device, enable the chip by taking \overline{CE}_1 LOW and CE_2 HIGH while forcing the Output Enable (\overline{OE}) LOW and the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins will appear on I/O₀ to I/O₇. If Byte High Enable (\overline{BHE}) is LOW, then data from memory will appear on I/O₈ to I/O₁₅. See "Truth Table" on page 8 for a complete description of Read and Write modes.

The input/output pins (I/O₀ through I/O₁₅) are placed in a high-impedance state when the device is deselected (\overline{CE}_1 HIGH/CE₂ LOW), the outputs are disabled (\overline{OE} HIGH), the BHE and BLE are disabled (BHE, BLE HIGH), or a Write operation is in progress (\overline{CE}_1 LOW, CE₂ HIGH, and \overline{WE} LOW).

Logic Block Diagram



198 Champion Court

٠

San Jose, CA 95134-1709 • 408-943-2600 Revised February 2, 2011



CY7C1061AV33

Contents

| Pin Configurations | Selection Guide | 3 |
|--|--|---|
| Operating Range DC Electrical Characteristics (Over the Operating Range) Capacitance AC Test Loads and Waveforms AC Switching Characteristics (Over the Operating Range) Data Retention Waveform Switching Waveforms Read Cycle No. 1 (Address Transition Controlled) Read Cycle No. 2 (OE Controlled) Write Cycle No. 1 (CE1 or CE2 Controlled) Write Cycle No. 2 (WE Controlled, OE LOW) | Pin Configurations | 3 |
| DC Electrical Characteristics (Over the Operating Range) | Maximum Ratings | 4 |
| (Over the Operating Range) Capacitance | Operating Range | 4 |
| Capacitance | DC Electrical Characteristics | |
| AC Test Loads and Waveforms AC Switching Characteristics (Over the Operating Range) Data Retention Waveform Switching Waveforms Read Cycle No. 1 (Address Transition Controlled) Read Cycle No. 2 (OE Controlled) Write Cycle No. 1 (CE1 or CE2 Controlled) Write Cycle No. 2 (WE Controlled, OE LOW) | (Over the Operating Range) | 4 |
| AC Switching Characteristics (Over the Operating Range) Data Retention Waveform | Capacitance | 4 |
| (Over the Operating Range) Data Retention Waveform Switching Waveforms Read Cycle No. 1 (Address Transition Controlled) Read Cycle No. 2 (OE Controlled) Write Cycle No. 1 (CE1 or CE2 Controlled) Write Cycle No. 2 (WE Controlled, OE LOW) | AC Test Loads and Waveforms | 4 |
| Data Retention Waveform Switching Waveforms Read Cycle No. 1 (Address Transition Controlled) Read Cycle No. 2 (OE Controlled) Write Cycle No. 1 (CE1 or CE2 Controlled) Write Cycle No. 2 (WE Controlled, OE LOW) | | |
| Switching Waveforms Read Cycle No. 1 (Address Transition Controlled) Read Cycle No. 2 (OE Controlled) Write Cycle No. 1 (CE1 or CE2 Controlled) Write Cycle No. 2 (WE Controlled, OE LOW) | (Over the Operating Range) | 5 |
| Read Cycle No. 1 (Address Transition Controlled) Read Cycle No. 2 (OE Controlled) Write Cycle No. 1 (CE1 or CE2 Controlled) Write Cycle No. 2 (WE Controlled, OE LOW) | Data Retention Waveform | 6 |
| Read Cycle No. 2 (OE Controlled) Write Cycle No. 1 (CE1 or CE2 Controlled) Write Cycle No. 2 (WE Controlled, OE LOW) | Switching Waveforms | 6 |
| Write Cycle No. 1 (CE1 or CE2 Controlled) Write Cycle No. 2 (WE Controlled, OE LOW) | Read Cycle No. 1 (Address Transition Controlled) | 6 |
| Write Cycle No. 2 (WE Controlled, OE LOW) | Read Cycle No. 2 (OE Controlled) | 6 |
| | Write Cycle No. 1 (CE1 or CE2 Controlled) | 7 |
| Write Cycle No. 3 (BHE/BLE Controlled) | Write Cycle No. 2 (WE Controlled, OE LOW) | 7 |
| | Write Cycle No. 3 (BHE/BLE Controlled) | 8 |

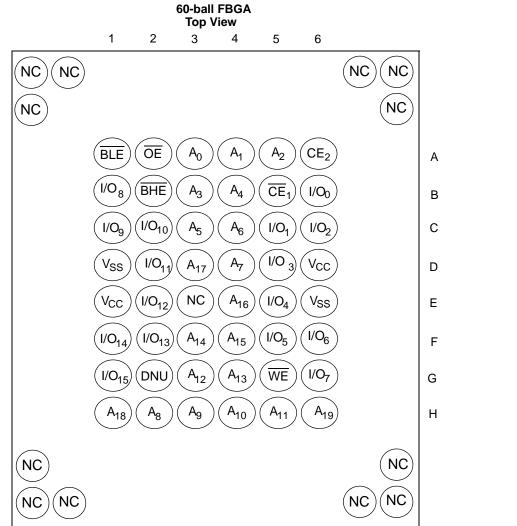
| Truth Table | 8 |
|---|----|
| Ordering Information | 9 |
| Ordering Code Definitions | 9 |
| Package Diagrams | 10 |
| Document History Page | 12 |
| Sales, Solutions, and Legal Information | 13 |
| Worldwide Sales and Design Support | 13 |
| Products | 13 |
| PSoC Solutions | 13 |



Selection Guide

| | | –10 | Unit |
|------------------------------|-----------------------|-----|------|
| Maximum Access Time | | 10 | ns |
| Maximum Operating Current | Commercial | 275 | mA |
| | Industrial | 275 | |
| Maximum CMOS Standby Current | Commercial/Industrial | 50 | mA |

Pin Configurations^[1, 2]



| 54-pin | TSOP | 11 |
|--------|-------|----|
| (Тор | View) | |

| I/O ₁₂ □ | 1 | 54 ⊒I/O ₁₁ |
|---------------------|----------|-----------------------------------|
| V _{CC} | 2 | 53 V _{SS} |
| I/Õ ₁₃ □ | 3 | 52 I/O ₁₀ |
| I/O14 | 4 | 51 I/Q |
| Vss⊑ | 5 | 50 □ V _{CC} |
| I/O ₁₅ □ | 6 | 49 ∐ I/Õ õ |
| Â₄⊑ | 7 | 48 🛛 A ₅ |
| A ₃ ⊑ | 8 | 47 🗆 A ₆ |
| A_2 | 9 | 46 🛛 A ₇ |
| A1 | 10 | 45 🛛 🗛 |
| A ₀ □ | 11 | 44 □ A ₉ |
| BHEL | 12 | 43 □ NC |
| CE1C | 13 | 42 🛛 OE |
| V _{CC} | 14 | 41 □ V _{SS} |
| WEL | 15 | 40 <u>DNU</u> |
| CE ₂ L | 16 | 39 🗆 BLE |
| A ₁₉ □ | 17 | ³⁸ 🛛 A ₁₀ |
| A ₁₈ | 18 | 37 🛛 A ₁₁ |
| A ₁₇ □ | 19 | 36 A12 |
| A ₁₆ | 20 | 35 A13 |
| | 21 | ³⁴ □ A ₁₄ |
| I/Q₀⊑ | 22 23 | 33 I/O7 |
| V _{CC} E | 23 24 | 32 □ V _{SS} 31 □ I/Qa |
| I/ପ୍ਰ⊑ I/ଠ୍ର⊑ | 24 25 | 30 TI/O |
| | 25 26 | 30 ∐ 1/O5 29 ∐ VCC |
| VSSL I/O3⊑ | 20 | 29 □ VCC 28 □ I/Q₁ |
| ., O3L | | 20 1/ 04 |
| | | |

Notes

1. NC pins are not connected on the die.

^{2.} DNU (Do Not Use) pins have to be left floating or tied to VSS to ensure proper operation.



Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

| Storage Temperature | –65 °C to +150 °C |
|--|--------------------------------|
| Ambient Temperature with | |
| Power Applied | |
| Supply Voltage on V_{CC} to Relative GND ^[3] | []] –0.5 V to +4.6 V |
| DC Voltage Applied to Outputs in High-Z State ^[3] 0. | |
| in High-Z State ^[3] –0. | 5 V to V _{CC} + 0.5 V |

Current into Outputs (LOW)...... 20 mA

Operating Range

| Range | Ambient Temperature | v _{cc} | |
|------------|------------------------|-----------------|--|
| Commercial | 0 °C to +70 °C | $3.3~V\pm0.3~V$ | |
| Industrial | –40 °C to +85 °C | | |

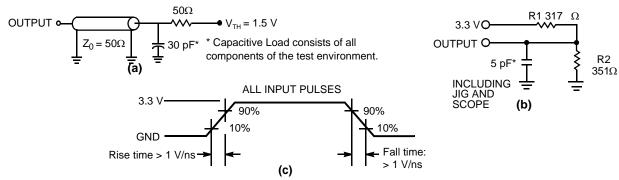
DC Electrical Characteristics (Over the Operating Range)

| Paramatar | Description | Tast Conditions | | | –10 | Unit |
|------------------|--|--|---------------------------|------|-----------------------|------|
| Parameter | Description Test Conditions | | | | Max | Unit |
| V _{OH} | Output HIGH Voltage | I _{OH} = -4.0 mA | | 2.4 | | V |
| V _{OL} | Output LOW Voltage | I _{OL} = 8.0 mA | | | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | | 2.0 | V _{CC} + 0.3 | V |
| V _{IL} | Input LOW Voltage [3] | | | -0.3 | 0.8 | V |
| I _{IX} | Input Leakage Current | $GND \le V_I \le V_{CC}$ | $GND \le V_1 \le V_{CC}$ | | | μA |
| I _{OZ} | Output Leakage Current | $GND \leq V_O \leq V_{CC}, O$ | utput Disabled | -1 | +1 | μA |
| I _{CC} | V _{CC} Operating | V _{CC} = max, | Commercial | | 275 | mA |
| | Supply Current | $f = f_{max} = 1/t_{RC}$ | Industrial | | 275 | mA |
| I _{SB1} | Automatic CE Power-down Current —TTL Inputs | $\begin{array}{l} CE_2 <= V_{IL,} \max V_{CC}, \ \overline{CE} \ge V_{IH} \\ V_{IN} \ge V_{IH} \text{ or } \\ V_{IN} \le V_{IL}, \ f = f_{max} \end{array}$ | | | 70 | mA |
| I _{SB2} | Automatic CE Power-down Current —CMOS Inputs | $\begin{array}{c} {\sf CE}_2 <= 0.3 \ {\sf V} \\ {\sf max} \ {\sf V}_{{\sf CC}}, \\ {\sf CE} \geq {\sf V}_{{\sf CC}} - 0.3 \ {\sf V}, \\ {\sf V}_{{\sf IN}} \geq {\sf V}_{{\sf CC}} - 0.3 \ {\sf V}, \\ {\sf or} \ {\sf V}_{{\sf IN}} \leq 0.3 \ {\sf V}, \ {\sf f} = 0 \end{array}$ | Commercial/ Industrial | | 50 | mA |

Capacitance [4]

| Parameter | Description | Test Conditions | TSOP II | FBGA | Unit |
|------------------|-------------------|---|---------|------|------|
| C _{IN} | Input Capacitance | $T_A = 25 \ ^{\circ}C, f = 1 \ MHz, V_{CC} = 3.3 \ V$ | 6 | 8 | pF |
| C _{OUT} | I/O Capacitance | | 8 | 10 | pF |

AC Test Loads and Waveforms ^[5]



Notes

- V_{IL} (min) = -2.0 V for pulse durations of less than 20 ns.
 Tested initially and after any design or process changes that may affect these parameters.
 Valid SRAM operation does not occur until the power supplies have reached the minimum operating V_{DD} (3.0 V). As soon as 1 ms (T_{power}) after reaching the minimum operating V_{DD}, normal SRAM operation can begin including reduction in V_{DD} to the data retention (V_{CCDR}, 2.0 V) voltage.



AC Switching Characteristics (Over the Operating Range) [6]

| D | | | -10 | |
|----------------------|---|-----|-----|------|
| Parameter | Description | Min | Мах | Unit |
| Read Cycle | | | | |
| t _{power} | V _{CC} (typical) to the first access ^[7] | 1 | | ms |
| t _{RC} | Read Cycle Time | 10 | | ns |
| t _{AA} | Address to Data Valid | | 10 | ns |
| t _{OHA} | Data Hold from Address Change | 3 | | ns |
| t _{ACE} | CE ₁ LOW/CE ₂ HIGH to Data Valid | | 10 | ns |
| t _{DOE} | OE LOW to Data Valid | | 5 | ns |
| t _{LZOE} | OE LOW to Low-Z | 1 | | ns |
| t _{HZOE} | OE HIGH to High-Z ^[8] | | 5 | ns |
| t _{LZCE} | CE ₁ LOW/CE ₂ HIGH to Low-Z ^[8] | 3 | | ns |
| t _{HZCE} | CE ₁ HIGH/CE ₂ LOW to High-Z ^[8] | | 5 | ns |
| t _{PU} | CE ₁ LOW/CE ₂ HIGH to Power Up ^[9] | 0 | | ns |
| t _{PD} | CE ₁ HIGH/CE ₂ LOW to Power Down ^[9] | | 10 | ns |
| t _{DBE} | Byte Enable to Data Valid | | 5 | ns |
| t _{LZBE} | Byte Enable to Low-Z | 1 | | ns |
| t _{HZBE} | Byte Disable to High-Z | | 5 | ns |
| Write Cycle [10, 11] | | | | |
| t _{WC} | Write Cycle Time | 10 | | ns |
| t _{SCE} | CE ₁ LOW/CE ₂ HIGH to Write End | 7 | | ns |
| t _{AW} | Address Setup to Write End | 7 | | ns |
| t _{HA} | Address Hold from Write End | 0 | | ns |
| t _{SA} | Address Setup to Write Start | 0 | | ns |
| t _{PWE} | WE Pulse Width | 7 | | ns |
| t _{SD} | Data Setup to Write End | 5.5 | | ns |
| t _{HD} | Data Hold from Write End 0 | | | ns |
| t _{LZWE} | WE HIGH to Low-Z ^[8] | 3 | | ns |
| t _{HZWE} | WE LOW to High-Z ^[8] | | 5 | ns |
| t _{BW} | Byte Enable to End of Write | 7 | | ns |

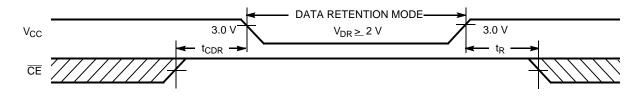
Notes

page 4, unless specified otherwise.
7. This part has a voltage regulator that steps down the voltage from 3 V to 2 V internally. t_{power} time must be provided initially before a Read/Write operation is started.
8. t_{HZOE}, t_{HZXE}, t_{HZEE} and t_{LZOE}, t_{LZWE}, t_{LZEE} are specified with a load capacitance of 5 pF as in (b) of "AC Test Loads and Waveforms ^[5]" on page 4. Transition is measured ±200 mV from steady-state voltage.
9. These parameters are guaranteed by design and are not tested.
10. The internal Write time of the memory is defined by the overlap of CE₁ LOW (CE₂ HIGH) and WE LOW. Chip enables must be active and WE and byte enables must be LOW to initiate a Write, and the transition of any of these signals can terminate the Write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the Write.
11. The minimum Write cycle time for Write Cycle No. 2 (WE controlled, OE LOW) is the sum of t_{HZWE} and t_{SD}.

Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and specified transmission line loads. Test conditions for the Read cycle use output loading shown in (a) of the "AC Test Loads and Waveforms" on page 4, unless specified otherwise. 6.

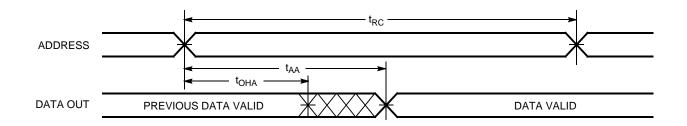


Data Retention Waveform

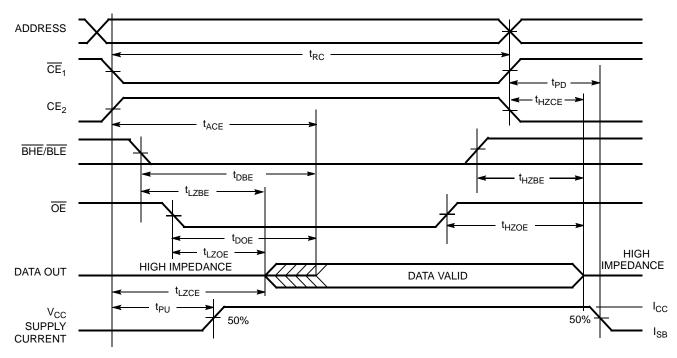


Switching Waveforms

Read Cycle No. 1 (Address Transition Controlled) [12, 13]



Read Cycle No. 2 (OE Controlled) [13, 14]



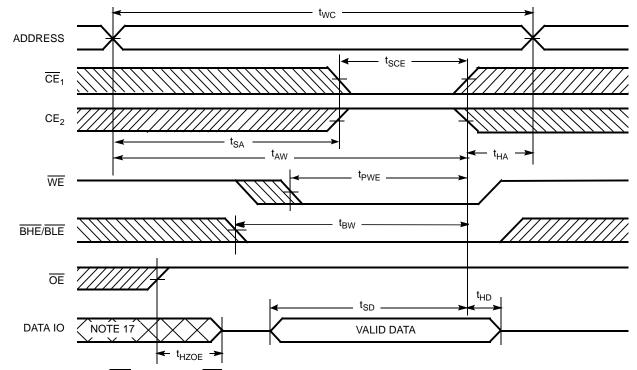
Notes

12. <u>Device</u> is continuously selected. \overline{OE} , \overline{CE} , \overline{BHE} or \overline{BHE} , or both = V_{IL} . $CE2 = V_{IH}$. 13. WE is HIGH for Read cycle. 14. Address valid prior to or coincident with \overline{CE}_1 transition LOW and CE_2 transition HIGH.

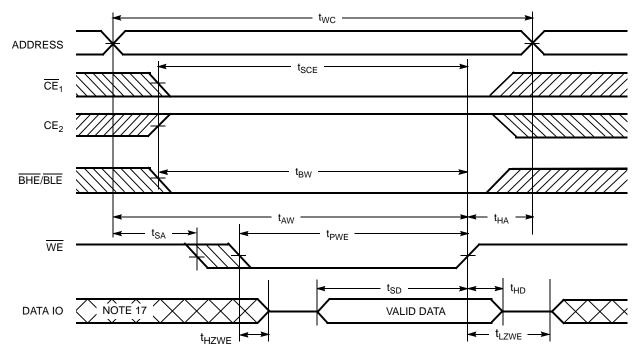


Switching Waveforms (continued)

Write Cycle No. 1 (\overline{CE}_1 or CE_2 Controlled) ^[15, 16]



Write Cycle No. 2 (WE Controlled, OE LOW) ^[15, 16]

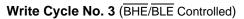


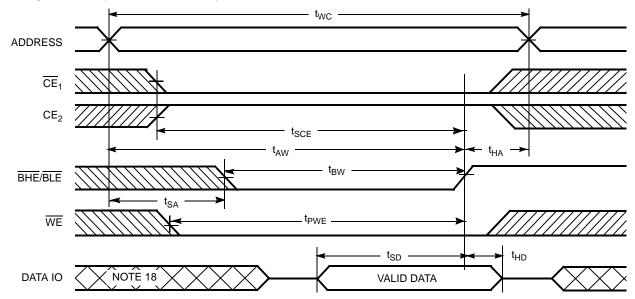
Notes

15. Data IO is high impedance if \overline{OE} , or \overline{BHE} or \overline{BLE} or both = V_{IH}. 16. If \overline{CE}_1 goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high impedance state. 17. During this period, the IOs are in output state and input signals should not be applied.



Switching Waveforms (continued)





Truth Table

| CE ₁ | CE ₂ | OE | WE | BLE | BHE | 1/0 ₀ -1/0 ₇ | I/O ₈ –I/O ₁₅ | Mode | Power |
|-----------------|-----------------|----|----|-----|-----|------------------------------------|-------------------------------------|----------------------------|----------------------------|
| Н | Х | Х | Х | Х | Х | High-Z | High-Z | Power Down | Standby (I _{SB}) |
| Х | L | Х | Х | Х | Х | High-Z | High-Z | Power Down | Standby (I _{SB}) |
| L | Н | L | Н | L | L | Data Out | Data Out | Read All Bits | Active (I _{CC}) |
| L | Н | L | Н | L | Н | Data Out | High-Z | Read Lower Bits Only | Active (I _{CC}) |
| L | Н | L | Н | Н | L | High-Z | Data Out | Read Upper Bits Only | Active (I _{CC}) |
| L | Н | Х | L | L | L | Data In | Data In | Write All Bits | Active (I _{CC}) |
| L | Н | Х | L | L | Н | Data In | High-Z | Write Lower Bits Only | Active (I _{CC}) |
| L | Н | Х | L | Н | L | High-Z | Data In | Write Upper Bits Only | Active (I _{CC}) |
| L | Н | Н | Н | Х | Х | High-Z | High-Z | Selected, Outputs Disabled | Active (I _{CC}) |

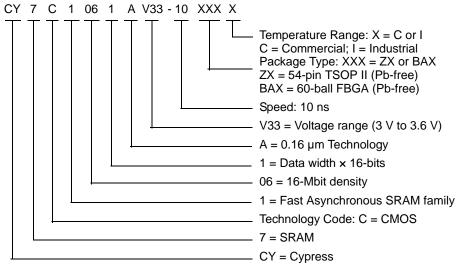


Ordering Information

The following table lists the CY7C1061AV33 key package features and ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products.

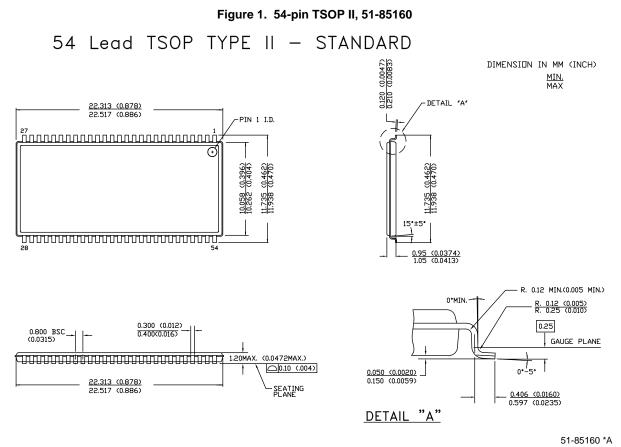
| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|------------|---------------------|--------------------|--------------------------|-----------------|
| 10 | CY7C1061AV33-10ZXC | 51-85160 | 54-pin TSOP II (Pb-free) | Commercial |
| | CY7C1061AV33-10ZXI | 51-85160 | 54-pin TSOP II (Pb-free) | Industrial |
| | CY7C1061AV33-10BAXI | 51-85162 | 60-ball FBGA (Pb-free) | |

Ordering Code Definitions





Package Diagrams





Package Diagrams (continued)

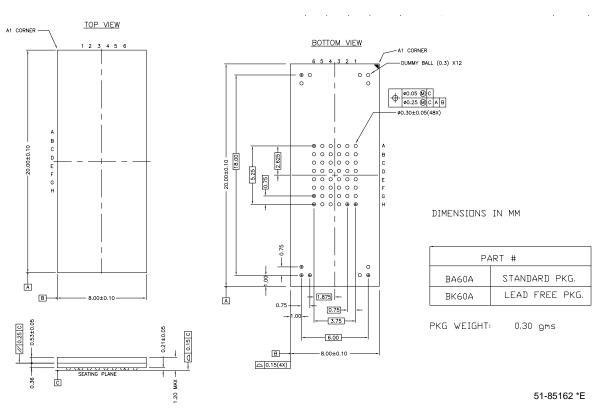


Figure 2. 60-ball FBGA (8 × 20 × 1.2 mm), 51-85162



Document History Page

| Revision | ECN | Submission Date | Orig. of Change | Description of Change |
|----------|---------|--------------------|--------------------|--|
| ** | 113725 | 03/28/02 | NSL | New Data Sheet |
| *A | 117058 | 07/31/02 | DFP | Removed 15-ns bin |
| *В | 117989 | 08/30/02 | DFP | Added 8-ns bin Changed Icc for 8, 10, 12 bins t_{power} changed from 1 µs to 1 ms. Load Cap Comment changed (for Tx line load) t_{SD} changed to 5.5 ns for the 10-ns bin Changed some 8-ns bin numbers (t_{HZ} , t_{DOE} , t_{DBE}) Removed hz <lz comments="" data="" from="" sheet<="" td=""></lz> |
| *C | 120383 | 11/06/02 | DFP | Final data sheet Added note 3 to "AC Test Loads and Waveforms" and note 7 to t_{pu} and t_{pd} Updated Input/Output Caps (for 48BGA only) to 8 pF/10 pF and for the 54-pin TSOP to 6/8 pF |
| *D | 124439 | 2/25/03 | MEG | Changed ISB1 from 100 mA to 70 mA Shaded fBGA production ordering information |
| *E | 492137 | See ECN | NXR | Corrected Block Diagram on page #1 Removed 8 ns speed bin Changed 48-Ball FBGA to 60-Ball FBGA in Pin Configuration Included Note #1 and 2 on page #2 Changed the description of I_{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Updated the Ordering Information Table |
| *F | 508117 | See ECN | NXR | Updated FBGA Pin Configuration Updated Ordering Information table |
| *G | 877322 | See ECN | VKN | Updated Ordering Information table |
| *H | 2897049 | 03/22/10 | KAO | Removed inactive parts from the ordering information table. Updated package diagrams, links in Sales, Solutions and Legal Information |
| * | 3109147 | 12/13/2010 | KAO | Added Ordering Code Definitions. |
| *J | 3160428 | 02/02/11 | PRAS | Ordering information updates. Template and style updates. |



Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

| Automotive | cypress.com/go/automotive |
|--------------------------|---------------------------|
| Clocks & Buffers | cypress.com/go/clocks |
| Interface | cypress.com/go/interface |
| Lighting & Power Control | cypress.com/go/powerpsoc |
| | cypress.com/go/plc |
| Memory | cypress.com/go/memory |
| Optical & Image Sensing | cypress.com/go/image |
| PSoC | cypress.com/go/psoc |
| Touch Sensing | cypress.com/go/touch |
| USB Controllers | cypress.com/go/USB |
| Wireless/RF | cypress.com/go/wireless |
| | |

PSoC Solutions

psoc.cypress.com/solutions PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2002-2011. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

Document #: 38-05256 Rev. *J

Revised February 2, 2011

Page 13 of 13

All products and company names mentioned in this document may be the trademarks of their respective holders.