DECT burst mode controller

PCD5040

The PCD5040 DECT Burst Mode Controller (BMC) is a custom IC that performs the DECT Physical Layer and Medium Access Control Layer (MAC) time critical functions for application in DECT handset and base station products which comply to the following standards (+ updates):

- DECT CI part 2: Physical layer (DE/RES 3001-2)
- DECT CI part 3: Medium Access Control layer (DE/RES 3001-3)
- DECT CI part 7: Security features for DECT (DE/RES 3001-7)
- DECT CI part 9: Public Access Profile (DE/RES 3001-9)

The BMC is designed to be connected to a ADPCM codec (PCD5032) and a 8051-type microcontroller without glue logic. Other codec's and microcontrollers (e.g. 68000-family) are also supported. Four versions of the BMC will become available. The PCD5040 will have a RAM memory containing the BMC firmware, while the PCD5041, 5042, 5043 have a ROM instead. All versions have the same pinning. ROM versions will also be available in SQFP-80.

Features

- An embedded RISC controller (PCC) with 4 kbyte (RAM / ROM) program memory for implementation of Traffic Bearer Control (TBC), MAC message handling, scanning, and the general control of the BMC hardware.
- PP & FP modes.
- TDMA frame (de)multiplexing.
- Encryption.
- Scrambling.
- CRC generation and checking.
- Beacon transmission control (P00 packets).
- Switches up to12 simultaneous active speech channels from speech interface to 1152 kb/s. radio interface, and vice versa.
- RSSI measurement with on-chip peak/hold detector and 6-bit A/D converter.
- Local call switching for up to 6 internal calls on RF side / local call switching on speech side.
- Quality control report.
- Digital Phase Locked Loop.
- Synchronisation (handset to active bearer, base station to cluster of RFP's).
- Seamless handover procedure.
- Fast (hardware) and slow (software) mute function.
- 1 kbyte extended RAM memory for the handset mode.
- On-chip crystal oscillator (13.824 MHz).
- Programmable microcontroller clock frequency.
- Programmable interrupts.
- Watchdog with two programmable timeouts
- Low power consumption in standby mode.
- Low supply voltage (2.7V-6V).
- SACMOS technology.

Interfaces to:

- Up to 2 ADPCM codec's in a simple base station (with up to 2 analogue lines) and in the handset mode.
- 2048 kb/s highway interface for systems requiring more than 2 connections to the network.
- A fully decoded radio interface including power down signals.
- 80C51-type microcontroller, or a 68000-type microcontroller.

1.0 BLOCK DIAGRAM

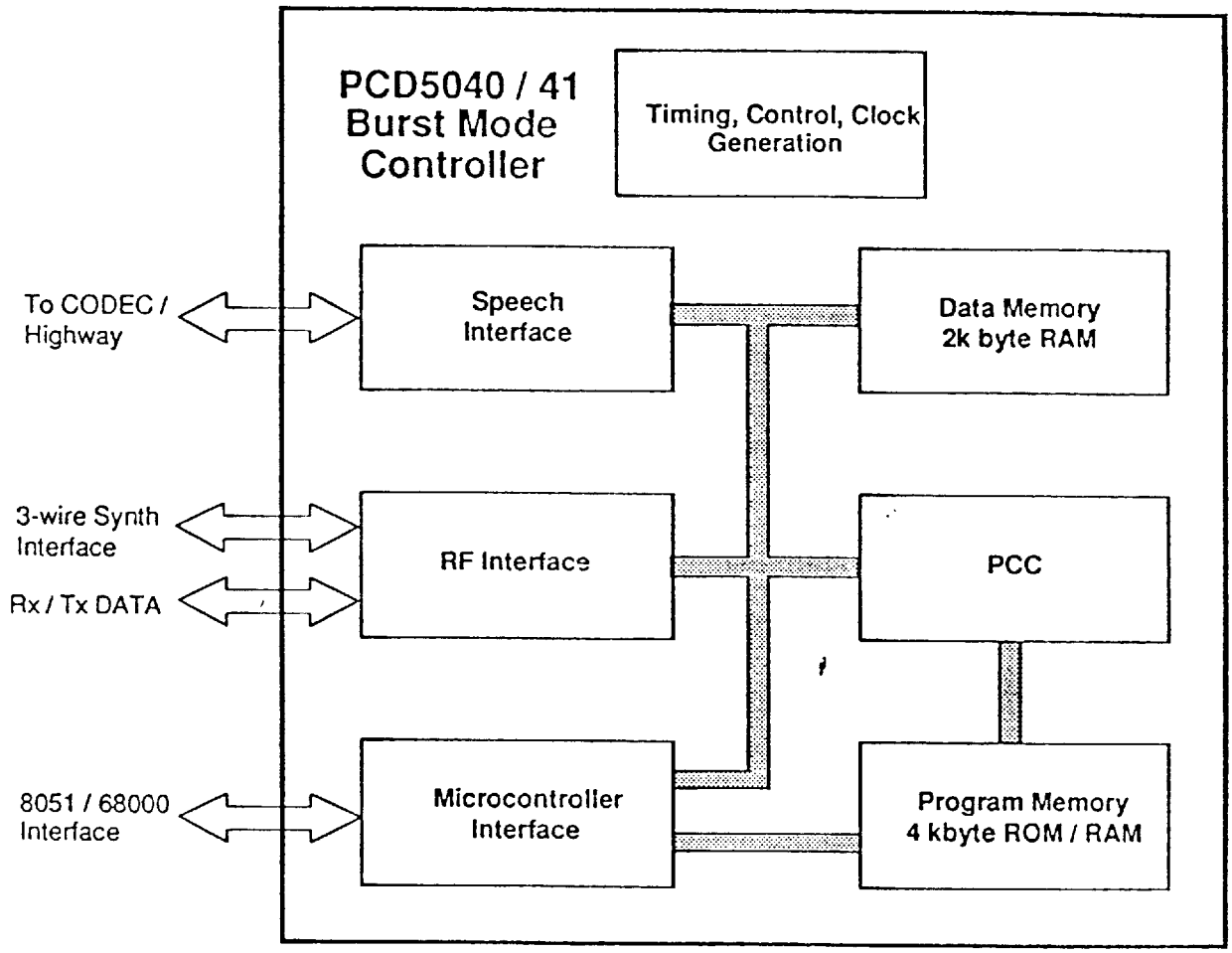

Fig. 1: Block diagram PCD5040 / 41 DECT Burst Mode Controller

DECT burst mode controller

PCD5040

2.0 PINNING

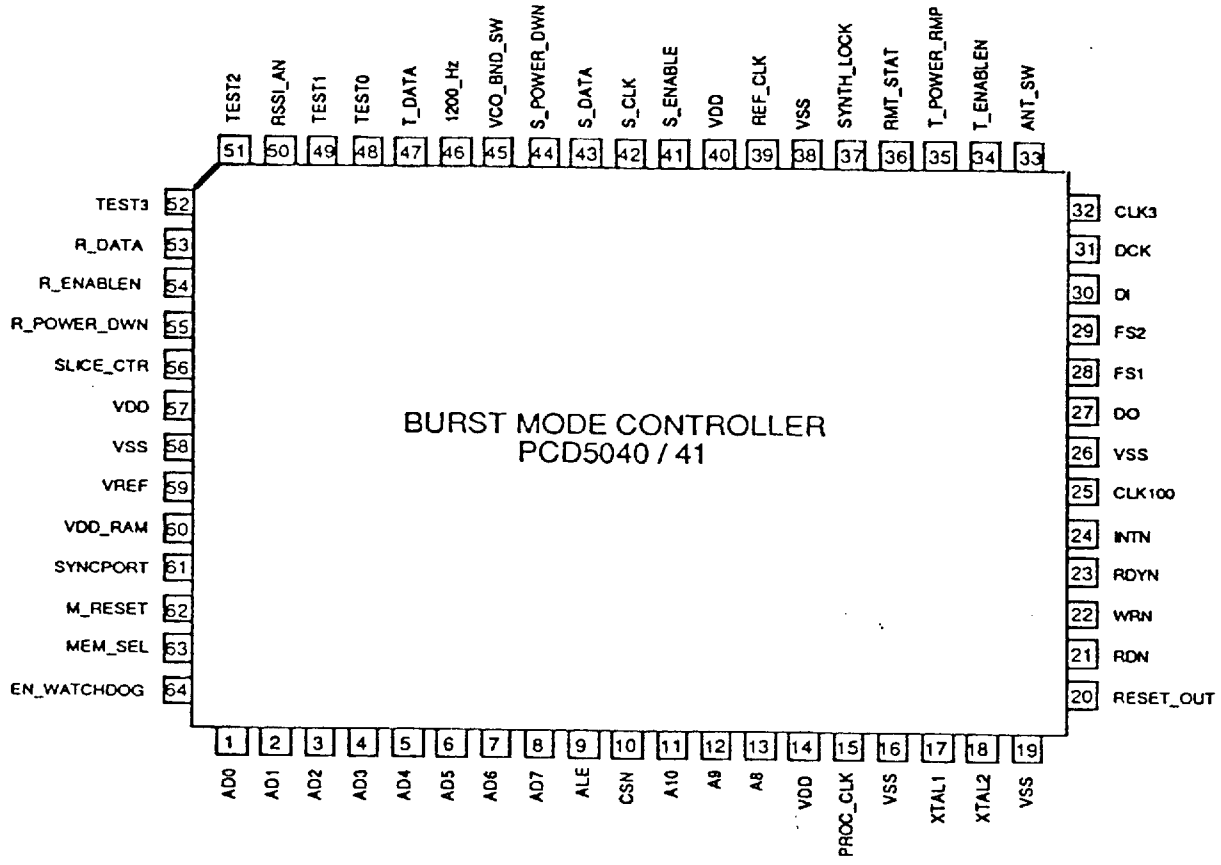

Fig 2: Pinning : QFP64REC (SOT319)

PIN	NAME	I/O	DESCRIPTION
14,40,57	V_{DD}	-	*
16,19,26,38,58	VSS	-	*
60	VDD_RAM	-	Power supply data RAM
48,49,51,52	TEST0..3	I	selects various test modes. Normal operation set to 0.
17	XTAL1	I	crystal oscillator input
18	XTAL2	O	crystal oscillator output
32	CLK3	O	3.456 MHz clock (nominal value, used to adjust system timing)
31	DCK	I/O	simple base + handset; 1152 kHz data clock (output), otherwise 2048 kHz data clock (input) signal
28	FS1	I/O	8 kHz framing signal to ADPCM codec 1 output, for simple base + handset, otherwise 8 kHz framing input.
29	FS2	O	8 kHz framing signal to ADPCM codec 2 in the base station mode.
27	DO	O	tri-state data output on the speech interface
30	DI	I	data input on the speech interface
15	PROC_CLK	O	microcontroller clock. Programmable from Fclk/64..Fclk, where Fclk is the crystal oscillator frequency.
63	MEM_SEL	I	Selects PCC program memory at microcontroller interface
9	ALE	I	address latch enable
21	RDN	I	read (active low)

PIN	NAME	I/O	DESCRIPTION
22	WRN	I	write (active low)
1..8	AD0..7	I/O	Address/Data bus
13..11	A8..10	I	Address bus
10	CSN	I	Chip Select (active low)
24	INTN	O	Interrupt (active low)
23	RDYN	O	Ready signal (active low), to initiate wait states in the microcontroller
54	R_ENABLEN	O	Receiver Enable (active low)
55	R_POWER_DWN	O	Receiver Power Down
56	SLICE_CTR	O	Slice Time Constant control
53	R_DATA	I	Receive Data
34	T_ENABLEN	O	Transmitter Enable (active low)
35	T_POWER_RMP	O	Transmitter Power Ramp control
47	T_DATA	O	Serial output data to transmitter
33	ANT_SW	O	Selects one of two antennas
44	S_POWER_DWN	O	Synthesizer Power Down control
46	1200_HZ	O	Control signal for dual synthesizer schemes
45	VCO_BND_SW	O	VCO bandswitch control signal
43	S_DATA	O	serial data to the synthesizer
42	S_CLK	O	clock signal, to be used with S_DATA.
41	S_ENABLE	O	Synthesizer enable
37	SYNTH_LOCK	I	Lock indication from synthesizer
39	REF_CLK	O	Reference Frequency for the synthesizer, ie. the crystal oscillator clock Fclk.
50	RSSI_IN	I	Analog signal (for basic DECT systems), peak signal strength measured after a low_pass filter.
36	RMT_STAT	I	Serial 8 bit data can be read in for each slot. REMote radio STATus
59	VREF	I	Reference input for the A/D converter
25	CLK100	O	100 Hz frame timer output
61	SYNCPORT	I/O	In the base station the signal is the SYNCPORT input/output. It is an output in a master base station, input in a slave base station, according to annex C, DECT CI specification part 2. The SYNCPORT signal is not active in the handset.
62	M_RESET	I	BMC master reset signal
64	EN_WATCHDOG	I	Enable watchdog input. When HI, the watchdog timer of the BMC is enabled
20	RESET_OUT	O	Watchdog timer output; intended to reset the external microcontroller when expired.

NOTE : ALL signals, which are input or I/O, and which can be floating, need to be pulled-up/down, in order to protect the BMC against cross-current. Exception are VREF and RSSI_AN, which do not have to be protected.

3.0 INTRODUCTION

The DECT Burst Mode Controller (BMC) is a custom IC, that performs the DECT Physical Layer and Medium Access Control Layer (MAC) time critical functions, for application in DECT handset and base station products, that comply to the following standards (+ updates):

- DECT CI part 2: Physical layer (DE/RES 3001-2)
- DECT CI part 3: Medium Access Control layer (DE/RES 3001-3)
- DECT CI part 7: Security features for DECT (DE/RES 3001-7)
- DECT CI part 9: Public Access Profile (DE/RES 3001-9)

The BMC is designed to be connected to the ADPCM codec (PCD5032) and a 8051-type microcontroller without glue logic. Also other codec's and microcontrollers (e.g. 68000-family) are supported.

Two versions of the BMC will become available. The PCD5040 will have a RAM memory, containing the BMC firmware, while the PCD504x have a ROM instead. All versions will have the same pinning. The firmware is used by the internal RISC processor, and is a part of the product. The product is described in two parts:

Part1: DECT Burst Mode Controller hardware (this document)
Part2: DECT Burst Mode Controller firmware

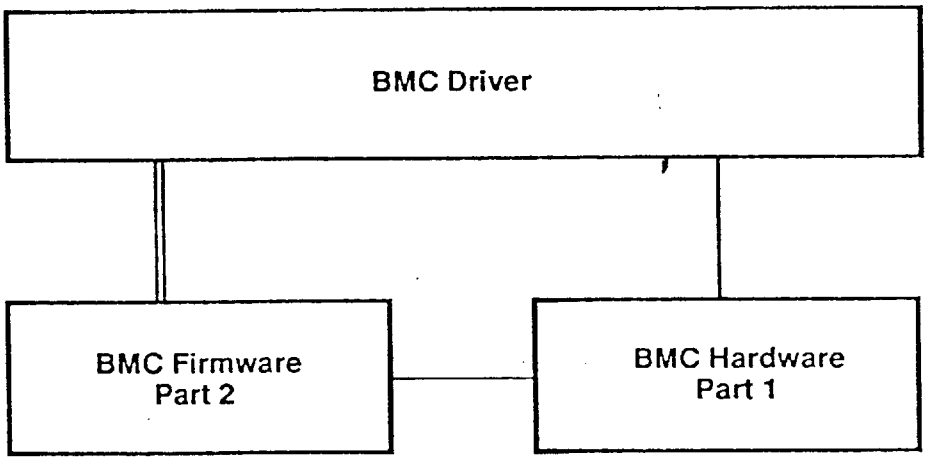

Figure 3: BMC document description

NOTE: This specification contains advance information and is subject to change without notice. Furthermore, this specification is valid for BMC versions from PCD5040-2 on.

4.0 FUNCTIONAL DESCRIPTION

The basic philosophy around the BMC implementation is to have a few dedicated hardware blocks containing logic for time critical functions (with bit/byte time accuracy); all other functions (with slot time accuracy) are contained in a small programmable core, the Programmable Communication Controller (PCC). This approach offers maximums flexibility during prototyping.

The block diagram of the BMC is shown below. In the following sections, the functional blocks and the internal bus are described.

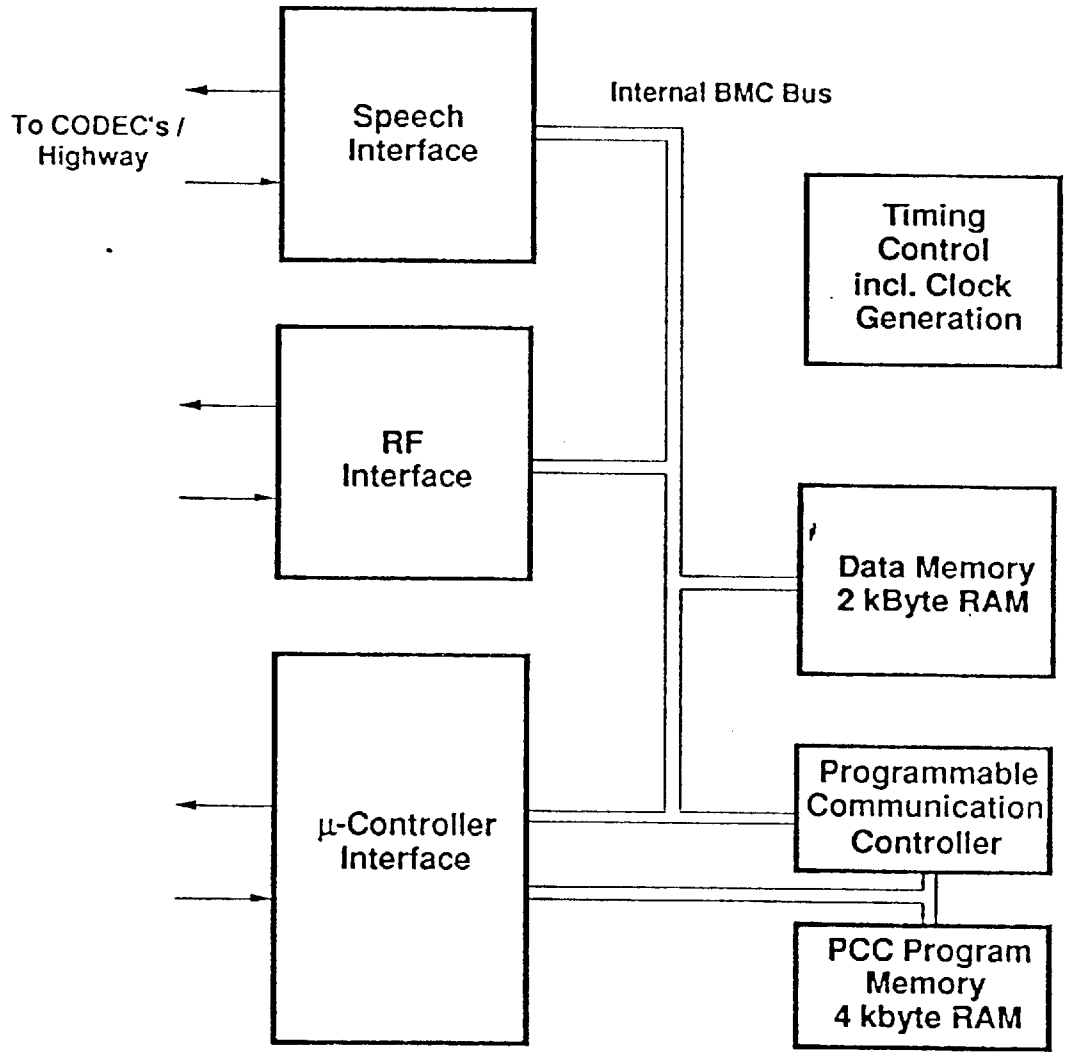

Figure 4.1: Internal Bus with main Functional Blocks

4.1.Internal Bus

4.1.1. Function of the Internal Bus

The function of the Internal Bus is:

- to provide access for all functional blocks to the common Data Memory,
- to provide access for the µC-Interface block and the Communication Controller (PCC) to all other functional blocks.

All functional blocks (speech, RF, cipher, µ-Controller, PCC) can autonomously use the internal bus to communicate with the common data memory.

A bus controller is used to handle the bus priority mechanism. When several blocks request access simultaneously, the request with the highest priority is handled first.

4.1.2. Data Memory

A large part of the data memory is used for the bit rate adaptation between the DECT radio interface and the speech interface.

In a handset, the BMC uses only 1 kbyte of the common data memory. The remainder (1 kbyte) can be used by the µ-controller as an extended data memory for the higher layer software. The µ-controller is not aware of the fact, that it is sharing the memory with the BMC; the µ-controller interface plus the common data memory behave as a standard RAM device, from the µ-controller point of view. In the base station, the BMC will use the full common data memory.

The data memory is also acting as the main communication interface between external micro-processor and PCC. The format of data structure is described in part 2 : 'DECT Burst Mode Controller Firmware'.

4.2. Clock Generation and Correction

The BMC has an on-chip 13.824 MHz crystal oscillator. From this source, a few frequencies are derived for internal and external use. Frequencies generated for external use are:

- 13.824 MHz — for the synthesizer reference (pin REF_CLK), which is only running if the synthesizer is not in power down mode (pin S_POWER_DWN).
- 0.144-13.824 MHz — for the µ-controller clock (pin PROC_CLK).
- 3.456 MHz — for the ADPCM codec (pin CLK3)
- 1200 Hz — for dual synthesizer switching
- 100 Hz — indicates start of frame

Nominally, the frequency on pin CLK3 is 3.456 Mhz. This frequency is divided from the crystal (divide-by-4). But sometimes, it will be divided by 3 or by 5, to synchronise the combination of the ADPCM codec and the BMC to an external source. Applications in which the BMC can be synchronised are:

- handset : the incoming radio channel, using the 'slot synchronisation' event of one active channel, so the handset is locked to one base station.

- master base station : The master base station is providing a 100 Hz signal to slave base stations on pin SYNCPORT. If the BMC is connected to a digital interface (32-slot mode speech interface), the external synchronisation will be done on the incoming 8 kHz signal. If it is connected to an analog line (12-slot mode speech interface), it will use its own crystal oscillator as reference.

- slave base station : The slave base station will use the incoming SYNCPORT signal as synchronisation reference.

Each of these three application area's define their own 'sync' event for adjusting the internal timing of the BMC (see section 5.5)

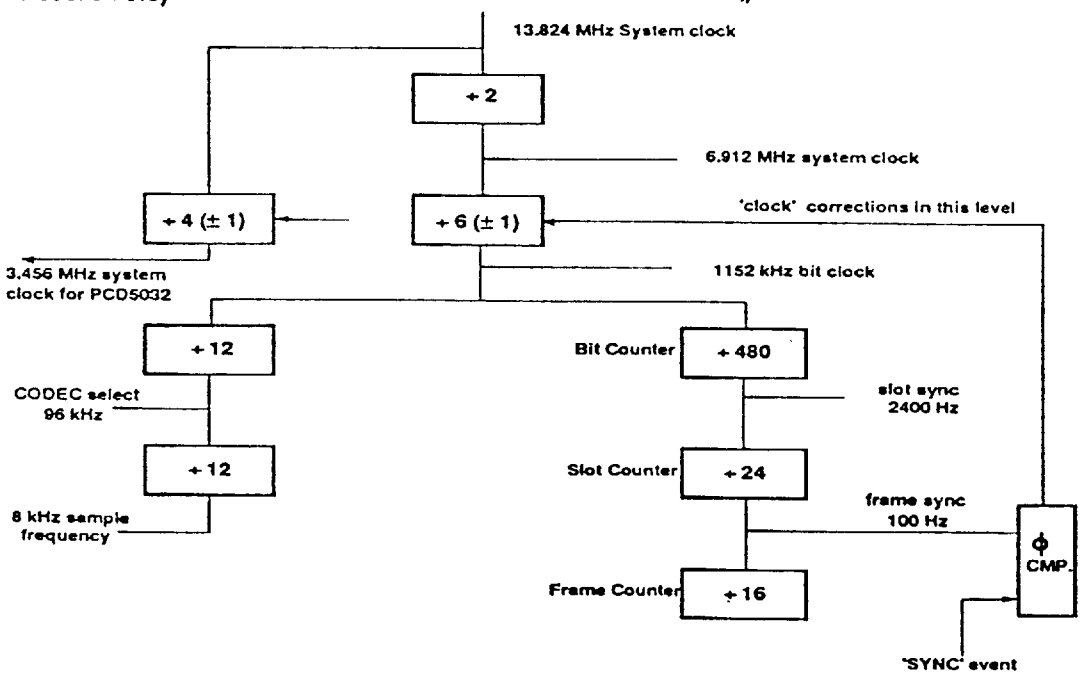

Figure 4.2: internal clocking scheme of the BMC

4.3. Programmable Communication Controller + Program Memory

4.3.1.PCC

The PCC is a RISC type controller and is used to control BMC functions, which are slot time accurate. It is well suited for bit manipulation, and runs at a clock frequency of 6.912 MHz (3.4 Mips). After having finished execution of a task, it switches to a power saving state, from which it returns after a pre-programmed time.

4.3.2.Program memory (PCD5040 only)

The PCC will fetch its program from a RAM memory, which is downloaded by the microcontroller during initialisation of the BMC, to allow maximum flexibility, with respect to:
- application area of DECT,
- parts of the MAC specification which are still to be evaluated,
- future radio architectures (zero-IF),
- flexibility to control different synthesizers,

To start the download procedure, the µ-Controller selects one of the two PCC program banks by writing the µC Interface Mode register. When MEM_SEL (pin 63) is made high, a memory bank is connected to the external address bus. The microcontroller will use the 2 kbyte BMC addressing range, to fill a Program Memory bank. Hereafter, MEM_SEL is made low, so the microcontroller can have normal access to the internal bus again. The same procedure is repeated for the second bank. The MEM_SEL pin must be kept HI during an internal bus transfer, because it is not latched internally.

Memory organisation

PCC program memory is 4 kbytes, organised as 2 blocks of each 2kbyte. The PCC can read them in parallel; in this way it reads one word at a time with the LO byte coming from Bank 0 and the HI byte coming from Bank 1. The µC-interface can read and write only in bytes. If Bank 0 is selected, the least significant bytes are addressed. If Bank 1 is selected, the most significant bytes are selected. See figure 4.3.

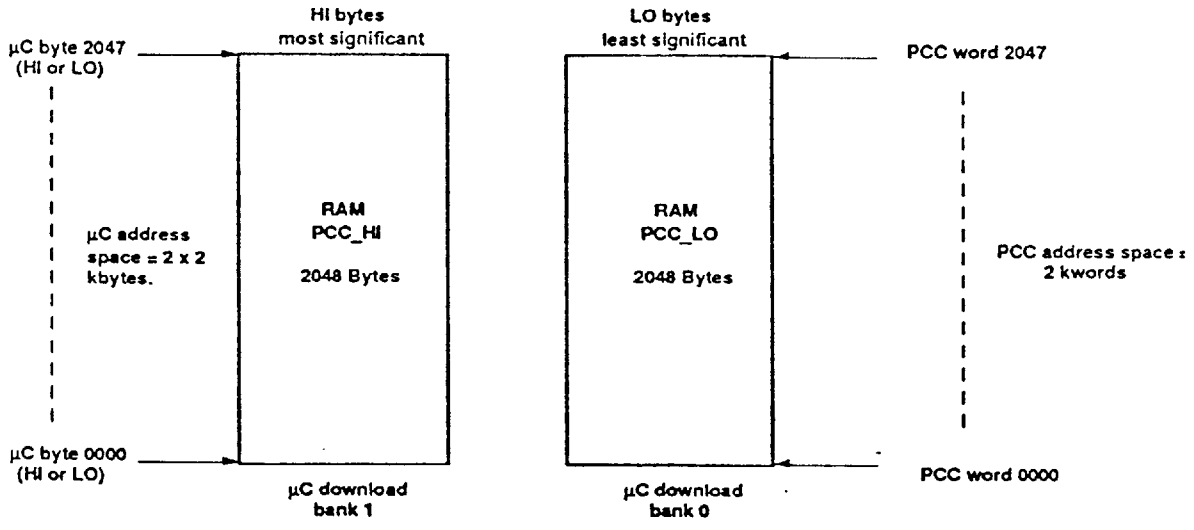

Figure 4.3: organisation of the PCC memory

4.3.3.PCC functions

Most important functions of the PCC are to:

- perform the appropriate actions on received messages, such as: identity checks, N_T-check procedure, TBC-handling, and thus also to;
- prepare A-field messages for transmission,
- prepare the RF-interface for the coming slot,
- perform the procedures for RSSI and set-up scan, maintaining scan counters and timers, assembling the RSSI field in the common data memory.
- filter events, and indicate them to the microcontroller (interrupt).

A complete description of the functional behaviour of the PCC program can be found in part 2 : DECT Burst Mode Controller Firmware.

4.4. Speech Interface

4.4.1. 12-Slot Mode

The 12-slot mode is selected, if 1 or 2 ADPCM codec(s) are connected to the BMC, where the BMC is the master of these codec's. In the handset, this is always the case. Also in simple base stations, which are connected with 1 or 2 analogue lines to the public network. Each codec is connected with a separate framing reference signal (FS1,FS2) to the BMC. Only two framing signals of the 12 are decoded externally. No interface logic is needed when using the PCD5032 ADPCM codec.

An indirection table is used, to determine (for reception and transmission) where to store/fetch speech data. The hardware speech-interface is capable to address the right speech buffer for the relevant speech slot, and will maintain a counter, carrying the offset to the fetched address.

4.4.2. 32-Slot Mode

The 32-slot mode is used to connect the BMC to a digital interface, with a 2Mb/sec interface. Up to 12 of the possible 32 slots on this interface can be used. The same indirection table, which is used in the 12-slot mode, is used for the 32-slot mode.

4.4.3. Muting

Due to various reasons the quality of the incoming speech data may be degraded significantly. By muting the speech data, these disturbances are not (or less) audible to the user. Two types of muting are distinguished by the BMC:

- fast muting
- slow muting

Fast muting, which is performed by the BMC automatically, is nothing more than a repetition of the previously received frame (80 speech samples) to the ADPCM codec. It is issued if no Sync word was detected.

Slow muting is issued by the µ-controller, after having detected a degradation of quality. A slow mute is implemented as a continuous '0000' nibble transmission to the ADPCM codec, until slow mute is released.

4.4.4. local call

A local call option is implemented, in order to loopback data from one codec to another codec, and vice versa, as illustrated below.

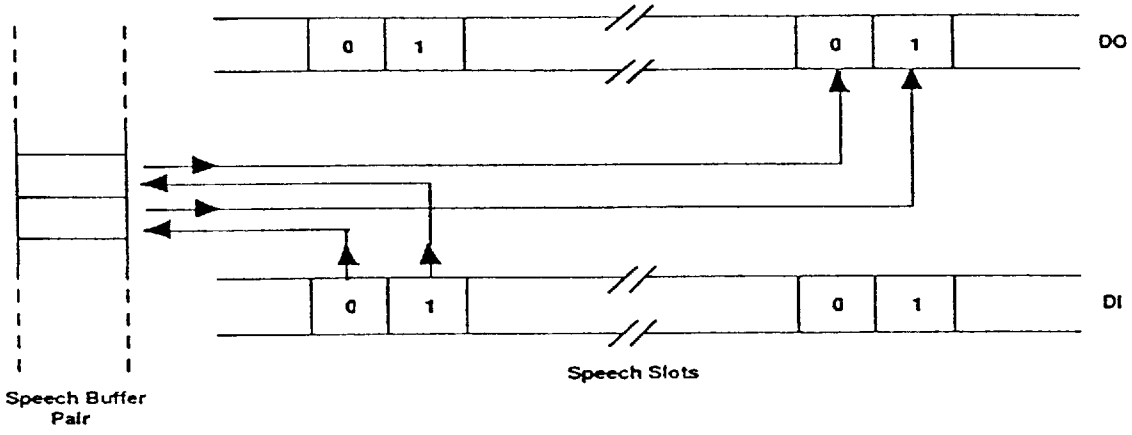

Figure 4.4 Local call switching on the speech-interface

4.5. RF Interface

Most of the functions, performed by the RF interface, are under control of the PCC. Especially the processing of non-speech data, programming of functions and registers, is done via the PCC.

4.5.1. Serial Receiver

The serial receiver processes the data, which comes from the radio head, and which is already filtered by the synchronisation part. The data is latched, using the recovered data clock.

The serial receiver will collect the complete A-field and B-field, and store it in the common data memory. Before the A-field is received, the A-field start address is programmed by the PCC. Upon reception of A-field nibbles, the address is updated by the serial receiver. Meanwhile, the PCC will program the B-field start address.

In figure 4.5 the data flow in the serial receiver is shown. The state machine, controlling the events and the data flow is not shown. Note that almost no decoding of messages is required. Only the header of the A-field needs to be decoded to check if a Cs message is received or transmitted, which requires the ciphering to be switched on also in the A-field

4.5.2. Serial Transmitter

The serial transmitter structure performs the reverse functions, compared to the receiver. Several blocks, used in the receiver, are also used in the transmitter. Amongst these are the CRC-generators, the scrambler, and the address registers. Figure 4.6 shows the serial transmitter structure

By transmitting the X-CRC twice, the Z-field is transmitted. The handling of the address registers is the same for the transmitter. Transmission of the synchronisation sequence (S-field) is done using the same method as the A-field and B-field. The S-field is stored in the common data memory, and will be fetched by the transmitter, just before transmission.

Not shown in the diagram, is that in the handset the data in the serial transmitter may be advanced by a programmable number of bit periods. This is done to compensate for the delay in the radio head.

Furthermore, the transmitted data can be inverted (using a switch in the BMC mode register), in order to connect the BMC to VCO's requiring a negative modulation.

4.5.3. Seamless Handover

Seamless handover guarantees that when the transfer of the speech information changes from one slot to an other, no speech samples are lost, added or displaced. Seamless handover is guaranteed by the following measures in the design of the Rx and Tx blocks in the RF interface:

- By using a lookup table, containing the correct start addresses of the B-fields in the data memory.
- The RF receive and transmit blocks will move and fetch data to/from the data memory block in 4-bit nibbles.

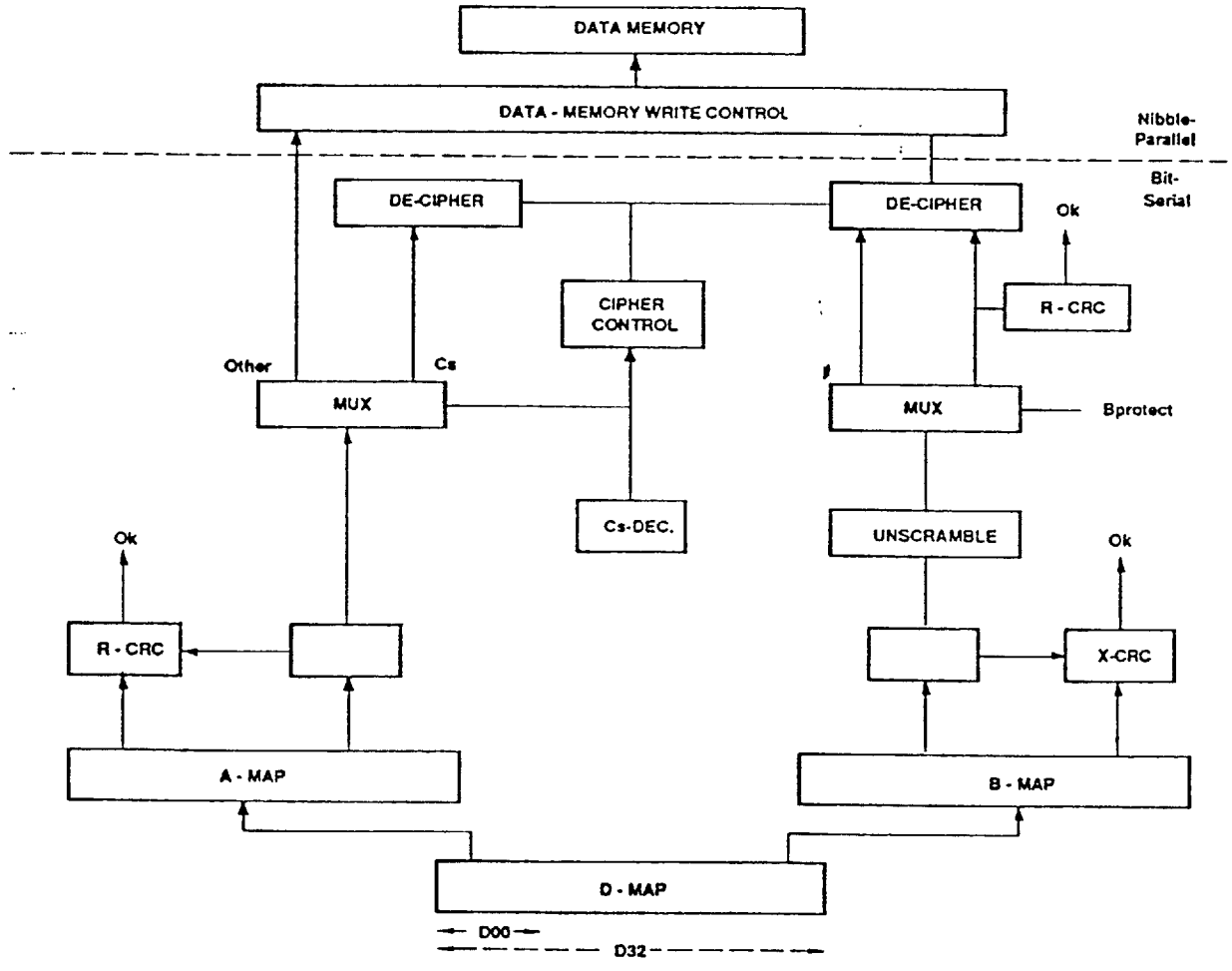

Figure 4.5 serial receiver structure

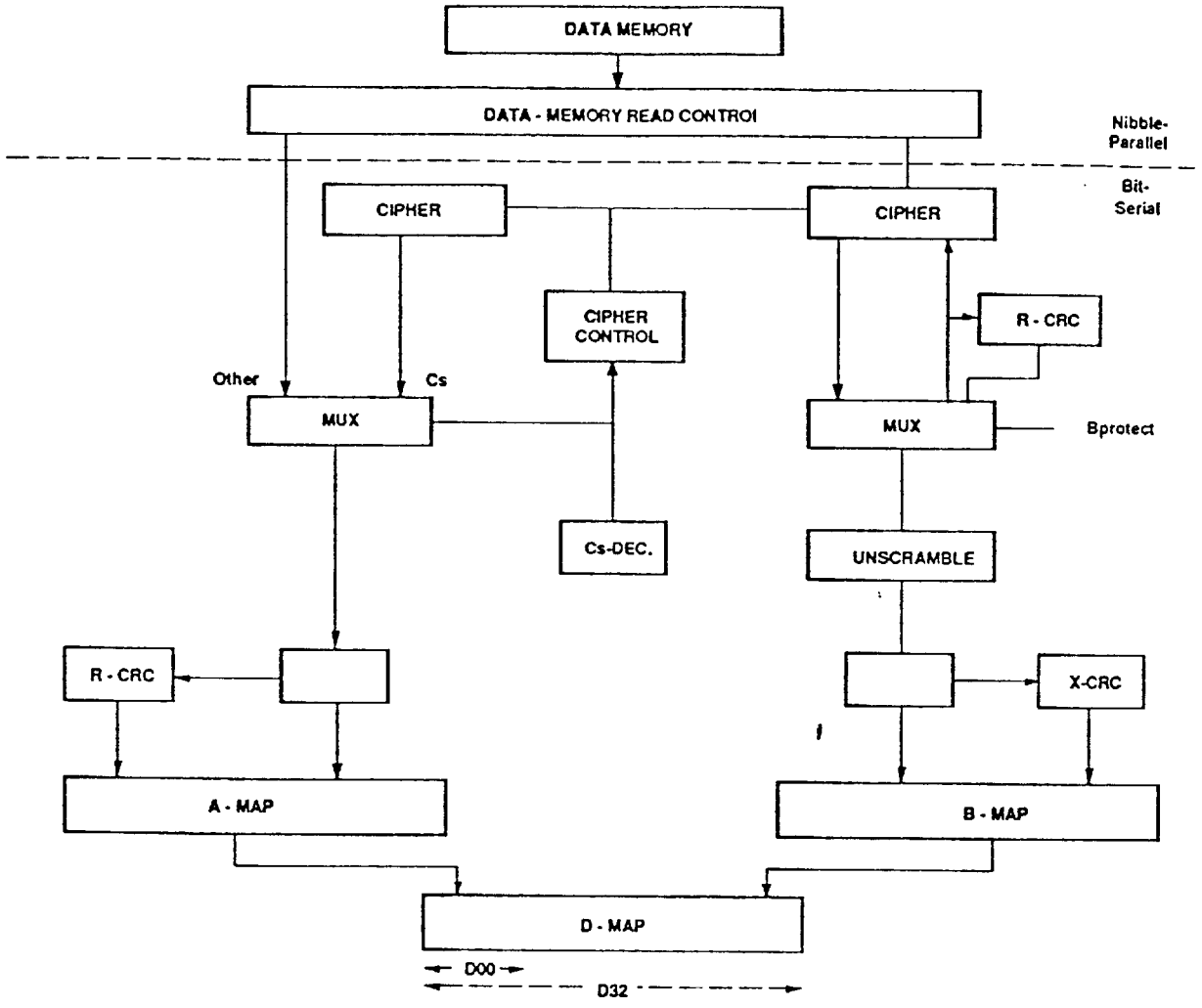

Figure 4.6 serial transmitter structure

4.5.4. RF Control Signals

The timing of the control signals to the radio head is fixed, but such that an RF delay between 1.5 and 7 µs can be tolerated (see section 5.3.2 for details). Only the transmitter ramp signal and the synthesizer enable are programmable within certain limits.

4.5.5. Synthesizer Programming

To program a synthesizer, a 3-wire serial interface is used. The signals on this interface are:

- S_ENABLE (enable)
- S_CLK (clock)
- S_DATA (data)

To program various types of synthesizers, a 3-byte shift register is present. Three data formats are supported: 8,16 or 24 bit words can be selected. The transfer of data from a frequency table in the common data memory to the shift register is under control of the PCC.

4.5.6. RSSI Measurement

The RSSI measurement in the BMC RF-interface block is done in 3 parts: a peak/hold detector, a 6-bit A/D converter, and an RSSI control block, which controls the peak/hold detector and the A/D converter. Once per slot time, a sample is fetched by the PCC, and saved in the appropriate area of the common data memory.

If the radio receiver is active in a particular time slot, the RSSI value will automatically be measured in that slot. Adjustment to the RSSI_AN input level can be made with VREF.

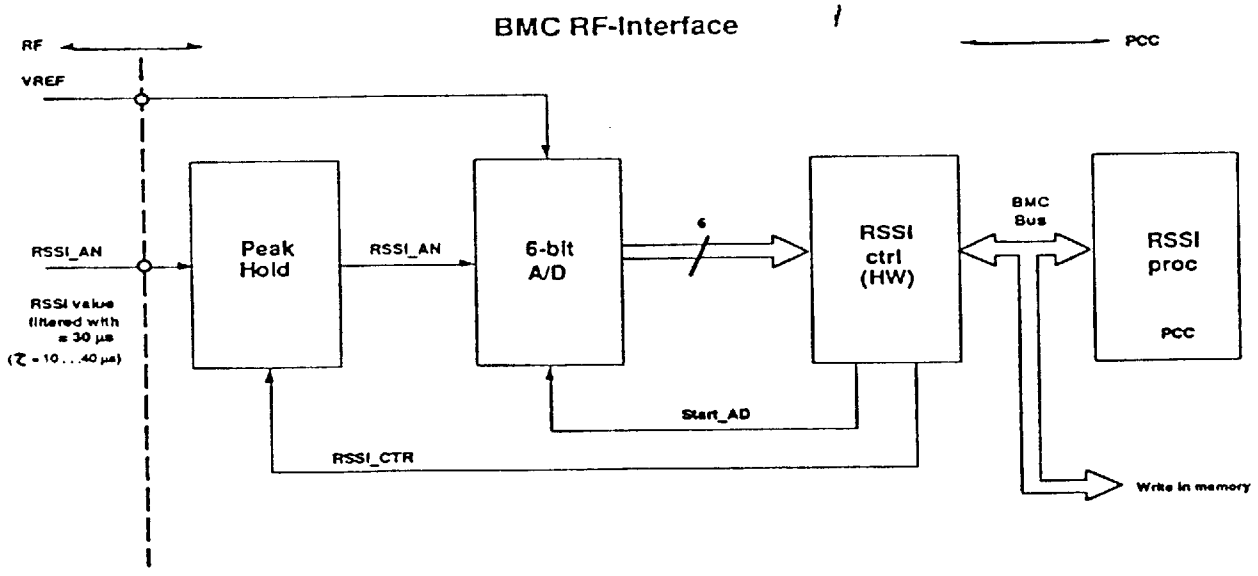

Figure 4.7 RSSI measurement path

4.5.7. Local call switching

The BMC provides a local call switching function in the base station. It will store incoming speech nibbles in the common data memory, in the area reserved for that particular receive slot. Then, during the transmit phase, it will pass to the transmit block, the start pointer of the same data memory area. Thus, the speech data is echoed to the other user (see illustration below). To handle quality degradation during local calls, a mute can be performed at the RF side of the speech buffer.

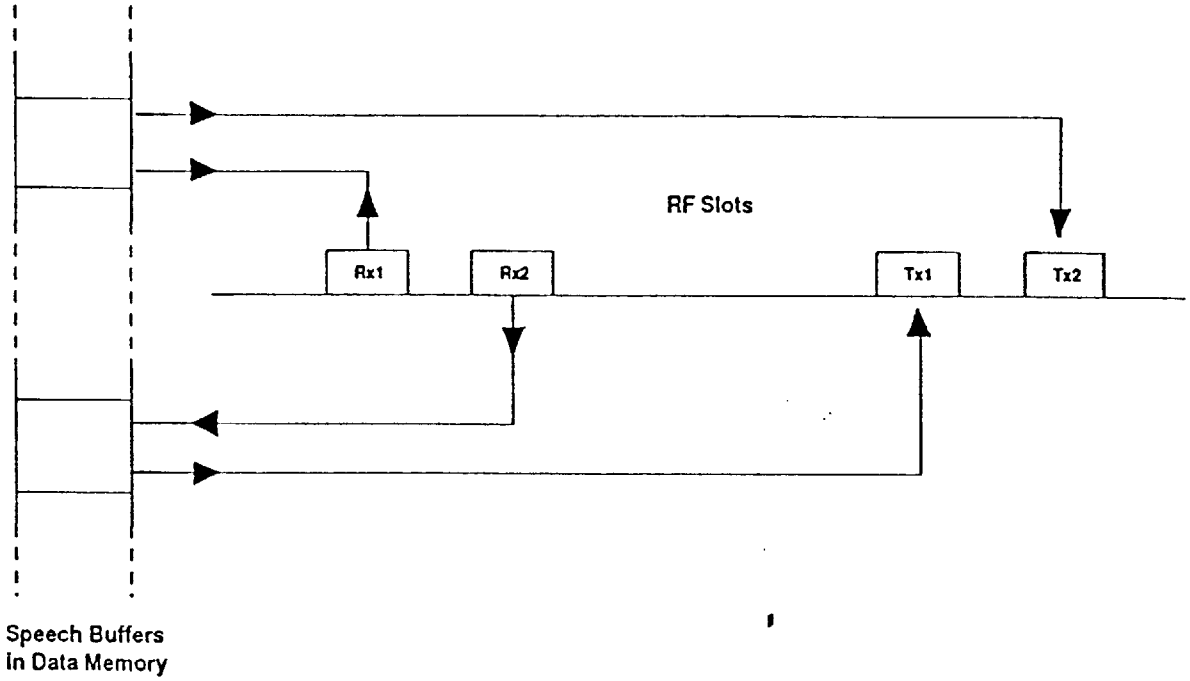

Figure 4.8: Local call switching on the RF-side

4.5.8. Data synchronisation

The data synchronisation is done in 2 phases:
- bit synchronisation
- sync word detection

Bit synchronisation is done using a Digital PLL (DPLL), with an oversampling factor of 12, i.e. the DPLL is running on a frequency, which is 12 times the data rate.

Sync word detection is achieved by checking the incoming data pattern with the expected synchronisation field pattern, using a correlator. The correlator has a programmable threshold, so it can accept bit errors in the sync field pattern up to the threshold level. Furthermore, the correlator window is programmable. This means, that only during a certain period (the time window), a 'SlotSync' can be detected, indicating the slot synchronisation event.

The flow of the signals in the synchronisation part is shown in figure 4.9. Note, that in the base station the inverted data bits are shifted into the register. This is done, because the synchronisation field pattern is inverted for the base station, compared to the handset.

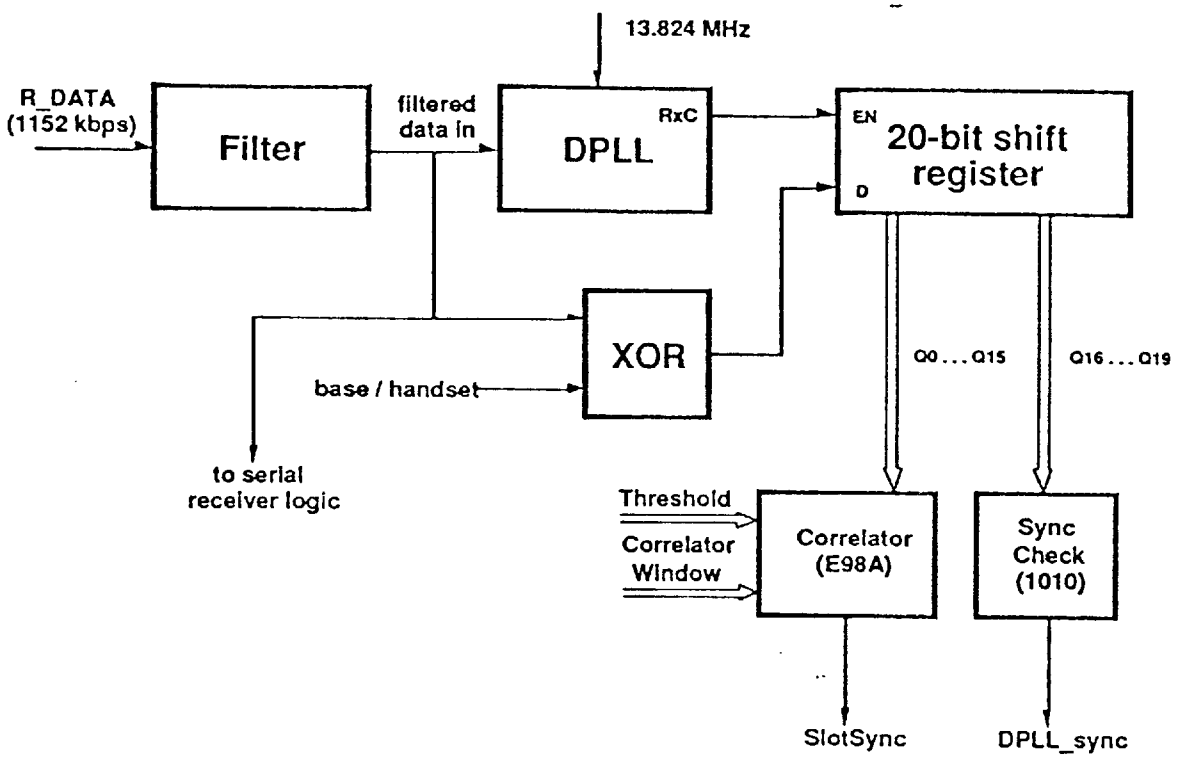

Figure 4.9: schematic of the receiver synchronisation part

The 'DPLL_sync' indication should only be used, when `SlotSync' is active. It indicates that the last 4 bits of the preamble field (the training sequence) are received correctly, and thus indicates that the DPLL was in lock (synchronised) in time. If the `SlotSync' is active, and the 'DPLL_sync' is not, then a sliding interferer might have been detected.

If `SlotSync' is not detected, effectively no data is received in that slot. This implies a "fast mute" because speech data received in the previous frame is not destroyed.

4.5.9. Ciphering Machine

The description of the cipher machine is subject to confidentiality. The specification of its algorithms are delivered by ETSI after a Non Disclosure Agreement.

The cipher machine is under control of the TBC, which is implemented in the PCC. The cipher machine generates 2 fields of ciphering bits:
- A_cipher (40 bits) for A-field messages (Cs tail ONLY !!)
- B_cipher (320 bits) for speech in B-field

The transmitted ciphered bits are then:
- A_ciphered := A XOR A_cipher
- B_ciphered := B XOR B_cipher

On reception by the peered endpoint, deciphering consists of the same operation thanks to the synchronous generation of A_cipher and B_cipher.

The cipher machine is time-multiplexed on a slot basis. Initially, the Initialisation Vector (IV) and the key must be loaded into the cipher machine. Transfer of the IV and key from the common data area to the cipher machine is done automatically by the cipher machine. The contents of the memory space where IV and key are found, are the responsibility of the PCC, and the external µC.

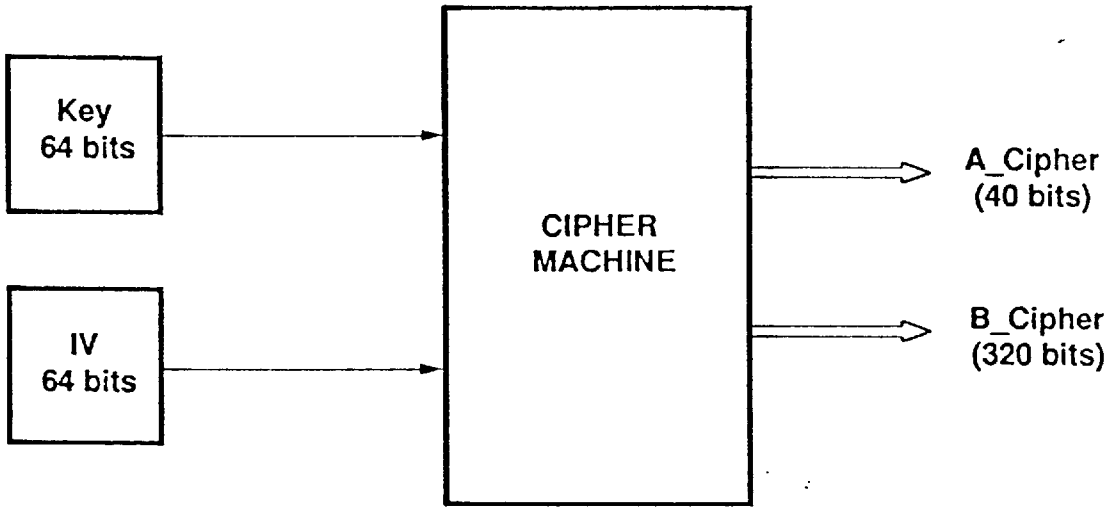

Figure 4.10: Cipher machine plus its sources

4.6. Microcontroller Interface

4.6.1. Function of the Microcontroller Interface.

The microcontroller Interface will provide the following services.

- Direct interface to processors which have an INTEL-8051 compatible interface.
- General interface to processors that can handle 'wait states' e.g. 68000-family. In this case glue logic is required.
- Processor clock signal of which the frequency is programmable in order to adjust instantaneously processor performance to processor work load.
- A programmable interrupt register
- A watchdog timer with timeout periods of 1.25 or 82 seconds, depending on the programming.

The µC can address the BMC as any other RAM memory connected to the µC bus. By writing the 'Interface-Mode Register', the µC can select the interface mode and it's own clock frequency.

4.6.2. Microcontroller Interrupts.

The function of µC Interrupts is to make optimal use of the µ-controllers processing power, and to achieve optimal cooperation between time-critical tasks and less time-critical tasks both executed in software. Three registers are available to handle interrupts. These are:

- Interrupt Event Register
- Interrupt Enable Register
- Interrupt Reset Register

These registers are to be regarded together. Corresponding bits in these registers relate to one and the same event. Bits in the Interrupt Event Register are set by the PCC and are to be reset by the external processor by writing '1's in the correponding bits in the Interrupt Reset Register. The mask in the Interrupt Enable Register enables the interrupt if corresponding events do occur.

4.6.3. Watchdog

The BMC is equipped with a watchdog timer, which generates a reset towards an external device (e.g. a µC) after timeout. Two (fixed) timeout periods can be programmed; 1.25 sec and 82 sec. The watchdog function can be disabled by using the EN_WATCHDOG input pin.

4.7. Power Down

The PCC may switch off the 6.912 MHz internal clock, to enter a power saving mode. All blocks, running on this clock are then switched off (i.e. RF-interface, cipher block, speech interface, PCC). This is called the power down state, and is only used in the handset mode.

The 13.824 MHz clock is never switched off. The Timing Control, µC interface, and Bus Controller keep running, in order to remain synchronous with a base station, and to keep the wake-up circuitry active. During power down the external µC has still access to the common data area.