# ANALOGUE ON CELLMOS

MEDL

PROVISIONAL INFORMATION

In order to have the extra facility of analogue functions on MEDL's ISO-CELLMOS, MEDL have designed and characterised a range of standard analogue cells. These cells are designed to fit the standard ISO-CELLMOS 12 micron grid, making the mixing of analogue and digital functions possible.

These analogue cells cannot be placed or routed by the current layout software so must be placed and routed manually.

Many other cells have been designed for specific applications and special analogue cells can be designed for your applications.

MEDL

# INDEX

# RESISTORS AND CAPACITORS FOR ISO-CMOS

**PROVISIONAL**

Resistors can be produced with the following characteristics:

| | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|
| Resistance Range | 2K | — | 350K | OHMS |
| Matching (for similar values) | | | ± 0.5 | % |
| Absolute Value Tolerance | | | ± 30 | % |
| Voltage Coefficient<br>(For 10 μm wide 10 μm clearance each side) | | | 0.5(1) | %/V |
| Resistivity | | 300 | | $\mu m^2/\Omega$ |

Note 1 Smaller voltage coefficients available when larger areas are used for resistors.

Capacitors can be produced having the following characteristics:

Size of Capacitors is 55 x 55 μm for 1 pF, i.e. a 10 pF capacitor is the same size as a reset D type F/F.

MEDL

# ISO-CMOS VOLTAGE REFERENCE

# AVABS

**PROVISIONAL INFORMATION**

This cell when connected to an appropriate amplifier (such as AOP1) will supply a voltage of −1.14V relative to an externally supplied ground reference which would normally be mid-way between the positive and negative supplies.

The temperature coefficient is expected to be below 500 ppm/°C.

The output current capability will depend on the amplifier used.

Cell size 240 µm × 252 µm

Current consumption typically 100 µA

# SIMPLE BIAS GENERATOR FOR ISO-CMOS ANALOGUE CIRCUITS

AVRNP3

MEDL

**PROVISIONAL INFORMATION**

This cell generates two voltages which may be used to bias other cells such as op-amps and comparators.

The current generated by a transistor biased by one of these voltages is compensated for changes in transistor parameters and supply voltage.

| CHARACTERISTIC | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Supply Voltage $V_{DD} - V_{SS}$ | | 4.5 | | 11 | Volts |
| Supply Current $I_{DD}$ | $V_{DD} - V_{SS} = 10V$ | | 20 | | µA |
| Current generated in W/L to N channel transistor by VRN | | | $\frac{3W}{L}$ | | µA |
| Current generated in W/LP channel transistor by VRP | | | $\frac{1.3W}{L}$ | | µA |

Cell Size 156 x 192 µm

Note 1 Neither VRN nor VRP outputs require a minimum capacitive load.

Note 2 This circuit is not intended for supplying resistive loads.

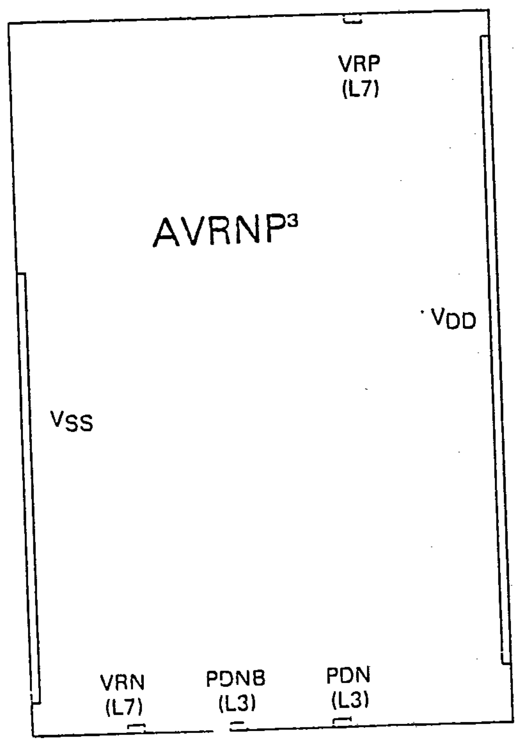
Note 3 Only one bias circuit is required for all analogue cells used on each die.

Note 4 Bias enable inputs must be driven with true and complement signals, to generate the power down signal and must not be driven from separate sources.
When disabled (PDN high) the supply current drawn by the bias circuit or any circuit attached, will be virtually zero, thus providing a standby condition.

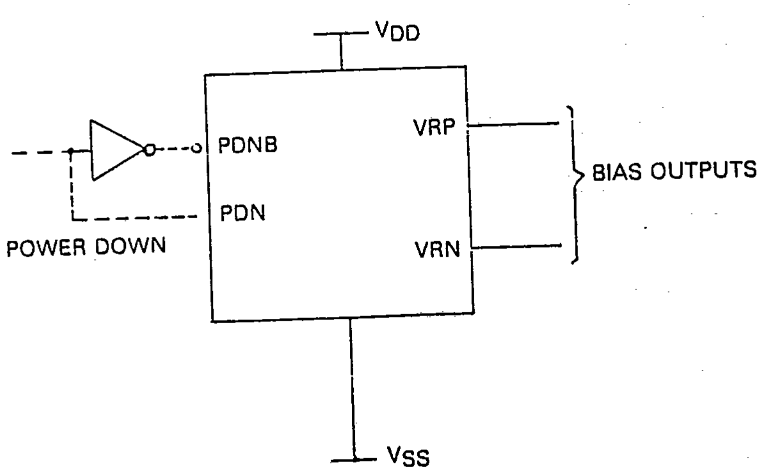
MEDL

# SIMPLE BIAS GENERATOR FOR ISO-CMOS ANALOGUE CIRCUITS AVRNP3

PROVISIONAL INFORMATION




**PLOT SYMBOL AVRNP3**




**CIRCUIT SYMBOL AVRNP3**

# GENERAL PURPOSE OPERATIONAL AMPLIFIER

# AOP1

MEDL

PROVISIONAL INFORMATION

Unless otherwise stated these figures assume:
$V_{DD}$ = −5V, $V_{SS}$ = −5V and temperature of 25°C

| CHARACTERISTIC | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Supply Voltage $V_{DD} - V_{SS}$ | | 4 | — | 11 | Volts |
| Supply Current $I_{DD}$ | $V_{DD} - V_{SS}$ = 10V | | 90 | | µA |
| Common Mode Range | | $V_{SS}$ - 1.5 | | $V_{DD}$ −1.0 | Volts |
| Input Offset Voltage Vio | | | 3 | 10 | mV |
| Input Referred Noise Voltage<br>See Fig. 1 | f = 10 Hz<br>B = 1 Hz | | 1.5 | | µV/Hz |
| Input Capacitance Cin | | | 3.0 | | pF |
| Capacitance at Bia Input $C_{RN}$ | | | 1.5 | | pF |
| Gain Av | | | 80 | | dB |
| Unity Gain Frequency fo | $C_L$ = 5 pF | | 1.0 | | MHz |
| Phase Margin Øm | $C_L$ = 5 pF | | 50 | | degrees |
| Common Mode Rejection Ratio | f ≤ 1 kHz | 80 | | | dB |
| Power Supply Rejection Ratio | f ≤ 1 kHz | 60 | | | dB |
| Output Voltage | $R_L$ = 100 kΩ | $V_{SS}$ - 0.5 | | $V_{DD}$ −0.5 | Volts |
| Slew Rate | $C_L$ = 5 pF | | 0.6 | | V/µs |
| Capacitive Load $C_L$<br>(See Note 1) | Unity Gain | | | 5.0 | pF |
| Small Signal Output Resistance Ro | | | 180 | | kΩ |

Cell Size 372 x 372 µm

Note 1 Larger values may be used if feedback is less than 100%.

Note 2 This analogue circuit requires a bias input.

MEDL

# GENERAL PURPOSE OPERATIONAL AMPLIFIER

# AOP1

PROVISIONAL INFORMATION

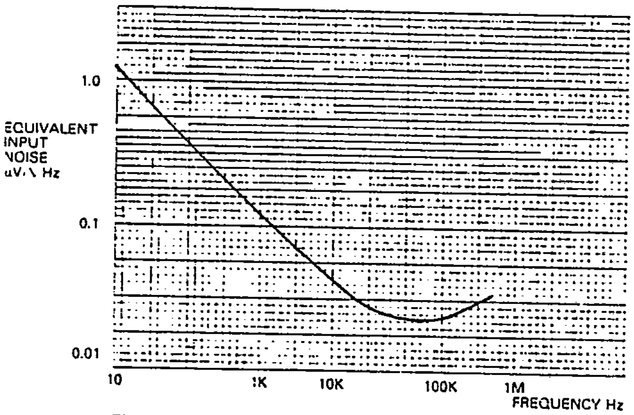



Fig. 1. AOP1 – ESTIMATED SPOT NOISE

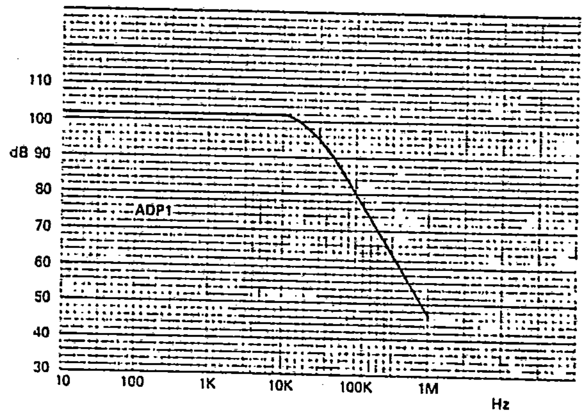



Fig. 2. COMMON MODE REJECTION RATIO

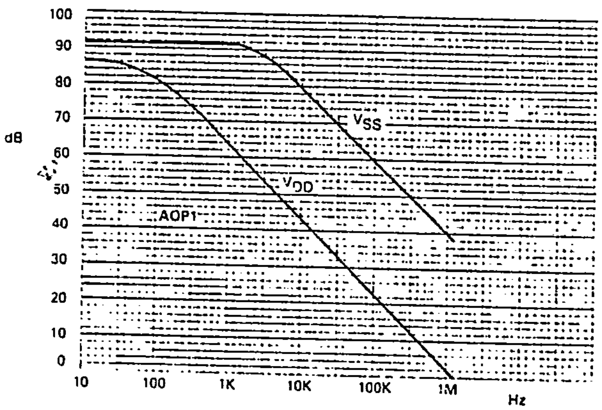



Fig. 3. POWER SUPPLY REJECTION RATIOS

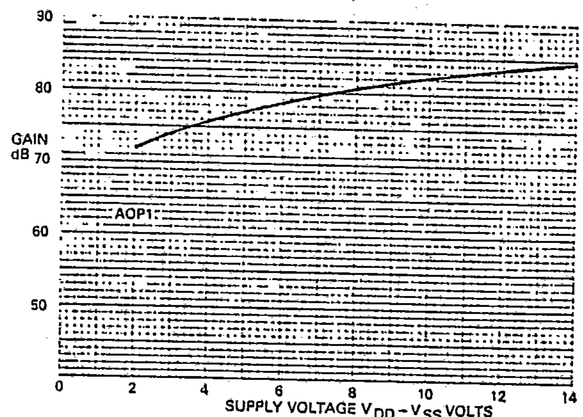



Fig. 4. GAIN vs SUPPLY VOLTAGE

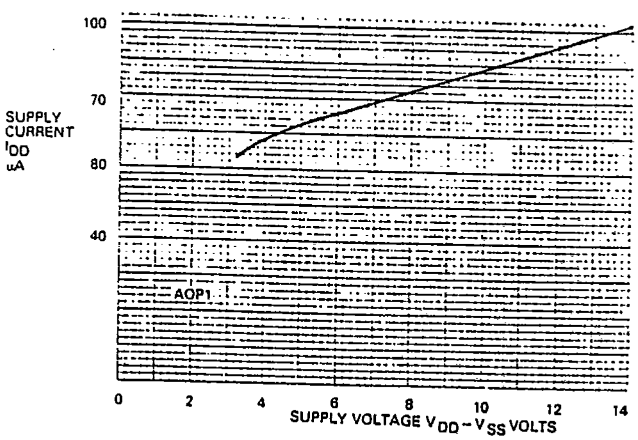



Fig. 5. SUPPLY CURRENT vs SUPPLY VOLTAGE

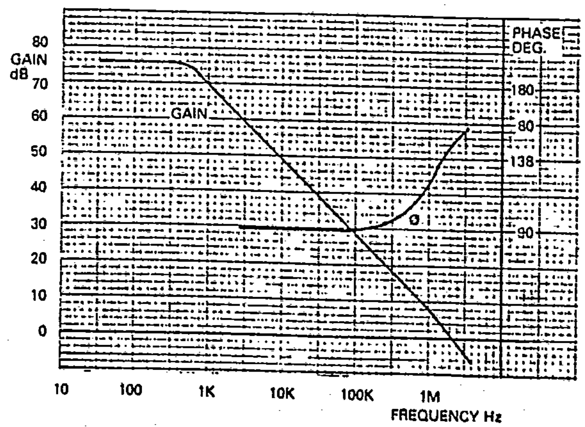


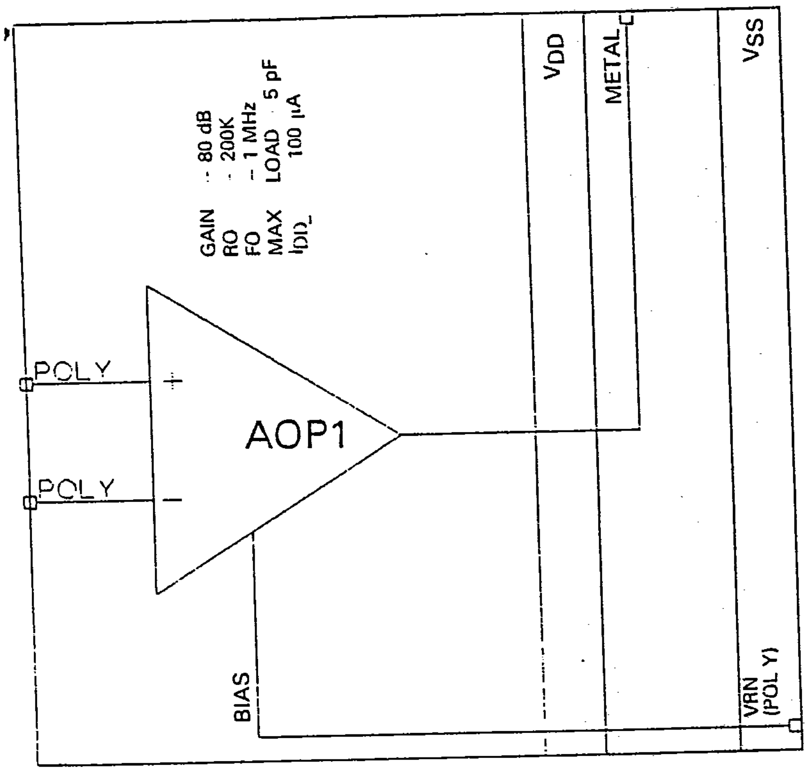

Fig. 6. GAIN AND PHASE vs FREQUENCY FOR AOP1

# GENERAL PURPOSE OPERATIONAL AMPLIFIER

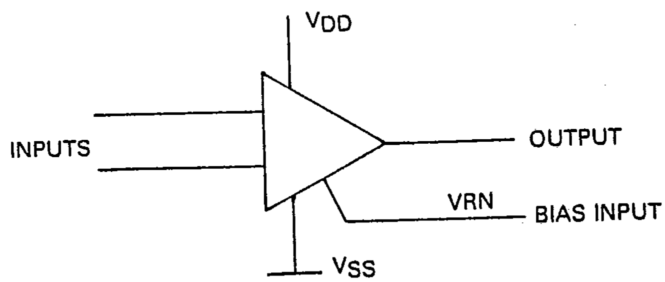
AOP1

MEDL

PROVISIONAL INFORMATION




PLOT SYMBOL AOP1




CIRCUIT SYMBOL AOP1

10

MEDL

# UNITY GAIN OUTPUT BUFFER FOR ISO-CMOS ANALOGUE CIRCUITS

# ABUF1

**PROVISIONAL INFORMATION**

This cell is designed primarily to be added to a basic operational amplifier such as AOP1 to enable it to drive off the chip.

Frequency response is such that it will not significantly affect the response of AOP1.

The circuit is based on an emitter follower, so the output voltage will be about 0.6V below the input voltage.

| CHARACTERISTIC | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Supply Voltage $V_{DD} - V_{SS}$ | | 4 | | 11 | Volts |
| Supply Current | $V_{DD} - V_{SS} = 10V$ | | 50 | | µA |
| Input Resistance Rin | | 1.0 | | | MΩ |
| Input Capacitance Cin | | | 2.0 | | pF |
| Positive Bias Input Capacitance $C_{RP}$ | | | 0.5 | | pF |
| Negative Bias Input Capacitance $C_{RN}$ | | | 0.5 | | pF |
| Output Resistance Ro | | | 80 | | ohms |
| Output Voltage | RL = 5 kΩ | $V_{SS}$ - 0.5 | | $V_{DD}$ −0.5 | Volts |
| Bandwidth (−3 dB) | CL = 50 pF | | 4.0 | | MHz |

Cell size (Including Bonding Pad 260 mm x 600 µm

Note 1 This analogue circuit requires bias inputs.

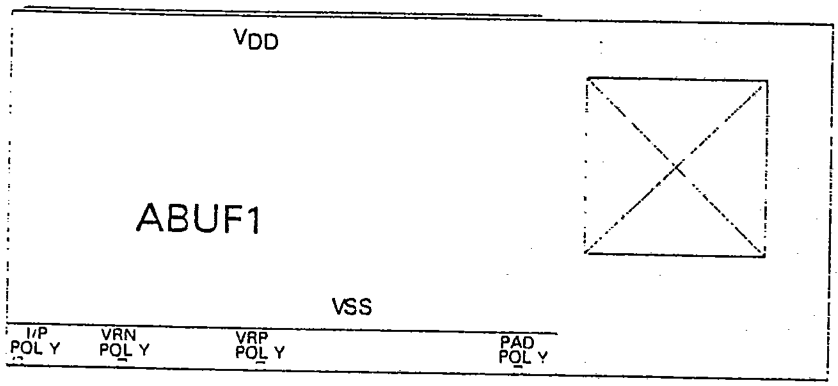
11

# UNITY GAIN OUTPUT BUFFER FOR ISO-CMOS ANALOGUE CIRCUITS

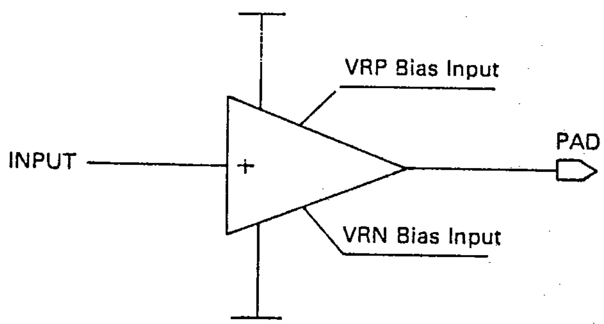
ABUF1

MEDL

PROVISIONAL INFORMATION




PLOT SYMBOL ABUF1




CIRCUIT SYMBOL ABUF1

MEDL

# ISO-CMOS ANALOGUE COMPARATOR

# ACMP1

PRELIMINARY INFORMATION

This cell is a general purpose voltage comparator whose output will drive 3 typical Cellmos gate inputs.

| CHARACTERISTIC | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Supply Voltage $V_{DD} - V_{SS}$ | | 4 | — | 11 | Volts |
| Supply Current $I_{DD}$ | $V_{DD} - V_{SS} = 10V$ | | 80 | | µA |
| Common Mode Range | | $V_{SS} - 1.5$ | | $V_{DD} - 1$ | Volts |
| Input Offset Voltage Vio | | | 8 | 20 | mV |
| Input Capacitance Cin | | | 0.7 | | pF |
| Capacitance at Bias Input $C_{RN}$ | | | 0.5 | | pF |
| Gain | $V_{DD} - V_{SS} = 10V$ | | 4000 | | |
| Response Time for 10 mV overdrive (See Fig. 1) | $C_L = 1$ pF | | | 1.5 | µs |

Cell Size 288 x 265 µm

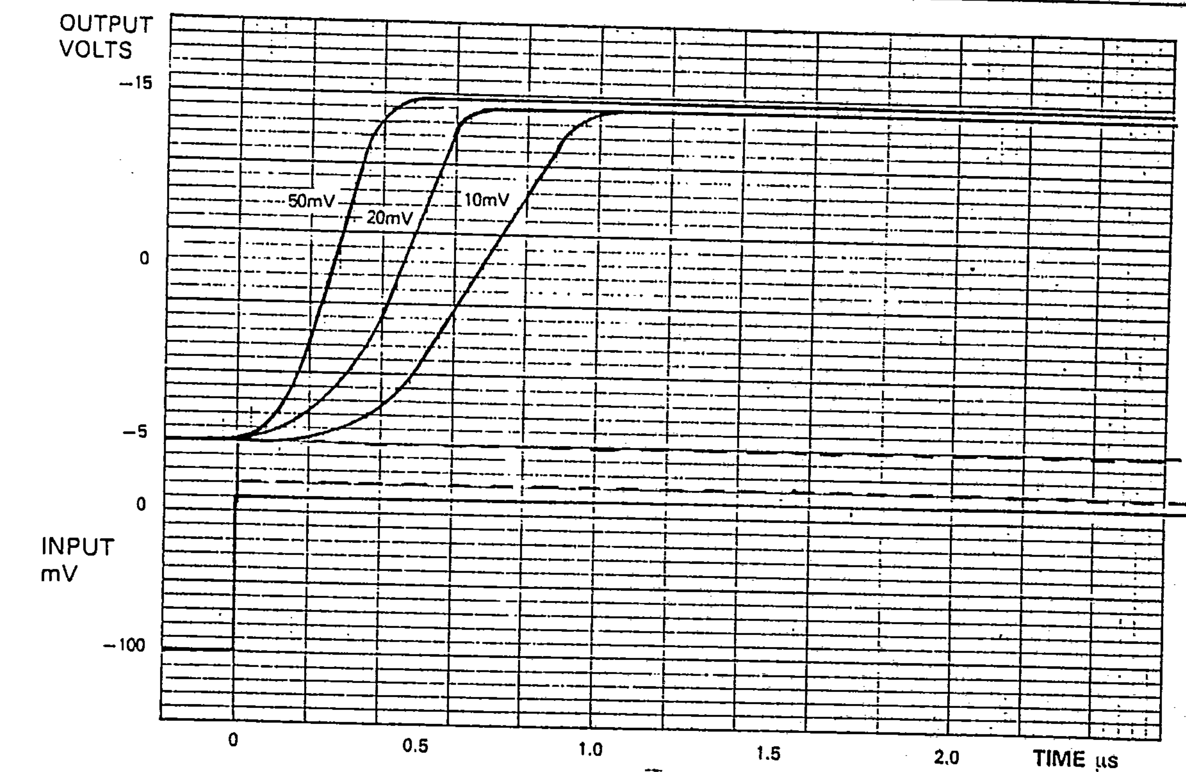
Note 1 This analogue circuit requires bias inputs.

# ISO-CMOS ANALOGUE COMPARATOR

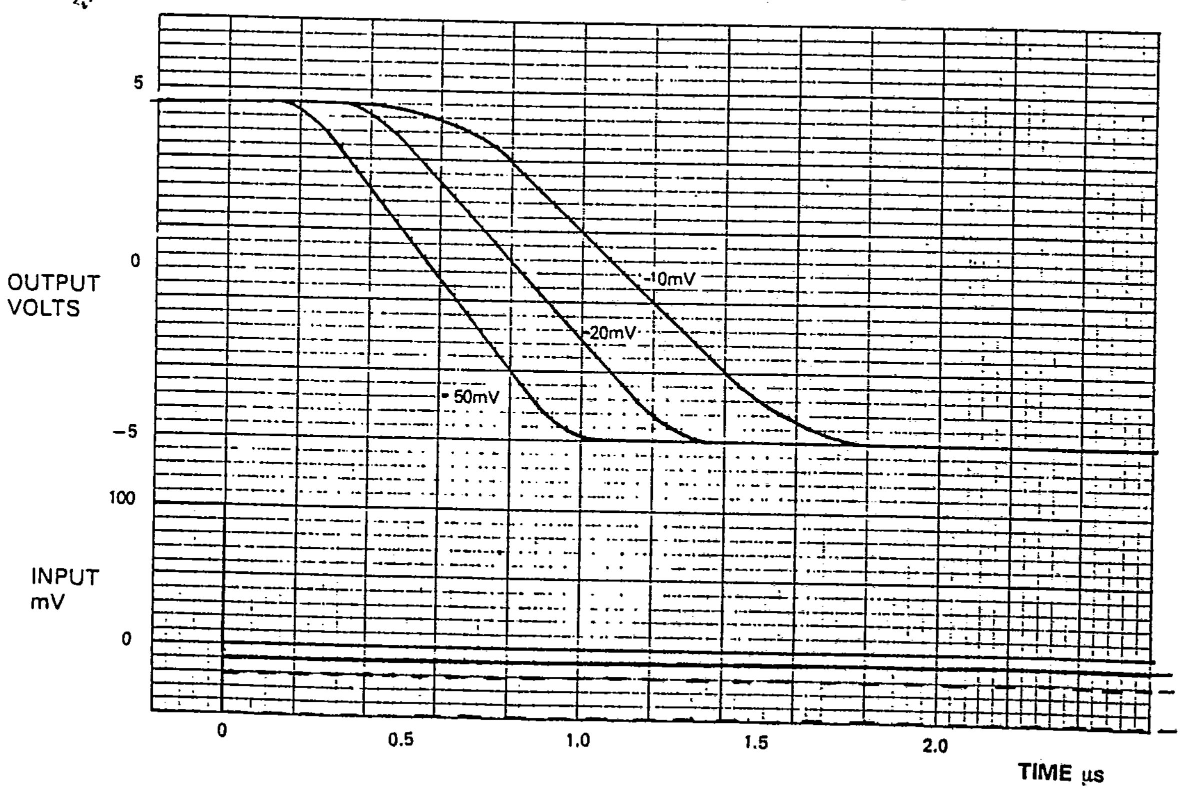
## ACMP1

MEDL

PRELIMINARY INFORMATION




ACMP1 — RESPONSE TIME FOR VARIOUS OVERDRIVE LEVELS

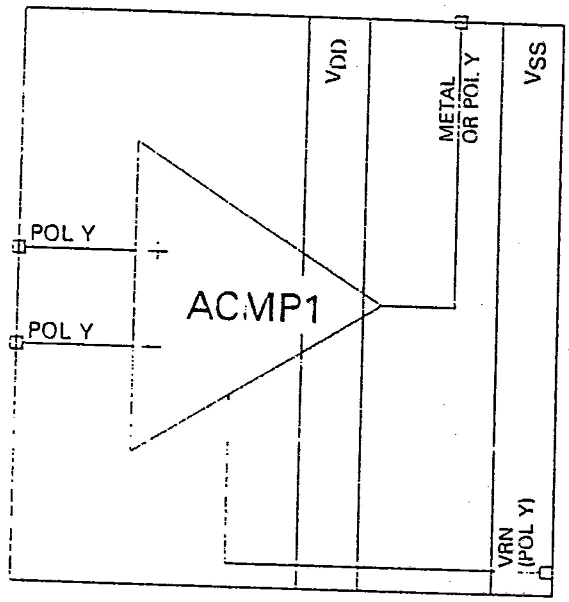


MEDL

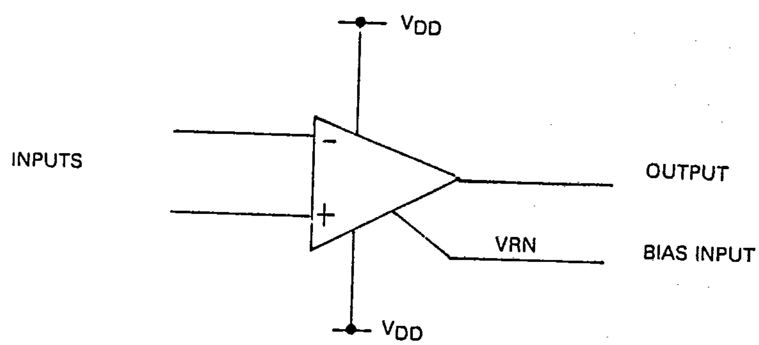
# ISO-CMOS ANALOGUE COMPARATOR

# ACMP1

PRELIMINARY INFORMATION




CIRCUIT SYMBOL ACMP1




PLOT SYMBOL ACMP1

# ISO-CMOS ANALOGUE SWITCH

# ANSW1

MEDL

PROVISIONAL INFORMATION

| CHARACTERISTIC | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Supply Voltage $V_{DD} - V_{SS}$ | | 4 | | 11 | Volts |
| ON Resistance $R_{ON}$ | $V_{DD} - V_{SS} = 5V$ | | 100 | 350 | ohms |
| $R_{ON}$ | $V_{DD} - V_{SS} = 10V$ | | 70 | 250 | ohms |
| Feedthrough-switch OFF | $V_{DD} - V_{SS} = 5V$ | | | | |
| (frequency at −60 dB) | $R_L = 10$ k | 10 | 16 | | MHz |
| | $C_L = 50$ pF | | | | |
| Charge Injection | $V_{DD} - V_{SS} = 5V$ | | 10 | | pC |
| Switching Time | $V_{DD} - V_{SS} = 5V$ | | | 50 | ns |

Cell Size 516µm x 228 µm

Note 1 The voltage drop across the switch when ON must not exceed 0.3V.

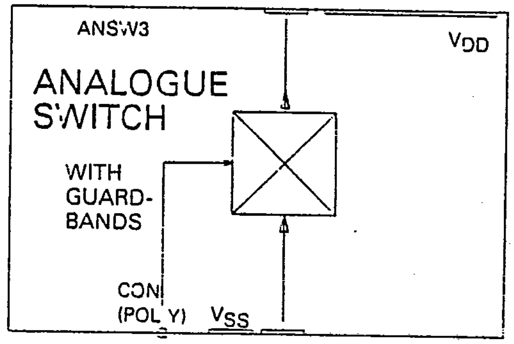
Note 2 The above shows a typical analogue switch, a range of cells are available with RONS of 50 or 100 ohm typical at 10V with or without guard banding for internal or direct external use. Smaller cells can be designed where higher resistances are acceptable.

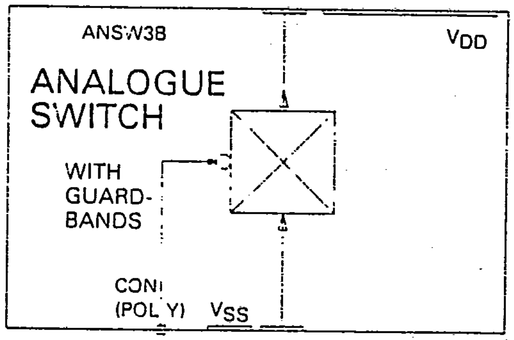
MEDL

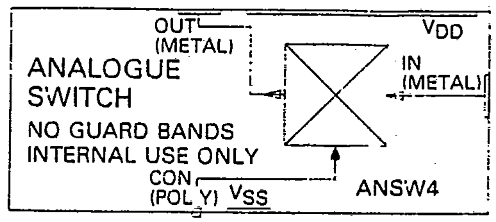
# ISO-CMOS ANALOGUE SWITCH

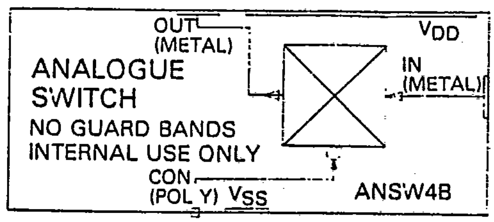
# ANSW1

PROVISIONAL INFORMATION



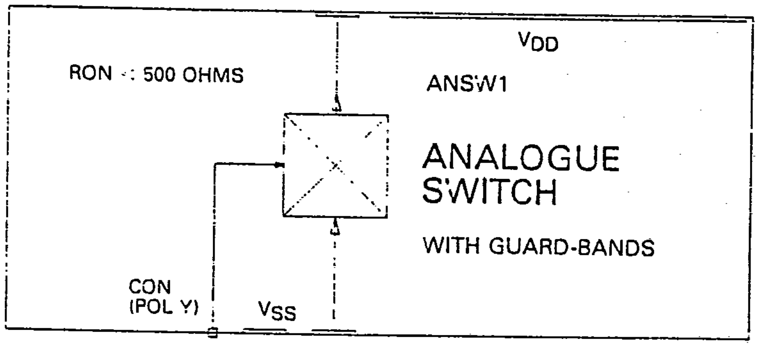



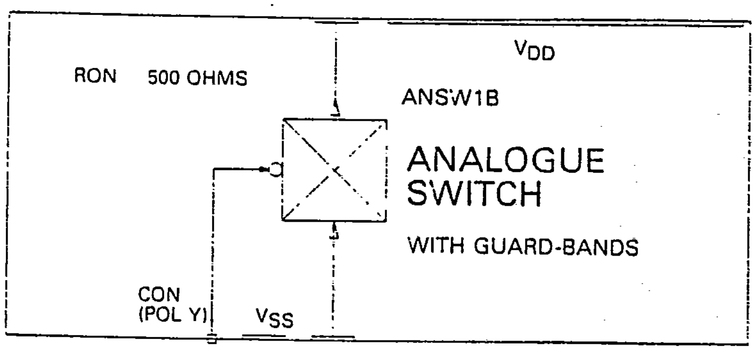
# ISO-CMOS ANALOGUE SWITCH

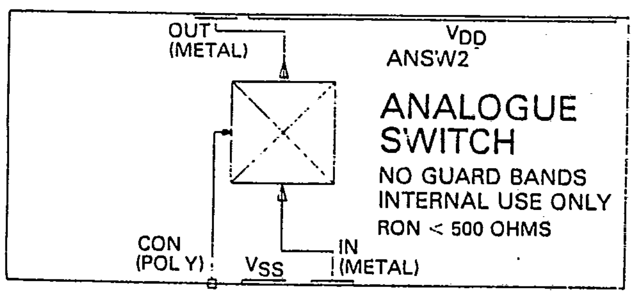
# ANSW1

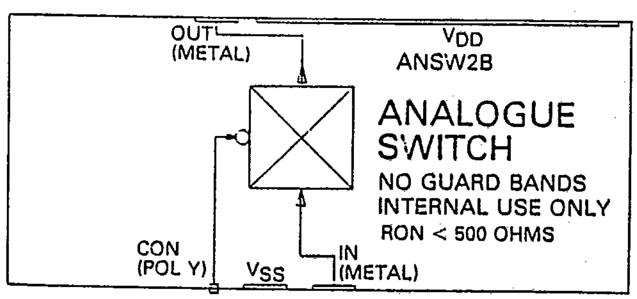
MEDL

PROVISIONAL INFORMATION



MEDL

# ISO-CMOS ARCOSC
# RC OSCILLATOR/MONOSTABLE

**PROVISIONAL INFORMATION**

This cell contains a resistor network, a discharge transistor and a bonding pad with input protection. A comparator must be connected to make the completed oscillator circuit. A monostable can be made by adding another cell containing some logic. This latter cell is designed as an ISO-CELLMOS core cell.

| CHARACTERISTIC | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Supply Voltage $V_{DD} - V_{SS}$ | | 4.5 | — | Note 1 | Volts |
| Oscillator Period T | | $5 \times 10^{-4}$ | | 10 | Seconds |
| Supply Current | $V_{DD} - V_{SS} = 10V$ | | | | |
| | RX = 100 k | | 100 | | μA |
| External Resistor Value RX | | 5 | | Note 2 | kilohms |
| External Capacitor Value Cx | | 1 nF | | 10 μF | |

Cell Size (including Bonding Pad etc) 432 μm x 432 μm

**Note 1** Maximum external timing resistor will depend on capacitor leakage.

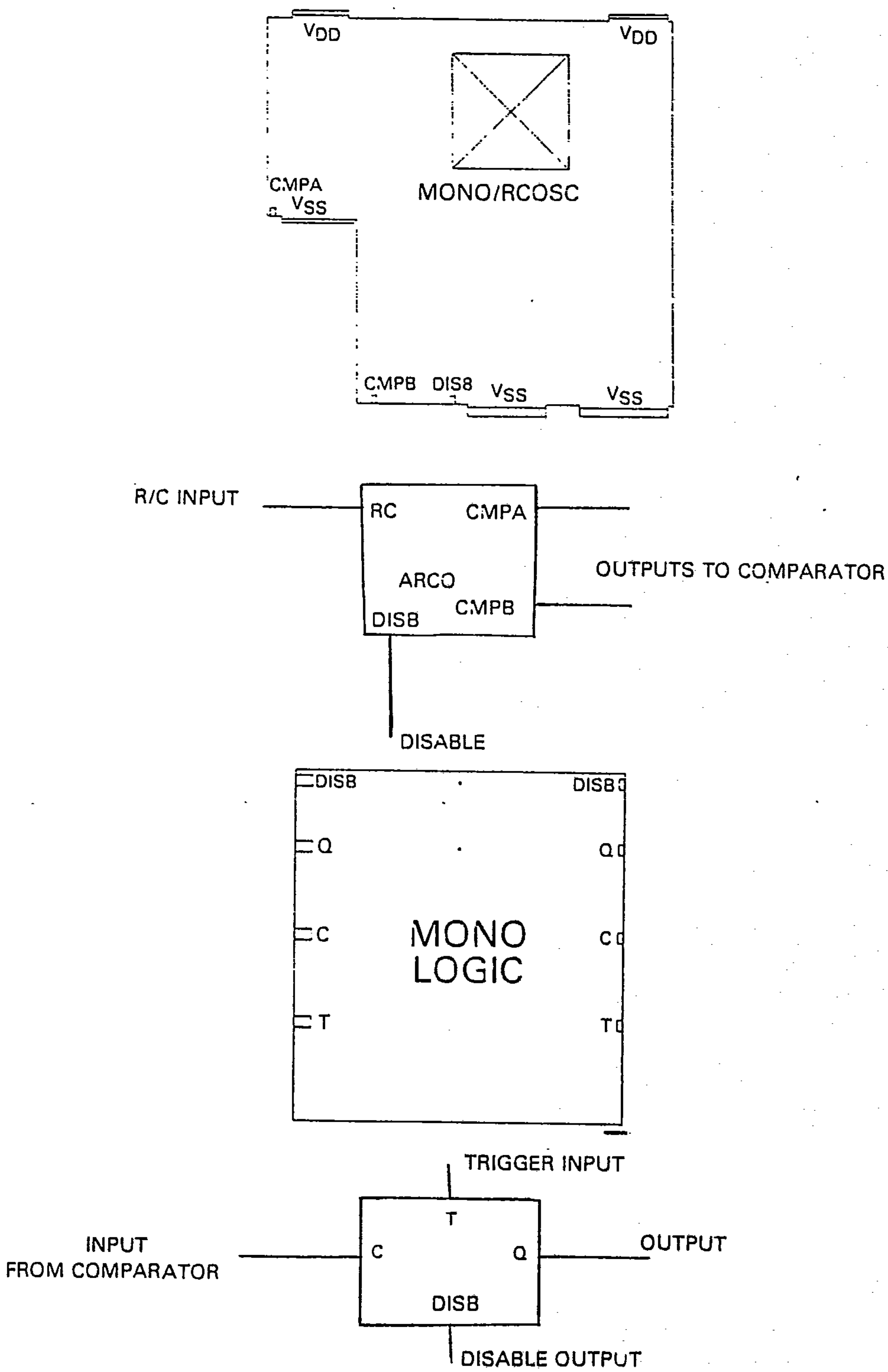
**Note 2** T ≃ 0.7 Cx Rx.

# ISO-CMOS RC OSCILLATOR/MONOSTABLE

# ARCOSC

MEDL

PROVISIONAL INFORMATION



MEDL

# CLASS AB OPERATIONAL AMPLIFIER



PROVISIONAL INFORMATION

## AOP3 = CLASS AB OPERATIONAL AMPLIFIER

## PROVISIONAL SPECIFICATION

This amplifier requires a special bias generator AVB1.

$V_{DD}$ = 10V T = 25°C unless otherwise stated.

| CHARACTERISTIC | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Supply Voltage | | 4.5 | | 11 | Volts |
| Supply Current | $V_{DD}$ = 10V | 200 | 450 | 1000 | μA |
| Common Mode Range | | $V_{SS}$ - 1.5 | | $V_{DD}$ −1 | Volts |
| Input Offset Voltage | | | 3 | 10 | mV |
| Gain | | 75 | 80 | | dB |
| Unity Gain Frequency | $C_L$ = 100 pF | | 1 | | MHz |
| Phase Margin | $C_L$ = 100 pF | | ~70 | | degrees |
| Common Mode Rejection | f · 1 kHz | | 80 | | dB |
| Power Supply Rejection $V_{DD}$ | f · 1 kHz | | 50 | | dB |
| Power Supply Rejection $V_{SS}$ | f · 1 kHz | | 60 | | dB |
| Output Resistance | | | 20 | | kohm |
| Output Voltage Swing | $R_L$ = 3500 Ω | −4 | | -4 | Volts |
| Slew Rate | $C_L$ = 100 pF | | 0.5 | | V/μs |
| Load Capacitance (see Note 1) | | | | 500 | pF |
| Supply Current | $V_{DD}$ = 5V | | 50 | | μA |
| Gain | $V_{DD}$ = 5V | | 90 | | dB |
| Unity Gain Frequency | $V_{DD}$ = 5V | | 200 | | kHz |
| Output Resistance | $V_{DD}$ = 5V | | 80 | | kohm |

Cell Size 480 x 670 μm including Bonding Pad.

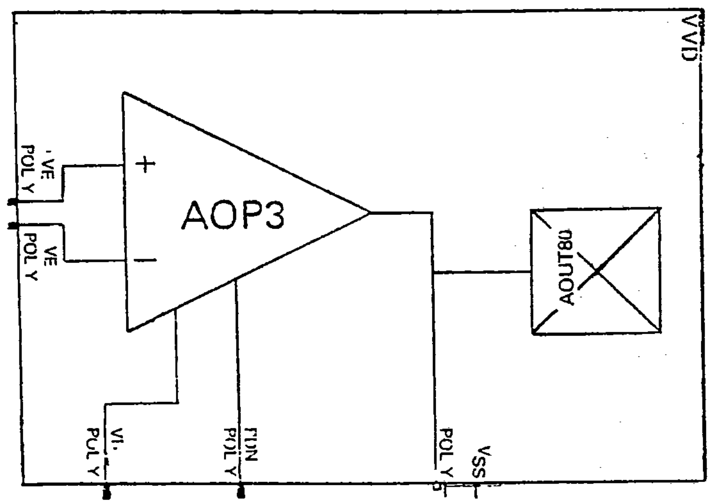
Note 1 Simulations indicate a peak of about 4 dB at 700 kHz when connected as a voltage follower with 500 pF load.

# CLASS AB OPERATIONAL AMPLIFIER

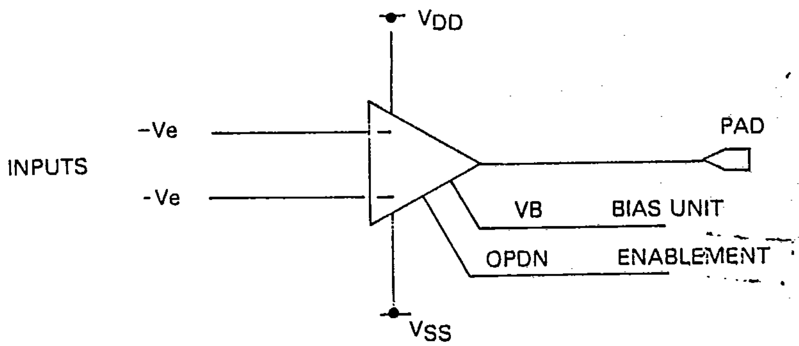
**AOP3**

MEDL

PROVISIONAL INFORMATION




PLOT SYMBOL AOP3



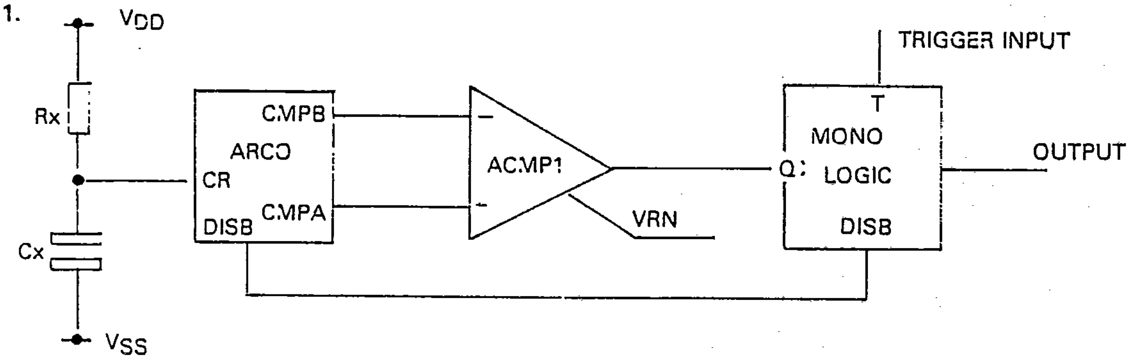

CIRCUIT SYMBOL AOP3

22

MEDL

## APPLICATIONS

1.



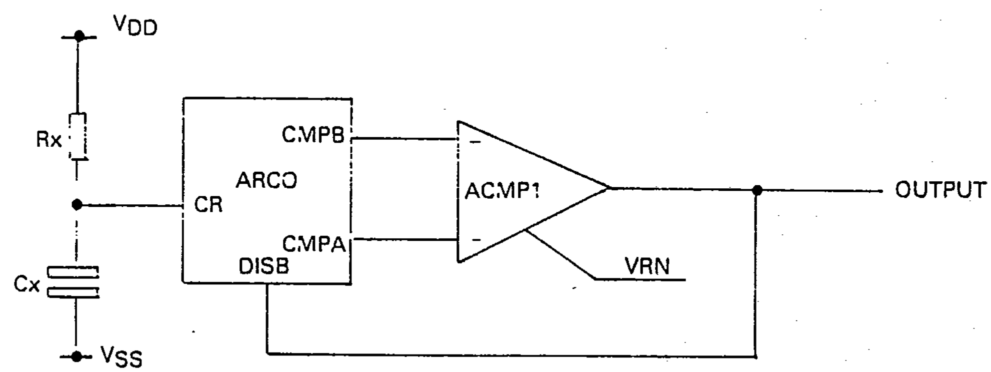

**MONOSTABLE**

Note 1 Requires bias input to comparator cell (ACMA1). Bias circuit disable when active will disable this circuit.

Note 2 Time constant (T) $\simeq$ 0.7 Cx Rx.

Note 3 This circuit (INARCO) has a fixed bias chain of 150 k and between $V_{DD}$ and $V_{SS}$ so $I_{DD}$ will not be zero.

2.




**R C OSCILLATOR**

Note 1 Requires Bias Input to comparator Cell (ACMP1) Bias circuit disable when active will disable this circuit.

Note 2 Time constant (T) $\simeq$ 0.7 CxRx.

$$f \simeq \frac{1}{0.7\,CxRx}$$

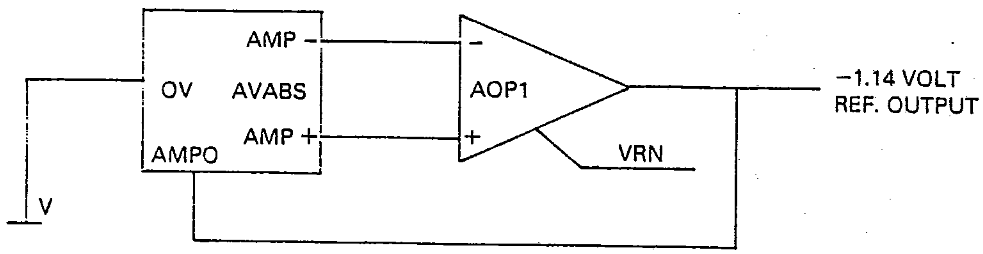
Note 3 Output has large mark to space ratio, Divide by 2 if symmetrical output is required.

Note 4 This circuit (in ACRO) has a fixed bias chain of 150 K between VDD and VSS. So this circuit will draw current in standby mode.

# APPLICATIONS

MEDL

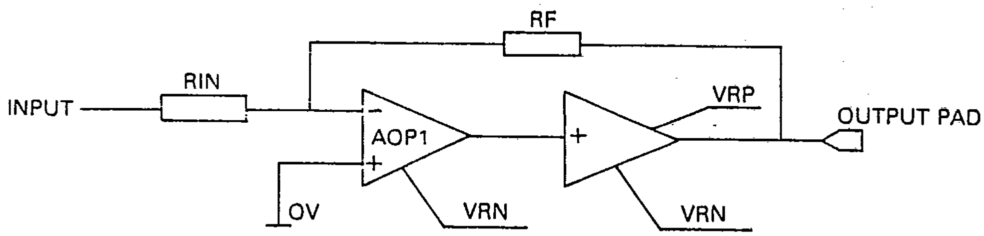
3.




**ABSOLUTE VOLTAGE REFERENCE**

**Note 1** Requires Bias Input to amplifier bias circuit, when active will disable this circuit, reducing the current drawn.

4.




**OPERATIONAL AMPLIFIER WITH OUTPUT BUFFER**

**Note 1** Voltage Gain $\simeq \frac{RF}{RIN}$

**Note 2** Both AOP1 and ABUF1 require a common circuit, which when disabled will reduce supply current consumption to virtually zero.

24

# MARCONI ELECTRONIC DEVICES, INC

Marconi

| PREFIX | DEVICE | SUFFIX |
|---|---|---|
| MA_ | 5101 | CBC - XXX |

- Add S for Radiation Hard CMOS/SOS — MA_
- Package — C
- Screening & Inspection — B
- Temperature Range — C
- Special Requirements/Enhancements — XXX

PACKAGE

A. Pin Grid Array
C. Ceramic DIL
E. Epic
F. Flat Pack
G. Cerdip
L. Leadless Chip Carrier
M. Module
N. Naked Die
P. Plastic DIL
Q. Quad Plastic J-Lead
R. Qual Cerpack J-Lead
S. SO Plastic
X. Special

TEMPERATURE RANGE

A. Special
B. 0 to 70°C
C. -55 to +125°C
D. -25 to +70°C
E. -25 to +85°C
F. -40 to +85°C
G. -55 to +85°C
H. -40 to +125°C
J. -10 to +80°C
K. 0 to +200°C

SCREENING & INSPECTION

B. Mil Std-883C Class B
G. Commercial Hermetic
L. Commercial Plastic
S. Mil Std-883C Class S
T. ESA9000
X. Special

45 DAVIDS DRIVE • HAUPPAUGE, N.Y. 11788 • Phone: (516) 231-7710 • Fax: (516) 231-7923 • Telex: 275801