IMP50E30 EPAC

Programmable Monitoring and Diagnostic IC

Electrically Programmable Analog Circuit

Introduction

The IMP50E30 is a programmable IC offering a variety of monitoring, diagnostic and data-acquisition capabilities. Its operating modes increase system observability, enabling it to both monitor and measure the state of a system and even take corrective action. Several IMP50E30s may be cascaded and serviced by one µC, making it ideal for multi-level on-card applications (see ***Figure 1***).

Each IMP50E30 contains a selected assortment of analog and digital modules plus an EEPROM, all on one chip. These are optimized for a specific range of applications. The user may configure and specify these modules without external parts. In addition, the device can be re-programmed after installation, even during system operation.

To speed the development of IMP50E30 applications, IMP also offers Windows-based Analog Magic™ development system software. It emulates a host controller, thus removing the need for programming before working silicon is available.

Applications

- Component and system fault monitoring
- Fault condition diagnosis/correction
- Remote datalogging/trend gathering
- On-card monitoring in cascaded designs
- UPS system monitor
- Automatic testing and calibration
- Wire bundle/connector verification
- Monitoring in network servers, power supplies, process controls, embedded systems, copiers, vending machines and office electronics

Figure 1 Multiple IMP50E30s, Each With Several Inputs, All Under the Control of One µC.

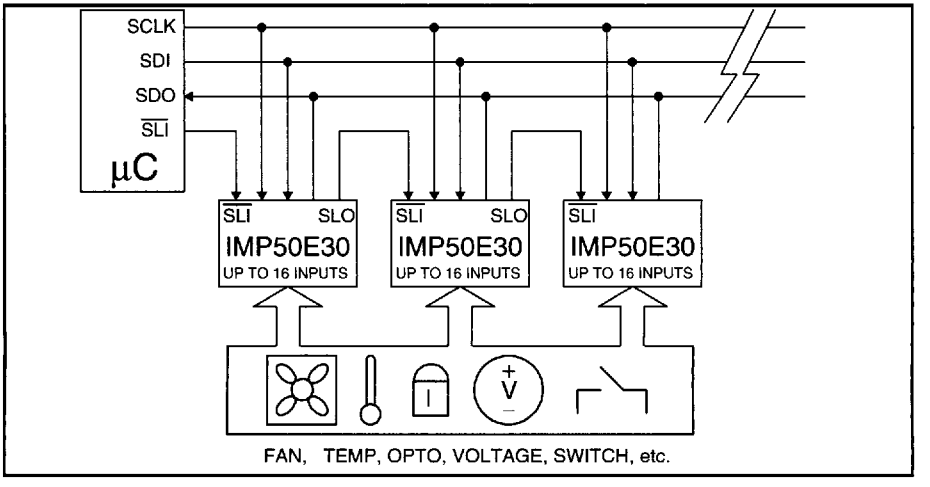

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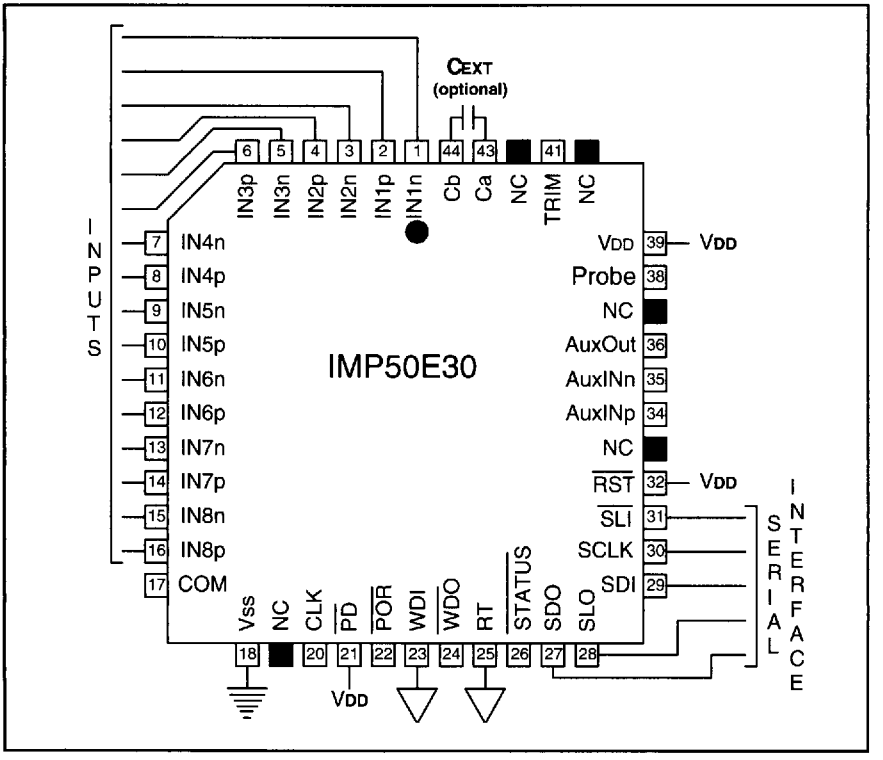
Figure 2 The IMP50E30 - Simple Interface



General Description

The IMP50E30 is, first and foremost, a *user-programmable* IC. Thanks to innovative switched-capacitor design techniques, the IMP50E30 modules can be configured and their specifications set via software commands. No external resistors or capacitors are needed. (See ***Figure 2.)***

A simple serial interface suffices to connect the IMP50E30 to a µC that can command its operations and send data to and from it. The µC can also re-program the chip, if desired, in-circuit, and on-the-fly.

To assist users in learning about and programming the IMP50E30, IMP offers an EPAC Development System with Analog Magic Software. This combination allows testing and modifying of the IMP50E30 while it is connected to the external circuit. This allows the immediate viewing of the effects of each change in programming.

The IMP50E30 chip has three basic circuit configurations:

- Level Comparator or LComp
- Window Comparator or WComp (***Figure 3***)
- Analog-to-Digital Converter or ADC (***Figure 4***)

Voltage inputs for these configurations are selected by a Mux, conditioned by a Filter and an Amplifier, and fed into a Comparator. Other functions include an auxiliary standard CMOS OpAmp, a Voltage Reference, a Master/Slave Clock, a Power Control Module, a Security Module and a CPU Watchdog. There is also a Connection Timer to supply the proper delay for signal acquisition and filter settling. All of these functions are programmable.

4850429 0002427 829

Figure 3 IMP50E30 Configured as a Window Comparator

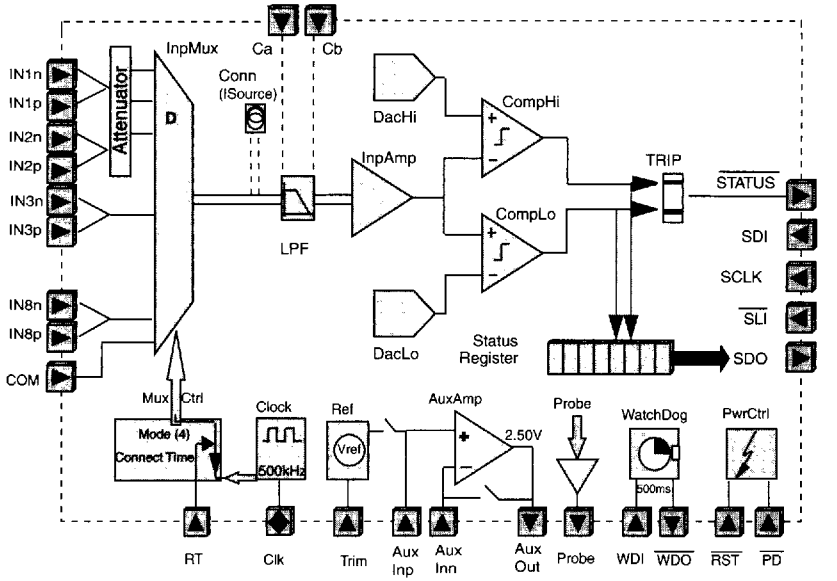


Figure 4 IMP50E30 Configured as an A/D Converter

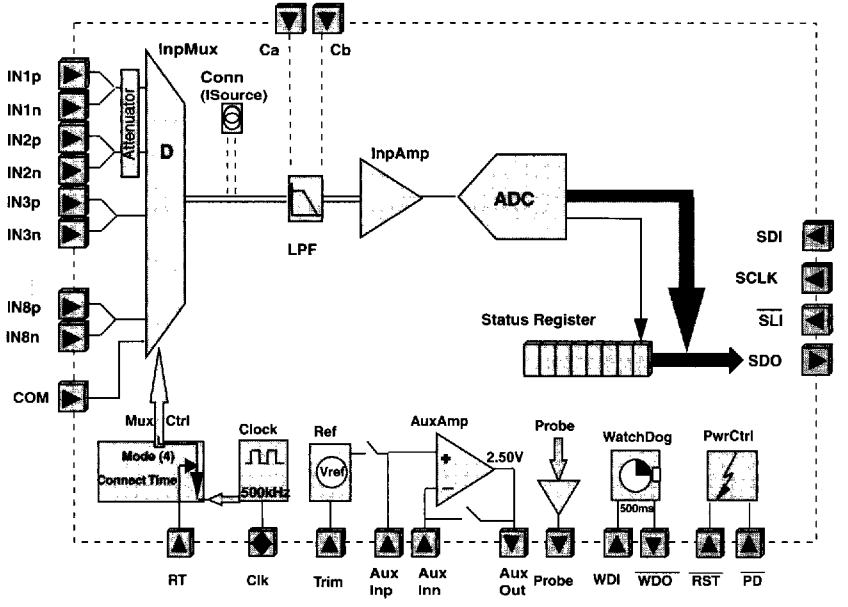
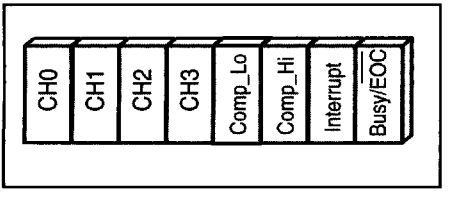


Figure 5 IMP50E30 Status Register



4850429 0002428 765

Features

- Multiplexed input channels
  - 16 Single-ended, 8 Differential
- Stepped or Continual channel scanning
- ±16.5V signal range on four input channels
- Programmable filter module
- Acquisition Delay Timer for signal/filter settling
- Programmable-gain instrumentation amplifier (***InpAmp***)
- Level and Window comparators with programmable thresholds (256-level DAC)
- Serial 8-bit A/D Converter
- Watchdog timer and Auxiliary Opamp for added functionality
- EEPROM to store circuit configuration
- SRAM for real-time, in-system circuit configuration changes
- Stand-alone or µC operation via on-chip serial interface (IMP50E30s can be cascaded)
- Low-power CMOS technology with programmable power-down mode
- Real-time probe of internal modules and timing signals (MagicProbe™)

Functional Overview

The IMP50E30 input multiplexer monitors 16 single-ended signals or 8 differential signals. Although the device operates from a single 5V supply, the first four input channels (two in differential mode) can accept signals from -16.5V up to +16.5V, thanks to an on-chip 8:1 attenuator plus level shifter (see ***Figure 6***). The multiplexer is followed by a programmable low-pass filter and an instrumentation amplifier (***InpAmp***) with programmable gains of 0.5, 1, 2, 3, 4, 6, 8 or 10.

In the Window-Comparator mode (***Figure 3***), the InpAmp samples-and-holds the input against which the programmed upper and lower DAC thresholds are sequentially compared. This time-multiplexed operation saves the physical duplication of a DAC and a comparator and makes the overall operation more accurate.

Under user-control, the chip may be reconfigured as a 16-channel A/D Converter (***Figure 4***) by using the internal DAC, comparator and successive-approximation register (SAR). The digitized signal is available through the serial-data-out interface port (SDO).

In any of these modes, different gains, high and low limits, and filter response characteristics for each individual channel can be stored in the on-chip memory. These characteristics automatically change with change of channel.

The ***MuxControl*** module can be programmed to continuously scan through all input signals as a background routine. If an out-of-limit condition is detected, an interrupt signal is generated. A µC can then read the STATUS register (***Figure 5***) and determine the location and type of system fault. This information is then used by the µC to make a "smart" decision. This might include re-test with different limits or programmed new ones. The µC also can take action (turn on a fan, slow the CPU, crowbar the system, etc.).

Alternatively, you can look for simple shorted or open circuits by using the programmable 10µA current source/sink module (ISource) at the multiplexer output and test if any input is driven by a low-impedance source or if it has been left floating. This connectivity test mode is useful during system start-ups to verify that critical external connections exist. In addition, button or switch closures can be detected.

Using the A/D, one can also test real system values such as system voltages or sensor inputs, either for diagnostic purposes or to gather trend data. By combining the A/D with the current source, quantitative input resistance measurements are also possible. Contact IMP for Application Notes on these topics.

Module Details

InpMux Module

This module sets input mode and voltage for each channel.

4850429 0002429 6T1

Input Channel Options: Single-Ended (S) or Differential (D)

Input Voltage Options: ±16.5V or 5V on channels 1 - 4 (S) or 1 and 2 (D). Channels 5 - 16 (S, or 3 - 8 D) are 0 - 5V only.

MuxCtrl Module

This module sets the triggering method, number of channels used, and acquisition time per channel.

Number of Input Channels: 8/16 (S) or 4/8 (D);

Channel Selection/Triggering Options: Single-Step, Single-Step (with) Advance, "Stare," and AutoScan (see **Operating Modes**). Triggering is via the RT pin or a software command.

Connection Time: This has 8 choices, from 12µs to 16.4ms. The Connection Timer controls the acquisition time for a signal (sample). This is followed by a fixed measurement time (hold).

Connectivity Module (CONN or ISource)

This is a current source that can inject 10µA into the input circuit. It can be used to test continuity on all input channels in the comparator modes. In the A/D mode, it can also be used to measure the resistance of the signal source. With the Connectivity Module (10µA) applied to the input, resistance can be measured. The range for this can be calculated from the formula:

$$R = V_{DAC}/(V_{InpAmp})(10\mu A).$$

The minimum R depends on the maximum gain and minimum DAC resolution. With a gain of 10, resolution is 1mV, so Rmin is 10mV/(10)(10µA) = 100Ω. The maximum R uses the minimum gain (0.5) and maximum DAC voltage, giving 510kΩ. The tolerance on the current source will control the final accuracy.

Low Pass Filter (LPF)

This is a single-pole, 15kHz continuous-time filter that can be switched into or out of the signal path. When out, it has no effect on any signal. It can also be used with an external capacitor connected to the Ca/Cb pins to achieve other cutoff frequencies. The filter for any channel depends on its Group. (See ***Figure 7.***)

InpAmp

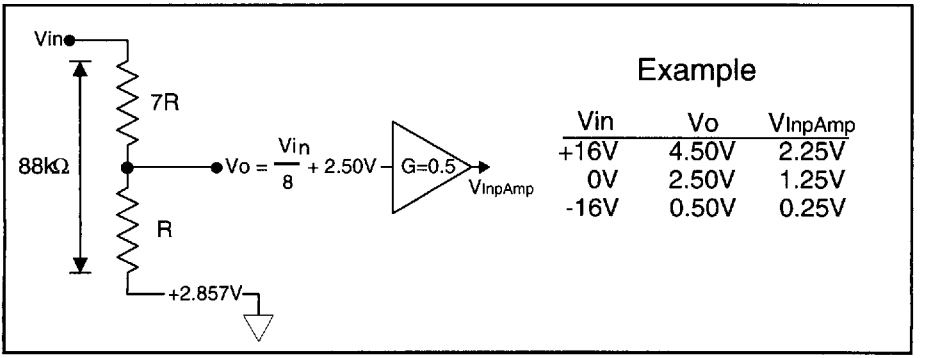
This instrumentation amplifier module gives a gain of 0.5, 1, 2, 3, 4, 6, 8 or 10, and has an integrated sample-and-hold function. The gain for any channel depends upon its Group. (See ***Figure 7.***)

Comparator/ADC Module

This module is actually four modules that can be configured (interconnected) by software commands to form either a level comparator (with high or low thresholds), a window comparator, or an A/D converter.

The $\overline{\text{STATUS}}$ pin serves as both the interrupt output for the comparator and as the EOC (End-Of-Conversion)

Figure 6 Input Attenuator
(Channels 1-4, Single-Ended Operation; Channels 1-2, Differential Operation)



4850429 0002430 313

indicator for the A/D. In the A/D configuration, a SAR (Successive-Approximation Register) is also connected into the circuitry: its contents (the converted value) are read out via the SDO pin.

Comparator thresholds (limits) are also selected with this module. The limits for any channel depends on its Group. (See ***Figure 7***.)

Groups

Referring to ***Figure 7***, it can be seen that the IMP50E30 has eight independently-programmable channels, called Groups. A Group can be programmed with its own filter, gain and comparator threshold (limit) values. Each Group also can be switched between two different input sources that require those same values, so up to 16 inputs (but only 8 different) can be accommodated.

In practice, most circuits and systems have such duplicated source voltages.

AuxAmp/RefBuffer

This is an uncommitted, low-power operational CMOS amplifier. It can be used alone or with external feedback components to make a variety of one-opamp circuits. Alternatively, the AuxAmp can be switched to the RefBuffer mode, where it is connected to the internal reference voltage and provides a buffered voltage reference output.

Clock

This module supplies control signals to the switched-capacitor modules and other circuitry inside the chip. The internal master clock runs at approximately 500kHz (High Speed mode), while the internal sampling clock runs at 250kHz. The Low-Speed mode runs the chip 8 times slower, thus extending all clock-dependent operations (Connection Time, A/D, etc.) by this factor.

The Clock module operates in either a Master or Slave mode. In Master mode, the clock signal is available at the CLK pin, divided by a programmmable prescaler (÷1, 2, 4 or 8). In Slave mode, an external clock may be input to the CLK pin. The prescaler can divide this input by 1, 2, 4 or 8.

Figure 7 Group Programming of the MUX, LPF, PGA and DAC (Comp Threshold) Modules

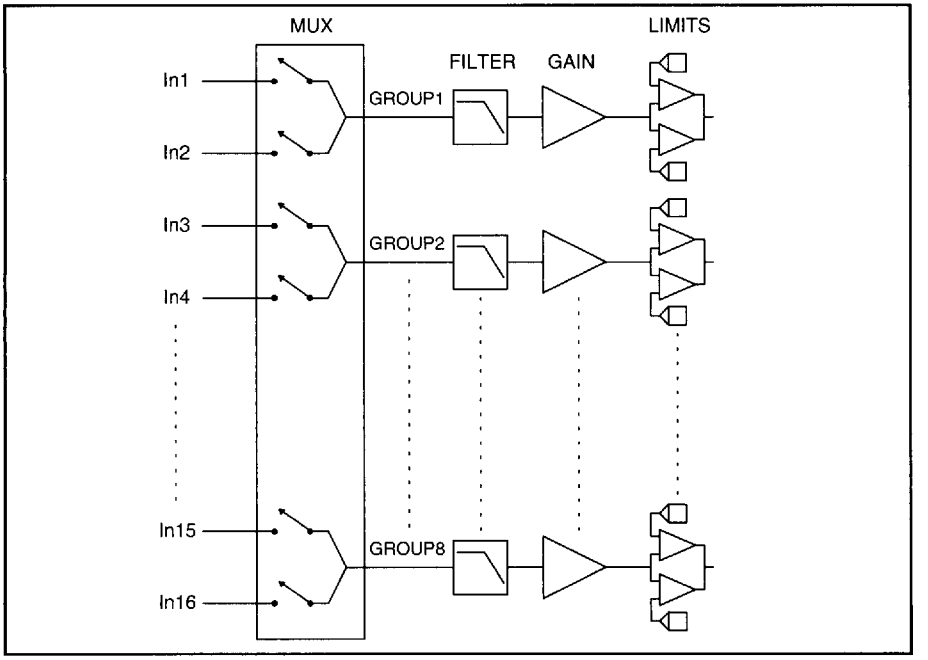


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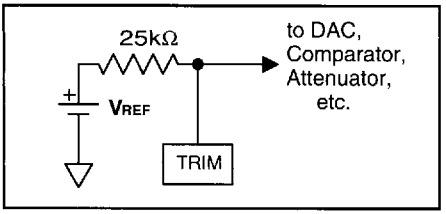
Figure 8 TRIM Pin Topology



Vref

The IMP50E30 has an on-chip reference trimmed to ±1% accuracy at the factory. One can overdrive it at the TRIM pin with an external reference. This affects all internal levels, including DAC limits, A/D values and Attenuator outputs (see ***Figure 8***).

Power Module

This module controls the chip's power options.

$\overline{PD}$: This command (Power-Down) puts the chip into the Sleep Mode. It can be issued in software or by grounding the $\overline{PD}$ pin.

$\overline{POR}$: This is an output at the $\overline{POR}$ (Power-On-Reset) pin. It is a pulse that can be used for resetting other circuits. It is issued only at Power-On.

$\overline{RST}$: This command (Reset) produces the same download to the EEPROM as PD, but V_{DD} doesn't have to be removed to do it. A $\overline{POR}$ pulse does not accompany $\overline{RST}$.

Watchdog

This module monitors external CPU operation and triggers a Reset if the WDI pin is not periodically pulsed. It can also be used as a general-purpose, fixed-period timer. The timeout period is programmable.

Security

This module has two states, OPEN and LOCKED. If LOCKED is selected, the chip configuration can no longer be read back, so it will be protected from unauthorized copying. However, one can overwrite the present configuration. The device is thus always usable for new configurations.

Probe (MagicProbe)

The Probe pin on the IMP50E30 is the output of both a digital driver and an amplifier (gain=2) that can monitor nodes inside the chip that would otherwise be inaccessible. This is the MagicProbe, and it has its own commands (see ***Table 4a***, "Function/Location of Command Bits for MagicProbe"). Under some circumstances, it can be used as an alternate output for selected digital and analog signals. This diagnostic tool is used extensively by Analog Magic software to aid in the debugging phases of application development.

EPAC System Design

Changing system requirements that produce different IMP50E30 circuit needs are easily done using PC Windows™-based Analog Magic software and IMP development tools. Like other EPAC products, the IMP50E30 is easily configured and programmed using its low-cost Development System with Analog Magic. The Development System supports all current EPAC devices.

Operating Modes

In any of its operating modes (Window Comparison, Level Comparison and ADC), input signals can be monitored differentially or in single-ended fashion. In addition, the user can program which channel(s) are to be monitored, the triggering method, and the Connection Time per channel. In the Level and Window Comparison Configurations, channel testing is triggered either singly or continually. In the ADC mode, it is singly-only.

Single-Step: The user selects a specific channel via software command to the serial I/O port. Monitoring can then be initiated in two ways: a software-based trigger (SW) or a hardware-based trigger (HW).

If a software trigger is sent, the Connection Timer controls the connection (acquisition) and comparison interval. If an external trigger is provided at the $\overline{RT}$ pin, its edge transitions start and stop the

4850429 0002432 196

connection and comparison process. The single-channel mode can thus provide manual control over which input signal is being monitored and for how long.

Single-Step Advance: SW or HW triggering begins the testing as above. It always begins with channel 1 and advances to the next higher channel when testing is completed. The user can program advancing through 16S/8D (full-scan) or 8S/4D (half-scan) channels (S=Single-ended, D=Differential).

"Stare": The user selects the channel in SW, and issues either a SW or HW trigger. Triggers will then repeat automatically; the IMP50E30 "stares" at that channel continually, monitoring it for an out-of-limit condition. This is useful for capturing either asynchronous or occasional events.

AutoScan: The user issues a HW/SW trigger as above, but now the channel selector cycles continuously through either 16S/8D or 8S/4D channels. The Mux Control will automatically move from one channel to the next in a "round-robin" fashion with each completed comparison.

The scanning sequence normally begins with channel 1. However, when the comparator detects an "outside-of-window" or "above or below threshold" condition, an error flag (INTerrupt) is set at the $\overline{\text{STATUS}}$ output pin and COMP_Hi or COMP_Lo is set in the STATUS register. At this point, the user may elect to perform an A/D conversion on the input, or simply use the STATUS information to make a decision. By issuing the appropriate Write Mode command, the chip configuration will change to A/D while leaving the channel unchanged. After the A/D measurement, another Write Mode command will change the configuration back to Comparator. The next trigger will then continue the scanning from that channel onward instead of resetting to channel 1.

4850429 0002433 022

Absolute Maximum Ratings

Stresses beyond those specified may cause damage to the device. The ratings are for stress only, and operation of the device at these levels is not implied.

V_{DD} to V_{SS}	0V to 7V
Voltage at Any Pin*	(V_{SS} - 0.3V) to (V_{DD} + 0.3V)*
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10sec)	300°C
ESD Rating (max) [see Note 1]	1.5kV
Input Current at Any Pin	100mA at 10V

* see **Input Multiplexer Module**, "Input Signal Ranges" for exceptions.

[1] Human body model, 100pF discharged through a 1.5KΩ resistor.

Recommended Operating Conditions

Supply Voltage	5.0V ± 10%	
Operating Temperature Range	IMP50E30-C	0°C to 70°C

General Electrical Characteristics

Unless otherwise specified, 4.5V < V_{DD} < 5.5V, T_A = 25°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{DD}		4.5	5	5.5	V
Power Supply Current[1]	I_{DD}	High-Speed, All Modules active			6	mA
		Low-Speed, All Modules active		3.8	6	mA
		Sleep Mode		70		µA
EEPROM Programming Time	T_{WEE}	Write	1.25			ms/bit
via Serial Interface	T_{REE}	Read	4			µs/bit
SRAM Programming Time	T_{SRAM}	Read or write	625			ns/bit
EEPROM Download Time (Auto-Configuration)	T_{DL}	To Configuration Register		0.77	1	ms
Write Cycles		To EEPROM	10,000			
EEPROM Data Retention			10			years
System Clock	T_{CLK}	Master mode	450	500	550	kHz
Internal Sampling Clock	T_{SAMP}	High Speed	225	250	275	kHz
		Low Speed	28.1	31.3	34.4	kHz
Channel Scan Period[2]	T_{CH}	High Speed	6		4100	cycles[2]
Channel Connect Time Delay	T_{DLY}	Variable Acquisition Time	3		4097	cycles[2]
Channel Measurement Time	T_{MEAS}	Fixed Hold Time	3			cycles[2]
Common-Mode Range	CMR	Non-attenuator channels	0		V_{DD}	V
		Attenuator On	-16.5		+16.5	V

[1] Change in current drain due to different module configurations is negligible.

[2] In AutoScan mode, switching time between channels is effectively zero. The time spent connected to a channel is (Acquisition Delay Time + Channel Measurement Time). The scan rate depends on the clocks: if the Master Clock = 500kHz, the Sampling Clock = 250kHz, thus 1 clock cycle = 4µs. Minimum Channel Measurement Time is then 3x4 = 12µs. Adding this to the minimum Connect-Time Delay (also 3x4µs) gives 24µs per channel.

Digital DC Characteristics

Unless otherwise specified, 4.5V < V_{DD} < 5.5V, T_A = 25°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Threshold	V_{IH}		2.0			V
Input Low Threshold	V_{IL}				0.8	V
Input Capacitance	C_{IN}	Digital Inputs			10	pF
Output Low Voltage	V_{OL}	I_{OL} = 3.2mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -2mA	2.4			V

4850429 0002434 T69

MODULE CHARACTERISTICS

Input Multiplexer Module (InpMux)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IN}	No Clock (e.g. Powered-Down)			1	nA
Input Capacitance	C_{IN}	Off-state			4	pF
Input Signal Ranges	V_{IN} (sig)	Channels 1- 4 (S) or 1-2 (D)	-16.5		+16.5	V
Attenuator On		Channels 5-16 (S) or 3-8 (D)	V_{SS}		V_{DD}	V
Input Signal Ranges	V_{IN} (sig)	Channels 1-16 (S) or 1-8 (D)	V_{SS}		V_{DD}	V
Attenuator Off						
Input Resistance	R_{IN}	Attenuator channel on		88		kΩ
Input Resistance	R_{IN}	Normal (5V) Channel	5	10		MΩ

Attenuator Module

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Absolute Attenuation Error	ε (att)	Attenuator channels on		0	1	%
Level-Shifter Voltage	V(2.857)	Attenuator channels on		2.857		V
Interchannel Mismatch	ΔV(ch)	Attenuator channels on		0	0.8	%

MuxCtrl Module

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Connection (Acquisition) Times	CT	Used in all software-triggered modes (ST command). Can be overridden by hardware trigger (RT pin).		12		µs
				20		µs
				36		µs
				68		µs
				260		µs
				1030		µs
				4100		µs
				16400		µs
Input-Sequence Lengths		Single-Ended Operation	8	or	16	channels
		Differential Operation	4	or	8	channels

4850429 0002435 9T5

Connectivity (ISource) Module

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Source Current	I_{SOURCE}	$V_I < V_{DD}$ - 0.5V	7.5	10	12.5	µA
Sink Current	I_{SINK}	$V_I > V_{SS}$ + 0.5V	7.5	10	12.5	µA
Output Resistance	R_{OUT}	V_{OUT} = 2.5V		5		MΩ

Low-Pass Filter Module

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Cutoff Frequency	f_C	INT CAP ON	13	15	17	kHz
		INT CAP OFF		845		kHz
Settling Time	t_{SETT}	5 time constants (99.3%)		53		µs
Resistor Value	R_{LPF}	To calculate RC filter; R_{SOURCE} =0		144		kΩ

InpAmp Module [Switched-Capacitor]

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Absolute Gain Error*	A_V (err)	V_{CM} =2.5V, any gain setting	-2		+2	%
Input Offset Voltage	V_{OS}	V_{CM} =2.5V, any gain setting	-5		+5	mV
Input Noise Spectral Density	e_N	f = 1kHz		0.5		$\mu V/\sqrt{Hz}$
Supply Rejection Ratio	PSRR			50		dB
Common-Mode Rej. Ratio	CMRR			55		dB

* IC is factory-calibrated for least error at gain=0.5

Comparator Module

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Time to STATUS reg. update	T_{STATUS}	From end of Connect Time			3	cycles[2]
Time to $\overline{\text{STATUS}}$ pin update	T_{LATCH}	From end of Connect Time			3	cycles[2]
Input Offset Voltage	V_{OS}				5	mV
Least Voltage Increment	LSB			10		mV
Full-Scale Comparison Voltage	V_{DAC}	255 steps @ 10mV each		2.55		V
Full-Scale Error	ΔV(FS)	Gain=0.5, Vin=4V			1	LSB
Trip-Point Error	ε(Comp)	Gain=0.5, Vin=4V			10	mV

[2] See footnote 2 under the General Electrical Characteristics table.

Note: Best accuracy is obtained by scaling inputs near 80% of full-scale, preferably with gain=0.5.

Reference Module (TRIM pin and RefBuffer Voltages) (see ***Figure 2***)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Internal Voltage Reference	V_{REF}	At TRIM pin.		2.42		V
TRIM Output Resistance	R_{TRIM}	At TRIM pin.		25		kΩ
Tempco	TC			30		ppm/°C
V_{REF} Output	V_{REFBUF}	At AuxAmp o/p, RefBuffer Mode	2.42	2.50	2.58	V
Output Resistance	R_{OUT}	At AuxAmp o/p, RefBuffer Mode			10	Ω

4850429 0002436 831

Magic-Probe Module

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Supply Current	I_Q (PROBE)			590	770	µA
Output Voltage Range	V(out)	I(out) = ±50µA	V_{SS} + 0.05		V_{DD} - 0.05	V
		I(out) = ±5mA	V_{SS} + 0.5		V_{DD} - 0.5	V
Gain	A_V (PROBE)			2.0		V/V
Gain Error	ε(PB)				1	%

Clock Module (frequency divider set to ÷1. It can also be set to ÷ f_{MSTR} by 2, 4 or 8)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Pin Output Frequency*	f_{MSTR}	High Speed or Low Speed Mode	460	500	540	kHz
Power Supply Sensitivity		V_{DD} ± 10%		1		kHz/V
Frequency Drift				350		Hz/°C
Waveform Rise Time	t_{RISE}	C_L = 50pF		25		ns
Waveform Fall Time	t_{FALL}	C_L = 50pF		10		ns

* Operation at Low Speed divides all internal times by 8. The output at the CLK pin in Master Mode does not change.

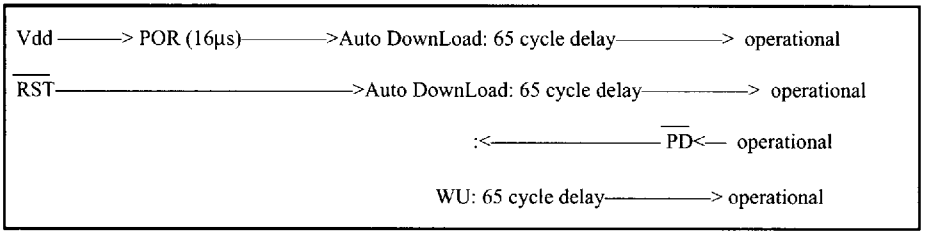
Power Module (see *Figure 9*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{POR}$ Detection Threshold	V_{POR}	V_{DD} trip voltage	1.5	2.5	4.0	V
$\overline{POR}$ Pulse Length	T_{POR}	Osc. on		16		µs
Wake-up Delay[1]	T_{WU}	After Auto-Download			66	cycles[2]

[1] Time does not include propagation delay through switched-capacitor modules or rise time for the LPF.

[2] See footnote 2 under the General Electrical Characteristics table.

Figure 9 Power Option Actions



Turn-on of Vdd is followed by a $\overline{POR}$ pulse and a download of the EEPROM data. Then, 65 Master clock cycles ensue, after which the chip is operational.

A Reset does the same, minus the $\overline{POR}$ pulse.

Power-down takes the chip into sleep mode immediately, but a Wake-Up command must go through the delay again.

4850429 0002437 778

AuxAmp (OpAmp) Module [Continuous Time]

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Supply Current	I_Q	Normal Mode		350	460	µA
		Turbo Mode		720	920	µA
Open-Loop Gain	A_{VOL}	Turbo OFF	82	88		dB
Unity-Gain Bandwidth	f_{UNITY}	Turbo ON, CL = 100pF		2		MHz
		Turbo OFF, CL = 100pF		1.4		MHz
Phase Margin		C_L = 100pF, Normal/Turbo		60		degrees
Input Offset Voltage	V_{OS}	Vcm = 2.5V	-7.5		+7.5	mV
Input Bias Current	I_B		-15		+15	nA
Input Voltage Noise	e_N	f = 10kHz		30		nV/√Hz
CM Range	V_{CM}		0		3. 5	V
Common-Mode Rej. Ratio	CMRR	At DC		60		dB
Supply Rejection Ratio	PSRR	At DC		74		dB
Output Voltage Range	V_{OUT}	RL =	V_{SS} + 0.05		V_{DD} - 0.05	V
Output Impedance	Z_{OUTPUT}	Normal mode		3		Ω
		Turbo mode		1		Ω
Output Current	I_{OUT}	Short Circuit		40		mA
Slew Rate	SR	Normal Mode, C_L = 100pF		1.5		V/µs
		Turbo Mode, C_L = 100pF		3		V/µs

SAR-ADC Module

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Accuracy	INL		-1	0	+1	LSB
	DNL		-1	0	+1	LSB
Resolution	ε(ADC)	Gain = 0.5		20		mV
		1		10		mV
		2		5		mV
		3		3.3		mV
		4		2.5		mV
		6		1.67		mV
		8		1.25		mV
		10		1		mV
Conversion Time	T_{CONV}	High or Low Speed Mode	17		18	cycles[1]

[1] See footnote 2 under the General Electrical Characteristics table.

Watchdog Module

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
WDO Timeout Period	T_{WD}	In High Speed Mode		8.1		ms
				65		ms
				520		ms
				1040		ms
		In Low Speed Mode		65		ms
				520		ms
				4160		ms
				8320		ms
WDI Pulse Width	t_{PW}		100			ns

4850429 0002438 604

Serial Programming for the IMP50E30

Description

The information needed for programming and control of the IMP50E30 is as follows:

- A block diagram of the information flow to, from, and within the device; this appears in the diagrams showing the A/D and Comparator configurations (***Figures 3*** and ***4***)
- A list of the device commands and their actions; see ***Table 1*** and its footnotes
- A bitstream table, that locates and defines all the configuration data; see ***Table 3***
- Timing information; see ***Table 3*** and ***Figure 10***
- Optional: Analog Magic facilities that greatly facilitate handling the above

Writing to (Programming of) the IMP50E30 is done via three pins, called $\overline{\text{SLI}}$ (Serial Load Input, the chip-select), SCLK (Serial CLocK), and SDI (Serial Data Input). In the initial programming phase (typically carried out using Analog Magic Software), the chip configuration and stored data values are decided upon and then downloaded to the non-volatile storage area, the EEPROM, or the volatile storage area, the SRAM (Note that this is not the only way to configure the SRAM).

Readback of data is done via the $\overline{\text{SLI}}$, SDO and SCLK. These pins combine for a simple interface that enables any µC to exercise the device in all of its measurement and diagnostic modes. Using this interface, the µC can also re-program the IMP50E30, on-the-fly, after installation.

All EPAC commands contain one or more 8-bit bytes. They can be commands only (RES, PD), commands that access 1-byte registers (RM, WM), or commands that access longer bitstreams. The first kind have the format 0000 cccc (c=cmd bit), and have no data bits attached. Those with format 0001 cccc that access longer bitstreams have a format that begins with the command (1 byte), followed by a length specifier (1 byte), followed by the number of bytes so specified. *Each part of a command is shifted LSB first.*

Table 1 Device Commands

COMMAND BYTE (MSB..LSB)	COMMAND NAME	FUNCTION	BYTE FORMAT (MSB..LSB)		
0001 0001	WCR	Write the following data to the Configuration register.	24 data bytes	24	Cmd
0001 0010	WCH	Write the following data to the Channel Register.	1 data byte	1	Cmd
0001 0011	WEE	Write the following data to the EEPROM.	24 data bytes*	24*	Cmd
0001 0100	WSP	Write the following data to the Software Probe ("MagicProbe").	1 data byte	1	Cmd
0001 1011	WM	Write the following data to the 8-bit Mode Register.	1 data byte	1	Cmd
0001 0101	REE	Read the contents of the EEPROM.	24 data bytes*	24*	Cmd
0001 0111	RCR	Read the contents of the Configuration Register.	24 data bytes	24	Cmd
0001 0110	RSAR	Read the contents of the 8-bit SAR[1]	1 data byte	1	Cmd
0001 1000	RS	Read the contents of the 8-bit Status Register.	1 data byte	1	Cmd
0001 1100	RM	Read the contents of the 8-bit Mode Register.	1 data byte	1	Cmd
0000 0001	BP	Bypass (Ignore following data & set SLO Low. For cascaded EPACs).	----------	-----	Cmd
0000 0010	RES	Reset and re-download from the EEPROM to the SRAMs.	----------	-----	Cmd
0000 0011	PD	Power Down.	----------	-----	Cmd
0000 0101	WU	Wake Up (from Power Down).	----------	-----	Cmd
0000 1010	ST	Soft(ware) Trigger in Comp Modes: STart conversion in A/D Mode[2].	----------	-----	Cmd

* Can be up to 31 bytes. See end of ***Table 2***.

[1] Successive-Approximation Register

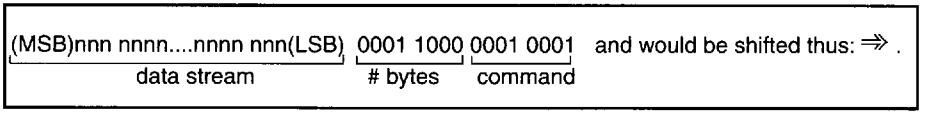
[2] To use ST (software command), ground the RT pin

4850429 0002439 540

A command such as WCR would be assembled as shown in ***Figure 10A***.

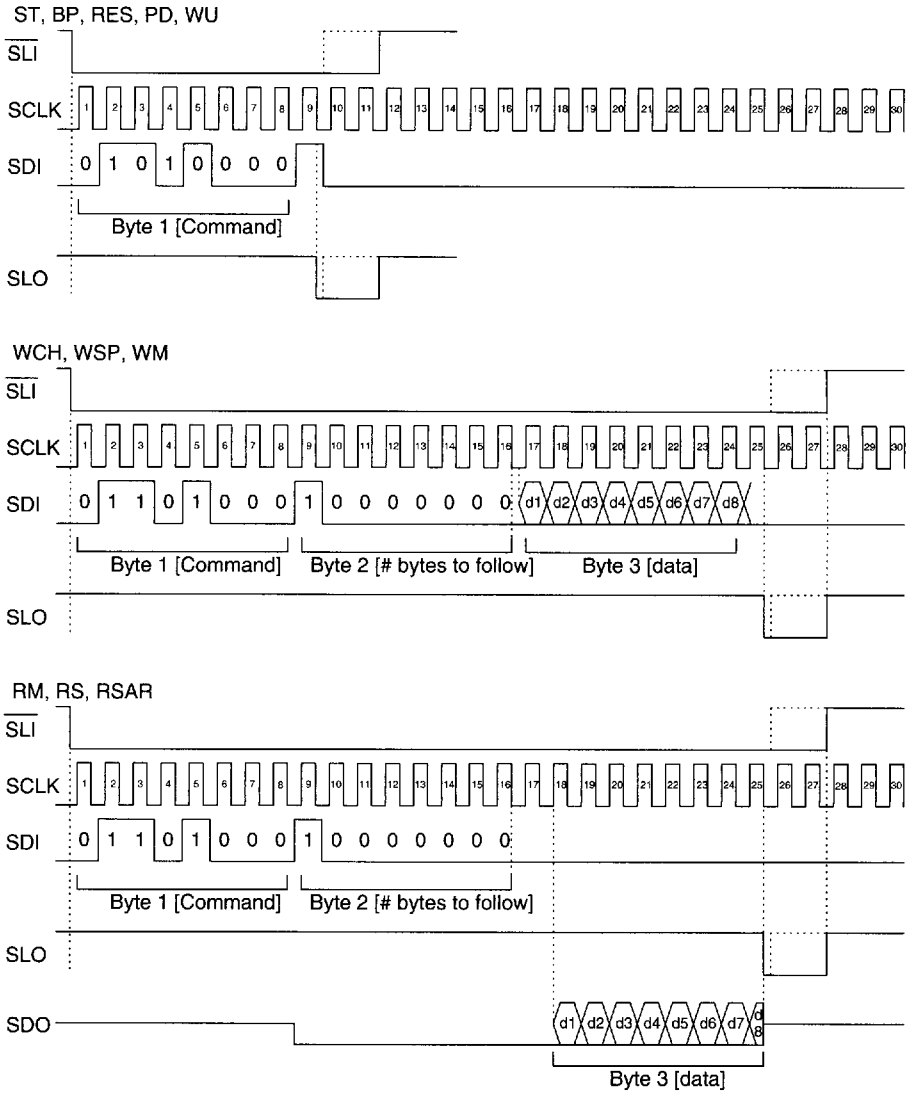
NOTE: This command and ***Table 1*** have bytes in conventional written order, left-to-right. This results in a byte format (***Figure 10A***), that must be **shifted to the right** in order that each byte have its LSB shifted first. The Bit Pattern Timing Diagrams have the opposite convention: they exhibit clocks that progress from left to right, resulting in all bytes being written LSB..MSB, and **shifting to the left.** An example of a command bit pattern is shown in ***Figure 10B.***

Figure 10A Command Line Format



4850429 0002440 262

Figure 10B Examples of Command Bit Pattern Timing [shift direction is ⇦LSB.....MSB]



1) All commands require three (3) extra clocks. The first is needed to make SLO go low (↓). It always comes after a byte boundary (8+1 bits, 24+1 bits, etc.)
2) We then take $\overline{\text{SLI}}$ HIGH (↑). The earliest that this can be done is shown as a dotted line.
3) When this happens, two (2) extra clocks are needed to latch the data (if a write command) or set the latch (if a Read command).
4) The only exception is the WEE command. AFter its 24 bytes have been issued, an extra byte (8 clocks) is required, followed by the three extra clocks, as above, for a total for eleven (11) extra clocks.
5) Extra clocks in excess of the final two clocks are OK.
6) When reading data out (RS, RM, RSAR, RCR), there is a one-clock delay before data appears on the SDO line.
7) The 8th data bit is not valid after the falling edge of the clock.

4850429 0002441 1T9

Table 2A Channel-Address Register Bits

Addressed with WCH command (Write to CHannelSelect Register).
These are NOT in the EEPROM bitstream.

Absolute Byte # 1=first in	Absolute Bit # 1=first in	Module Name	Bit Function	Definition
1	1	Multiplexer		don't care
1	2	("MUX")		don't care
1	3			don't care
1	4			don't care
1	5		ChanAddr0	Channel LSB (SE mode: ignore in Diff mode)
1	6		ChanAddr1	Channel (LSB when in Differential mode)
1	7		ChanAddr2	Channel
1	8		ChanAddr3	Channel MSB

Table 2B Status Register Bits
Addressed with RS command, Read Status (Register).
These are NOT in the EEPROM bitstream.

Bit	Name	Description
1	CHaddr0	Channel address (LSB)
2	CHaddr1	Channel address
3	CHaddr2	Channel address
4	CHaddr3	Channel address (MSB)
5	COMP_LO	Comp LOW output (1= trip)
6	COMP_HI	Comp HIGH output (1= trip)
7	INTERRUPT	Scan aborted flag (1= halt)
8	BUSY/$\overline{EOC}$	Sequencer/SAR active ($\overline{EOC}$/Busy)

4850429 0002442 035

Table 3 EEPROM and Configuration Register (CR) Bitstream
Addressed with REE, RCR (both Read) and WEE, WCR (both Write) commands.

In ***Table 3,*** Groups are abbreviated as "Grp".

Abs. Byte 1= first in	Abs. #Bit # 1= first in	Module Name	Bit Function	Definition	
1	1	Security	Block Readback	1=locked, 0=open (readback ok) 1st bit of CR	
1	2		ID Code	50e30 ID code, LSB, "1"	(Issue SR cmd before
1	3		ID Code	50e30 ID code, "1"	readback of ID)
1	4		ID Code	50e30 ID code, "0"	
1	5		ID Code	50e30 ID code, MSB, "1"	
1	6		User Tag	User Space	
1	7	Attenuator	5V or 16.5V	0=±16.5V, 1=5.0V	
1	8		5V or 16.5V	0=±16.5V, 1=5.0V	
2	9		5V or 16.5V	0=±16.5V, 1=5.0V	
2	10		5V or 16.5V	0=±16.5V, 1=5.0V	
2	11	Filter	FilGrp0	0=Filter Off, 1=FilterOn	
2	12		FilGrp1	0=Filter Off, 1=FilterOn	
2	13		FilGrp2	0=Filter Off, 1=FilterOn	
2	14		FilGrp3	0=Filter Off, 1=FilterOn	
2	15		FilGrp4	0=Filter Off, 1=FilterOn	
2	16		FilGrp5	0=Filter Off, 1=FilterOn	
3	17		FilGrp6	0=Filter Off, 1=FilterOn	
3	18		FilGrp7	0=Filter Off, 1=FilterOn	
3	19		ExtCap	0=Filter Off, 1=FilterOn	(affects all Groups)
3	20	InpAmp	GainGrp1	Gain, LSB, Grp1	Grp1=Ch1 and Ch2,
3	21			Gain,	SE mode, or Ch1,
3	22			Gain, MSB	DIfferential mode
3	23		GainGrp2	Gain, LSB, Grp2	Grp2=Ch3 and Ch4,
3	24			Gain,	SE mode, or Ch2,
4	25			Gain, MSB	DIfferential mode
4	26		GainGrp3	Gain, LSB, Grp3	Grp3=Ch5 and Ch6,
4	27			Gain,	SE mode, or Ch3,
4	28			Gain, MSB	DIfferential mode
4	29		GainGrp4	Gain, LSB, Grp4	Grp4=Ch7 and Ch8,
4	30			Gain,	SE mode, or Ch4,
4	31			Gain, MSB	DIfferential mode
4	32		GainGrp5	Gain, LSB, Grp5	Grp5=Ch9 and Ch10,
5	33			Gain,	SE mode, or Ch5,
5	34			Gain, MSB	DIfferential mode
5	35		GainGrp6	Gain, LSB, Grp6	Grp6=Ch11 and Ch12,
5	36			Gain,	SE mode, or Ch6,
5	37			Gain, MSB	DIfferential mode
5	38		GainGrp7	Gain, LSB, Grp7	Grp7=Ch13 and Ch14,
5	39			Gain,	SE mode, or Ch7,
5	40			Gain, MSB	DIfferential mode
6	41		GainGrp8	Gain, LSB, Grp8	Grp8=Ch15 and Ch16,
6	42			Gain,	SE mode, or Ch8,
6	43			Gain, MSB	DIfferential mode
6	44	DAC	Lo_Grp1	Low Threshold, LSB	
6	45			Low Threshold	
6	46			Low Threshold	
6	47			Low Threshold	

4850429 0002443 T71

6	48			Low Threshold	
7	49			Low Threshold	
7	50			Low Threshold	
7	51			Low Threshold, MSB	
7	52		Hi_Grp1	High Threshold, LSB	WinComp mode only
7	53			High Threshold	WinComp mode only
7	54			High Threshold	WinComp mode only
7	55			High Threshold	WinComp mode only
7	56			High Threshold	WinComp mode only
8	57			High Threshold	WinComp mode only
8	58			High Threshold	WinComp mode only
8	59			High Threshold, MSB	WinComp mode only
8	60	DAC	Lo_Grp2	Low Threshold, LSB	
8	61			Low Threshold	
8	62			Low Threshold	
8	63			Low Threshold	
8	64			Low Threshold	
9	65			Low Threshold	
9	66			Low Threshold	
9	67			Low Threshold, MSB	
9	68		Hi_Grp2	High Threshold, LSB	WinComp mode only
9	69			High Threshold	WinComp mode only
9	70			High Threshold	WinComp mode only
9	71			High Threshold	WinComp mode only
9	72			High Threshold	WinComp mode only
10	73			High Threshold	WinComp mode only
10	74			High Threshold	WinComp mode only
10	75			High Threshold, MSB	WinComp mode only
10	76	DAC	Lo_Grp3	Low Threshold, LSB	
10	77			Low Threshold	
10	78			Low Threshold	
10	79			Low Threshold	
10	80			Low Threshold	
11	81			Low Threshold	
11	82			Low Threshold	
11	83			Low Threshold, MSB	
11	84		Hi_Grp3	High Threshold, LSB	WinComp mode only
11	85			High Threshold	WinComp mode only
11	86			High Threshold	WinComp mode only
11	87			High Threshold	WinComp mode only
11	88			High Threshold	WinComp mode only
12	89			High Threshold	WinComp mode only
12	90			High Threshold	WinComp mode only
12	91			High Threshold, MSB	WinComp mode only
12	92	DAC	Lo_Grp4	Low Threshold, LSB	
12	93			Low Threshold	
12	94			Low Threshold	
12	95			Low Threshold	
12	96			Low Threshold	
13	97			Low Threshold	
13	98			Low Threshold	
13	99			Low Threshold, MSB	
13	100		Hi_Grp4	High Threshold, LSB	WinComp mode only
13	101			High Threshold	WinComp mode only
13	102			High Threshold	WinComp mode only
13	103			High Threshold	WinComp mode only
13	104			High Threshold	WinComp mode only
14	105			High Threshold	WinComp mode only

4850429 0002444 908

14	106			High Threshold	WinComp mode only
14	107			High Threshold, MSB	WinComp mode only
14	108	DAC	Lo_Grp5	Low Threshold, LSB	
14	109			Low Threshold	
14	110			Low Threshold	
14	111			Low Threshold	
14	112			Low Threshold	
15	113			Low Threshold	
15	114			Low Threshold	
15	115			Low Threshold, MSB	
15	116		HiGrp5	High Threshold, LSB	WinComp mode only
15	117			High Threshold	WinComp mode only
15	118			High Threshold	WinComp mode only
15	119			High Threshold	WinComp mode only
15	120			High Threshold	WinComp mode only
16	121			High Threshold	WinComp mode only
16	122			High Threshold	WinComp mode only
16	123			High Threshold, MSB	WinComp mode only
16	124	DAC	Lo_Grp6	Low Threshold, LSB	
16	125			Low Threshold	
16	126			Low Threshold	
16	127			Low Threshold	
16	128			Low Threshold	
17	129			Low Threshold	
17	130			Low Threshold	
17	131			Low Threshold, MSB	
17	132		HiGrp6	High Threshold, LSB	WinComp mode only
17	133			High Threshold	WinComp mode only
17	134			High Threshold	WinComp mode only
17	135			High Threshold	WinComp mode only
17	136			High Threshold	WinComp mode only
18	137			High Threshold	WinComp mode only
18	138			High Threshold	WinComp mode only
18	139			High Threshold, MSB	WinComp mode only
18	140	DAC	Lo_Grp7	Low Threshold, LSB	
18	141			Low Threshold	
18	142			Low Threshold	
18	143			Low Threshold	
18	144			Low Threshold	
19	145			Low Threshold	
19	146			Low Threshold	
19	147			Low Threshold, MSB	
19	148		Hi_Grp7	High Threshold, LSB	WinComp mode only
19	149			High Threshold	WinComp mode only
19	150			High Threshold	WinComp mode only
19	151			High Threshold	WinComp mode only
19	152			High Threshold	WinComp mode only
20	153			High Threshold	WinComp mode only
20	154			High Threshold	WinComp mode only
20	155			High Threshold, MSB	WinComp mode only
20	156	DAC	Lo_Grp8	Low Threshold, LSB	
20	157			Low Threshold	
20	158			Low Threshold	
20	159			Low Threshold	
20	160			Low Threshold	
21	161			Low Threshold	
21	162			Low Threshold	

4850429 0002445 844

21	163			Low Threshold, MSB	
21	164		Hi_Grp8	High Threshold, LSB	WinComp mode only
21	165			High Threshold	WinComp mode only
21	166			High Threshold	WinComp mode only
21	167			High Threshold	WinComp mode only
21	168			High Threshold	WinComp mode only
22	169			High Threshold	WinComp mode only
22	170			High Threshold	WinComp mode only
22	171			High Threshold, MSB	WinComp mode only
22	172	Clock	Divider	Divider, LSB	
22	173		Divider	Divider, MSB	
22	174		MastrSlave	0=Master, 1=Slave	
22	175		LowSpeed	0=High Speed, 1=Low Speed	
22	176	AuxAmp	RefBuf	0=disconnected, 1=connected	
23	177		Turbo	0=Off, 1=On	
23	178		PD	0=Off, 1=On	
23	179	WatchDog	Enable	0=Inactive, 1=Active	
23	180		WDO	Timer, LSB	
23	181		WDI	Timer, MSB	
23	182	CompCtrl	High-Trip	Alarm: 0=Lo, 1=Hi	
23	183		Win/Lvl	0=Level, 1=Window	
23	184	MuxCtrl	SeqLength	0=full (16S/8D), 1=half (8S/4D)	
24	185		TrigMode	0=Single-Step, 1=FreeRun	(ModeRegBit1)
24	186		Advance	0=Off, 1=On	(ModeRegBit2)
24	187	CnctTimer	Delay0	Divider, LSB	(ModeRegBit3)
24	188		Delay1	Divider	(ModeRegBit4)
24	189		Delay2	Divider, MSB	(ModeRegBit5)
24	190	SARMode	SAR/Comp	0=Comp, 1=ADC (=SAR)	(ModeRegBit6)
24	191	InpMux	Single/Diff	0=Single-Ended, 1=Differential	(ModeRegBit7)
24	192	Connectivity	ISource	0=Off, 1=On	(ModeRegBit8)
25 - 31	**193- 248**	**UNUSED BITS**		**User ScratchPad Area**	**EEPROM Only**

The command bits for MagicProbe (***Table 4A***) are addressed with the WSP ("Write to Software Probe") command. These bits are NOT in the EEPROM bitstream. Internal signals existing at the locations listed (see ***Table 4B***) may be read via the PROBE output pin.

Table 4A Function/Location of Command Bits for MagicProbe

Abs. Byte # 1=first in	Abs. Bit # 1=first in	Relative Bit #	Module Name	Bit Function	Definition
1	1	1	Probe	DriveCap	Turbo: 0 = Off, 1 = On
1	2	2		OutpZero	0 = Vss, 1= 2.5V
1	3	3		Filter	0 = Off, 1= On
1	4	4		AnaProbe	Analog Probe: 0 = Off, 1= On
1	5	5		DigProbe	Digital Probe: 0 = Off, 1= On
1	6	6		Hwy1	Address LSB (see Table 4b)
1	7	7		Hwy2	Address (see Table 4b)
1	8	8		Hwy3	Address MSB (see Table 4b)

4850429 0002446 780

Table 4B Highway Addresses and Function Bits for MagicProbe

Relative	Hwy Address			Signals Probed			
Bit #	Hwy3	Hwy2	Hwy1	Digital	Comment	Analog	Comment
1	0	0	0	SDO	Serial Data Out	n/c	
2	0	0	1	Ph1	CLK Phase1	InpAmp	Output of InpAmp
3	0	1	0	Ph2	CLK Phase2	DAC	DAC Output
4	0	1	1	Comp	Comparator Output	Cext	Ca/Cb pins on LPF
5	1	0	0	$\overline{PD}$	Power Down	3.78V	Internal Cal. Voltage
6	1	0	1	Busy/$\overline{EOC}$	Seq/SAR busy signal	2.58V	Internal Cal. Voltage
7	1	1	0	ConnectTime	Timer Delay signal	2.857V	Internal Cal. Voltage
8	1	1	1	StartofCnct	InpAmp HOLD signal	2.50V	Internal Cal. Voltage

Figure 11 Timing Diagram for the Serial Interface

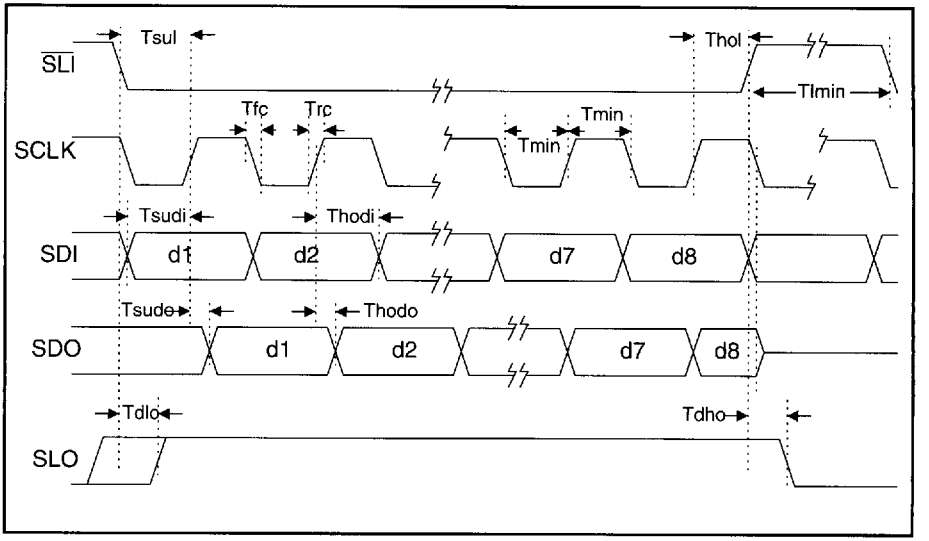
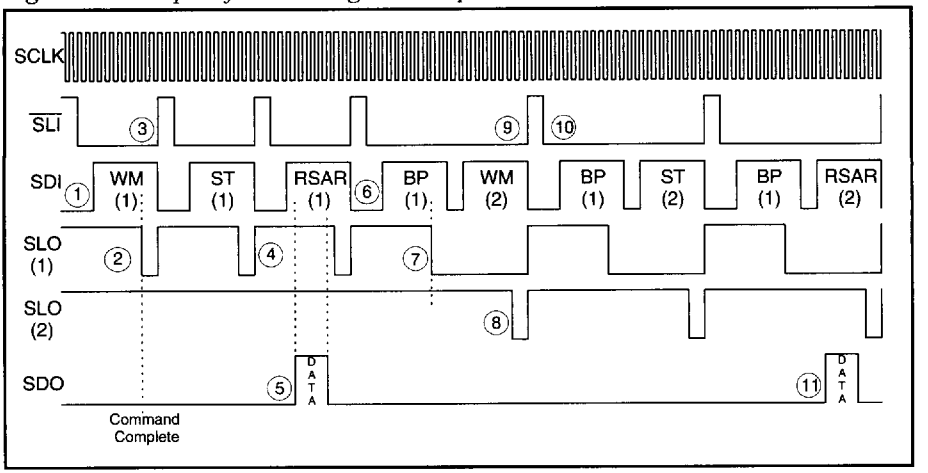


Table 5 Timing Specifications for the Serial Interface

Parameter	Conditions	MIN	MAX	UNITS
Tsul	$\overline{SLI}$ setup time to SCLK	50		ns
Thol	$\overline{SLI}$ hold time after SCLK	50		ns
Trc	SCLK rise time		500	ns
Tfc	SCLK fall time		500	ns
Tmin	SCLK HIGH time and LOW time when shifted into SR	100		ns
Tsud	SDI setup time to SCLK	50		ns
Thod	SDI hold time after SCLK	50		ns
Tlmin	$\overline{SLI}$ HIGH time	100		ns
Tsudo	SDO setup time after SCLK		50	ns
Thodo	SDO hold time after SCLK (data bits 1-7)	50		ns
Tdlo	$\overline{SLI}$ LOW to SLO HIGH		20	ns
Tdho	$\overline{SLI}$ HIGH to SLO LOW		20	ns

Figure 12 Example of Addressing Two Chips in Cascade.



1. After $\overline{SLI}\downarrow$, command (Write Mode) can be issued to chip(1).
2. When command is complete, SLO(1)$\downarrow$. [Including 1 extra clock; see Figure 10B]
3. When $\overline{SLI}\uparrow$, command ends, causing SLO(1)$\uparrow$. [Including 2 extra clocks; see Figure 10B]
4. After next command is completed, $\overline{SLI}$ and SLO(1)$\uparrow$ again.
5. After RSAR command begins, data is clocked out on SDO, and ends when command completes.
6. To command chip(2), $\overline{SLI}\downarrow$ again, but now we issue the Bypass command (BP1) for chip (1). Any additional commands will now not affect chip(1), but *will* affect chip(2) if we enable it. Note that SLO(1) = $\overline{SLI}$(2).
7. When BP1 completes, SLO(1)$\downarrow$, enabling chip(2). We now issue the Write Mode command to chip(2).
8. When WM(2) completes, SLO(2)$\downarrow$.
9. Then $\overline{SLI}\uparrow$, ending the WM command and deselecting chip(2).
10. The same pattern is repeated for the ST(2) command.
11. For the RSAR command, data is again clocked out on SDO.

4850429 0002448 553

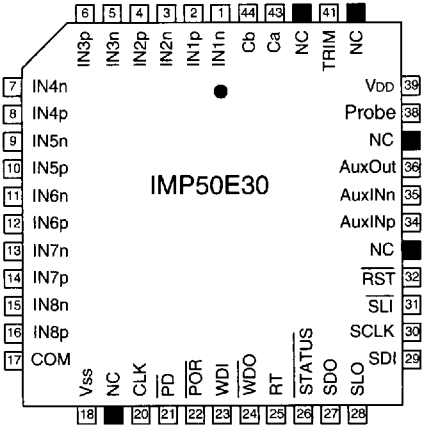
Table 6 Pin Descriptions

The following table provides a list of the pin names, the type of pin (P)ower, (D)igital, or (A)nalog, and a description of the pin function(s).

PIN #	Name	Type	Description
1	IN1n	A	Analog inputs to multiplexer.
2	IN1p	A	
3	IN2n	A	
4	IN2p	A	Configurable as 16 single-ended inputs or 8 differential inputs.
5	IN3n	A	Pins 1-4 can be selected to accept inputs up to ±16.5V; this
6	IN3p	A	High-Voltage mode puts an attenuator (÷8) in front of the Mux
7	IN4n	A	for single-channels 1-4 or differential channels 1 and 2.
8	IN4p	A	
9	IN5n	A	
10	IN5p	A	
11	IN6n	A	
12	IN6p	A	
13	IN7n	A	
14	IN7p	A	
15	IN8n	A	
16	IN8p	A	
17	COM	A	"Ground", "Common" or "Zero-Reference" Input. Connect to Vss (usually) or to the source's ground, if it is remote.
18	VSS	P	Negative Power Supply (0V).
19	NC		
20	CLK	D	In Master Mode, output of internal clock, divided by 1, 2, 4 or 8. In Slave mode, CLK input to timing logic.
21	$\overline{PD}$	P	Input. Chip active if HIGH, in sleep mode when LOW. Tie HIGH if unused.
22	POR	P	Power-On-Reset. At power-on, outputs LOW for ~16µs, then HIGH (resets µC, etc.)
23	WDI	D	Watchdog Timer Input. Times out unless reset. Tie LOW if unused.
24	$\overline{WDO}$	D	Flag Output. HIGH if µC is OK. Outputs a LOW-going pulse if it times out.
25	RT	D	Run/Trigger Input. In single-step modes, connects a channel for a comparison, or an A/D conversion. In free-running mode, starts or stops the channel scan. Tie LOW if triggering via the serial interface.
26	$\overline{STATUS}$	D	Flag output (interrupt) for failed comparisons, or EOC output for A/D conversions.
27	SDO	D	Serial Data Output. For readback.
28	SLO	D	Serial Load Output. Flag output that current command has been executed.
29	SDI	D	Serial Data Input. "0"=LOW. Data sampled on SCLK LOW-to-HIGH.
30	SCLK	D	Serial Interface Clock. For shifting-in EPAC program data.
31	$\overline{SLI}$	D	Serial Load Input. Chip-Select for Serial Interface. Data is shifted into registers while $\overline{SLI}$ is LOW, and latched when $\overline{SLI}$ goes HIGH.
32	$\overline{RST}$	D	Input. Resets the IC and causes a download of the EEPROM to the SRAMs. Tie HIGH if unused.
33	NC		
34	AuxINp	A	Non-inverting input of Auxiliary Amplifier.
35	AuxINn	A	Inverting input of Auxiliary Amplifier.
36	AuxOut	A	Output of Auxiliary Amplifier and Buffered Vref Output.
37	NC		
38	Probe	A/D	Probe Output. Internal analog or digital signals can be routed to this test pin.
39	V_{DD}	P	Positive Power Supply (+5V).
40	NC		
41	Trim	A	Used to alter Vref. This affects all DACs, the attenuator channels and the Vref Buffer output.
42	NC		
43	Ca	A	Input for external C for reducing LPF corner frequency. Hi-Impedance when unused.
44	Cb	A	Input for external C for reducing LPF corner frequency. Hi-Impedance when unused.

NC = No Internal Connection

Pin Assignments



Ordering Information	Package	Temperature Range
IMP50E30C-018AC	44-pin PLCC	0°C to 70°C

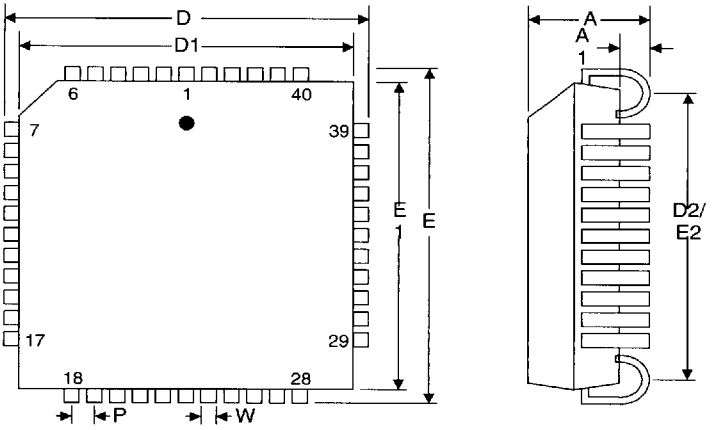
4850429 0002450 101

44-Pin Plastic LCC Package

Package Description

44-pin Plastic Leaded Chip Carrier
JEDEC Part Number MS-018AC

Package Outline



Description	Symbol	Min. (in./mm)	Max. (in./mm)
Height	A	0.165/4.19	0.180/4.57
Standoff	A1	0.020/0.51	——
Width/Length (incl. pins)	D,E	0.685/17.40	0.695/17.65
Width/Length (pkg. only)	D1,E1	0.650/16.51	0.656/16.66
Footprint	D2,E2	0.590/14.99	0.630/16.00
Pin Width	W	0.013/0.33	0.021/0.53
Pin Spacing	P	0.050/1.27	(nominal)

4850429 0002451 048