NTMFS4709N

Power MOSFET

30 V, 94 A, Single N−Channel, SOIC−8 FL

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- These are Pb−Free Devices

Applications

- VCORE Applications
- DC−DC Converters
- Low Side Switching

MAXIMUM RATINGS (T_J=25°C unless otherwise stated)

Rating			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	30	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	T_A = 25°C	I_D	18	A
		T_A = 85°C		13	
Power Dissipation $R_{\theta JA}$ (Note 1)		T_A = 25°C	P_D	2.35	W
Continuous Drain Current $R_{\theta JA}$ (Note 2)		T_A = 25°C	I_D	11	A
		T_A = 85°C		8.0	
Power Dissipation $R_{\theta JA}$ (Note 2)		T_A = 25°C	P_D	0.91	W
Continuous Drain Current $R_{\theta JC}$ (Note 1)		T_C = 25°C	I_D	94	A
		T_C = 85°C		68	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	62.5	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	140	A
Current limited by package	T_A = 25°C		$I_{DmaxPkg}$	140	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to +150	°C
Source Current (Body Diode)			I_S	62.5	A
Drain to Source			dV/dt	10	V/ns
Single Pulse Drain−to−Source Avalanche Energy T_J = 25°C, V_{DD} = 50 V, V_{GS} = 10 V, I_L = 30 A_{pk}, L = 1.0 mH, R_G = 25 Ω			E_{AS}	450	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

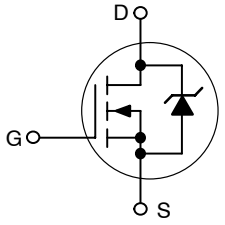
1. Surface−mounted on FR4 board using 1 sq−in pad, 1 oz Cu.
2. Surface−mounted on FR4 board using the minimum recommended pad size.

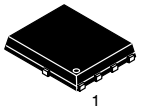
ON Semiconductor®

http://onsemi.com

$V_{(BR)DSS}$	$R_{DS(on)}$ Typ	I_D Max
30 V	2.85 mΩ @ 10 V	94 A
	4.0 mΩ @ 4.5 V	

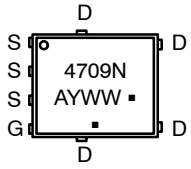
N−Channel





SOIC−8 FLAT LEAD
CASE 488AA
STYLE 1

MARKING DIAGRAM & PIN ASSIGNMENT



4709N = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4709NT1G	SOIC−8 FL (Pb−Free)	1500 / Tape & Reel
NTMFS4709NT3G	SOIC−8 FL (Pb−Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL RESISTANCE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Junction−to−Case (Drain)	$R_{\theta JC}$	2.0	°C/W
Junction−to−Ambient − Steady State (Note 3)	$R_{\theta JA}$	53.2	
Junction−to−Ambient − Steady State (Note 4)	$R_{\theta JA}$	137.8	

3. Surface−mounted on FR4 board using 1 sq in pad, 1 oz Cu.
4. Surface−mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		30			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				5.6		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 24 V	T_J = 25°C			1.0	μA
			T_J = 125°C			10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, ID = 250 μA		1.0		3.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				5.6		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 11.5 V	I_D = 30 A		2.8		mΩ
			I_D = 15 A		2.8		
		V_{GS} = 10 V	I_D = 30 A		2.85	3.6	
		V_{GS} = 4.5 V	I_D = 30 A		4.0	5.5	
			I_D = 15 A		4.0		
Forward Transconductance	g_{FS}	V_{DS} = 15 V, I_D = 15 A			41		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 12 V			2370		pF
Output Capacitance	C_{OSS}				1240		
Reverse Transfer Capacitance	C_{RSS}				305		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 15 V; I_D = 30 A			20		nC
Threshold Gate Charge	$Q_{G(TH)}$				2.4		
Gate−to−Source Charge	Q_{GS}				4.5		
Gate−to−Drain Charge	Q_{GD}				11		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 11.5 V, V_{DS} = 15 V; I_D = 30 A			48		nC
Threshold Gate Charge	$Q_{G(TH)}$				4.0		
Gate−to−Source Charge	Q_{GS}				6.5		
Gate−to−Drain Charge	Q_{GD}				10.6		
SWITCHING CHARACTERISTICS (Note 6)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 30 A, R_G = 3.0 Ω			16		ns
Rise Time	t_r				173		
Turn−Off Delay Time	$t_{d(OFF)}$				20		
Fall Time	t_f				105		

5. Pulse Test: pulse width ±300 μs, duty cycle ±2%
6. Switching characteristics are independent of operating junction temperatures.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (Note 6)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 11.5 V, V_{DS} = 15 V, I_D = 30 A, R_G = 3.0 Ω			8.5		ns
Rise Time	t_r				87		
Turn−Off Delay Time	$t_{d(OFF)}$				31.5		
Fall Time	t_f				8.5		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 20 A	T_J = 25°C		0.75	1.0	V
		V_{GS} = 0 V, I_S = 50 A	T_J = 25°C		0.85		
		V_{GS} = 0 V, I_S = 20 A	T_J = 125°C		0.7		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, d_{IS}/d_t = 100 A/μs, I_S = 25 A			48		ns
Charge Time	t_a				23		
Discharge Time	t_b				25		
Reverse Recovery Charge	Q_{RR}				55		nC
Package Parasitic Values							
Gate Resistance	R_G	T_A = 25°C			0.65		Ω

5. Pulse Test: pulse width ±300 μs, duty cycle ±2%
6. Switching characteristics are independent of operating junction temperatures.

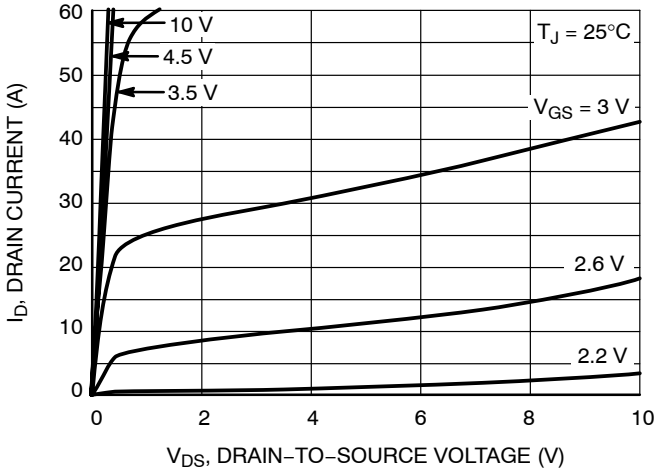


Figure 1. On−Region Characteristics

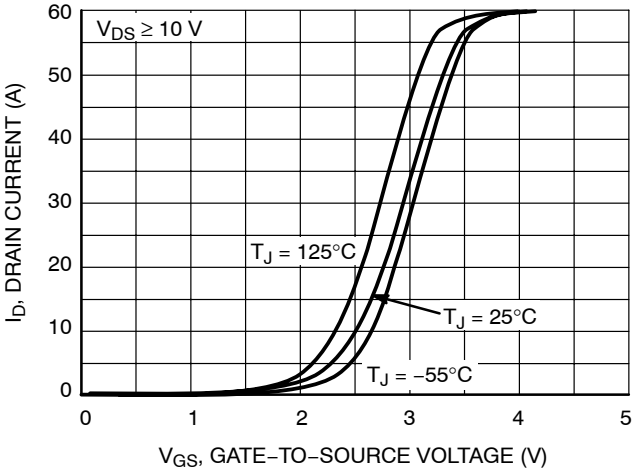


Figure 2. Transfer Characteristics

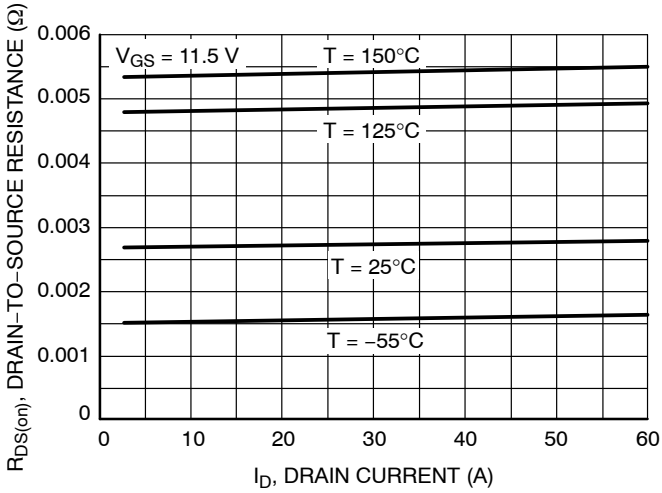


Figure 3. On−Resistance versus Drain Current and Temperature

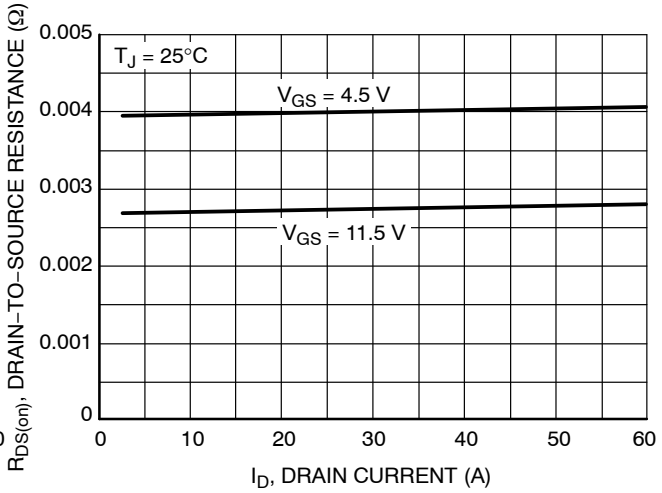


Figure 4. On−Resistance versus Drain Current and Gate Voltage

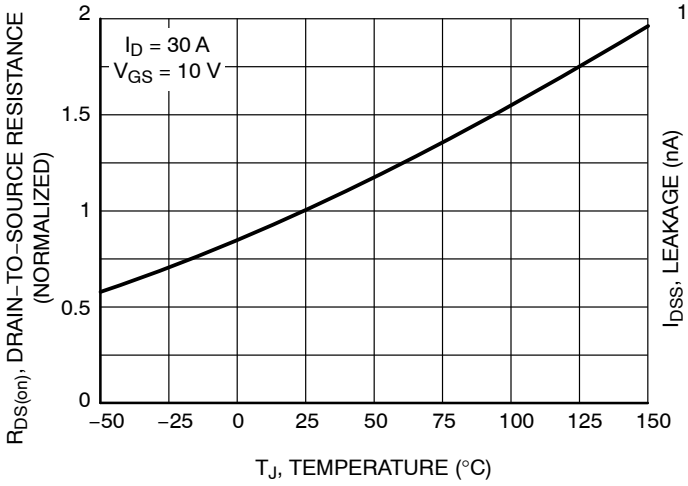


Figure 5. On−Resistance Variation with Temperature

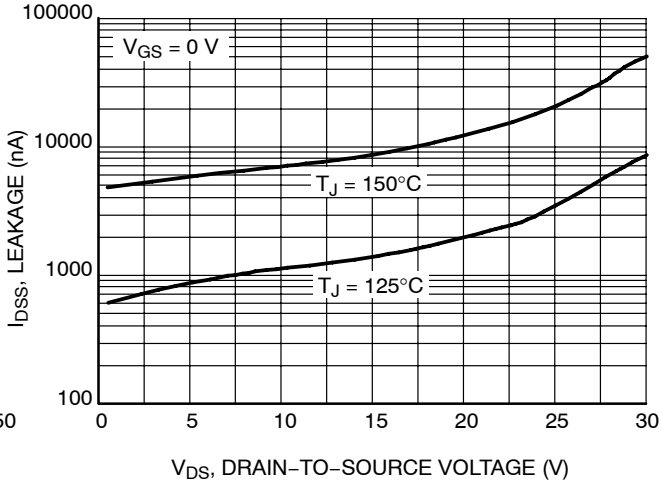


Figure 6. Drain−to−Source Leakage Current versus Voltage

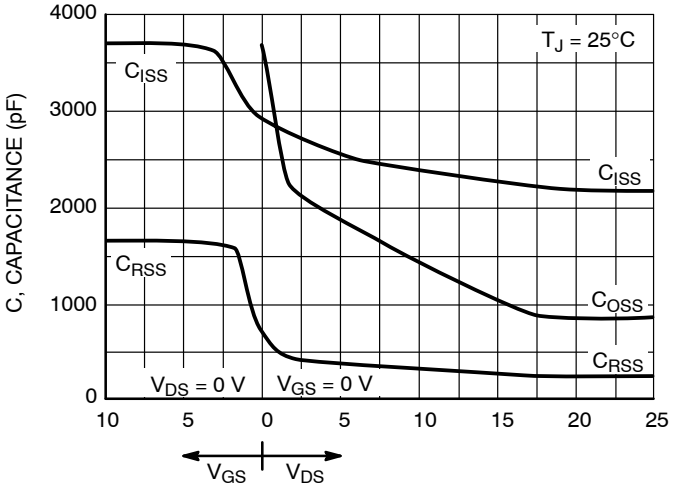


Figure 7. Capacitance Variation

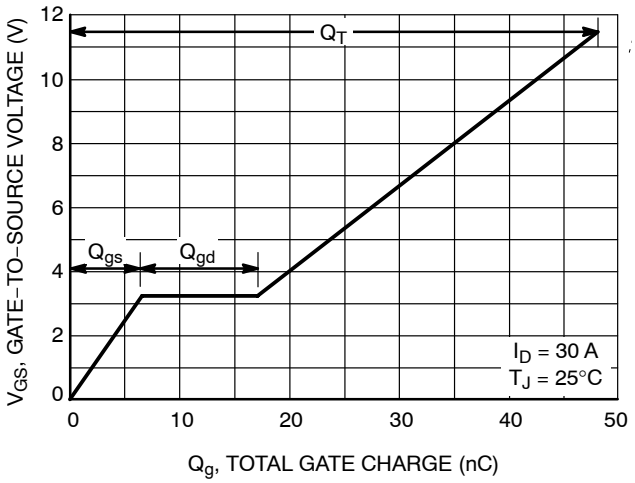


Figure 8. Gate−to−Source and Drain−to−Source Voltage versus Total Charge

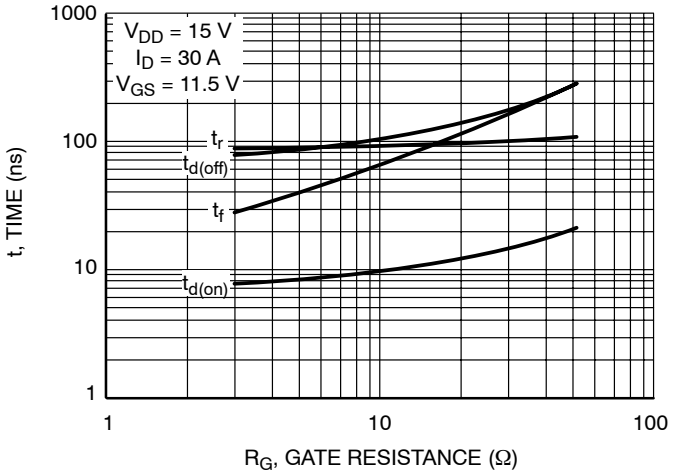


Figure 9. Resistive Switching Time Variation versus Gate Resistance

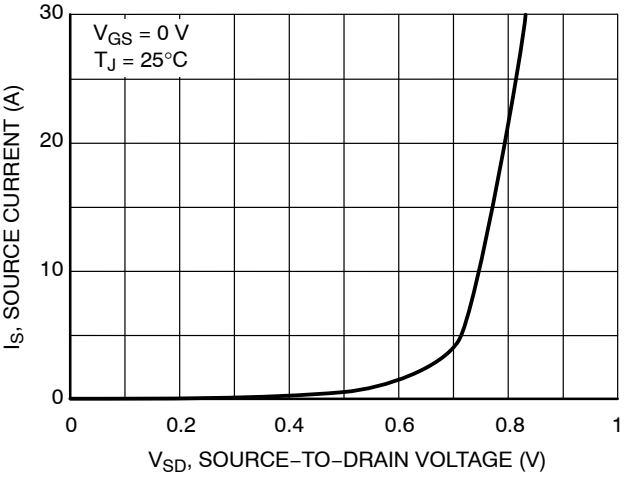


Figure 10. Diode Forward Voltage versus Current

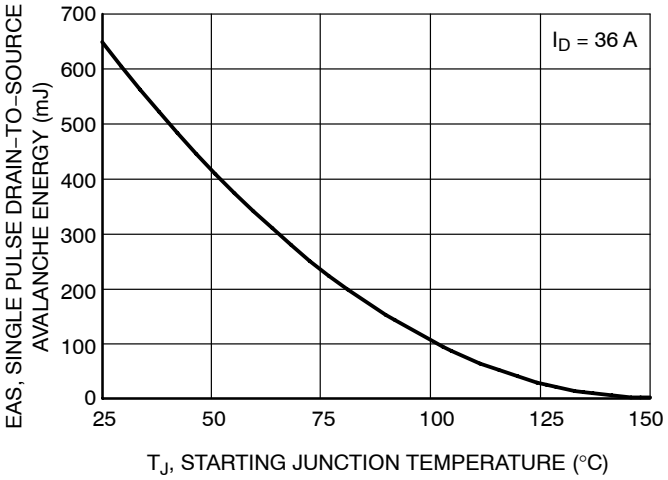
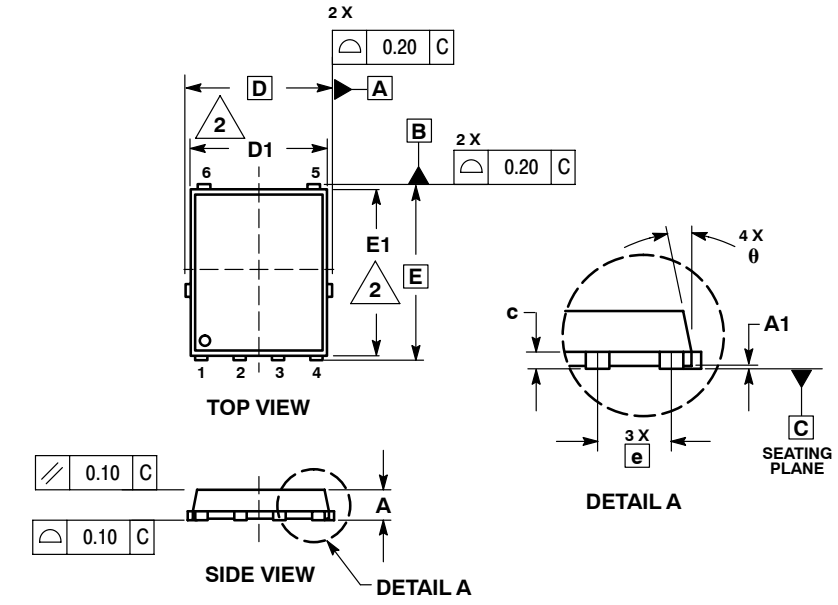
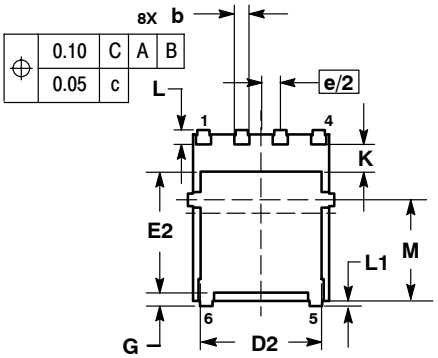


Figure 11. Maximum Avalanche Energy versus Starting Junction Temperature

PACKAGE DIMENSIONS

DFN6 5*6*1 1.27 PITCH
(SO8 FL)
CASE 488AA−01
ISSUE B



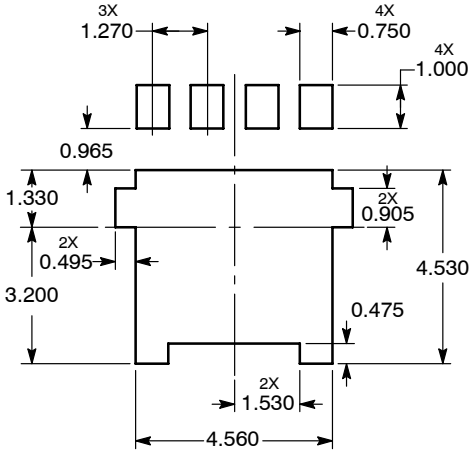


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	0.99	1.20
A1	0.00	−−−	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D		5.15 BSC	
D1	4.50	4.90	5.10
D2	3.50	−−−	4.22
E		6.15 BSC	
E1	5.50	5.80	6.10
E2	3.45	−−−	4.30
e		1.27 BSC	
G	0.51	0.61	0.71
K	0.51	−−−	−−−
L	0.51	0.61	0.71
L1	0.05	0.17	0.20
M	3.00	3.40	3.80
θ	0 °	−−−	12 °

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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