M36W0R6050T1
M36W0R6050B1

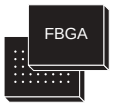
64 Mbit (4 Mb ×16, Multiple Bank, Burst) Flash memory and 32 Mbit (2 Mb ×16) PSRAM, multi-chip package

Features

- Multi-Chip Package
  - 1 die of 64 Mbit (4 Mb × 16) Flash memory
  - 1 die of 32 Mbit (2 Mb × 16) Pseudo SRAM
- Supply voltage
  - $V_{DDF} = V_{DDP} = V_{DDQF} = 1.7$ V to 1.95 V
- Low power consumption
- Electronic signature
  - Manufacturer Code: 20h
  - Device code (top flash configuration), M36W0R6050T1: 8810h
  - Device code (bottom flash configuration), M36W0R6050B1: 8811h
- Package
  - ECOPACK®

Flash memory

- Programming time
  - 8 µs by Word typical for Fast Factory Program
  - Double/Quadruple Word Program option
  - Enhanced Factory Program options
- Memory blocks
  - Multiple Bank memory array: 4 Mbit Banks
  - Parameter Blocks (Top or Bottom location)
- Synchronous / Asynchronous Read
  - Synchronous Burst Read mode: 66 MHz
  - Asynchronous/ Synchronous Page Read mode
  - Random Access: 70 ns
- Dual operations
  - Program Erase in one Bank while Read in others
  - No delay between Read and Write operations



Stacked TFBGA88
(ZA)

- Block locking
  - All blocks locked at Power-up
  - Any combination of blocks can be locked
  - $\overline{WP}_F$ for Block Lock-Down
- Security
  - 128-bit user programmable OTP cells
  - 64-bit unique device number
- Common Flash Interface (CFI)
- 100 000 program/erase cycles per block

PSRAM

- Access time: 70 ns
- Asynchronous Page Read
  - Page size: 8 words
  - First access within page: 70 ns
  - Subsequent read within page: 20 ns
- Three Power-down modes
  - Deep Power-Down
  - Partial Array Refresh of 4 Mbits
  - Partial Array Refresh of 8 Mbits

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1 Description

The M36W0R6050T1 and M36W0R6050B1 combine two memories in a Multi-Chip Package:

- a 64-Mbit, Multiple Bank Flash memory, the M58WR064HT/B, and
- a 32-Mbit Pseudo SRAM, the M69KB048BD.

The purpose of this document is to describe how the two memory components operate with respect to each other. It must be read in conjunction with the M58WR064HT/B and M69KB048BD datasheets, where all specifications required to operate the Flash memory and PSRAM components are fully detailed. These datasheets are available from the ST web site: *www.st.com*.

Recommended operating conditions do not allow more than one memory to be active at the same time.

The memory is offered in a Stacked TFBGA88 (8 ×10 mm, 8 × 10 ball array, 0.8 mm pitch) package. It is supplied with all the bits erased (set to '1').

Figure 1. Logic diagram

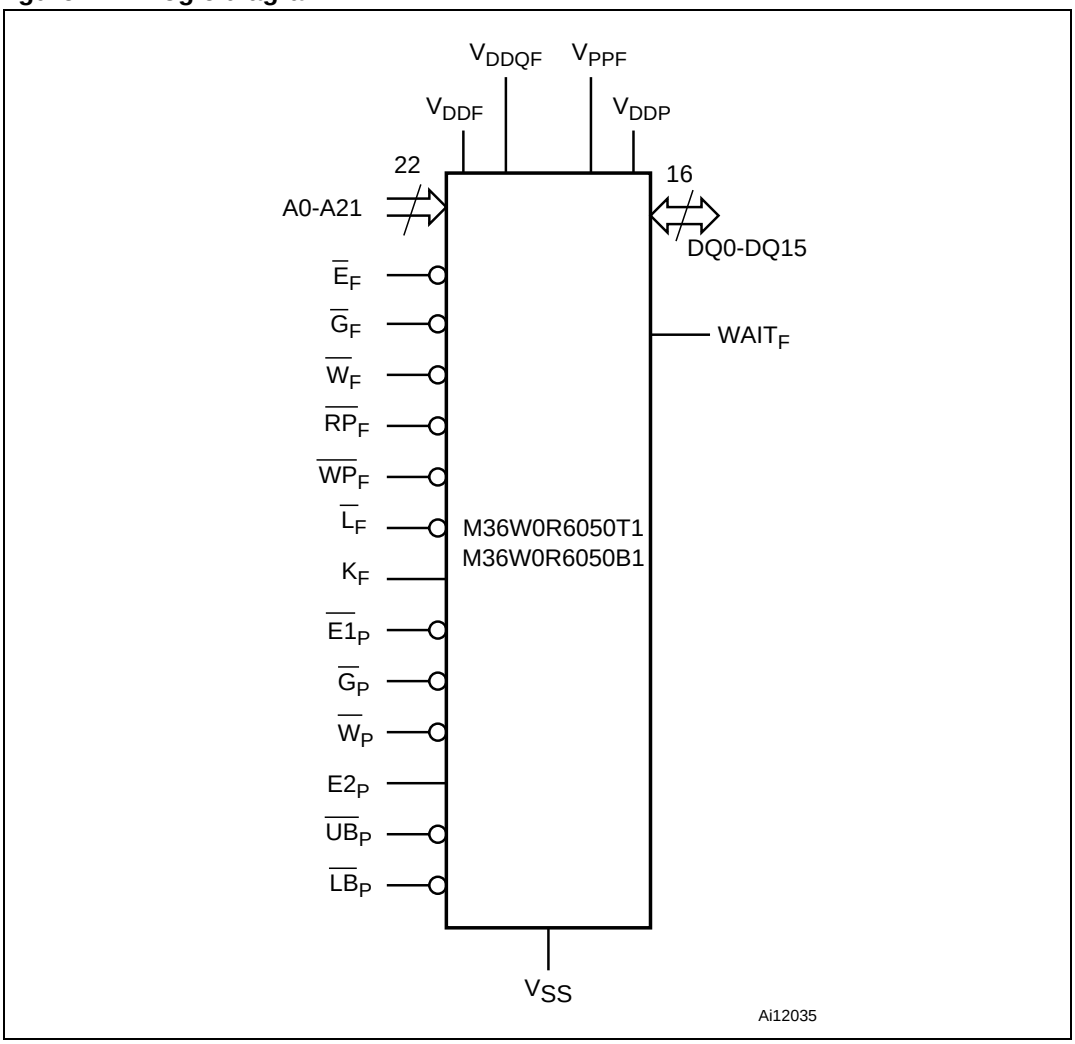
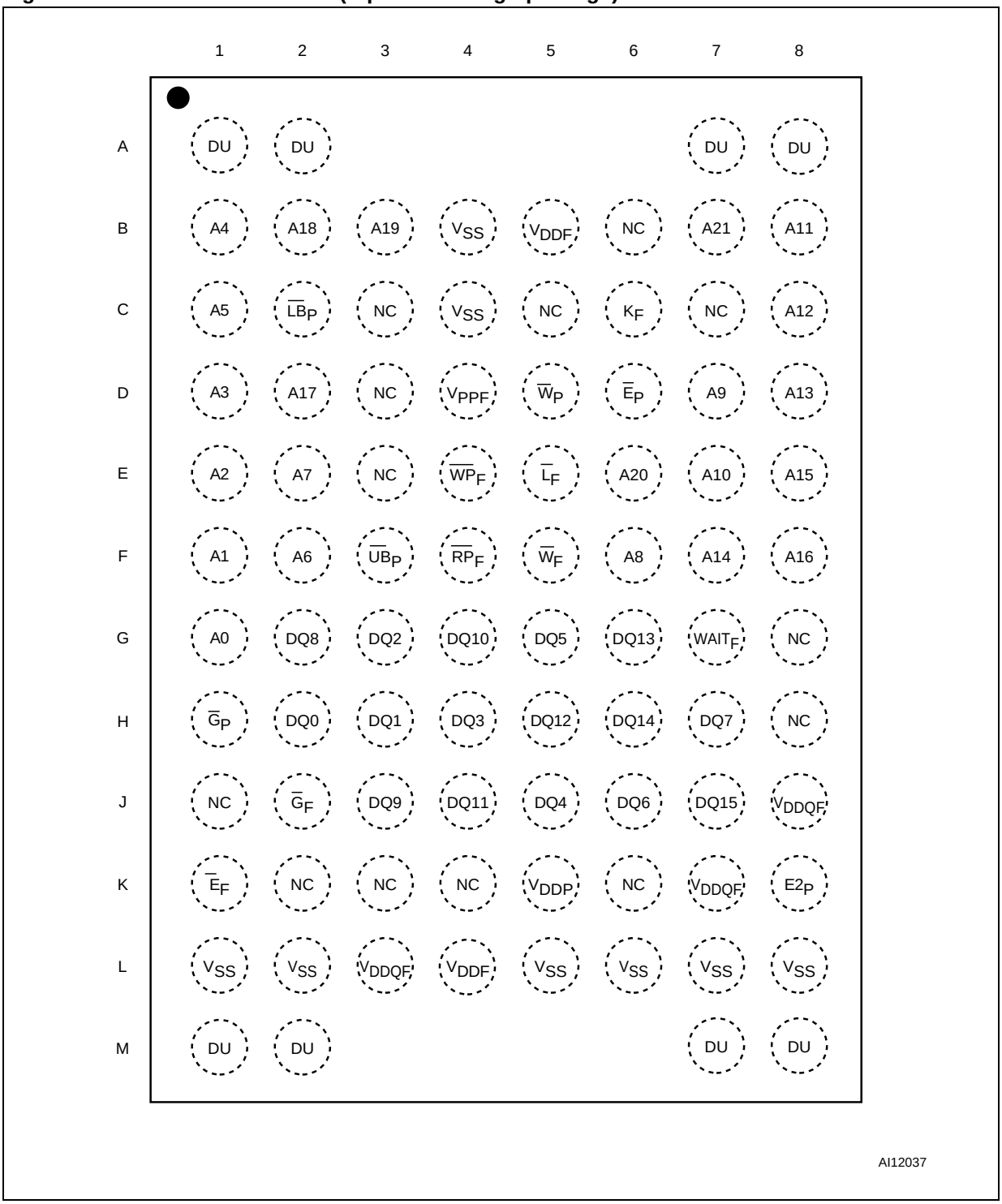


Table 1. Signal names

A0-A21[1]	Address Inputs
DQ0-DQ15	Common Data Inputs/Outputs
V_{DDF}	Flash Memory Power Supply
V_{DDQF}	Flash memory Power Supply for I/O Buffers
V_{PPF}	Common Flash Optional Supply Voltage for Fast Program & Erase
V_{SS}	Ground
V_{DDP}	PSRAM Power Supply
NC	Not Connected Internally
DU	Do Not Use as Internally Connected
Flash memory control functions	
$\overline{L}_F$	Latch Enable input
$\overline{E}_F$	Chip Enable input
$\overline{G}_F$	Output Enable input
$\overline{W}_F$	Write Enable input
$\overline{RP}_F$	Reset input
$\overline{WP}_F$	Write Protect input
K_F	Burst Clock
$WAIT_F$	Wait Data in Burst Mode
PSRAM control functions	
$\overline{E1}_P$	Chip Enable input
$\overline{G}_P$	Output Enable input
$\overline{W}_P$	Write Enable input
$E2_P$	Power-down input
$\overline{UB}_P$	Upper Byte Enable input
$\overline{LB}_P$	Lower Byte Enable input

1. A21 is an address input for the Flash memory component only.

Figure 2. TFBGA connections (top view through package)



2 Signal descriptions

See *Figure 1: Logic diagram* and *Table 1: Signal names*, for a brief overview of the signals connected to this device.

2.1 Address inputs (A0-A21)

Addresses A0-A21 are common inputs for the Flash memory and PSRAM components, whereas A21 is an address input for the Flash memory component only. The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the Flash memory Program/Erase Controller, and they select the cells to access in the PSRAM.

2.2 Data inputs/outputs (DQ0-DQ15)

For the Flash memory, the Data I/O outputs the data stored at the selected address during a Bus Read operation or inputs a command or the data to be programmed during a Write Bus operation.

For the PSRAM, the Upper Byte Data Inputs/Outputs carry the data to or from the upper part of the selected address during a Write or Read operation, when Upper Byte Enable ($\overline{UB}_P$) is driven Low.

Likewise, the Lower Byte Data Inputs/Outputs carry the data to or from the lower part of the selected address during a Write or Read operation, when Lower Byte Enable ($\overline{LB}_P$) is driven Low.

2.3 Flash Chip Enable ($\overline{E}_F$)

The Chip Enable inputs activate the memory control logics, input buffers, decoders and sense amplifiers. When Chip Enable is Low, V_{IL}, and Reset is High, V_{IH}, the device is in active mode. When Chip Enable is at V_{IH} the Flash memory is deselected, the outputs are high impedance and the power consumption is reduced to the standby level.

2.4 Flash Output Enable ($\overline{G}_F$)

The Output Enable pins control data outputs during Flash memory Bus Read operations.

2.5 Flash Write Enable ($\overline{W}_F$)

The Write Enable controls the Bus Write operation of the Flash memories' Command Interface. The data and address inputs are latched on the rising edge of Chip Enable or Write Enable whichever occurs first.

2.6 Flash Write Protect ($\overline{WP_F}$)

Write Protect is an input that gives an additional hardware protection for each block. When Write Protect is Low, V_{IL}, Lock-Down is enabled and the protection status of the Locked-Down blocks cannot be changed. When Write Protect is at High, V_{IH}, Lock-Down is disabled and the Locked-Down blocks can be locked or unlocked. (Refer to Lock Status Table in M58WR064HT/B datasheet).

2.7 Flash Reset ($\overline{RP_F}$)

The Reset input provides a hardware reset of the memory. When Reset is at V_{IL}, the memory is in Reset mode: the outputs are high impedance and the current consumption is reduced to the Reset Supply Current I_{DD2}. Refer to the M58WR064HT/B datasheet, for the value of I_{DD2}. After Reset all blocks are in the Locked state and the Configuration Register is reset. When Reset is at V_{IH}, the device is in normal operation. Exiting Reset mode the device enters Asynchronous Read mode, but a negative transition of Chip Enable or Latch Enable is required to ensure valid data outputs.

The Reset pin can be interfaced with 3V logic without any additional circuitry. It can be tied to V_{RPH} (refer to the M58WR064HT/B datasheet).

2.8 Flash Latch Enable ($\overline{L_F}$)

Latch Enable latches the address bits on its rising edge. The address latch is transparent when Latch Enable is Low, V_{IL}, and it is inhibited when Latch Enable is High, V_{IH}. Latch Enable can be kept Low (also at board level) when the Latch Enable function is not required or supported.

2.9 Flash Clock (K_F)

The Clock input synchronizes the Flash memory to the microcontroller during synchronous read operations; the address is latched on a Clock edge (rising or falling, according to the configuration settings) when Latch Enable is at V_{IL}. Clock is don't care during Asynchronous Read and in write operations.

2.10 Flash Wait ($WAIT_F$)

WAIT is a Flash output signal used during Synchronous Read to indicate whether the data on the output bus are valid. This output is high impedance when Flash Chip Enable is at V_{IH} or Flash Reset is at V_{IL}. It can be configured to be active during the wait cycle or one clock cycle in advance. The $WAIT_F$ signal is not gated by Output Enable.

2.11 PSRAM Chip Enable ($\overline{E1_P}$)

When asserted (Low), the Chip Enable, $\overline{E1_P}$, activates the memory state machine, address buffers and decoders, allowing Read and Write operations to be performed. When de-asserted (High), all other pins are ignored, and the device is automatically put in Standby mode.

2.12 PSRAM Chip Enable ($E2_P$)

When de-asserted (Low), the Chip Enable input $E2_P$, puts the device in Power-Down mode. This is the lowest power mode according to the Configuration Register settings (see M69KB048BD datasheet).

2.13 PSRAM Output Enable ($\overline{G}_P$)

The Output Enable, $\overline{G}_P$, provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus.

2.14 PSRAM Write Enable ($\overline{W}_P$)

The Write Enable, $\overline{W}_P$, controls the Bus Write operation of the memory's Command Interface.

2.15 PSRAM Upper Byte Enable ($\overline{UB}_P$)

The Upper Byte Enable, $\overline{UB}_P$, gates the data on the Upper Byte Data Inputs/Outputs (DQ8-DQ15) to or from the upper part of the selected address during a Write or Read operation.

2.16 PSRAM Lower Byte Enable ($\overline{LB}_P$)

The Lower Byte Enable, $\overline{LB}_P$, gates the data on the Lower Byte Data Inputs/Outputs (DQ0-DQ7) to or from the lower part of the selected address during a Write or Read operation.

2.17 V_{DDF} supply voltage

V_{DDF} provides the power supply to the internal core of the Flash memory component. It is the main power supplies for all Flash memory operations (Read, Program and Erase).

2.18 V_{DDP} supply voltage

The V_{DDP} Supply Voltage supplies the power for all operations (Read or Write) and for driving the refresh logic, even when the device is not being accessed.

2.19 V_{DDQF} supply voltage

V_{DDQF} provides the power supply for the Flash memory I/O pins. This allows all Outputs to be powered independently of the Flash memory core power supply, V_{DDF}.

2.20 V_{PPF} program supply voltage

V_{PPF} is both a Flash Memory control input and a Flash Memory power supply pin. The two functions are selected by the voltage range applied to the pin.

If V_{PPF} is kept in a low voltage range (0V to V_{DDQF}) V_{PPF} is seen as a control input. In this case a voltage lower than V_{PPLKF} gives an absolute protection against Program or Erase, while $V_{PPF} > V_{PP1F}$ enables these functions (see the M58WR064HT/B datasheet for the relevant values). V_{PPF} is only sampled at the beginning of a Program or Erase; a change in its value after the operation has started does not have any effect and Program or Erase operations continue.

If V_{PPF} is in the range of V_{PPHF} it acts as a power supply pin. In this condition V_{PPF} must be stable until the Program/Erase algorithm is completed.

2.21 V_{SS} ground

V_{SS} is the common ground reference for all voltage measurements in the Flash memory (core and I/O Buffers) and PSRAM components.

Note: Each Flash memory device in a system should have its supply voltages (V_{DDF}, V_{DDQF}) and the program supply voltage V_{PPF} decoupled with a 0.1µF ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package). See Figure 5: AC measurement load circuit. The PCB track widths should be sufficient to carry the required V_{PPF} program and erase currents.

3 Functional description

The Flash memory and PSRAM components have separate power supplies but share the same grounds. They are distinguished by three Chip Enable inputs: $\overline{E}_F$ for the Flash memory and $\overline{E1}_P$ and $E2_P$ for the PSRAM.

Recommended operating conditions do not allow more than one device to be active at a time. The most common example is simultaneous read operations on the Flash memory and the PSRAM which would result in a data bus contention. Therefore it is recommended to put the other devices in the high impedance state when reading the selected device.

Figure 3. Functional block diagram

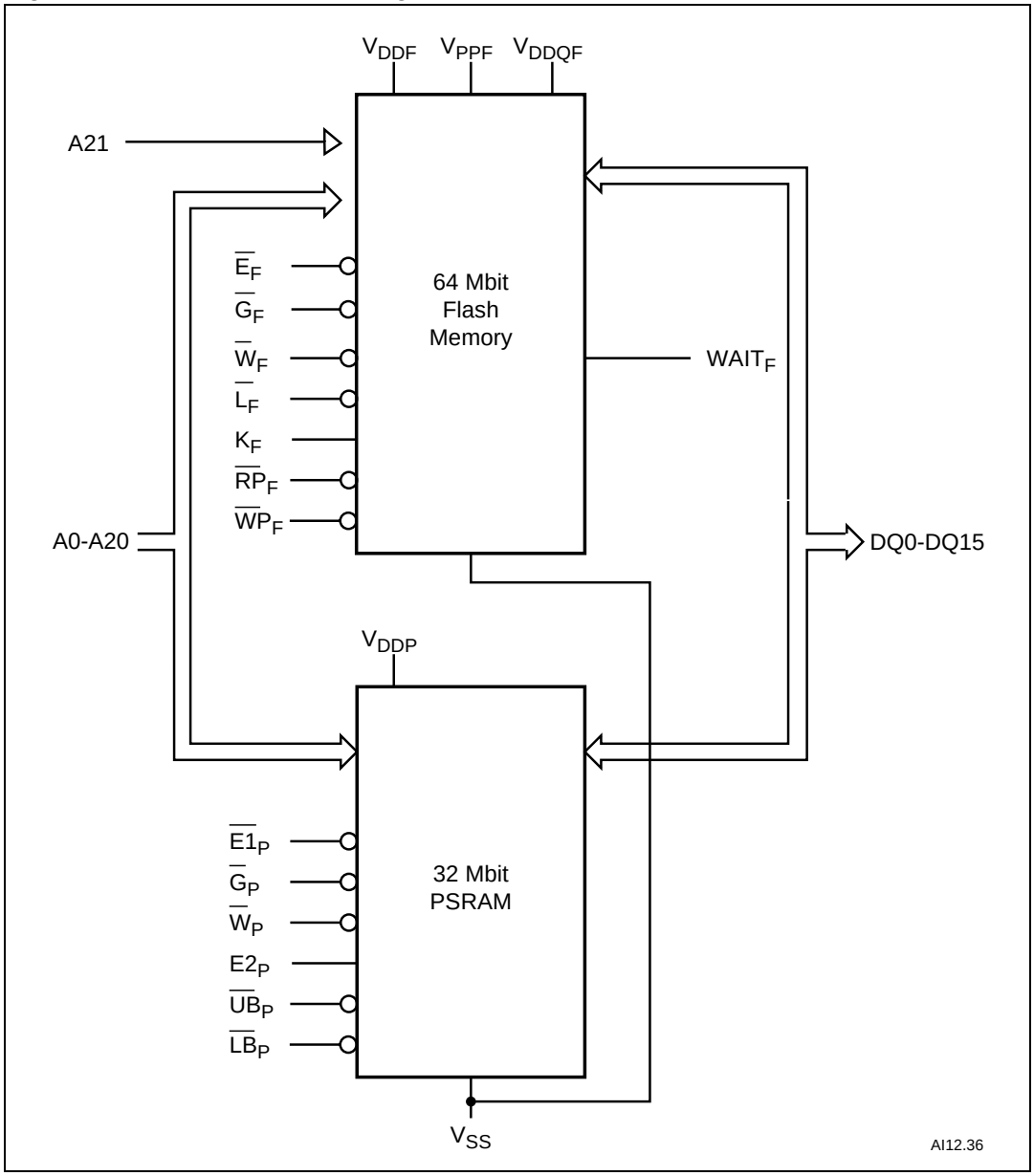


Table 2. Main operating modes

Operation	$\overline{E}_F$	$\overline{G}_P$	$\overline{W}_P$	$\overline{L}_F$	$\overline{RP}_F$	$WAIT_F$ (4)	$\overline{E1}_P$	$\overline{E2}_P$	$\overline{G}_P$	$\overline{W}_P$	$\overline{UB}_P$	$\overline{LB}_P$	DQ15-DQ0
Flash Read	V_{IL}	V_{IL}	V_{IH}	$V_{IL(2)}$	V_{IH}		PSRAM must be disabled						Flash Data Out
Flash Write	V_{IL}	V_{IH}	V_{IL}	$V_{IL(2)}$	V_{IH}								Flash Data In
Flash Address Latch	V_{IL}	X	V_{IH}	V_{IL}	V_{IH}								Flash Data Out or Hi-Z (3)
Flash Output Disable	V_{IL}	V_{IH}	V_{IH}	X	V_{IH}		Any PSRAM mode is allowed						Flash Hi-Z
Flash Standby	V_{IH}	X	X	X	V_{IH}	Hi-Z							Flash Hi-Z
Flash Reset	X	X	X	X	V_{IL}	Hi-Z							Flash Hi-Z
PSRAM Read	Flash Memory must be disabled						V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	PSRAM data out
PSRAM Write							V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	PSRAM data in
Output Disable	Any Flash mode is allowed.						V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	PSRAM Hi-Z
PSRAM Standby							V_{IH}	V_{IH}	X	X	X	X	PSRAM Hi-Z
PSRAM Deep Power-Down							X	V_{IL}	X	X	X	X	PSRAM Hi-Z

1. X = Don't care.
2. $\overline{L}_F$ can be tied to V_{IH} if the valid address has been previously latched.
3. Depends on $\overline{G}_F$.
4. WAIT signal polarity is configured using the Set Configuration Register command. Refer to M58WR064HT/B datasheet for details.

4 Maximum rating

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_A	Ambient Operating Temperature	–30	85	°C
T_{BIAS}	Temperature Under Bias	–40	125	°C
T_{STG}	Storage Temperature	–55	125	°C
V_{IO}	Input or Output Voltage	–0.5	V_{DDQF}+0.6	V
V_{DDF}	Flash Memory Core Supply Voltage	–0.2	2.45	V
V_{DDQF}	Input/Output Supply Voltage	–0.2	2.45	V
V_{DDP}	PSRAM Supply Voltage	–0.5	3.6	V
V_{PPF}	Flash Memory Program Voltage	–0.2	14	V
I_O	Output Short Circuit Current		100	mA
t_{VPPFH}	Time for V_{PPF} at V_{PPFH}		100	hours

5 DC and ac parameters

This section summarizes the operating measurement conditions, and the dc and ac characteristics of the device. The parameters in the dc and ac characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in *Table 4: Operating and ac measurement conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 4. Operating and ac measurement conditions

Parameter	Flash memory		PSRAM		Unit
	Min	Max	Min	Max	
V_{DDF} Supply Voltage	1.7	1.95	–	–	V
V_{DDP} Supply Voltage	–	–	1.7	1.95	V
V_{DDQF} Supply Voltage	1.7	1.95	–	–	V
V_{PPF} Supply Voltage (Factory environment)	11.4	12.6	–	–	V
V_{PPF} Supply Voltage (Application environment)	–0.4	V_{DDQF} +0.4	–	–	V
Ambient Operating Temperature	–30	85	–30	85	°C
Load Capacitance (C_L)	30		50		pF
Input Rise and Fall Times		5			ns
Input Pulse Voltages	0 to V_{DDQF}		0 to V_{DDP}		V
Input and Output Timing Ref. Voltages	$V_{DDQF}/2$		$V_{DDP}/2$		V

Figure 4. AC measurement I/O waveform

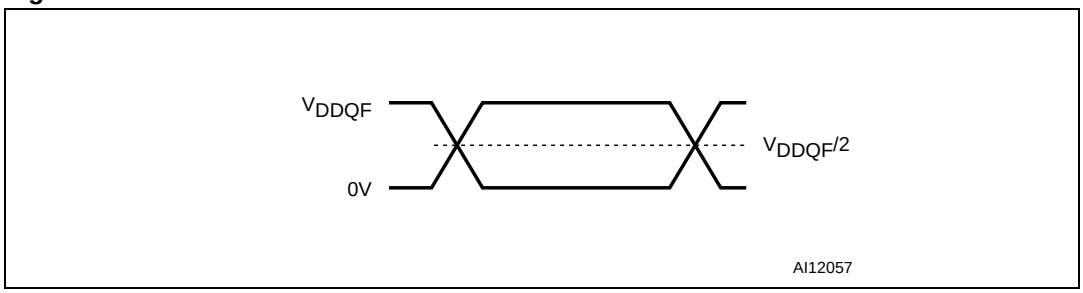


Figure 5. AC measurement load circuit

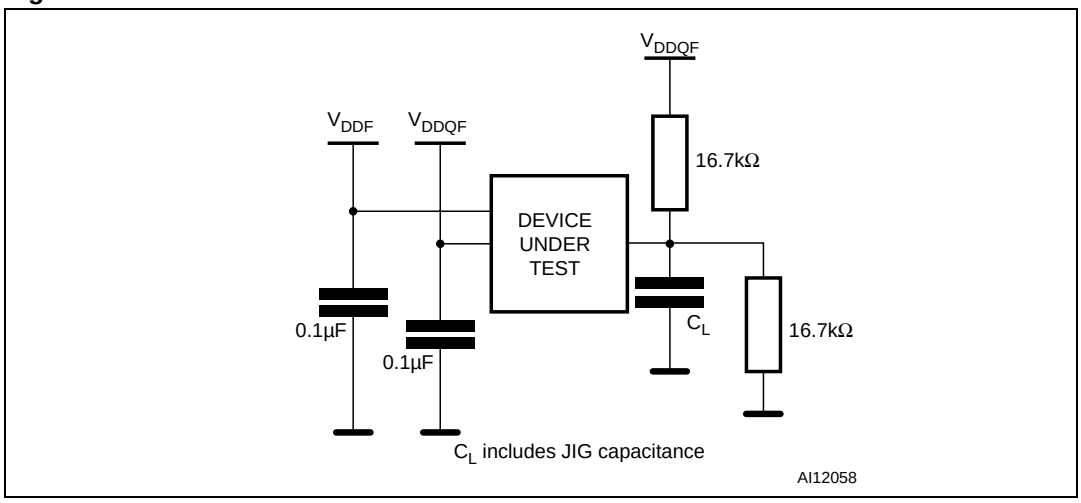


Table 5. Device capacitance

Symbol	Parameter	Test condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		15	pF

1. Sampled only, not 100% tested.

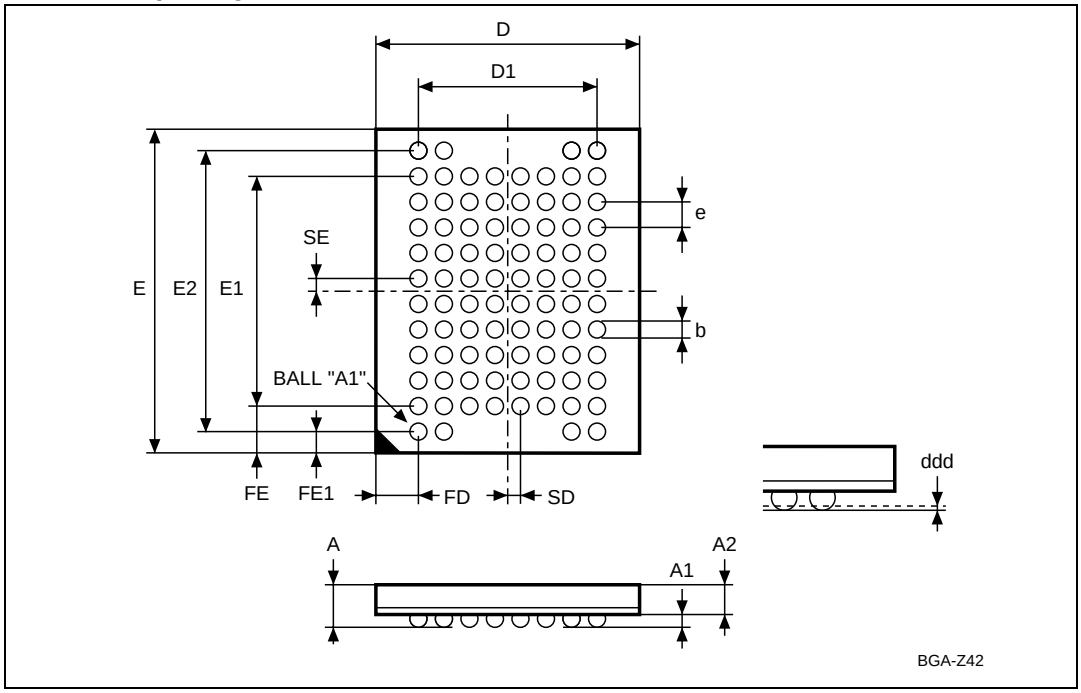
Please refer to the M58WR064HT/B and M69KB048BD datasheets for further dc and ac characteristics values and illustrations.

6 Package mechanical

In order to meet environmental requirements, ST offers the M36W0R6050T1 and M36W0R6050B1 devices in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*.

Figure 6. Stacked TFBGA88 8 × 10 mm - 8 × 10 active ball array, 0.8 mm pitch, package outline



1. Drawing is not to scale.

Table 6. Stacked TFBGA88 8 × 10 mm - 8 × 10 ball array, 0.8 mm pitch, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.200			0.0079	
A2	0.850			0.0335		
b	0.350	0.300	0.400	0.0138	0.0118	0.0157
D	8.000	7.900	8.100	0.3150	0.3110	0.3189
D1	5.600			0.2205		
ddd			0.100			0.0039
E	10.000	9.900	10.100	0.3937	0.3898	0.3976
E1	7.200			0.2835		
E2	8.800			0.3465		
e	0.800	–	–	0.0315	–	–
FD	1.200			0.0472		
FE	1.400			0.0551		
FE1	0.600			0.0236		
SD	0.400			0.0157		
SE	0.400			0.0157		

7 Part numbering

Table 7. Ordering information scheme

Example: M36 W0 R 6 0 5 0 T 1 ZAQ E

Device Type
M36 = Multiple Memory Product (Multiple Flash + RAM)

Flash 1 Architecture
W = Multiple Bank, Burst mode

Flash 2 Architecture
0 = none present

Operating Voltage
R = V_{DDF} = V_{DDQF} = V_{DDP} = 1.7 V to 1.95 V

Flash 1 Density
6 = 64 Mbit

Flash 2 Density
0 = none present

RAM 1 Density
5 = 32 Mbit

RAM 0 Density
0 = none present

Parameter Blocks Location
T = Top Boot Block Flash
B = Bottom Boot Block Flash

Product Version
1 = 90 nm Flash technology, 70 ns; 0.13 µm RAM, 70 ns speed

Package
ZAQ = Stacked TFBGA88 8 × 10 mm - 8 × 10 active ball array, 0.8 mm pitch

Option
E = ECOPACK® Package, Standard Packing
F = ECOPACK® Package, Tape & Reel Packing

Devices are shipped from the factory with the memory content bits erased to '1'. For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

8 Revision history

Table 8. Document revision history

Date	Revision	Changes
06-Dec-2005	0.1	Initial release.
12-Jan-2007	1	Document status promoted to Full Datasheet. Small text changes.

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