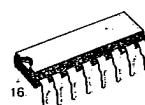




## QUAD LINE DRIVER

- MEETS EIA RS-422A REQUIREMENTS
- PROPAGATION DELAY IS LESS THAN 20 ns
- ENABLE OR ENABLE TO OUTPUT DELAY IS LESS THAN 40 ns
- TTL COMPATIBLE ENABLE AND ENABLE INPUTS
- POWER SUPPLY CURRENT IS REDUCED TO LESS THAN 40 mA WHEN DEVICE IS DISABLED
- OUTPUT SKEW (TIME DELAY BETWEEN DIRECT OUTPUT AND INVERSE OUTPUT) TYPICALLY 2 ns

The LB1023 Quad Line Driver is an integrated circuit consisting of four independent line drivers with a common control for both ENABLE and ENABLE. It provides high speed differential drive

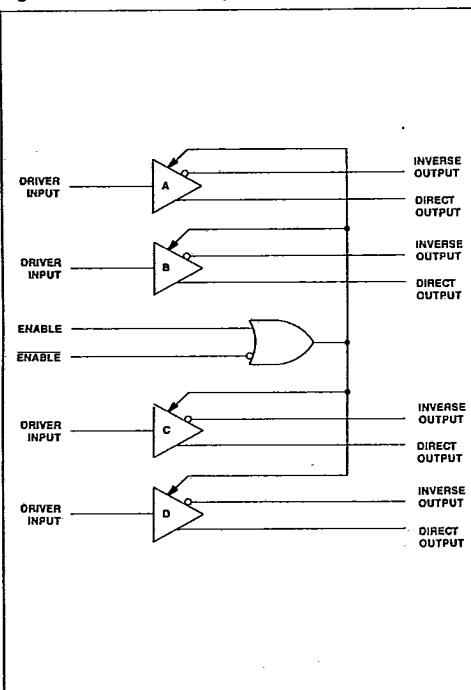


DIP-16 A Plastic

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to transmission lines having an impedance of at least 100 ohms. Each of the four drivers has a complementary tristate output. The LB1023 requires only a single 5 volt supply ( $\pm 10\%$ ) for operation.

Fig. 1 - Functional Diagram



### PIN CONFIGURATION

AIN	1	16	V+
AO-D	2	15	DIN
AO-I	3	14	DO-D
ENABLE	4	13	DO-I
Bo-I	5	12	ENABLE
Bo-D	6	11	Co-I
BIN	7	10	Co-D
COMMON	8	9	CIN

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D T-75-45-05

LB1023

**PIN DESCRIPTION**

Name	Description
A <sub>IN</sub> B <sub>IN</sub> C <sub>IN</sub> D <sub>IN</sub>	TTL compatible inputs for Line Drivers A through D respectively.
A <sub>OD</sub> B <sub>OD</sub> C <sub>OD</sub> D <sub>OD</sub>	Non-inverting Line Driver outputs for drivers A through D respectively.
A <sub>OI</sub> B <sub>OI</sub> C <sub>OI</sub> D <sub>OI</sub>	Inverting Line Driver outputs for drivers A through D respectively.
ENABLE	Logic-High-Enable, TTL compatible input. See Truth Table under Applications for logic programming of this pin.
ENABLE	Logic-Low-Enable, TTL compatible input. See Truth Table under Applications for logic programming of this pin.
V <sub>+</sub>	Connection for external power supply.
COMMON	Circuit common (not necessarily physical or system ground).

**ABSOLUTE MAXIMUM RATINGS** (at 25°C unless otherwise specified)

Parameter	Value	Unit
Ambient Operating Temperature Range	0 to +70	°C
Storage Temperature Range	-40 to +125	°C
Pin Soldering Temperature (t = 15 sec.)	300	°C
Power Supply Voltage (V <sub>+</sub> )	7.0	V
Input Operating Voltages, V <sub>+</sub> , Driver Inputs, ENABLE and $\bar{E}NABLE$	5.5	V
Driver Output Current	$\pm 35$	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TIMING CHARACTERISTICS** (T<sub>A</sub> = 25°C, V<sub>+</sub> = 5V, See Fig. 7)

Symbol	Characteristics	Min.	Typ.	Max.	Unit
T <sub>THL</sub> or T <sub>TLH</sub>	Transition time; (see Figure 2)	—	—	20	ns
T <sub>PHL</sub> or T <sub>PLH</sub>	Propagation Delay Time; (see Figure 3)	—	—	20	ns
T <sub>SKEW</sub>	V <sub>OD</sub> to V <sub>OI</sub> Time Difference; (see Figure 2)	—	$\pm 2.0$	$\pm 6.0$	ns
$\frac{V_{peak}-V_+}{V_+}$	Overshoot, (see Figure 3)	—	—	10	%



### TIMING CHARACTERISTICS (Continued)

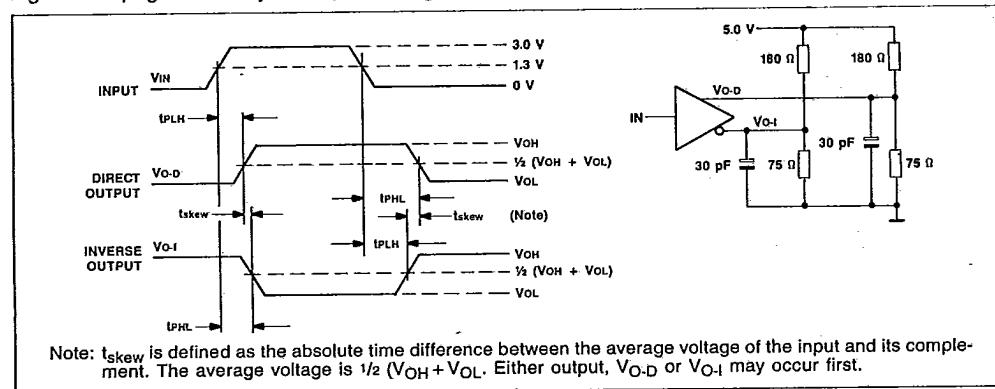
*Driver Disable and Enable Times (see Figures 4, 5 and 6)*

Symbol	Characteristics	Min.	Typ.	Max.	Unit
$t_{HZ}$	Output ENABLE Times (See Fig. 5 and Note 1): Output high to "high impedance"	—	—	40	ns
$t_{LZ}$	Output low to "high impedance"	—	—	40	ns
$t_{ZH}$	Output Enable Times (See Fig. 4 and Note 1): "High impedance" to output high;	—	—	30	ns
$t_{ZL}$	"High impedance" to output low	—	—	30	ns

NOTE 1: The device is disabled when ENABLE = LOW and ENABLE = HIGH. All other conditions of ENABLE and ENABLE will allow the device to operate (see Truth Table under Applications).

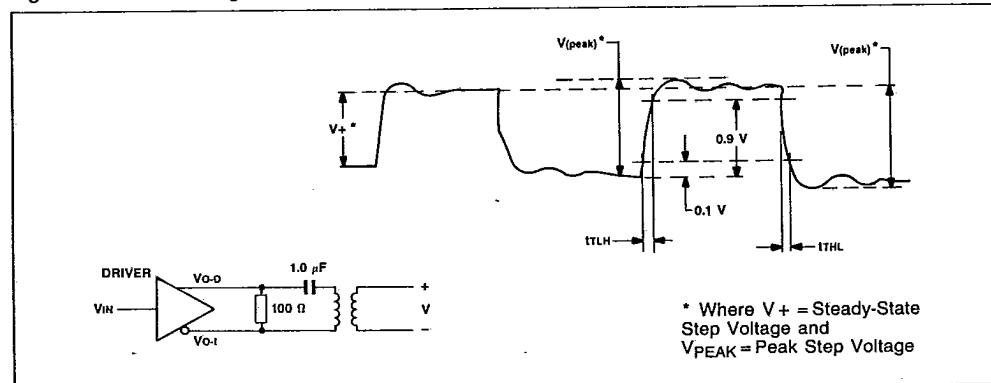
### TIMING DIAGRAMS

Fig. 2 - Propagation Delay and  $t_{SKew}$  Diagram and Associated Load Schematic



Note:  $t_{skew}$  is defined as the absolute time difference between the average voltage of the input and its complement. The average voltage is  $1/2(V_{OH} + V_{OL})$ . Either output,  $V_{O-D}$  or  $V_{O-I}$  may occur first.

Fig. 3 - Overshoot Diagram and Associated Load Schematic



\* Where  $V_+$  = Steady-State Step Voltage and  
 $V_{PEAK} =$  Peak Step Voltage

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### TIMING DIAGRAMS

Fig. 4 - Enable and Output Waveforms

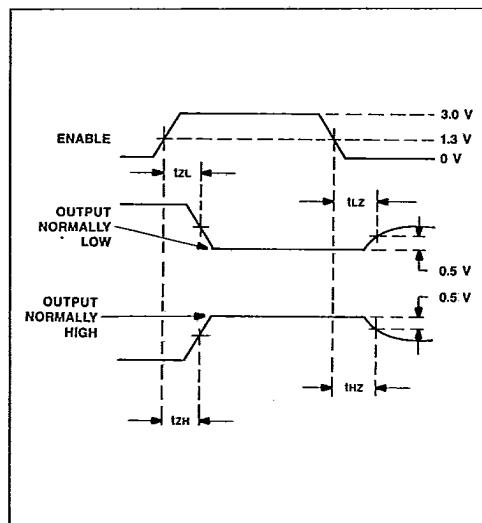


Fig. 5 - Enable and Output Waveforms

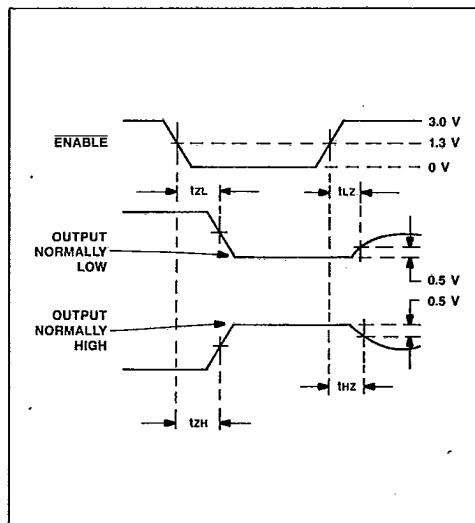


Fig. 6 - Associated Enable, Enable Loading Diagrams

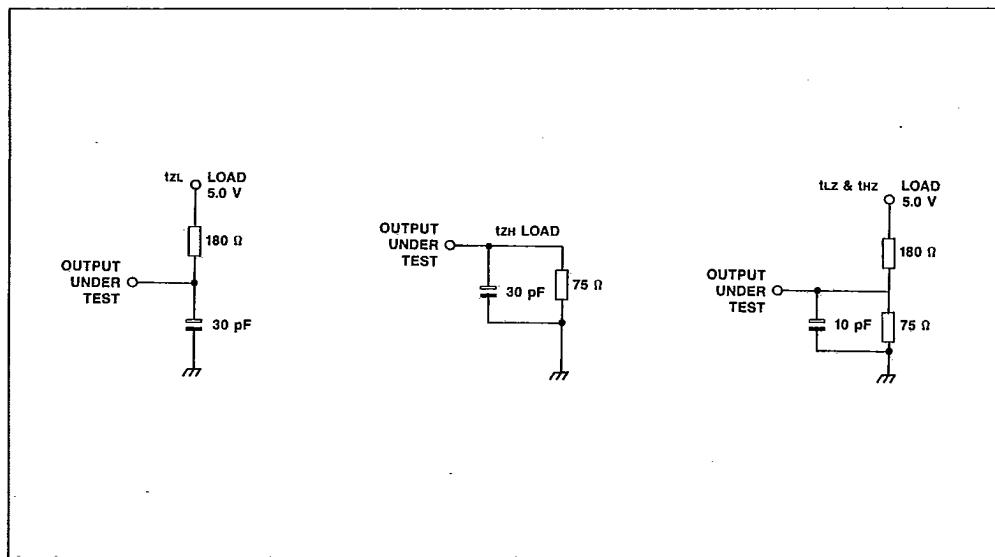
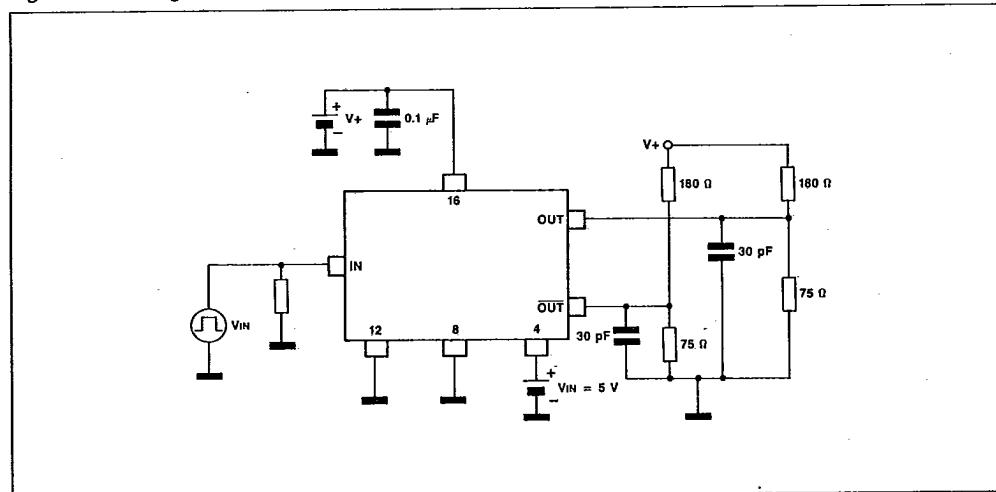




Fig. 7 - Switching Time Test Configuration

ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$  unless otherwise specified)

Parameter	Test Conditions	Min	Typ	Max	Unit
Power Supply Operating Voltage	(See Fig. 8)	4.5	—	5.5	V
Output Voltage	$V_+ = 4.5\text{V}$ , $I_O = 20\text{mA}$ , (See Fig. 8)	2.5	—	3.5	V
	$V_{IH} = 2.0\text{V}$ , $V_{IL} = 0.8\text{V}$ (See Fig. 8)	0.05	—	0.5	
Input Clamp Voltage	$V_+ = 4.5\text{V}$ , $I_{IN} = -18\text{mA}$	0	—	-1.5	
Power Supply Current	$V_+ = 5.5\text{V}$ , $V_{IN} = 0$ (See Fig. 10)	45	—	90	mA
	$V_+ = 5.5\text{V}$ , $V_{IN} = 2.0\text{V}$ (See Fig. 10)	20	—	40	
Output Current	$V_O = 0.5$ or $2.5\text{V}$ (See Fig. 11)	—	—	$\pm 20$	μA
	$V_O = -0.25$ or $6.0\text{V}$ (See Fig. 12)	—	—	$\pm 100$	
	$V_+ = 5.5\text{V}$ (See Fig. 13)	—	—	-150	
Input Current	$V_{IN} = 0.4\text{V}$ (See Fig. 14)	Low	0	—	mA
	$V_{IN} = 2.7\text{V}$ (See Fig. 14)	High	—	—	
	$V_{IN} = 7.0\text{V}$ (See Fig. 14)	Reverse	0	—	

LB1023

## TEST CIRCUITS

Fig. 8 - Output Voltage (High) (Low)

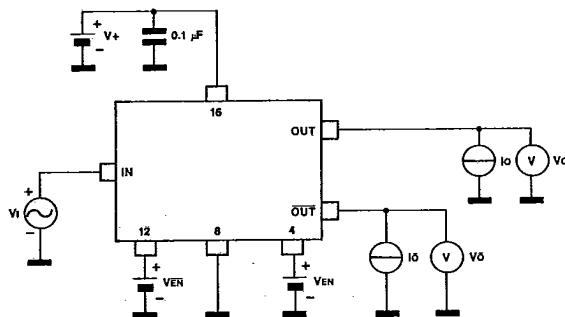


Fig. 9 - Input Clamp Voltage

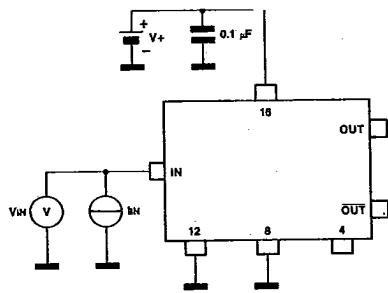


Fig. 10 - Power Supply Current No Load & Disabled

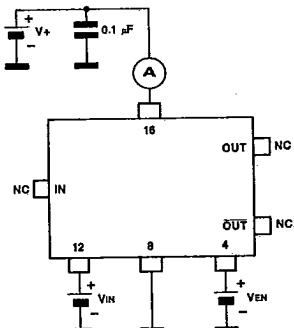


Fig. 11 - Output Current (Disabled)

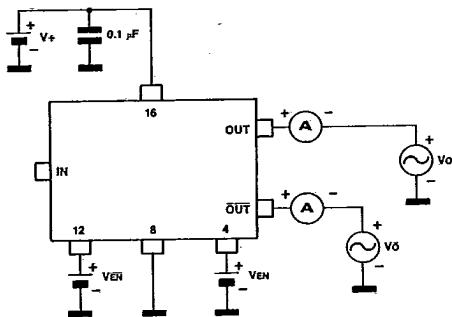
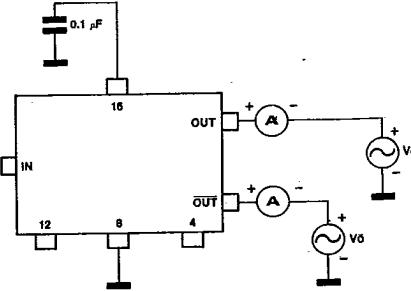
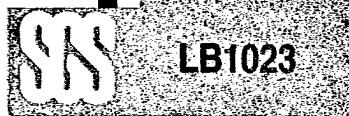


Fig. 12 - Output Current (Power OFF)





### TEST CIRCUITS (Continued)

Fig. 13 - Output Current, Short Circuit

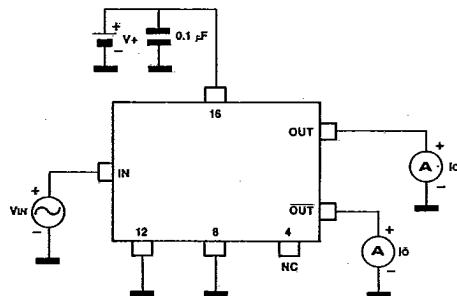
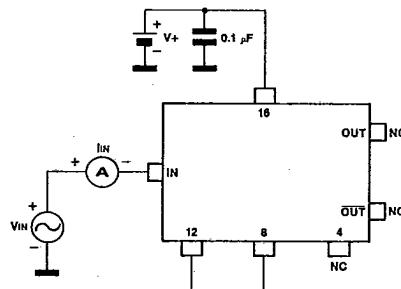


Fig. 14 - Input Current (Low) (High) (Reverse)



### APPLICATION

The following Truth Table shows the V+, ENABLE, ENABLE and "Data In" conditions which must be met to provide specific "Driver Output States" (both direct and inverse outputs). Figure 15 illustrates basic information for applica-

tion of the LB1023 line driver devices in a Two-Wire Balanced RS-422A System. This particular diagram shows the LB1023 Line Driver interfacing with the LB1022A type Line Receivers.

### TRUTH TABLE

Condition 1	Data In 1	Direct Output	Inverse Output
Enable is High	High	High	Low
Enable is High	Low	Low	High
Enable is Low	High	High	Low
Enable is Low	Low	Low	High
Enable is Low AND Enable is High	Don't Care	High Impedance	High Impedance
V+ is Low ( $\leq 0.5V$ )	Don't Care	High Impedance	High Impedance

NOTE 1: High and Low levels for Enable, Enable and Data In are TTL levels ( $V_{IH} \geq 2.0V$ ,  $V_{IL} \leq 0.8V$ ).

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Fig. 15 - LB1023 Quad Line Driver Application Diagram

