



SANYO Semiconductors

# DATA SHEET

## LA6565 — Monolithic Linear IC For CD and DVD players 5-channel Driver (BTL:4ch,H-bridge:1ch)

### Overview

The LA6565 is a 4-channel BTL plus 1-channel H-bridge actuator driver developed for use in CD and DVD drives. The BTL driver channels 1 and 2 include built-in operational amplifiers allowing the LA6565 to support a wide range of applications.

### Functions

- Five power amplifier channels on a single chip (Bridge connection (BTL): 4-channels, H-bridge: 1-channel)
- $I_O$  max: 1A
- Built-in level shifters (except for the H bridge channel)
- Muting circuits (output on/off, two systems)  
(The muting circuits operate for the BTL amplifiers. They do not apply to the H-bridge or regulator circuits.)
- Built-in regulator (Uses an external PNP-transistor and is set with an external resistor.)
- Output voltage setting function (loading driver)
- Built-in independent operational amplifiers
- Thermal shutdown circuit

### Specifications

Maximum Ratings at  $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC}$ max		14	V
Maximum output current	$I_O$ max		1	A
Maximum input voltage	$V_{INB}$		13	V
MUTE pin voltage	$V_{MUTE}$		13	V
Allowable power dissipation	$P_d$ max	Independent IC	0.8	W
		Mounted on a specified board *	2	W
Operating temperature	$T_{opr}$		-40 to +85	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-55 to +150	$^\circ\text{C}$

\* Specified board: 114.3mm × 76.1mm × 1.6mm, glass epoxy board.

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# LA6565

## Recommended Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{CC}$		5.6 to 13	V

## Electrical Characteristics at $T_a = 25^\circ\text{C}$ , $V_{CC1} = V_{CC2} = 8\text{V}$ , $V_{REF} = 2.5\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
<b>Overall</b>						
Quiescent current when on	$I_{CC-ON}$	BTL amplifier output on, loading block off *1		30	50	mA
Quiescent current when off	$I_{CC-OFF}$	All outputs off *1		10	15	mA
Thermal shutdown circuit operating temperature	TSD	*7	150	175	200	$^\circ\text{C}$
<b>VREF Amplifier</b>						
VREF amplifier offset voltage	VREF-OFFSET		-10		+10	mV
VREF input voltage range	VREF-IN		1		$V_{CC}-1.5$	V
VREF-OUT output current	I-VREF-OUT			1		mA
<b>Operational Amplifier (Independent)</b>						
Input voltage range	$V_{IN(OP)}$		0		$V_{CC}-1.5$	V
Output current (sink)	SINK(OP)		2			mA
Output current (source)	SOURCE(OP)		300	500		$\mu\text{A}$
Output offset voltage	$V_{OFF(OP)}$		-10		+10	mV
Residual current (sink)	$V_{CE-SINK(OP)}$	$I_O(\text{sink side}) = 1\text{mA}$			0.6	V
<b>BTL Amplifier Block (Channels 1 to 4)</b>						
Output offset voltage	$V_{OFF}$	The voltage difference between each channel outputs *2, *3	-50		+50	mV
Input voltage range	$V_{IN}$	Input voltage range of the input operational amplifiers	0		$V_{CC}-1.5$	V
Output voltage	$V_O$	$I_O = 0.5\text{A}$ , the voltage between $V_{O^+}$ and $V_{O^-}$ in each channel	5.7	6.2		V
Closed circuit voltage gain	VG	The gain from the input to the output with the input amplifier set to $0\text{dB}$ *2, *3	7.2	8	9	times
Slew rate SR	SR	For the independent amplifier. Times 2 when between outputs.*7		0.5		$\text{V}/\mu\text{s}$
Muting on voltage	$V_{MUTE-ON}$	The output on voltage, for each mute function *4	2.5			V
Muting off voltage	$V_{MUTE-OFF}$	The output off voltage, for each mute function *4			0.5	V
<b>Input Amplifier Block (Channels 1 and 2)</b>						
Input voltage range	$V_{IN-OP}$		0		$V_{CC}-1.5$	V
Output current (sink)	SINK-OP		2			mA
Output current (source)	SOURCE-OP	*5	300	500		$\mu\text{A}$
Output offset voltage	$V_{OFF-OP}$		-10		+10	mV
<b>Loading Block (Channel 5, H bridge circuit)</b>						
Output voltage	$V_{O-LOAD}$	For forward/reverse operation, $I_O = 0.5\text{A}$ , $V_{CONT} = V_{CC}$ *	5.7	6.5		V
Braking output saturation voltage	$V_{CE-BREAK}$	The output voltage during braking *6			0.3	V
Low-level input voltage	$V_{IN-L}$				1	V
High-level input voltage	$V_{IN-H}$		2			V
<b>Power Supply Block (Uses an external 2SB632K PNP-transistor)</b>						
Power supply output	$V_{OUT}$	$I_O = 200\text{mA}$	1.260	1.285	1.310	V
REG-IN sink current	REG-IN-SINK	External PNP-transistor base current	5	10		mA
Line regulation	$\Delta V_{OLN}$	$6\text{V} \leq V_{CC} \leq 12\text{V}$ , $I_O = 200\text{mA}$		10	100	mV
Load regulation	$\Delta V_{OLD}$	$5\text{mA} \leq I_O \leq 200\text{mA}$		10	100	mV

\*1: The total current dissipation for  $V_{CCP1}$ ,  $V_{CCP2}$ , and  $V_{CCS}$  with no load.

\*2: The input amplifier is a buffer amplifier.

\*3: The voltage difference between the two sides of the load ( $12\Omega$ ).

\*4: When the MUTE pin is high, the output will be on, and when low, the output will be off (high-impedance state).

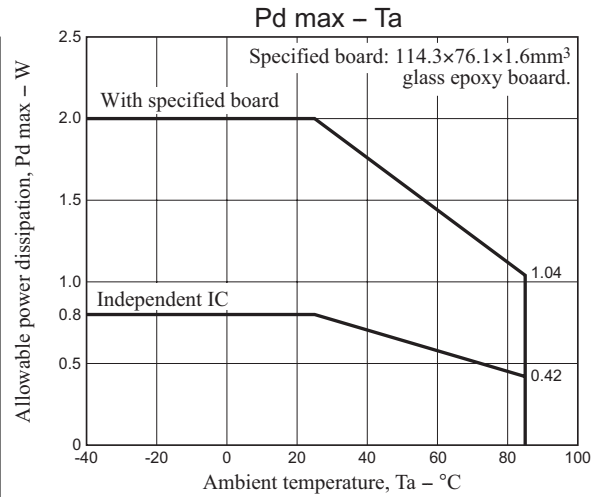
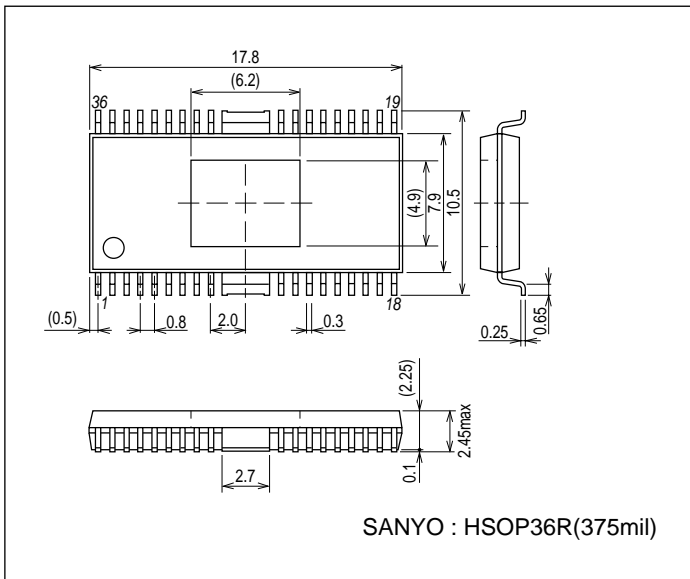
\*5: The input operational amplifier source is constant current. Since the  $11\text{k}\Omega$  resistor between this and the next stage functions as the load, the input operational amplifier gain must be set carefully.

\*6: The braking operation is a short (to ground) braking operation. The sink side output is on at this time.

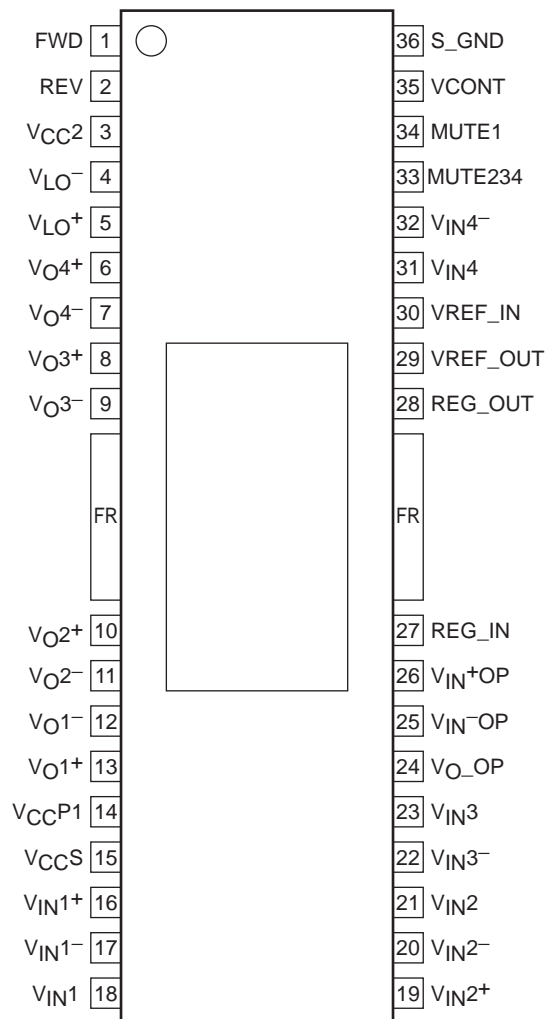
\*7: Design guarantee.

Package Dimensions

unit : mm (typ)  
3251

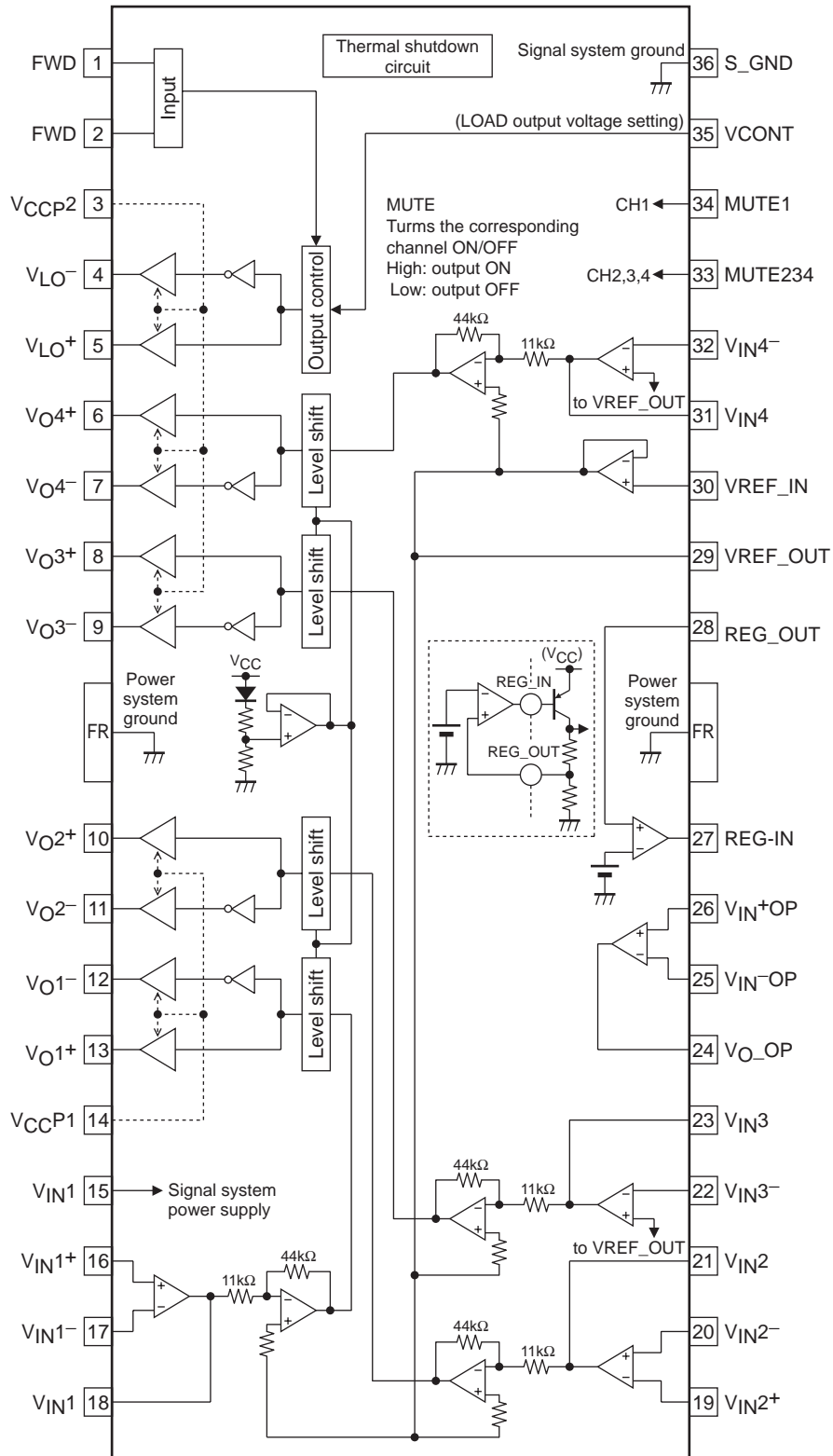


Pin Assignment



Top View

Block Diagram



# LA6565

## Pin Function

Pin No.	Pin name	Pin function
1	FWD	Loading output direction switching (FWD). Loading system logic input.
2	REV	Loading output direction switching (REV). Loading system logic input.
3	V <sub>CC2</sub>	Channels 3, 4, and loading power stage power supply.
4	V <sub>LO</sub> <sup>-</sup>	Loading output (-)
5	V <sub>LO</sub> <sup>+</sup>	Loading output (+)
6	V <sub>O4</sub> <sup>+</sup>	Channel 4 output (+)
7	V <sub>O4</sub> <sup>-</sup>	Channel 4 output (-)
8	V <sub>O3</sub> <sup>+</sup>	Channel 3 output (+)
9	V <sub>O3</sub> <sup>-</sup>	Channel 3 output (-)
10	V <sub>O2</sub> <sup>+</sup>	Channel 2 output (+)
11	V <sub>O2</sub> <sup>-</sup>	Channel 2 output (-)
12	V <sub>O1</sub> <sup>-</sup>	Channel 1 output (-)
13	V <sub>O1</sub> <sup>+</sup>	Channel 1 output (+)
14	V <sub>CCP1</sub>	Channels 1 and 2 power stage power supply.
15	V <sub>CCS</sub>	Signal system power supply.
16	V <sub>IN1</sub> <sup>+</sup>	Channel 1 input. Input operational amplifier + input.
17	V <sub>IN1</sub> <sup>-</sup>	Channel 1 input. Input operational amplifier - input.
18	V <sub>IN1</sub>	Channel 1 input. Input operational amplifier output.
19	V <sub>IN2</sub> <sup>+</sup>	Channel 2 input. Input operational amplifier + input.
20	V <sub>IN2</sub> <sup>-</sup>	Channel 2 input. Input operational amplifier - input.
21	V <sub>IN2</sub>	Channel 2 input. Input operational amplifier output.
22	V <sub>IN3</sub> <sup>-</sup>	Channel 3 input. Input operational amplifier - input.
23	V <sub>IN3</sub>	Channel 3 input. Input operational amplifier output.
24	V <sub>O</sub> _OP	Operational amplifier output.
25	V <sub>IN</sub> <sup>-</sup> OP	Operational amplifier - input
26	V <sub>IN</sub> <sup>+</sup> OP	Operational amplifier + input
27	REG_IN	Regulator error amplifier output. Connect this pin to the base of the external PNP-transistor.
28	REG_OUT	Regulator error amplifier input (+).
29	VREF_OUT	VREF amplifier (voltage follower) output.
30	VREF_IN	VREF input. Apply the external reference voltage to this pin.
31	V <sub>IN4</sub>	Channel 4 input. Input operational amplifier output.
32	V <sub>IN4</sub> <sup>-</sup>	Channel 4 input. Input operational amplifier - input.
33	MUTE234	Controls the on/off state of channels 2, 3, and 4.
34	MUTE1	Channel 1 output on/off control
35	VCONT	Loading block output high-level voltage setting.
36	S_GND	Signal system ground.

\* center frame (FR) becomes GND for the power system, Set this to the minimum potential together with S\_GND (signal system ground).

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## Pin Description

Pin No.	Pin name	Function	Description	Equivalent circuit
16 17 18 19 20 21 22 23 32 31 26 25 24	$V_{IN1}^+$ $V_{IN1}^-$ $V_{IN1}$ $V_{IN2}^+$ $V_{IN2}^-$ $V_{IN2}$ $V_{IN3}^-$ $V_{IN3}$ $V_{IN4}^-$ $V_{IN4}$ $V_{IN}^+OP$ $V_{IN}^-OP$ $V_{O\_OP}$	Input (CH1 to 4)	Inputs (channels 1 to 4 and the independent operational amplifier)	
1 2	FWD REV	Input (H-bridge)	Logic inputs. The IC is set to one of four modes, forward, reverse, brake, and free running by the combination of high and low values applied to these pins.	
12 13 10 11 8 9 6 7	$V_{O1}^+$ $V_{O1}^-$ $V_{O2}^+$ $V_{O2}^-$ $V_{O3}^+$ $V_{O3}^-$ $V_{O4}^+$ $V_{O4}^-$	Output (BTL-AMP)	Channel 1 to 4 outputs.	
4 5	$V_{LO}^-$ $V_{LO}^+$	Output (H-bridge)	H-bridge (loading) output.	
35	VCONT	Input	Loading output setting.	
33 34	MUTE234 MUTE1	MUTE	BTL amplifier output ON/OFF state setting. High: output ON Low: output OFF	

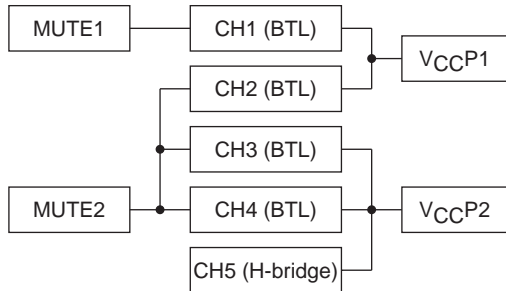
**Truth Table** (Loading (H bridge) block)

FWD	REV	V <sub>LO</sub> <sup>+</sup>	V <sub>LO</sub> <sup>-</sup>	Loading output
L	L	OFF	OFF	OFF *1
	H	H	L	Forward
H	L	L	H	Reverse
	H	L	L	Short-circuit braking *2

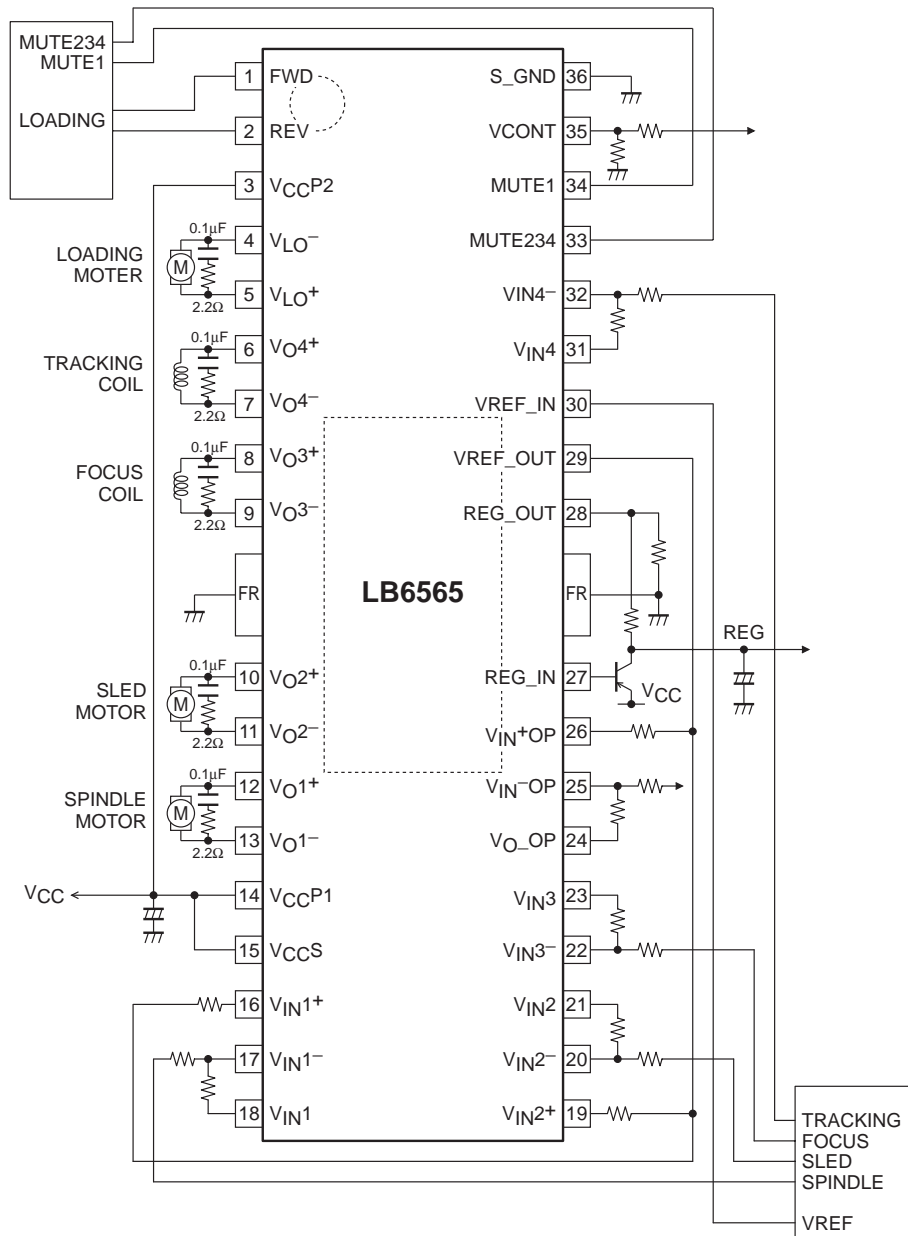
\*1. The output goes to the high-impedance state.

\*2. In braking mode, the sink side transistor is turned on (for short-circuit braking). The V<sub>LO</sub><sup>+</sup> and V<sub>LO</sub><sup>-</sup> pins go to a level that is essentially the ground level.

**Relationship between the MUTE pins and the power supply systems (V<sub>CCP</sub>\*)**



**Application Circuit Example**



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