



Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUFFERS

IDT 54/74FCT827A/B
IDT 54/74FCT828A/B*

FEATURES:

- Faster than AMD's Am29827-28 series
- Equivalent to AMD's Am29827-28 bipolar buffers in pinout/function, speeds and output drive over full temperature and voltage supply extremes
- High-speed buffers
 - Non-inverting $t_{PD} = 3.5ns$ typ.
 - Inverting $t_{PD} = 4.0ns$ typ.
- $I_{OL} = 48mA$ (commercial), 32mA (military)
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels (5 μ W typ. static)
- TTL Input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 Series (5 μ A max.)
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

T-52-07

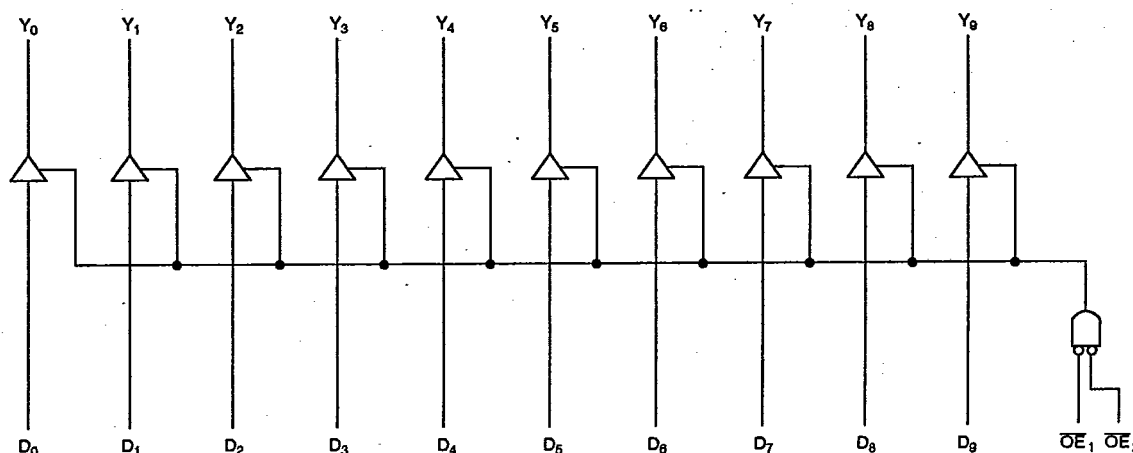
The IDT54/74FCT800 Series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT827A/B and IDT54/74FCT828A/B 10-bit bus drivers provide high-performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NOR-ed output enables for maximum control flexibility. All buffer data inputs have 200mV minimum input hysteresis to provide improved noise rejection.

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high impedance state.

FUNCTIONAL BLOCK DIAGRAM

IDT54/74FCT827A/B-IDT54/74FCT828A/B 10-BIT BUFFERS



PRODUCT SELECTOR GUIDE

	10-BIT BUFFER
Non-Inverting	IDT54/74FCT827A/B
Inverting	IDT54/74FCT828A/B

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*Advance information only for IDT54/74FCT828.

MILITARY AND COMMERCIAL TEMPERATURE RANGES

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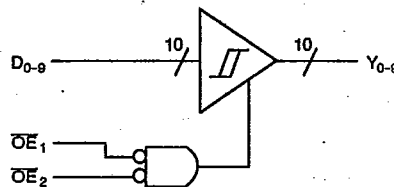
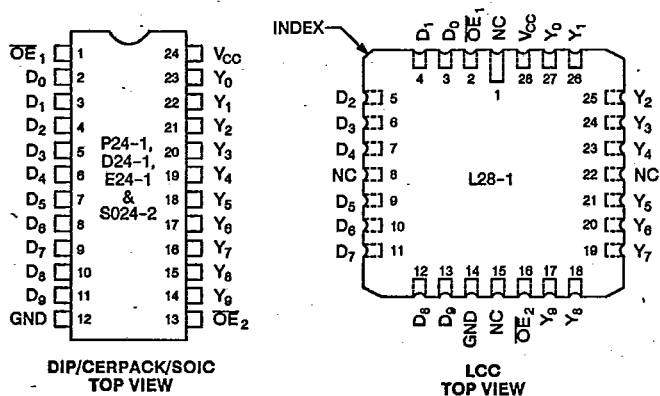
DSC-4010/-1

PIN CONFIGURATIONS

IDT54/74FCT827A/B/IDT54/74FCT828A/B

LOGIC SYMBOL

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PIN DESCRIPTION

NAME	I/O	DESCRIPTION
$\overline{OE}_1$	I	When both are LOW the outputs are enabled. When either one or both are HIGH the outputs are High Z.
D_i	I	10-bit data input.
Y_i	O	10-bit data output.

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FUNCTIONAL TABLES

IDT54/74FCT827A/B (NON-INVERTING)⁽¹⁾

INPUTS			OUTPUT	FUNCTION
$\overline{OE}_1$	$\overline{OE}_2$	D_i	Y_i	
L	L	L	L	Transparent
L	L	H	H	
H	X	X	Z	Three-State
X	H	X	Z	

NOTE:

1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance

IDT54/74FCT828A/B (INVERTING)⁽¹⁾

INPUTS			OUTPUT	FUNCTION
$\overline{OE}_1$	$\overline{OE}_2$	D_i	Y_i	
L	L	L	H	Transparent
L	L	H	L	
H	X	X	Z	Three-State
X	H	X	Z	

NOTE:

1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance

IDT54/74FCT827A/B-IDT54/74FCT828A/B
HIGH-PERFORMANCE CMOS BUFFERS

MILITARY AND COMMERCIAL TEMPERATURE RANGES

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	100	100	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE ($T_A = +25^\circ\text{C}$, $f = 1.0\text{MHz}$)

SYMBOL	PARAMETER ⁽¹⁾	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$	6	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0\text{V}$	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

$V_{LO} = 0.2\text{V}$; $V_{HC} = V_{CC} - 0.2\text{V}$

Commercial: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$; $V_{CC} = 5.0\text{V} \pm 5\%$

Military: $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$; $V_{CC} = 5.0\text{V} \pm 10\%$

SYMBOL	PARAMETER	TEST CONDITIONS ⁽¹⁾	MIN.	TYP. ⁽²⁾	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level	2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level	—	—	0.8	V
I_{IH}	Input HIGH Current	$V_{CC} = \text{Max.}$	$V_I = V_{CC}$	—	5	μA
			$V_I = 2.7\text{V}$	—	5 ⁽⁴⁾	
			$V_I = 0.5\text{V}$	—	-5 ⁽⁴⁾	
			$V_I = \text{GND}$	—	-5	
I_{IL}	Input LOW Current	$V_{CC} = \text{Max.}$	$V_O = V_{CC}$	—	10	μA
			$V_O = 2.7\text{V}$	—	10 ⁽⁴⁾	
			$V_O = 0.5\text{V}$	—	-10 ⁽⁴⁾	
			$V_O = \text{GND}$	—	-10	
I_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}$, $I_N = -18\text{mA}$	—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}$ ⁽³⁾ , $V_O = \text{GND}$	-75	-120	—	mA
V_{OH}	Output HIGH Voltage	$V_{CC} = 3\text{V}$, $V_{IN} = V_{LC}$ or V_{HC} , $I_{OH} = -32\mu\text{A}$	V_{HC}	V_{CC}	—	V
		$V_{CC} = \text{Min.}$, $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -300\mu\text{A}$	V_{HC}	V_{CC}	
			$I_{OH} = -15\text{mA MIL.}$	2.4	4.0	
			$I_{OH} = -24\text{mA COM'L.}$	2.4	4.0	
V_{OL}	Output LOW Voltage	$V_{CC} = 3\text{V}$, $V_{IN} = V_{LC}$ or V_{HC} , $I_{OL} = 300\mu\text{A}$	—	GND	V_{LC}	V
		$V_{CC} = \text{Min.}$, $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 300\mu\text{A}$	GND	V_{LC}	
			$I_{OL} = 32\text{mA MIL.}$	—	0.3	
			$I_{OL} = 48\text{mA COM'L.}$	—	0.3	
V_H	Input Hysteresis on Clock Only	—	—	200	—	mV

NOTES:

- For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^\circ\text{C}$ ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

 $V_{LO} = 0.2V$; $V_{HO} = V_{CC} - 0.2V$

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SYMBOL	PARAMETER	TEST CONDITIONS ⁽¹⁾		MIN.	TYP. ⁽²⁾	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} \geq V_{HO}; V_{IN} \leq V_{LC}$ $f_I = 0$		—	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $OE = \text{GND}$ $T/R = \text{GND or } V_{CC}$ One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HO}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_I = 10\text{MHz}$ 50% Duty Cycle $OE = \text{GND}$ One Bit Toggling	$V_{IN} \geq V_{HO}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.5	4.0	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	1.8	5.0	
		$V_{CC} = \text{Max.}$ Outputs Open $f_I = 2.5\text{MHz}$ 50% Duty Cycle $OE = \text{GND}$ Eight Bits Toggling	$V_{IN} \geq V_{HO}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.0	6.6 ⁽⁵⁾	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	5.0	14.5 ⁽⁵⁾	

NOTES:

- For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient and maximum loading.
- Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
 $I_{CC} = \text{Quiescent Current}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $f_I = \text{Input Frequency}$
 $N_I = \text{Number of Inputs at } f_I$
 All currents are in milliamperes and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

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PARAMETER	DESCRIPTION	TEST ⁽¹⁾ CONDITIONS	IDT54/74FCT827A/28A				IDT54/74FCT827B/28B				UNI
			COM'L		MIL		COM'L		MIL		
			MIN. ⁽²⁾	MAX.	MIN. ⁽²⁾	MAX.	MIN. ⁽²⁾	MAX.	MIN. ⁽²⁾	MAX.	
t_{PLH} t_{PHL}	Propagation Delay from D_i to Y_i IDT54/74FCT827A/B (Non-Inverting)	$C_L = 50\text{pF}$ $R_L = 500\Omega$	—	8	—	9	—	5.0	—	6.5	ns
t_{PLH} t_{PHL}		$C_L = 300\text{pF}^{(3)}$ $R_L = 500\Omega$	—	15	—	17	—	13.0	—	14.0	ns
t_{PLH} t_{PHL}	Propagation Delay from D_i to Y_i IDT54/74FCT828A/B (Inverting)	$C_L = 50\text{pF}$ $R_L = 500\Omega$	—	9	—	10	—	5.5	—	6.5	ns
t_{PLH} t_{PHL}		$C_L = 300\text{pF}^{(3)}$ $R_L = 500\Omega$	—	14	—	16	—	13.0	—	14.0	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y_i	$C_L = 50\text{pF}$ $R_L = 500\Omega$	—	12	—	13	—	8.0	—	9.0	ns
t_{PZH} t_{PZL}		$C_L = 300\text{pF}^{(3)}$ $R_L = 500\Omega$	—	23	—	25	—	15.0	—	16.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Y_i	$C_L = 5\text{pF}^{(3)}$ $R_L = 500\Omega$	—	9	—	10	—	6.0	—	7.0	ns
t_{PHZ} t_{PLZ}		$C_L = 50\text{pF}$ $R_L = 500\Omega$	—	10	—	10	—	7.0	—	8.0	ns

NOTES:

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.
- These parameters are guaranteed but not tested.

ORDERING INFORMATION

