Order this data sheet by 6706/D

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

T-46-23-14

Military 6706

Advance Information

32K x 8 Bit BiCMOS Static Random Access Memory

SRAM

The 6706 is a 262,144 bit static random access memory organized as 32,768 words of 8 bits, fabricated using high performance silicon-gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

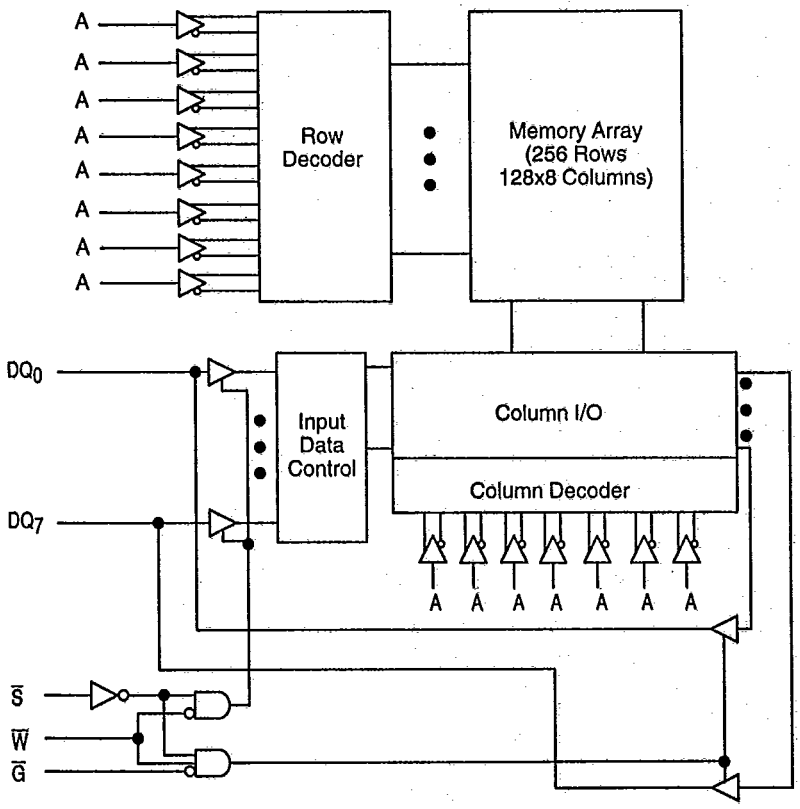
The 6706 is available in a 600 mil, 28 lead sidebraze package.

- Single 5.0 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs are TTL Compatible
- Three State Outputs
- Fast Access Times: 15/20 ns

AVAILABLE AS
1) JAN: N/A
2) SMD: N/A
3) 883: 6706 - XX/BXAJC
X = CASE OUTLINE AS FOLLOWS:
PACKAGE: DIL: X

XX = Speed in ns (15, 20)

BLOCK DIAGRAM



PIN NAMES	
A_0 - A_{14}	Address
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
$\overline{G}$	Output Enable
DQ_0 - DQ_7	Data Input/Output
V_{CC}	+5.0 V Power Supply
V_{SS}	Ground

Truth Table

$\overline{S}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle
H	X	X	Not Selected	High - Z	—
L	H	H	Read	High - Z	—
L	L	H	Read	D_{OUT}	Read Cycle
L	X	L	Write	D_{IN}	Write Cycle

X = Don't Care

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA

T-46-23-14

PIN ASSIGNMENTS		
Function	DIL Case 719-03	Burn-In (Condition-D)
A_{14}	1	CP17
A_{12}	2	CP4
A_7	3	CP5
A_6	4	CP6
A_5	5	CP7
A_4	6	CP8
A_3	7	CP9
A_2	8	CP10
A_1	9	CP11
A_0	10	CP12
DQ_2	11	CP18 to R_1
DQ_1	12	CP18 to R_1
DQ_0	13	CP18 to R_1
V_{SS}	14	GND
DQ_3	15	CP18 to R_1
DQ_4	16	CP18 to R_1
DQ_5	17	CP18 to R_1
DQ_6	18	CP18 to R_1
DQ_7	19	CP18 to R_1
$\overline{S}$	20	CP2
A_{10}	21	CP13
$\overline{G}$	22	CP1
A_{11}	23	CP14
A_9	24	CP15
A_8	25	CP16
A_{13}	26	CP3
$\overline{W}$	27	CP1
V_{CC}	28	V_{CC}, C_1 to GND

BURN-IN CONDITIONS:
V_{CC} = 5.0 V(min)/ 6.0 V(max), R_1 = 39.2 kΩ ± 20%, C_1 = 0.1 µF ± 20%, V_H = 3.0 V(min)/5.0 V(max), V_L = – 0.5 V(min)/0.0 V(max),

CP1:	100 kHz	CP6:	3.125 kHz	CP11:	97.66 Hz	CP16:	3.052 Hz
CP2:	50 kHz	CP7:	1.563 kHz	CP12:	48.83 Hz	CP17:	1.526 Hz
CP3:	25 kHz	CP8:	0.781 kHz	CP13:	24.41 Hz	CP18:	0.763 Hz
CP4:	12.5 kHz	CP9:	0.391 kHz	CP14:	12.21 Hz	CP19:	0.382 Hz
CP5:	6.25 kHz	CP10:	0.195 kHz	CP15:	6.104 Hz	CP20:	0.191 Hz

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 lfpm is maintained.

Absolute Maximum Ratings: (See Note)			
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-0.5 to +7.0	V
Voltage Relative to V_{SS} for any Pin Except V_{CC}	V_{IN}, V_{OUT}	-0.5 to V_{CC} +0.5	V
Output Current	I_{OUT}	± 30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	-55 to +125	°C
Operating Temperature	T_A	-55 to +125	°C
StorageTemperature	T_{stg}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

T-46-23-14

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = – 55°C to +125°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3 *	V
Input Low Voltage	V_{IL}	– 0.5 **	—	0.8	V

* V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = + 2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20 mA.

** V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20 mA.

DC CHARACTERISTICS				
Parameter	**Symbol**	**Min**	**Max**	**Unit**
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	±2.0	µA
Output Leakage Current ($\overline{S}$ = V_{IH}, V_{OUT} = 0 to V_{CC})	$I_{lkg(O)}$	—	±2.0	µA
AC Supply Current (I_{OUT} = 0 mA) 6706-15: t_{AVAV} = 15 ns	I_{CCA}	—	190	mA
AC Supply Current (I_{OUT} = 0 mA) 6706-20: t_{AVAV} = 20 ns	I_{CCA}	—	180	mA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)			
Characteristic	**Symbol**	**Max**	**Unit**
Address Input Capacitance	C_{in}	5.0	pF
Control Pin Input Capacitance ($\overline{S}$, $\overline{G}$, $\overline{W}$)	C_{in}	6.0	pF
I/O Capacitance	$C_{I/O}$	6.0	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = – 55°C to +125°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level	1.5 V
Input Pulse levels	0 to 3.0 V
Input Rise/Fall Times	≤ 3.0 ns
Output Timing Measurement Reference Level	1.5 V

AC TEST LOADS OR EQUIVALENT

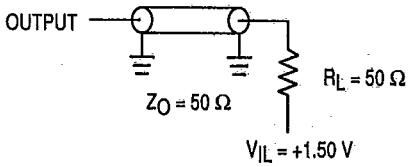


Figure 1A.

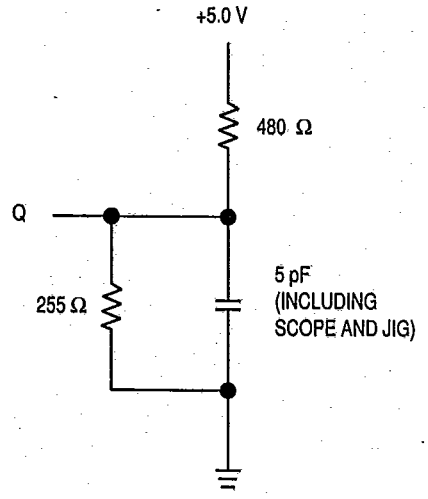


Figure 1B.

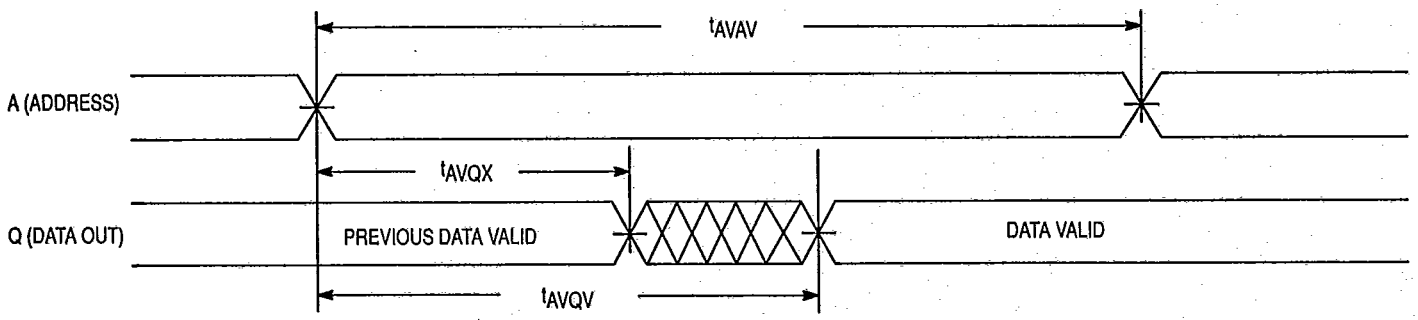
T-46-23-14

READ CYCLE (See Notes 1 and 2)

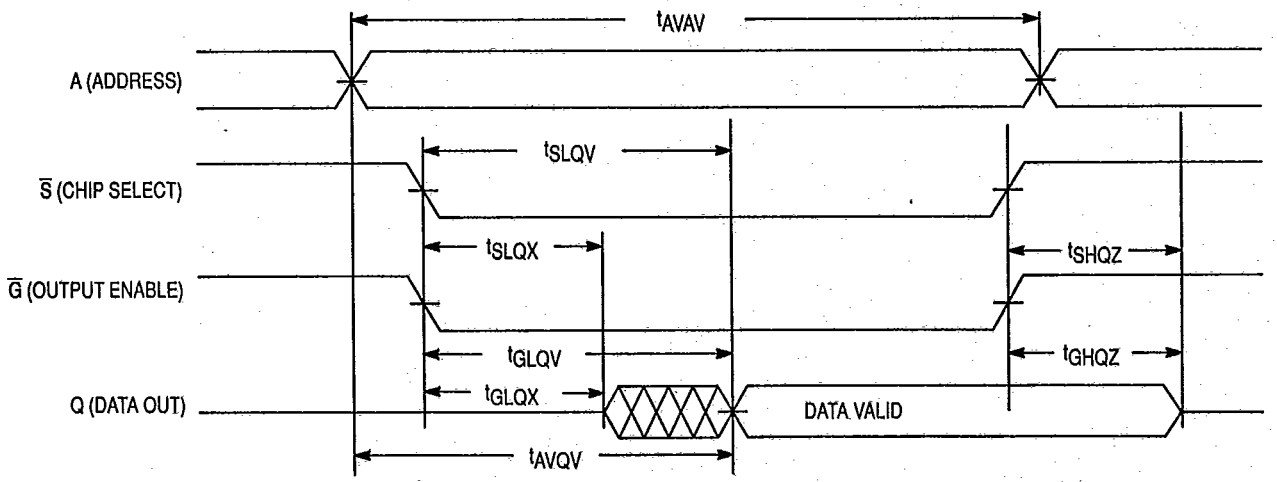
Parameter	Symbol Standard	Symbol Alternate	6706-15		6706-20		Unit	Notes
			Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	15	—	20	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	15	—	20	ns	—
Chip Select Access Time	t_{SLQV}	t_{ACS}	—	15	—	20	ns	—
Output Enable Access Time	t_{GLQV}	t_{OE}	—	9.0	—	12	ns	—
Output Hold from Address Change	t_{AXQX}	t_{OH}	3.0	—	3.0	—	ns	—
Chip Select Low to Output Active	t_{SLQX}	t_{LZ}	0	—	0	—	ns	4, 5, 6
Chip Select High to Output High-Z	t_{SHQZ}	t_{HZ}	0	7.0	0	9.0	ns	4, 5, 6
Output Enable to Output Active	t_{GLQX}	t_{LZ}	0	—	0	—	ns	4, 5, 6
Output Enable to Output High-Z	t_{GHQZ}	t_{HZ}	0	7.0	0	9.0	ns	4, 5, 6

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of the power supplies as well as minimization or elimination of the buss contention conditions during the read and write cycles.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{SHQZ} max is less than t_{SLQX} min, and t_{GHQX} max is less than t_{GHQX} min, both for a given device and from device to device.
5. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
6. These parameters are periodically sampled and not 100% tested.
7. Device is continuously selected ($\overline{S}$ = V_{IL}, $\overline{G}$ = V_{IL}).
8. Address valid prior to coincident with $\overline{S}$ going low.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)



T-46-23-14

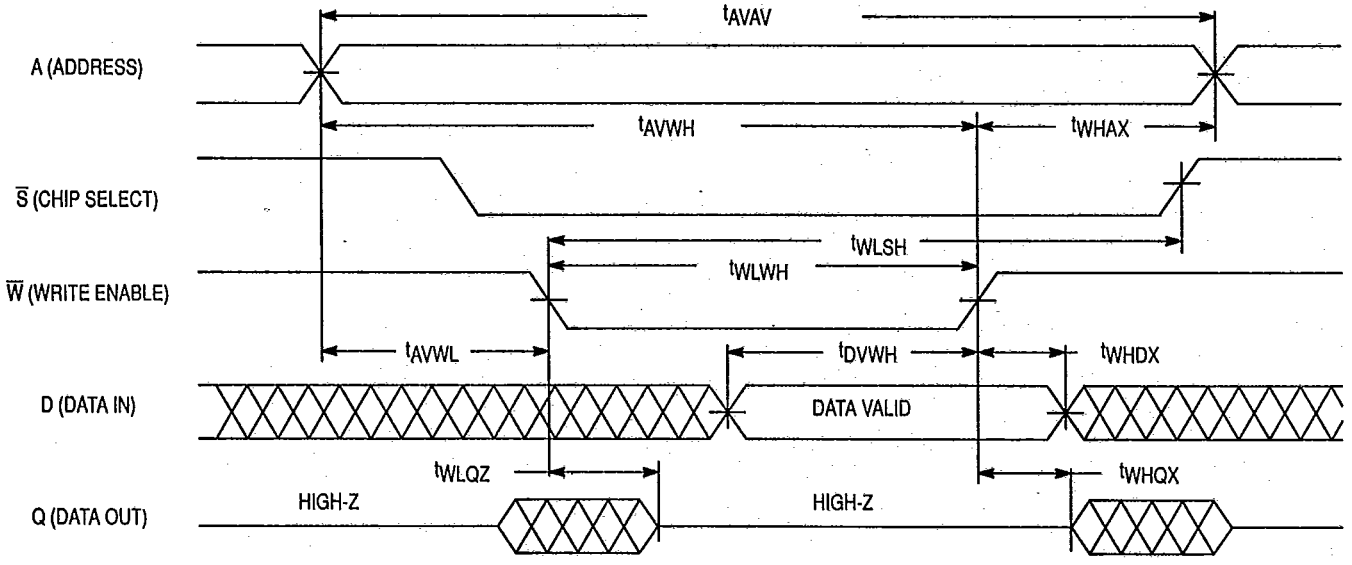
WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol Standard	Symbol Alternate	6706-15 Min	6706-15 Max	6706-20 Min	6706-20 Max	Unit	Notes
Write Cycle Time	t_{AVAV}	t_{WC}	15	—	20	—	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	ns	—
Address Valid to End of Write	t_{AVWH}	t_{AW}	10	—	12	—	ns	—
Write Pulse Width	t_{WLWH}, t_{WLSH}	t_{WP}	9.0	—	11	—	ns	—
Data Valid to End of Write	t_{DVWH}	t_{DW}	6.0	—	8.0	—	ns	—
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	ns	—
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	7.0	—	9.0	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	t_{OW}	0	—	0	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	t_{WR}	1.0	—	1.0	—	ns	—

NOTES:

1. A write occurs during the overlap of $\overline{S}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of the power supplies as well as minimization or elimination of the buss contention conditions during the read and write cycles.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
5. Parameters is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled)

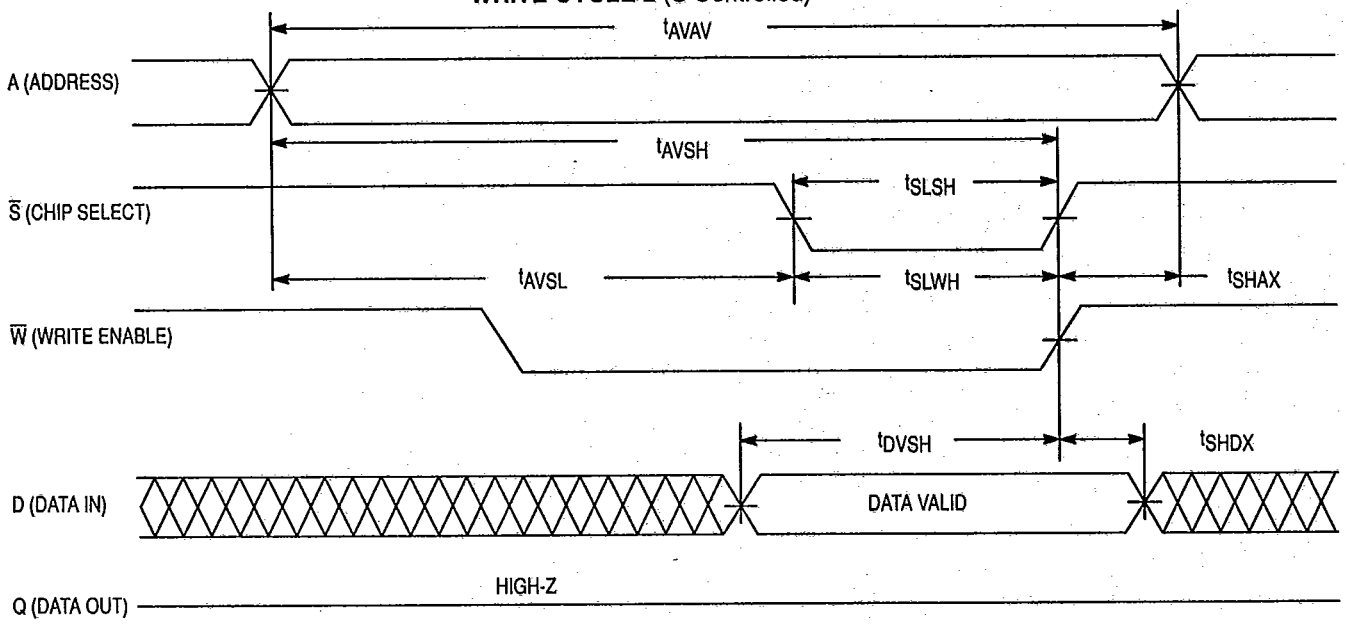


WRITE CYCLE 2 ($\overline{S}$ Controlled, See Notes 1 and 2 above)								
Parameter	Symbol Standard	Symbol Alternate	6706-15		6706-20		Unit	Notes
			Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	15	—	20	—	ns	3 (above)
Address Setup Time	t_{AVSL}	t_{AS}	0	—	0	—	ns	—
Address Valid to End of Write	t_{AVSH}	t_{AW}	10	—	12	—	ns	—
Chip Select to End of Write	t_{SLWH}, t_{SLSH}	t_{CW}	9.0	—	11	—	ns	1, 2 (below)
Data Valid to End of Write	t_{DVSH}	t_{DW}	7.0	—	9.0	—	ns	—
Data Hold Time	t_{SHDX}	t_{DH}	0	—	0	—	ns	—
Write Recovery Time	t_{SHAX}	t_{WR}	1.0	—	1.0	—	ns	—

NOTES:

1. If $\overline{S}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
2. If $\overline{S}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2 ($\overline{S}$ Controlled)



TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Literature Distribution Centers:
USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Center; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan.
ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.